



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)

Accredited with "A" Grade by NAAC

Jepplaar Nagar, Rajiv Gandhi Salai, Chennai - 600 119.

Phone: 044 - 2450 3150 / 51 / 52 / 54 / 55 Fax: 044 - 2450 2344
www.sathyabama.ac.in



BOARD OF STUDIES

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VENUE: CENTRE FOR EXCELLENCE IN EMBEDDED AND IoT

Date: 30.03.2019

Time: 3.30 PM

Minutes of Meeting

Dr. N. M. Nandhitha, Dean, School of EEE welcomed all members of Board of Studies. On the suggestions of various Experts, the contents are designed by the Board of Studies Members considering the various aspects and need of the society.

- Dr.T,Ravi, Head Department of Electronics and Communication started the meeting by welcoming both the external and the internal numbers to the Board of Studies meeting.
- The guidelines of the syllabus given by the management were explained by HOD to all the members of the BOS.
- The external members also ratified the decision to revise the syllabus under the mentioned guidelines.
- Initial discussion was started with course outcome and it has been assessed that COs could be modified slightly and need not be confined to six in number. It can also be reduced as per the content of syllabus. All the framed COs has to be matched with the PO for attainment. Engineering Graphics, Indian culture related more courses have to be included. Reference text books and edition has to be modified. It is decided to have the electives exclusively for school of EEE. Curriculum could be restricted to 3 pages. Include standard authors in references.
- Dr.M.Sumathi presented the changes incorporated in 'Digital Logic Circuits'. Dr M D Selvaraj. Professor, IIITDM accepted the changes suggested.
- Dr.Sivakumaran, Prof., NIT, Trichy accepted the changes proposed in 'Analog Communication' suggested by Dr.P.Chitra.



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

Accredited with "A" Grade by NAAC

Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai - 600 119.

Phone: 044 - 2450 3150 / 51 / 52 / 54 / 55 Fax: 044 - 2450 2344

www.sathyabama.ac.in



4 units and 5th unit may be taken as case studies related to the course. This would enhance the student community to have a clear picture about the course opted.

- Dr.Sivakumaran suggested that have Machine learning technique could be added as replacement of Neural and Fuzzy Logic Systems and Deep Learning algorithms as replacement of Artificial Intelligence . Dr.T.Ravi putforth the introduction of new courses such as Machine Learning, Wireless sensor network, MEMS and its Applications, Optical Networks, Python Programing and Biomedical Signal Processing.
- Dr.T.Ravi also presented the new course introduced for PG courses are Industry 4.0 and Gateway Design for IoT Devices. The Syllabus Revision carried out in PG courses is Network Oriented OS.
- Dr.Sivakumaran also suggested that replacement of Fundamentals of Fuzzy logic and neural networks for EIE and also discussed to have two units of neural network, two units of Fuzzy logic and one unit of Genetic Algorithm. Followed by his suggestion Dr.R.Ramadevi suggested the course as Soft computing Techniques.
- Dr.V.Sivachidambaranathan, Prof.& Head, Dept. of Electrical and Electronics Engineering put forth about the Breakup of credits (15) for Project and Professional Training before the board of members.
- Professional Training 1, which is to be taken up at the end of 4th semester and before commencement of 5th semester would be allotted 2 credits. This credit would be reflected in 5th sem mark sheet.
- The Professional Training 2 as per Regulations 2015 would be modified as Minor Project, should be carried out during 6th semester. This would carry a credit of 3, which would be reflected in 6th semester mark sheet.
- The Phase 2 would be carried out in 8th semester, allotted a credit of 7, to be reflected in 8th semester marks sheet.



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

Accredited with "A" Grade by NAAC

Jeppiaar Nagar, Rajiv Gandhi Salai, Chennai - 600 119.

Phone: 044 - 2450 3150 / 51 / 52 / 54 / 55 Fax: 044 - 2450 2344

www.sathyabama.ac.in

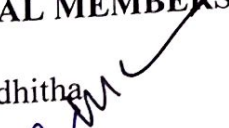



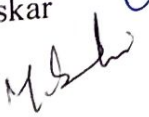


- The Phase 2 would be carried out in 8th semester, allotted a credit of 7, to be reflected in 8th semester marks sheet.
- The students would have to take seminar on a turn basis every week. The seminar would be evaluated and added with CAE1 and CAE2 marks. No credits for Placement training
- The board of members appreciated the breakup credits given for professional training and Project phase
- Dr.V.Sivachidambaranathan, Prof.& Head, Dept. of Electrical and Electronics Engineering requested Mr.Barnabas, Faculty/EEE to put revision of the courses Basic Electrical and Electronics Engineering, Circuit Theory & Network Analysis. Dr.G.T.Sundar Rajan, Faculty /EEE proposed the revision of PG "Power Electronics and Drives" courses "Embedded Systems, Power Electronics in Power Systems, Special Machines and Their controller, & Modeling and Simulation in power Electronics Systems". The new syllabus presented before the board and discussed the valid additions made in the syllabus.
- Dr.V.Sivachidambaranathan, Prof.& Head, Dept. of Electrical and Electronics Engineering requested Dr.Rameshbabu, Faculty/EEE to put forth the syllabus of the new courses, 'Embedded Systems and IoT' for the approval of the board. Dr. A. Amalin Prince approved the Syllabus for this new course.

The following internal members were present in the meeting.

INTERNAL MEMBERS

SIGNATURE

1. Dr.N.M.Nandhitha 
2. Dr.T.Ravi 
3. Dr.V.Sivachidambaranathan 
4. Dr.V.Vijaya Baskar 
5. Dr.M.Sumathy 



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)

Accredited with "A" Grade by NAAC
Joppa Nagar, Rajiv Gandhi Salai, Chennai - 600 119.

Phone: 044 - 2450 3150 / 51 / 52 / 54 / 55 Fax: 044 - 2450 2344
www.sathyabama.ac.in



6. Dr.S.Lakshmi *S. Lakshmi*
7. Dr.P.Chitra *P. Chitra*
8. Dr. P. Kavipriya *P. Kavipriya*
9. Dr.S.Barani *S. Barani*
10. Mrs.K.Srilatha *K. Srilatha*
11. Mrs.L.Magthelin Therase *L. Magthelin Therase*
12. Mrs.S.Yogalakshmi *S. Yogalakshmi*
13. Mrs.K.Sujatha *K. Sujatha*
14. Dr.R.Ramadevi *R. Ramadevi*
15. Dr.Susitra *Susitra*

External Members

Dr.N.Shivakumaran
Professor
Dept. of I& C
NIT, Trichy.

N. Shivakumaran
28/3/19.

Dr.M.D.Selvaraj
Associate Professor
IIITDM, kancheepuram.

M. D. Selvaraj
30/3/19.



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)
Accredited with Grade "A" by NAAC



BOARD OF STUDIES

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VENUE: CENTRE FOR EXCELLENCE IN EMBEDDED AND IoT

Date: 30.11.2019

Time: 3.30 PM

Minutes of Meeting

- Dr. N. M. Nandhitha, Dean, School of EEE welcomed all members of Board of Studies. On the suggestions of various Experts, the contents are designed by the Board of Studies Members considering the various aspects and need of the society. The meeting was convened by the Dr.N.Shivakumaran, Prof / NIT, Trichy. The guidelines of the syllabus given by the management were explained by HOD to all the members of the BOS. The external members also ratified the decision to revise the syllabus under the mentioned guidelines. The Board discussed the matters as per the agenda.
- Dr M D Selvaraj. Professor, IIITDM accepted the changes suggested by Dr P.Chitra in the subject' Digital communication. Dr.N.Shivakumaran also accepted the inclusion of error control coding in the course.
- Dr.T.Ravi discusses the syllabus of Machine learning, Industry 4.0 are discussed with the members.
- Dr.N.Shivakumaran Suggested to include the following topics in Signal and System course such as modelling of signal, speech signal processing, analysis and modelling of system and application of Fourier Transform.
- Dr.T.Ravi also presented the new course introduced for PG courses are Advanced Wireless Sensor Networks and Security in IoT.
- The Syllabus Revision carried out in PG courses is SCADA System Application.
- Dr M D Selvaraj suggested to Remove first unit in Digital Signal Processing course and include DSP processor in the fifth unit. Since first unit is the review of signals and system and to include industrial topic. Include Signal Conditioning, generation and detection for real time applications, DSP Hardwares, FPGA, ARM Processor with DSP Extension in Digital Signal Processing.

- Dr M D Selvaraj Suggested to update the fifth unit of programming in HDL with FPGA Design Flow , Architecture of Xilinx Artix7 FPGA , Configurable Logic Blocks (CLB),
- Dr.N.Shivakumaran Suggested to include applications in FPGA and Case Study: study of protocols I2C, SPI and UART in microprocessor and microcontroller course.
- Dr.T.Ravi put forth the new courses introduced such as Artificial Intelligence, Rf IC Design, Soft Computing Techniques and Cryptography and Network security
- Dr.R.Ramadevi proposed the introduction of new Elective 'Instrumentation in Aerospace and Navigation'. Dr.Sivakumaran suggested to incorporate more topics related to instrumentation.
- Dr.V.Sivachidambaranathan, Prof.& Head, Dept. of Electrical and Electronics Engineering requested Dr.Susitra, Faculty/EEE to put forth revision of the course DC Machines and Transformer and Digital Signal Processing and its Applications. The new syllabus presented before the board and discussed the valid additions made in the syllabus.
- Dr.V.Sivachidambaranathan, Prof.& Head, Dept. of Electrical and Electronics Engineering requested Dr.Rameshbabu, Faculty/EEE to put forth the syllabus of the new courses, 'Computer Aided Electrical Drawing' for the approval of the board. Dr. A. Amalin Prince approved the Syllabus for this new course.

The next BOS meeting may be scheduled on April 2020 to review and finalize the syllabus revision process.

Faculty Head, Dr. T.Ravi proposed vote of thanks and the Board of Meeting ended by 4.30 PM on 30.11.2019.

The following internal members were present in the meeting.

INTERNAL MEMBERS

1. Dr.N.M.Nandhitha



2. Dr.T.Ravi



SIGNATURE

3. Dr.V.Sivachidambaranathan *Dr. V. Sivachidambaranathan*
4. Dr.V.Vijaya Baskar *Vijaya Baskar*
5. Dr.M.Sumathy *MS*
6. Dr.S.Lakshmi *S. Lakshmi*
7. Dr.P.Chitra *Chitra*
8. Dr. P. Kavipriya *P. Kavipriya*
9. Dr.S.Barani *S. Barani*
10. Mrs.K.Srilatha *K. Srilatha*
11. Mrs.L.Magthelin Therase *L. Magthelin Therase*
12. Mrs.S.Yogalakshmi *S. Yogalakshmi*
13. Mrs.K.Sujatha *K. Sujatha*
14. Dr.R.Ramadevi *R. Ramadevi*
15. Dr.Susitra *Susitra*

External Members

Dr.N.Shivakumaran
Professor
Dept. of I& C
NIT, Trichy.

Dr. N. Shivakumaran
30/11/19

Dr.M.D.Selvaraj
Associate Professor
IIITDM, kancheepuram.

Dr. M. D. Selvaraj
30/11/19

Sathyabama Institute of Science and Technology

Department of Electronics and Communication Engineering

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SYLLABUS REVISION(2019-2020)

SL.NO	COURSE CODE	COURSENAME
1	SECA1201	DIGITAL LOGIC CIRCUITS
2	SECA1303	ANALOG COMMUNICATION SYSTEMS
3	SECA1403	DIGITAL COMMUNICATION

SEC1207 (OLD)	DIGITAL LOGIC CIRCUITS (For ECE, EEE, EIE, ETCE and E&C)	L	T	P	Credits	Total Marks
		3	0	0	3	100

UNIT 1 BOOLEAN ALGEBRA AND LOGIC GATES **9 hrs**

Review of number systems - Binary arithmetic – Binary codes – Boolean algebra and theorems - Boolean functions–Minimization of Boolean functions-Sum of Products(SOP)-Product of Sums(POS)-Simplifications of Boolean functions using Karnaugh map and tabulation methods – **Logic gates- NAND and NOR implementation**

UNIT 2 DESIGN OF COMBINATIONAL CIRCUITS **9 hrs**

Introduction to Combinational circuits – **Analysis and design procedures** – Half Adder, Full Adder-Half Subtractor, Full Subtractor- Parallel binary Adder, Parallel binary Subtractor- Carry look ahead Adder- BCD Adder- Decoders- Encoders- Priority Encoder- Multiplexers- MUX as universal combinational modules- Demultiplexers- Code convertors- Magnitude Comparator

UNIT 3 DESIGN OF SEQUENTIAL CIRCUITS **9 hrs**

Introduction to Sequential circuits – Flip flops – SR, JK, D and T flip flops, Master Slave flip flops, Characteristic and excitation table – Realization of one flip flop with other flip flops – Registers – Shift registers – Counters – Synchronous and Asynchronous counters – Modulus counters, **Up/Down counters** – Ring Counter – Johnson Counter – State diagram, State table, State minimization – Hazards

UNIT 4 DIGITAL LOGIC FAMILIES **9 hrs**

Classification and characteristics of logic family – Bipolar logic family – Saturated logic family – **RTL, DTL,DCTL, I²L,TTL, HTL** – Non saturated family – **Schottky TTL, ECL** – Unipolar family – MOS, CMOS logic families. **Tristate logic Interfacing of CMOS and TTL families. Comparison of logic families**

UNIT 5 MEMORIES AND PROGRAMMABLE LOGIC DEVICES **9 hrs**

Classification of memories – ROM – ROM organization – PROM – EPROM – EEPROM – RAM – RAM organization– Write operation – Read operation – Memory decoding – Memory expansion – Static RAM – Dynamic RAM – Programmable Logic Devices – Programmable Logic Array (PLA) – Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) – **Implementation of combinational logic circuits using ROM, PLA, PAL.**

COURSE OUTCOMES:

On completion of this course, students are able to

CO1	Describe the procedure of Number systems, binary codes , binary arithmetic, Boolean algebra and Logic gates
CO2	Apply the concepts of Combination circuits for their implementation
CO3	Design the various types of sequential logic circuits
CO4	Analyze the different types of Digital Logic families
CO5	Investigate the behavior and characteristics of digital logic families , PLDs
CO6	Create the structures of SRAM and DRAM

TEXT / REFERENCE BOOKS:

1. Milos Ercegovac, Jomas Lang, "Introduction to Digital Systems", Wiley publications, 1998
2. John M. Yarbrough, "Digital logic: Applications and Design", Thomas - Vikas Publishing House, 2002
3. R.P.Jain, "Modern digital Electronics",3rd Edition, TMH, 2003
4. Morris Mano, "Digital design", 3rd Edition, Prentice Hall of India, 2008
5. Floyd and Jain, " Digital fundamentals", 10th Edition 2009, Pearson Publishers
6. Charles H.Roth. "Fundamentals of Logic Design", 6th Edition, Thomson Learning, 2013

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100

Exam Duration: 3 hrs

Part A: 10 questions of 2 marks each -No choice

20 Marks

Part B: 5 questions from each unit with internal choice, each carrying 16 marks

80 Marks

SECA1201 NEW	DIGITAL LOGIC CIRCUITS	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To impart knowledge on various types of Binary logics.
- To design a binary logic circuit for an arithmetic expressions.
- To understand the usage of registers and counters used in various digital circuits.
- To understand the design of memory devices used.
- To get an exposure about the electronics behind design of Basic digital logical elements.

UNIT 1 NUMBER SYSTEMS, LOGIC FUNCTIONS AND BOOLEAN ALGEBRA 9 Hrs.

Number systems – Number systems conversions - Binary arithmetic – Binary codes – Logic functions-Universal gate functions - Boolean algebra – Functionally complete operation sets, **Reduction of switching equations using Boolean algebra, Realization of switching function.**

UNIT 2 DESIGN OF COMBINATIONAL LOGIC 9 Hrs.

Design procedure of Combinational Logic – Design of two level gate networks -Sum of Products (SOP) - Product of Sums(POS) - **Canonical SOP - Canonical POS** - Karnaugh Map - Simplifications of Boolean functions using Karnaugh Map and implementation using Logic function – **Advantages and limitations of K-Map** - Tabulation method - Simplifications of Boolean functions using Tabulation method.

UNIT 3 COMBINATIONAL CIRCUITS 9 Hrs.

Introduction to Combinational circuits – Half Adder, Full Adder - Half Subtractor, Full Subtractor- Parallel binary Adder, Parallel binary Subtractor - Carry look ahead Adder- BCD Adder- Decoders- Encoders - Priority Encoder- Multiplexers- MUX as universal combinational modules- Demultiplexers- Code convertors- Magnitude Comparator.

UNIT 4 SEQUENTIAL CIRCUITS 9 Hrs.

Introduction to Sequential circuits – Flip flops – SR, JK, D and T flip flops, Master Slave flip flop, Characteristic and excitation table – Realization of one flip flop with other flip flops – Registers – Shift registers – Counters – Synchronous and Asynchronous counters – Modulus counters – Ring Counter – Johnson Counter – State diagram, State table, State minimization – Hazards.

UNIT 5 DIGITAL LOGIC FAMILIES, MEMORIES AND PROGRAMMABLE DEVICES 9 Hrs.

Classification and characteristics of logic family – Bipolar logic family – Saturated logic family – Non saturated family – Unipolar family – MOS, CMOS logic families. Classification and Organization of memories – Programmable Logic Devices – Programmable Logic Array(PLA) – Programmable Array Logic (PAL) – Field Programmable Gate Arrays (FPGA) .

Max. 45 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

CO1 - Classify various types of Digital Number systems and Boolean algebra.

CO2 - Illustrate Combinational logic.

CO3 - Design and implement the digital circuit using combinational logic.

CO4 - Design and implement the digital circuit using sequential logic.

CO5 - Illustrate the digital logic families.

CO6 - Solve the arithmetic expressions using memories and programable logic devices and implement memory units with Programmable logic devices.

TEXT / REFERENCE BOOKS

1. John M. Yarbrough, "Digital logic: Applications and Design", Thomas - Vikas Publishing House, 2002.
2. Morris Mano, "Digital design-With an Introduction to the Verilog HDL", 5th Edition, Pearson, 2013.
3. R.P.Jain, "Modern Digital Electronics", 4th Edition, TMH, 2010.
4. Thomas L Floyd, " Digital Fundamentals", 11th Edition, Pearson, 2015
5. William H. Gothmann, "Digital Electronics", Prentice Hall, 2001.
6. Tutorial Website: https://www.tutorialspoint.com/digital_circuits/index.htm.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100

Exam Duration: 3 Hrs.

PART A: 10 Questions of 2marks each-No choice

20 Marks

PART B: 2 Questions from each unit of internal choice; each carrying 16 marks

80 Marks

SEC1209	ANALOG COMMUNICATIONS	L	T	P	Credits	Total Marks
		3	0	0	3	100

- UNIT1 BASICS OF ELECTRONIC COMMUNICATION AND NOISE THEORY** **9 hrs**
- Review of time and frequency domain description of signals - Communication system: point to point and broad cast - Basic model of a communication system: transmitter, receiver and channel - Fundamental limitations: Technological, Physical; Noise, bandwidth (signal and channel) and information capacity - Need for modulation and types - classification of communication based on modulation and channel - Base band and Pass band transmission - Electromagnetic spectrum allocation for various communication systems. Noise in Communication systems: Types and sources of noise; Atmospheric Noise, Thermal Noise, Shot noise, Partition noise, Flicker noise, Transit time noise - noise factor, noise factor for cascaded amplifier (Friss formula) -Noise figure - Equivalent noise temperature and bandwidth - Signal toNoise Ratio
- UNIT 2 AMPLITUDE MODULATION AND DEMODULATION** **9 hrs**
- STD-AM (DSB-FC) Mathematical representation - waveform, frequency spectrum, bandwidth, power relations and Modulation index - Multi tone modulation - Limitations and Modifications in STD-AM: DSB-SC, SSB-SC and VSB, AM Generation (Modulators): DSB-FC; square law modulator, Collector and base modulator circuits - DSB- SC; Balanced modulator circuit using BJT/FET - SSB: Phase shift method and Filter method - VSB; Filter method- Application and Comparison of various AM schemes - AM transmitter: Low and high level Modulation. AM Detection (Demodulators) - Envelope detector, Significance of RC time constant - Square law detector - Costa's PLL detector
- UNIT 3 ANGLE (FM & PM) MODULATION AND DEMODULATION** **9 hrs**
- Single tone FM: Mathematical representation, waveform, frequency spectrum, modulation index, bandwidth and power - Multi-tone FM - Types and comparison of FM: Narrowband and Wideband - Compare FM and AM Phase modulation (PM): Mathematical representation and waveform - Relation between FM and PM - Conversion: FM to PM and PM to FM - Application of FM and PM. FM Generation: Direct method using Varactor diode and indirect method (Armstrong modulator) - Pre-emphasis - FM stereo broadcast transmitter. FM Detector: Balanced slope detector, Foster seelay frequency discriminator and Ratio detector - De- emphasis
- UNIT 4 ANALOG PULSE MODULATION, DEMODULATION AND MULTIPLEXING** **9 hrs**
- Analog pulse modulation - Sampling theorem - Nyquist rate - Concepts of PAM, PWM (PDM) and PPM - Modulators and demodulators. Multiplexing- classifications: Frequency Division Multiplexing, Time Division Multiplexing and Quadrature Multiplexing - Comparison of multiplexing
- UNIT 5 RECEIVERS AND SYSTEMS** **9 hrs**
- AM Receivers: TRF receivers -Super heterodyne receivers: choice of IF, double conversion technique, tracking, AGC- characteristics of receiver - noise in AM receiver. FM Receivers: FM stereo broadcast receivers - AFC - Noise in FM - Capture effect, FM threshold effect. Communication Receivers: Sensitivity, fidelity and selectivity - Squelch circuit - Beat frequency Oscillator- Overview of Telephony, Telegraphy, Television, CCTV and Cable television

Sathyabama Institute of Science and Technology
Department of Electronics and Communication Engineering

COURSE OUTCOMES:

On completion of this course, students are able to

CO1	Describe the functional blocks of communication system, noise sources and types
CO2	Derive the mathematical equations and demonstrate the generation & detection of AM, FM, PM, PAM, PDM and PPM
CO3	Design AM and FM transmitters
CO4	Apply sampling theorem and demonstrate the significance of various multiplexing techniques
CO5	Analyze the TRF and Super heterodyne receivers and concepts of Telephony, Telegraphy, Television, CCTV and Cable television
CO6	Develop appropriate modulation technique for real time applications

TEXT / REFERENCE BOOKS:

1. Dennis Roody and John Coolen, Electronic Communication, Pearson, 4/e, 2011
2. Tomasi, Electronic Communications System, Pearson, 5/e, 2011
3. Simon Haykin, —Communication SystemsII, Wiley Publication, New Delhi, 2011
4. Kennedy G, - Electronic Communication systems, Tata McGraw Hill, New Delhi, 2009
5. Sanjay Sharma, "Analog Communication Systems", 2009
6. B. P. Lathi, Modern digital and analog Communication systems, Oxford University Press., 4th edition, 2010

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

**Max. Marks: 100
hrs**

Exam Duration: 3

Part A: 10 questions of 2 marks each -No choice
Marks

20

Part B: 5 questions from each unit with internal choice, each carrying 16 marks

80 Marks

SECA130 (Revised)	ANALOG COMMUNICATION SYSTEMS (For ECE)	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To discuss and understand fundamental concepts of amplitude modulation and demodulation techniques.
- To understand the concepts of Frequency Modulation and De-Modulation techniques and compare with AM and PM.
- To understand the concepts of Analog Pulse modulation and De-Modulation techniques (PAM, PDM/PWM and PPM) & Multiplexing techniques and classifications.
- To apply different multiplexing techniques for AM, FM, PAM, PWM and PPM systems.
- To understand the various noises and their effect on Analog modulation systems.
- To discuss the working of Analog Communication Receivers and Telephone and Television Systems.

UNIT 1 AMPLITUDE MODULATION AND DEMODULATION

9 Hrs.

Need for modulation – Model of communication system and classification, Representation of AM – Modulation index and power calculation – Types of AM; DSB-FC: Collector and base modulation circuits, square law modulator- DSB-SC: Balanced modulator circuit using FET – SSB: Filter method and phase shift method – VSB, Comparison of various AM schemes-AM transmitter: Low level and high level Modulation. Demodulation – Envelope detector, Significance of RC time constant- Square law detector.

UNIT 2 ANGLE (FM AND PM) MODULATION AND DEMODULATION

9 Hrs.

Single tone FM: Mathematical representation, frequency spectrum and bandwidth- Multi-tone FM - NBFM and WBFM - Phase modulation (PM): Mathematical representation - Conversion: FM to PM and PM to FM – Comparison of AM, FM and PM- FM Generation: Direct method using Varactor diode and indirect method (Armstrong modulator) - Pre-emphasis - FM transmitter. FM Detector: Balanced slope detector, Foster seeley frequency discriminator and Ratio detector - De- emphasis.

UNIT 3 ANALOG PULSE MODULATION AND MULTIPLEXING

9 Hrs.

Sampling theorem – Types of sampling-Concepts of PAM, PWM, PPM and PCM- Modulators and demodulators. Types of Multiplexing- Frequency Division Multiplexing, Time Division Multiplexing and Quadrature Multiplexing - Comparison of multiplexing.

UNIT 4 ANALOG RECEIVERS AND NOISE

9 Hrs.

AM Receivers: TRF receivers - Super heterodyne receivers - FM Receivers: FM stereo broadcast receivers - AFC - Capture effect, FM threshold effect. Communication Receivers: Sensitivity, fidelity and selectivity - Squelch circuit - Beat frequency Oscillator- Types of Noise- Noise factor and noise temperature for cascaded amplifier (Friis formula)- Noise in AM and FM systems.

UNIT 5 COMMUNICATION SYSTEMS

9 Hrs.

Telephone Systems-Electronics Telephone and cellular Telephone System - Fax-Television Systems-Scanning-camera tube and Transmitter, Picture tube and Receiver, CCTV and Set top box.

Max. 45 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

- CO1 - Explain the Functional blocks of communication system, modulation techniques and Various noise sources and types.
- CO2 - Analyse AM, FM, PM, PAM, PDM, PPM and PCM using mathematical equations and demonstrate their modulation and demodulation techniques.
- CO3 - Illustrate sampling theorem and explain the importance of various multiplexing techniques.
- CO4 - Demonstrate the working of AM and FM transmitters, Receivers and communication Systems.
- CO5 - Performance evaluation and selection of appropriate modulation technique for real time applications.
- CO6 - Working of Analog Communication Receivers and Telephone and Television Systems.

TEXT/REFERENCE BOOKS

1. R.P Singh Sanjay Sharma, "Analog Communication Systems", 2009.
2. B.P.Lathi, "Modern Digital and Analog Communication Systems", 3rd Edition, Oxford University Press, 2007.
3. Deshpande, N.D, "Communication Electronics", Tata McGraw Hill Publishers,1989.
4. Louis. E. Frenzel, "Communication Electronics Principles and applications", 3rd Edition, Tata Mc.Graw Hill, 2002.
5. Dennis Reddy and John Coolen, "Electronic Communications", 4th Edition, Prentice Hall Publishers,1995.
6. Kennedy, "Electronic Communications Systems", 4th Edition, McGraw-Hill Publishers,1992.
7. R.Gulati, "Monochrome and colour television", 2nd Edition, New age international 2005.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100

Exam Duration: 3 Hrs.

PART A: 10 Questions of 2 marks each - No choice

20 Marks

PART B: 2 Questions from each unit of internal choice; each carrying 16 marks

80 Marks

Sathyabama Institute of Science and Technology
Department of Electronics and Communication Engineering

SEC1313 (Old)	DIGITAL COMMUNICATIONS (For ECE and ETCE)	L	T	P	Credits	Total Marks
		3	0	0	3	100

UNIT 1 SAMPLING AND QUANTIZATION

9 hrs

Review of Sampling process -Natural Sampling-Flat Sampling - Aliasing - Signal Reconstruction-Quantization - Uniform & non-uniform quantization - quantization noise Bandwidth -Noise trade off-PCM- Noise considerations in PCM- differential pulse code modulation - Delta modulation -Linear prediction - Adaptive Delta Modulation

UNIT 2 BASEBAND PULSE TRANSMISSION

9 hrs

Base band transmission - Wave form representation of binary digits -Matched filter- error rate due to noise -- Nyquist's criterion for distortion less base band binary transmission- Inter symbol interference - ideal Nyquist channel - Raised cosine channels- correlative level coding - Baseband M-ary pam transmission- equalization - Eye patterns- companding - A law and μ law- Correlation receiver

UNIT 3 DIGITAL MODULATION TECHNIQUES

9hrs

Introduction - ASK- FSK - PSK- coherent modulation techniques-BFSK-BPSK-signal space diagram-robability of error- coherent quadrature modulation techniques- QPSK-signal space diagram-probability of error- non coherent modulation techniques-M-ary modulation techniques - Vectorial view of MPSK and MFSK - error performance

UNIT 4 SYNCHRONIZATION

9 hrs

Synchronization: Receiver synchronization - Coherent systems - Symbol and frame synchronization - Network synchronization - Open and closed loop transmitter synchronization - Tracking and acquisition in spread spectrum system

UNIT 5 SPREAD SPECTRUM MODULATION

9 hrs

Pseudo- noise sequences - a notion of spread spectrum - Direct sequence spread spectrum with coherent binary phase shift keying - Signal space Dimensionality and processing gain -Probability of error - Frequency -hop spread spectrum- Use of spread spectrum with code division multiple access

Max. 45 hrs

COURSE OUTCOMES:

On completion of this course, students are able to

CO1	Describe the working of digital communication systems and different source encoding schemes
CO2	Analyze the degradation in Baseband Pulse Transmission and techniques to overcome it
CO3	Compare the performance of different digital modulation techniques with different modulation schemes in the presence of noise

Sathyabama Institute of Science and Technology

Department of Electronics and Communication Engineering

CO4	Analyze the performance of various synchronization schemes in digital communication receivers
CO5	Evaluate the performance of spread spectrum based digital communications systems
CO6	Design modulator and demodulator for digital communication systems

TEXT / REFERENCE BOOKS:

1. Simon Haykin, Michael Moher, "Communication Systems" John Wiley, 5th Edition, March 2009
2. Herbut Taub, Donald L. Schilling , Goutam Saha , "Principles of Communication",4thMcGraw Hill edition,2013
3. John G. Proakis, Masoud Salehi, "Digital Communication", McGraw Hill 5th edition, 2014
4. Bernard Sklar, "Digital Communication, Fundamentals and Application", Pearson Education Asia, 3rd Edition, 2013

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100

Exam Duration: 3 hrs

Part A: 10 questions of 2 marks each -No choice

20 Marks

Part B: 5 questions from each unit with internal choice, each carrying 16 marks

80 Marks

SECA1403 (Revised)	DIGITAL COMMUNICATION	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To know the principles of sampling & quantization.
- To understand the various Base Band signaling schemes.
- To introduce the basic concepts of digital modulation of baseband signals.
- To get introduced to the basics of source and channel coding/decoding.
- To understand the basics of spread spectrum modulation schemes.

UNIT 1 SAMPLING AND QUANTIZATION

9 Hrs.

Digital communication systems: performance metrics and specifications-Review of Sampling process -Natural Sampling-Flat Sampling - Aliasing - Signal Reconstruction-Quantization- Uniform & non-uniform quantization - quantization noise - PCM- Noise considerations in PCM- differential pulse code modulation - Delta modulation - - Adaptive Delta Modulation.

UNIT 2 BASEBAND PULSE TRANSMISSION

9 Hrs.

Base band transmission - Wave form representation of binary digits -Matched Filter- Error Rate due to noise - Nyquist's criterion for Distortion less Base band Binary Transmission- Inter symbol Interference - Ideal Nyquist channel - Raised cosine channels- Correlative level coding - Equalization- Adaptive Equalization – Eye patterns- Companding - correlation receiver.

UNIT 3 DIGITAL MODULATION TECHNIQUES

9 Hrs.

Introduction - ASK- FSK - PSK- coherent modulation techniques-BFSK-BPSK-signal space diagram-probability of error- Coherent Quadrature modulation techniques- QPSK-signal space diagram-probability of error- Non coherent modulation techniques-DPSK-M-ary modulation techniques - Vectorial view of MPSK.

UNIT 4 ERROR CONTROL CODING

9 Hrs.

Discrete memoryless channels – Linear block codes - Cyclic codes - Convolutional codes – Maximum likelihood decoding of convolutional codes-Viterbi Algorithm, Trellis coded Modulation, Turbo codes.

UNIT 5 SPREAD SPECTRUM MODULATION

9 Hrs.

Pseudo- noise sequences - a notion of spread spectrum - Direct sequence spread spectrum with coherent binary phase shift keying - Signal space Dimensionality and processing gain -Probability of error - Frequency –hop spread spectrum- Synchronization and its types.

Max. 45 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

CO1 - Design PCM systems.

CO2 - Apply the knowledge of signals and system and evaluate the performance of digital communication system in the presence of noise.

CO3 - Design and implement band pass signaling schemes and analyze the spectral characteristics of band pass signaling schemes.

CO4 - Design encoder and decoder for the error control codes like block code, cyclic code.

CO5 - Analyze the digital communication system with spread spectrum modulation.

CO6 - Examine the theoretical concepts through laboratory experiments, analyze and interpret the results to provide valid conclusions.

TEXT/REFERENCE BOOKS

1. Simon Haykins, "Communication Systems" John Wiley, 5th Edition, March 2009.
2. Taub. HDL Schilling, G Saha, "Principles of Communication", 5th Edition, 2009.
3. John G. Proakis, Masoud Salehi, "Digital Communication", McGraw Hill, 5th Edition, 2007.
4. Bernard Sklar, "Digital Communication, Fundamentals and Application", Pearson Education Asia, 2nd Edition, 2009

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100

Exam Duration: 3 Hrs.

PART A: 10 Questions of 2 marks each – No choice

20 Marks.

PART B: 2 Questions from each unit of internal choice; each carrying 16 marks

80 Marks.

SECA7025	NETWORK ORIENTED OS	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To introduce students to the state of the art in wireless sensor actuator networks.
- To provide hands on training in programming these networks and several applications such as environmental monitoring, perimeter security, structural control, asset tracking and personal health care systems.

UNIT 1 OVERVIEW OF IOT CONTIKI OS

9Hrs.

Internet of Things: current solutions and an outlook on future evolutions of current technologies - Basic introduction to Contiki OS: Basic operations, proto-threads, timers, event management

UNIT 2 COOJA SIMULATOR AND 6LOWPAN

9Hrs.

Introduction to the Cooja emulator. Introduction to 6LoWPAN. 6LoWPAN architecture: simple, extended and ad-hoc networks. Issues in determining IPv6 links in LLNs and illustration of the undetermined link addressing model-IPv6 addressing in 6LoWPAN. 6LoWPAN forwarding: route-over and mesh under approaches.

UNIT 3 ROUTING IN LOSSY NETWORK

9Hrs.

Routing in low power and Lossy networks: pros and cons of the mesh-under and route-over solutions.

UNIT 4 INTRODUCTION TO RPL

9Hrs.

Introduction to RPL: the IPv6 Routing Protocol for LLNs. RPL: multi-point to point routing with destination oriented directed acyclic graphs.

UNIT 5 RPL CONSTRAINT AND CONFIGURATION

9Hrs.

RPL instances, routing metrics and constraints. Introduce 6LBR. RPL protocol configuration in Contiki.- Overview of the general configuration parameters.

Max. 45Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

- CO1 - Identify suitable light weight operating system for a specific IoT based applications.
- CO2 -Apply right IoT communication stack for given application requirements.
- CO3 -Develop IoT applications using Contiki Operating System.
- CO4 -Design a Low power PAN and analyze its performance using Cooja emulator.
- CO5 -Analyze the performance of various routing protocols for low power and lossy wireless sensor networks.
- CO6 - Evaluate the performance metrics of LoWPAN and MicroIP stack using an IoT operating system.

TEXT / REFERENCE BOOKS

1. Tanenbaum, "Computer Networks", PHI, 5th Edition, 2015. Andrew S.
2. Daniel Minoli, Taieb Znati, "Wireless Sensor Network", Wiley, 1st Edition, 2007. Kazem Sohraby,
3. C.Siva Ram Murthy and B.S.Manoj "AdHoc Wireless Networks: Architectures and Protocols", Prentice Hall, 1st Edition, 2004.
4. Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", Wiley, 1st Edition, 2007. Holger Karl and
5. Leonidas J. Guibas, "Wireless Sensor Networks: An Information Processing Approach", Morgan Kaufmann, 1st Edition, 2004. Feng Zhao and

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

**Max. Marks: 100
Hrs.**

Exam Duration: 3

PART A: 5 Questions of 6 Marks each – No choice

30 Marks

PART B: 2 Questions from each unit of internal choice, each carrying 14 Marks

70 Marks

SECA7025 (Revised)	NETWORK ORIENTED OS	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To introduce students to the state of the art in wireless sensor actuator networks.
- To provide hands on training in programming these networks and several applications such as environmental monitoring, perimeter security, structural control, asset tracking and personal health care systems.
- To introduce students to network oriented operating systems.

UNIT 1 OVERVIEW OF IOT CONTIKI OS 9Hrs.

Need for light weight operating systems for IoT - Open Source Operating Systems for IoT- Basic introduction to Contiki OS: Basic operations, proto-threads, timers, event management -**Contiki Communication components: MicroIP, ,uIPv6 and RIME, 6LoWPAN**

UNIT 2 COOJA SIMULATOR AND 6LOWPAN 9Hrs.

Introduction to the Cooja emulator. Introduction to 6LoWPAN.6LoWPAN architecture: simple, extended and ad-hoc networks. Issues in determining IPv6 links in LLNs and illustration of the undetermined link addressing model-IPv6 addressing in 6LoWPAN. 6LoWPAN forwarding: route-over and mesh under approaches.

UNIT 3 ROUTING IN LOSSY NETWORK 9Hrs.

Heterogeneous Traffic Networks - Routing in low power and Lossy networks: pros and cons of the mesh-under and route-over solutions.

UNIT 4 INTRODUCTION TO RPL 9Hrs.

Introduction to RPL: the IPv6 Routing Protocol for LLNs. RPL: multi-point to point routing with destination oriented directed acyclic graphs.

UNIT 5 RPL CONSTRAINT AND CONFIGURATION 9Hrs.

RPL instances, routing metrics and constraints. Introduce 6LBR. RPL protocol configuration in Contiki.- Overview of the general configuration parameters.

Max. 45Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

- CO1 - Identify suitable light weight operating system for a specific IoT based applications.
- CO2 - Apply right IoT communication stack for given application requirements.
- CO3 - Develop IoT applications using Contiki Operating System.
- CO4 - Design a Low power PAN and analyze its performance using Cooja emulator.
- CO5 - Analyze the performance of various routing protocols for low power and lossy wireless sensor networks.
- CO6 - Evaluate the performance metrics of LoWPAN and MicroIP stack using an IoT operating system.

TEXT / REFERENCE BOOKS

1. AgusKurniawan, " PracticalContiki-NG: Programming for Wireless Sensor Networks",Apress; 1st ed. Edition, 2018.
2. KazemSohraby, Daniel Minoli, Taieb Znati, "Wireless Sensor Network", Wiley, 1st Edition, 2007. ISBN:978-0-471-74300-2.
3. C.Siva Ram Murthy and B.S.Manoj "AdHocWirelessNetworks:ArchitecturesandProtocols", Prentice Hall, 1st Edition, 2004.
4. James F. Kurose and Keith W. Ross, "Computer Networking: A Top-Down Approach Featuring the Internet", Pearson Education, 6th Edition, 2016.
5. Holger Karl and Andreas Willig, "Protocols and Architectures for Wireless Sensor Networks", Wiley, 1st Edition, 2007.
6. Feng Zhao and Leonidas J. Guibas, "Wireless Sensor Networks: An Information Processing Approach", Morgan Kaufmann, 1stEdition, 2004.

Sathyabama Institute of Science and Technology

Department of Electronics and Communication Engineering
END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100
Hrs.

Exam Duration: 3

PART A: 5 Questions of 6 Marks each – No choice

30 Marks

PART B: 2 Questions from each unit of internal choice, each carrying 14 Marks

70 Marks