

DESIGN AND DEVELOPMENT OF FIVE LEVEL CASCADE H-BRIDGE INVERTER FOR RENEWABLE ENERGY APPLICATION

**Submitted in partial fulfillment of the requirements for the award of
Bachelor of Engineering Degree in
Electrical and Electronics Engineering**

By

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**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade “A” by NAAC

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **K.R. DEEPAN RAM (37140022)**, **P.S. DHINESH KUMAR (37140026)** and **D.K. KEERTHIVAASAN (37140043)** who carried out the project entitled "DESIGN AND DEVELOPMENT OF FIVE LEVEL CASCADE H-BRIDGE INVERTER FOR RENEWABLE ENERGY APPLICATION" under our supervision from December 2020 to April 2021

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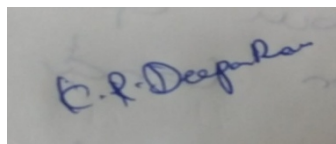
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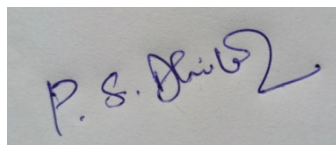
DECLARATION

We **K.R.DEEPAN RAM (37140022)**, **P.S.DHINESH KUMAR (37140026)** and **D.K.KEERTHI VAASAN (37140043)** hereby declare that the Project Report entitled “**DESIGN AND DEVELOPMENT OF FIVE LEVEL CASCADE H-BRIDGE INVERTER FOR RENEWABLE ENERGY APPLICATION**” done by us under the guidance of **Dr. S. NIRMAL RAJ** is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electrical and Electronics Engineering.

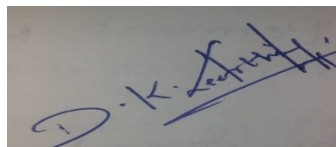
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ABSTRACT

This project presents an asymmetrical five level cascaded H-bridge multilevel inverter, using multicarrier pulse width modulation technique. Cascaded H – Bridge five level inverter with less number of power electronic components for improving the power quality and better harmonic profile in Renewable Energy Systems. And also, comparison is made between multicarrier pulse width modulation and the embedded mat lab function

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LIST OF ABBREVIATIONS

CHB	-	Cascaded H-bridge
CHBMC	-	Cascaded Hbridge Structure Convertor
DSP	-	Digital Signal Processor
DTC	-	Direct Torsion Management
EVs	-	Electrical Vehicles
PWM	-	Pulse Dimension Modulation
RC	-	Resistance and Condenser
SHE	-	Selective Harmonic Elimination
USART	-	Universal Synchronous/Asynchronous Receiver/Transmitter

CHAPTER 1

INTRODUCTION

1.1 GENERAL

Large inverters have historically happy the ever-increasing demand of high-octane industrial applications, that presently extends from the tens to many megawatts. Some samples of this truth area unit the medium voltage vary (2.3 to 13.8 KV) AC motor drives. Nowadays, it's problematic to attach just one power semiconductor switch on to the grid thanks to the high voltage vary. So as to unravel this problem, a brand new style of power convertor has been introduced as an answer in high power applications. Converters use high speed switch parts, avoiding the matter of linking them on to the grid by connecting single devices among multiple DC levels. Converters area unit found in several applications; industrial motor drives, utility interfaces for renewable energy systems (photovoltaic, wind energy and fuel cells), versatile AC transmission systems (FACTS), high voltage DC transmission (HVDC), and traction drives systems.

The advantages of this kind of convertor over the standard 2 level convertor are:

- They will operate through a lower switch frequency.
- They draw input current with terribly low harmonic distortion.
- They turn out a smaller common mode voltage, reducing the strain within the motor bearings.
- They generate a stairs undulation as AN output with abundant lower harmonic distortion and dv/dt stresses.

These area unit a number of the disadvantages once the amount of levels within the convertor is increased:

1. Unbalanced voltages area unit introduced.
2. A larger quantity of switches area unit needed.
3. A additional advanced controller is needed thanks to the quantity of capacitors, which require to be balanced.

Several construction topologies are developed within the previous few years. {they area unit|they're} additional advanced to modulate than the 2 level ancient converters attributable to the amount of switch alternatives that are accessible. Within the last 3 decades, 3 main convertor topologies have emerged from the various proposed:

- Diode Clamped (Neutral Clamped).
- Flying electrical device (Capacitor Clamped).
- Cascade Voltage supply, standard construction Converter (M2C).

Furthermore, many modulation techniques are developed for these converters. The modulation techniques include: curved pulse dimension modulation (SPWM), selective harmonic elimination (SHE-PWM) and area vector modulation (SVM). The most recent and most promising such topology for prime power applications is that the standard construction convertor (M2C). Varied management and modulation strategies are recommended for this topology. The aim of this master thesis project is to deeply investigate and measure one in every of them, supported a carrier phase-shifted Pulse dimension Modulation (PWM) technique. Four totally different management topologies exploitation part Shift PWM techniques on standard construction Converters area unit studied and explored during this work. These topologies might have 3 loops of control: Averaging management supported the currents within the convertor, Individual equalization management supported the output current and capacitors voltages, and Arm equalization management supported the voltage distinction between the arms of the convertor. what is more these topologies area unit simple to implement

and don't demand high process levels. This project proposes a switch frequency that meets the 2 needed criteria: low enough to take care of value practicableness, and high enough to achieve a harmonic performance target. to boot, this work proposes AN analytic expression for the output voltage spectrum of the convertor, that allows prediction of harmonic performance.

1.2 CONSTRUCTION CONVERTOR TOPOLOGIES

In the gift chapter of the work there's shortly description of the foremost necessary topologies developed. During this regard, there'll be mentioned their blessings and downsides whereas discussing the various configurations and their operation principles.

1.2.1 *Diode Chamber Construction Converter*

The first invention in construction converters was the questionable neutral purpose clamped electrical converter. It absolutely was at first planned as a 3 level electrical converter. It's been shown that the principle of diode clamping will extended to any level. A diode clamped leg circuit is shown in Figure 1.1.

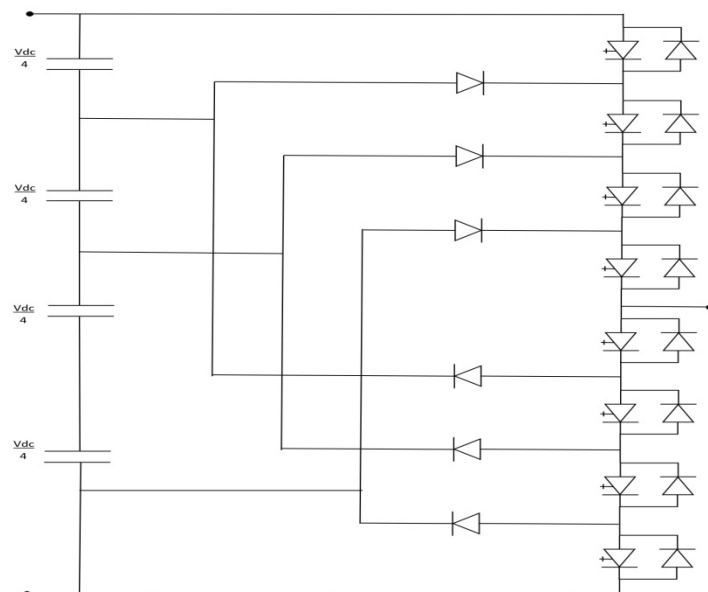


Figure 1.1 One part 5-level structure of a Diode Clamped electrical converter

Some of the applications exploitation construction Diode Clamped converters are:

- An interface between High voltage DC line and AC line.
- High power medium voltage variable speed drives.
- Static volt-ampere compensation

The main blessings and downsides of this topology are:

Advantages

- High potency for the basic switch frequency.
- The capacitors is pre-charged along at the specified voltage level.
- The capacitance demand of the electrical converter is decreased thanks to all phases sharing a typical DC link.

Disadvantages

- Packaging for inverters with a high range of levels can be a haul thanks to the quadratically relation between the amount of diodes and therefore the numbers of levels.
- Intermediate DC levels tend to be uneven while not the acceptable management creating the 64000 power transmission a haul.
- Uneven rating within the diodes required for the convertor.

1.2.2 Flying Electrical Device Construction Convertor

As another for the diode clamped electrical converter is that the electrical device clamped electrical converter planned by Meynard and Foch, that shared several of the benefits. The structure of the electrical device clamped {inverter|electrical convertor} is analogous thereto of the diode clamped converter.

The most distinction is that the diodes used for the clamping area unit replaced by capacitors. A Flying electrical device convertor leg circuit is shown in Figure 1.2. For this topology the foremost common application is static volt-ampere generation.

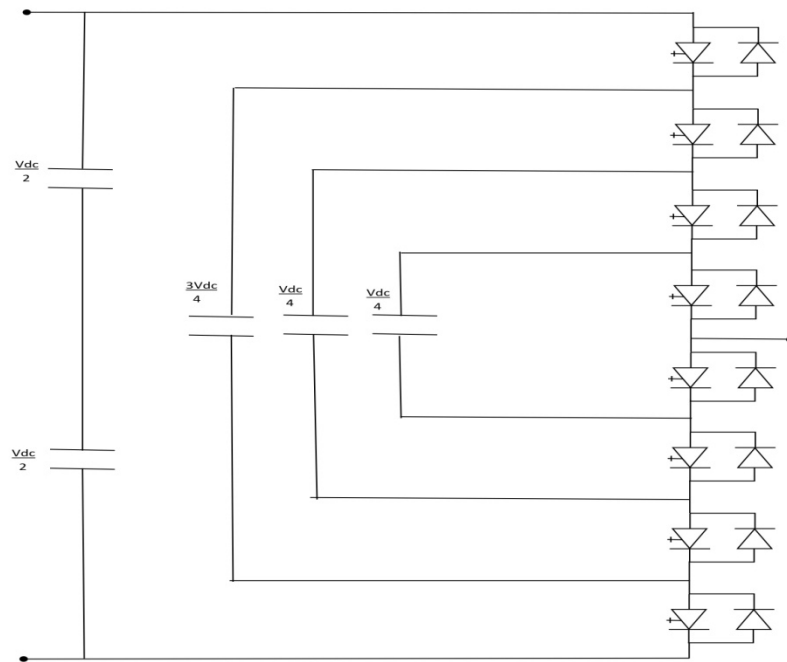


Figure 1.2 One part 5-level structure of a Flying Capacitor Inverter

The main blessings and advantages and disadvantage of this topology are:

Advantages

- Management of the important and reactive power transmission.
- The big amounts of capacitors enable the electrical converter to handle voltages drops and spikes, and short outages.
- Redundancies within the change states square measure obtainable so as to balance the voltages within the capacitors.

Disadvantages

- Potency is reduced for real power transmission.
- The big quantity of capacitors is dearer and ponderous than the diodes within the neutral purpose clamped electrical converter. Conjointly packaging is a problem in high range of level converters.
- Initialisation of the system and pre charging the electrical device voltages may be a advanced procedure.

1.2.3 Cascade Voltage Supply

The cascaded construction electrical converter is predicated on the series association of single leg or double leg (H bridges) inverters with separate DC sources or capacitors. for every of those 2 sorts of configurations many states exist relating to to the switches states. Figure 1.3, the one leg unit, has two states for every of the 2 attainable current(s) directions whereas the double unit has four states.



Fig

ure 1.3: Left: Single Leg Unit, Right Double Leg Unit

The main blessings advantages and disadvantage of this topology are:

Advantages

- The modularized structure permits straightforward packaging and storage.
- The amount of attainable voltage levels is quite double the quantity of capacitors within the double leg unit (H bridge).

Disadvantages

- Separated DC sources or electrical device square measure needed for every module.
- A additional advanced controller is needed thanks to the number of capacitors, which require to be balanced.

Summary

The project proposes a change frequency that meets the 2 needed criteria: low enough to take care of price feasibility, and high enough to achieve a harmonic performance target. To boot, this work proposes Associate in Nursing analytic expression for the output voltage spectrum of the convertor, that allows prediction of harmonic performance.

CHAPTER 2

LITERATURE SURVEY

2.1 LITERATURE SURVEY

Comparison of the traditional CHB five-level inverters with different inverters is self-addressed during this literature survey.

E. Villanueva et al [2009] developed a single-phase cascaded H-bridge convertor for a grid-connected electrical phenomenon (PV) application. The construction topology consists of many H-bridge cells connected nonparallel, every one connected to a string of PV modules. The adopted management theme permits the freelance management of every dc-link voltage, enabling, during this method, the trailing of the utmost electrical outlet for every string of PV panels. to boot, low ripple sinusoidal-current waveforms square measure generated with virtually unity power issue.

The convertor options many blessings like the generation of high-quality currents, the capability to work at a lower change frequency than a two-level convertor, and therefore the modularity that may scale back the value of the answer

S. Kouro et al [2010] conferred a quick summary of well-established construction converters powerfully homeward to their current state in industrial applications to then center the discussion on the new converters that have created their method into the business. Additionally, new promising topologies were mentioned. Recent advances created in modulation and management of construction converters was conjointly self-addressed. An excellent a part of this paper was dedicated to show untraditional applications hopped-up by construction converters and the way construction converters have become Associate in Nursing

sanctionative technology in several industrial sectors. Finally, some future trends and challenges within the more development of this technology were mentioned to inspire future contributions that address open issues and explore new prospects.

M. Bronislaw Malinowski et al [2010] conferred a survey of various topologies, management ways and modulation techniques employed by cascaded construction inverters. The cascaded construction inverters had evolved from a theoretical thought to real applications thanks to many exceptional options sort of a high degree of modularity, the chance of connecting on to medium voltage, high power quality, each input and output, high handiness, and therefore the management of power flow within the regenerative version.

Regenerative and advanced topologies were conjointly mentioned. Applications wherever the mentioned options play a key role square measure shown. Finally, future developments were self-addressed.

F. Khoucha et al [2010] projected hybrid cascaded H-bridge construction motor drive direct torsion management (DTC) theme for electrical vehicles (EVs) or hybrid EVs. The management technique was supported DTC in operation principles. The stator coil voltage vector reference is computed from the stator coil flux and torsion errors obligatory by the flux and torsion controllers. This voltage reference is then generated employing a hybrid cascaded H-bridge construction electrical converter, wherever every section of the electrical converter is enforced employing a dc supply, which might be obtainable from fuel cells, batteries, or ultra-capacitors. This electrical converter provides nearly curving voltages with terribly low distortion, even while not filtering, exploitation fewer change devices. Additionally, the construction electrical converter will generate a high and glued change frequency output voltage with fewer change losses, since solely the little power cells of the electrical converter operate at a high change rate.

Therefore, a high performance and conjointly economical torsion and flux controllers square measure obtained, sanctionative a DTC answer for multilevel-inverter-powered motor drives.

S. Vazquez et al [2010] projected many management and modulation techniques for construction cascaded H-bridge (CHB) power convertor topology. During this paper, the steady-state power balance within the cells of a single-phase two-cell CHB is studied. The aptitude to be equipped active power from the grid or to deliver active power to the grid in every cell is analyzed per the dc-link voltages and therefore the desired ac output voltage worth. the boundaries of the utmost and minimum input active powers for a stable operation of the CHB square measure self-addressed. The conferred Associate in Nursing analysis is an applicable tool to determine the planning criteria for the 2C-CHB synchronous rectifier or succeeding application.

J. Napoles et al [2013] a new control strategy, based on the SHM-PWM technique that can tolerate different capacitor voltage levels for Cascaded H-Bridge Multilevel Converters. In comparison with other techniques, in this case it is possible to control the amplitude of each cell under balanced or unbalanced conditions with a reduced number of lookup tables while still manufacturing terribly high quality waveforms at low change frequency. Associate degree example of associate degree application which can take pleasure in such a theme is during a structure UPS. During this case the technique might be able to meet grid voltage standards even once the batteries square measure charged to completely different voltages. The experimental results support that the strategy {in a|during a|in associate degree exceedingly |in a very} twocell convertor validates the technique for an imbalance vary from third to 100%.

J. Chavarria et al [2013] planned associate degree energy balance management strategy for a cascaded single phase grid connected Hbridge structure electrical converter linking n freelance electrical phenomenon (PV) arrays to the grid. The management theme was supported associate degree energy sampled information model of the PV system and allows the look of a voltage loop linear separate controller for every array, guaranteeing the soundness of the system for the full vary of PV array operative conditions. The management style was tailored to phase shifted and level shifted carrier pulse dimension modulations to share the management action among the cascade connected bridges so as to

at the same time synthesize a structure wave and to stay every of the PV arrays at its most power operative purpose.

An FPGA based style operative at a lower change frequency to cut back change losses would be envisaged for the PSPWM case however would result tougher if LSPWM is adopted since the bottom change frequency is restricted by each the magnitude relation rotating frequency/grid frequency and also the management action resolution supported by the FPGA platform.

G. Farivar et al [2016] planned a cascaded HBridge (CHB) structure convertor primarily based electrical phenomenon (PV) system with no voltage or current sensors at the dc side. The most good thing about eliminating the dc side Page 1 sensors simplifies the hardware, resulting in lower value and better responsibility of the PV system. a unique theme estimating the capacitors' voltages from the output ac voltage of the electrical converter was developed. The theme permits commutation all dc side voltage sensing elements by one voltage sensor at the ac side of the convertor. what is more, the dc current sensors, conventionally needed for the utmost power following (MPPT) were additionally eliminated. Instead, the outputs from the capacitors' voltage management systems square measure utilised for the MPPT.

The operation of the planned system beneath the change device failure has to be studied very well within the future to enhance the responsibility of the system.

M. movie maker et al [2016] planned a sophisticated management strategy for grid tied electrical phenomenon (PV) cascaded H bridge (CHB) electrical converter. The circuit topology consists of a correct range of power cells (H bridge configuration) connected serial and equipped by individual PV modules. The adopted management technique was a mixed stairs PWM technique performed by suggests that of a algorithmic program to work out cells' change state. The cells' state was associated with the requirement of charging or discharging a selected cell far more than the others by calculative the voltage error at every dc link (e.g. by considering the distinction between the MPPT reference and also the measured quantity). An avid P&O MPPT permits to manage severally

the voltage of every dc link, therefore increasing the facility extraction even in mate conditions. The management section is enforced on FPGA by employing a dSPACE real time hardware platform, therefore getting absolutely dedicated digital circuits.

G. Farivar et al [2016] introduced a cascaded Hbridge structure convertor (CHBMC) primarily based StatCom system that was able to operate with very low dc capacitance values. The theoretical limit is calculated for the utmost electrical device voltage ripple, and therefore minimum dc capacitance values which will be utilized in the convertor. The planned low capacitance StatCom (LCStatCom) was able to operate with massive electrical device voltage ripples, that square measure terribly on the point of the calculated theoretical most voltage ripple. The utmost voltage stress on the semiconductors within the LCStatCom is less than during a typical StatCom system. The variable cluster voltage magnitude in the LC-StatCom system drops well below the maximum grid voltage, which allows a fixed maximum voltage on the individual capacitors.

A high-bandwidth control system is designed for the proposed StatCom to provide control of the capacitor voltages during highly dynamic transient events. The required energy storage for the LC-StatCom system shows significant reduction compared to a conventional StatCom design.

2.2 EXISTING SYSTEM- CONSTRUCTION CASCADE Dc to DC BOOST DEVICE

The construction cascade dc to dc boost device is that the extension topology of single level boost device. The utilization of construction device is to boost the conversion quantitative relation and potency of the device. The most advantage of the construction topology is that the voltage conversion quantitative relation is directly increased by the addition of levels. The construction cascade dc to dc boost device is illustrated in Figure 2.1, the input supply of boost device is denoted as V_s . The 1th level of the dc to dc device inductance, diode, switch and condenser area unit denoted as L_1 , D_1 , S_1 and C_1 severally.

Then, the ordinal level of the device parts area unit denoted as L_n , D_n , atomic number 50 and C_n severally. Once the switches ($S_1, S_2 \dots S_n$) ON in Figure 2.1, the inductors $L_1, L_2, \dots L_n$ area unit connected to the input voltage (V_s).

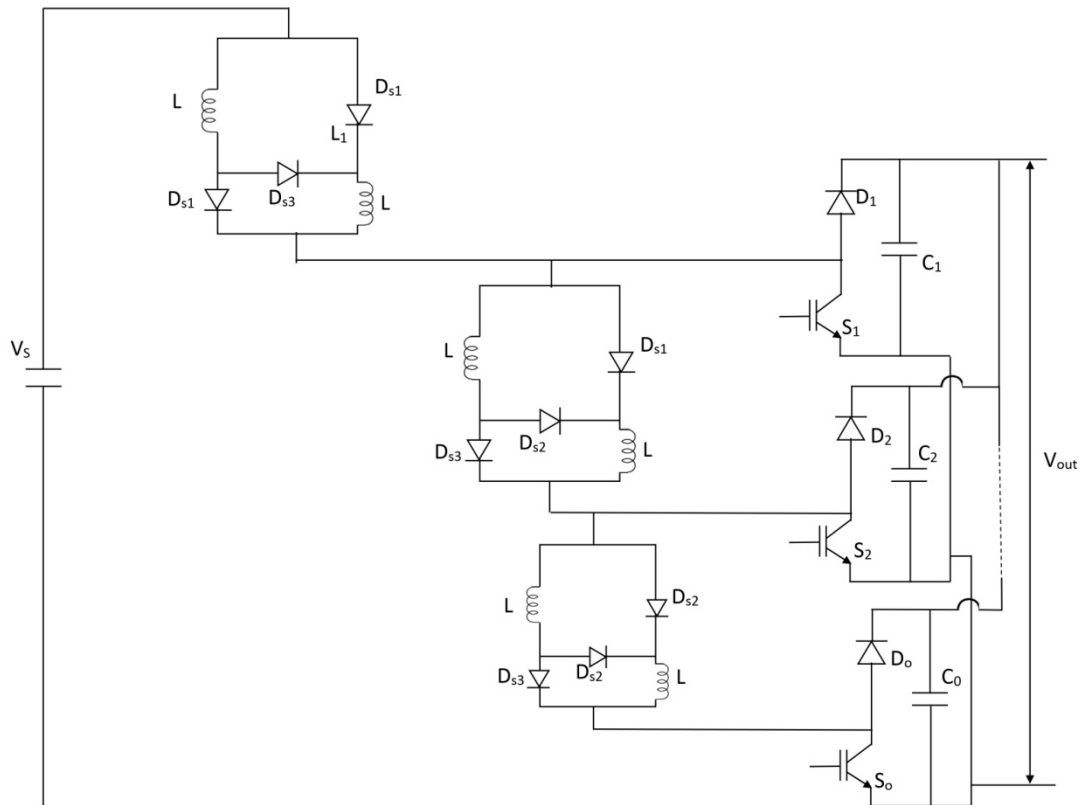


Figure 2.1 Structure of cascade DC-DC boost device

The output voltage of C_1 is smaller than voltage through $D_2, \dots D_n$. At identical time, the negative level of voltages of $C_2, \dots C_n$ is adequate the positive level worth of C_1 . Hence, the whole voltage across $C_2 \dots C_n$ is smaller than C_1 . throughout the turns off condition of switches, the inductance current is closed to D_1 of all switched diodes. Throughout the throw condition, the inductance current closes D_1 charging C_1 and therefore the output voltage level is resulted because the device voltage. The voltage on the C_1 is adequate the summary voltage on the input supply and therefore the voltage level of $C_2 \dots C_n$. Thus, it's potential to attain high voltage gain against the duty cycle. But, once embrace the switched inductance circuit; the shift frequency level is restricted with high gain.

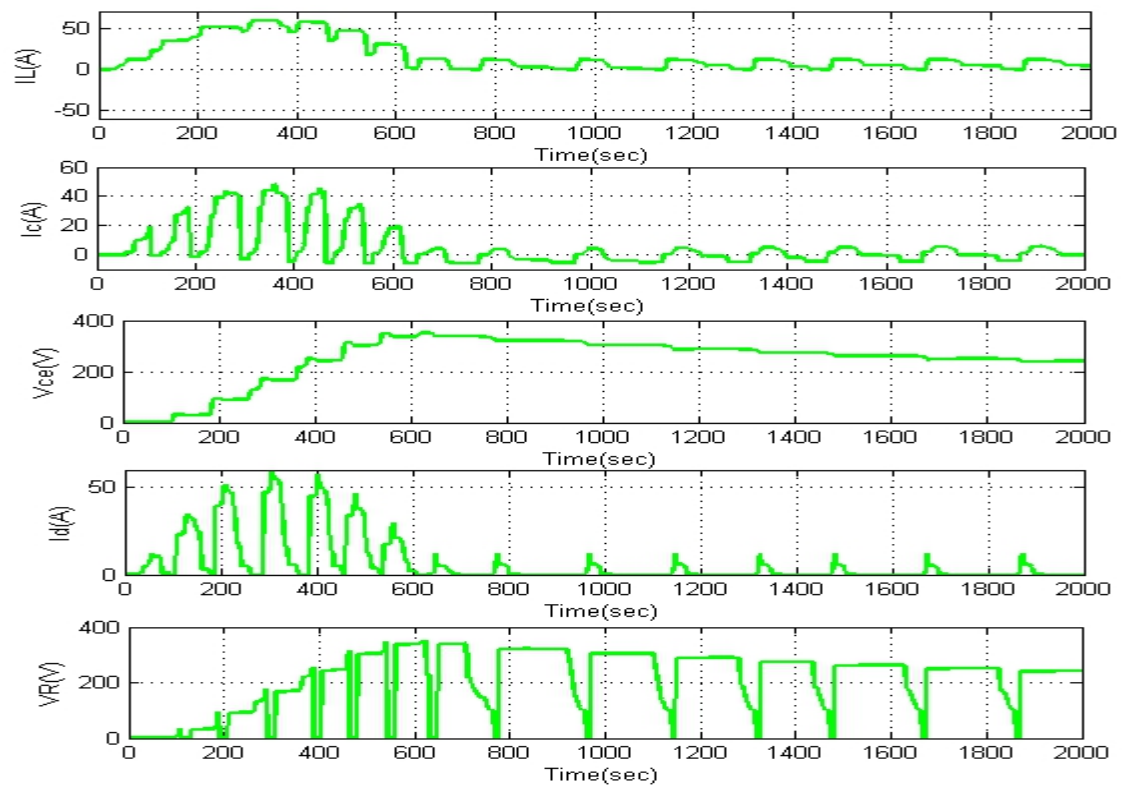


Figure 2.2: Output voltage, current waveforms of the boost electrical converter

Drawbacks

- It wants further boost device.
- The voltage stress is high.
- Its having discharge electrical phenomenon downside thanks to boost device.
- Higher Doctor of Theology thanks to 3 level output voltage.

CHAPTER 3

PROPOSED SYSTEM

3.1 INTRODUCTION

This project presents a single-phase 5 level Pulse dimension Modulation (PWM) electrical converter. The planned electrical converter has the advantage of mistreatment less variety of parts. 2 carrier signals the image of associate degree other with an offset admire the amplitude of the triangular carrier signal area unit accustomed generate PWM signals for the switches. Some switches operate at fundamental et al operate at shift frequency. Operational principles with shift functions area unit analyzed. Simulation and experimental results are done to demonstrate the validity of the planned electrical converter. Switches signals area unit generated mistreatment dspic30F4011 controller.

3.2 PLANNED SYSTEM DIAGRAM

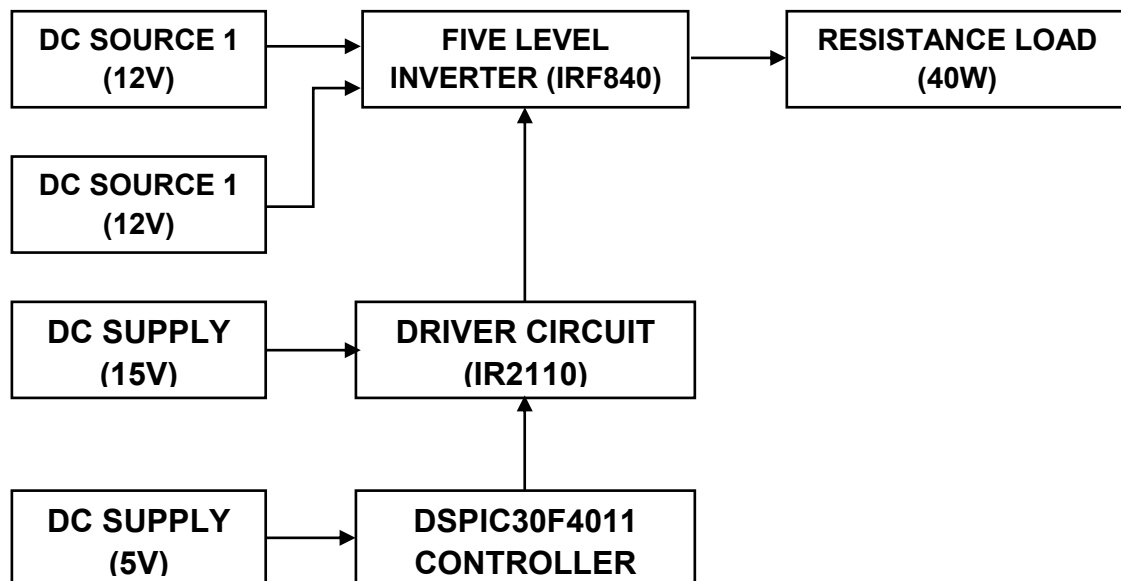


Figure 3.1: diagram of cascade 5 level electrical converter

3.3 PLANNED SYSTEM CIRCUIT DIAGRAM

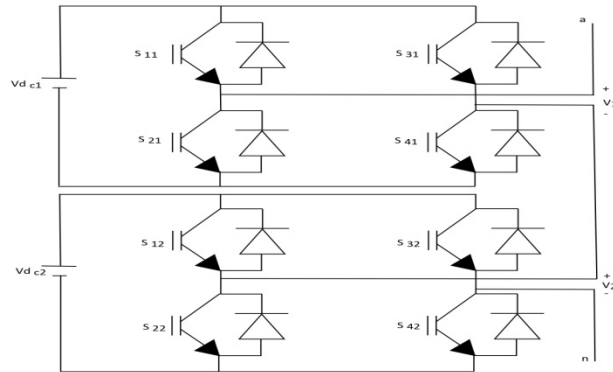


Figure 3.2: Circuit diagram of cascade 5 level electrical converter

3.3.1 H-Bridge Inverter

Here the MOSFET (IRF840) primarily based 2 full bridge electrical converter circuit is cascaded for this five-level electrical converter. 3 switches additionally connected with this H bridge electrical converter circuit. The snubber circuit (RC) is connected across all the switches for safeguarding the shift devices from dv/dt and di/dt ratings.

3.3.2 DSPIC30F4011 Controller

This controller is employed for generating the PWM signals for each the H bridge electrical converter circuit and therefore the bifacial shift devices. The embedded program is developed for generating the PWM signals.

3.3.3 Load

During this project the output power level of the electrical converter is 40W. The utmost output voltage level of the electrical converter is twenty four volts. For this power rating we are able to use lamp or tiny size motors. This project enforced in a very image.

The voltage levels of 5 levels area unit (V_{dc} , $V_{dc}/2$, 0, $-V_{dc}/2$, $-V_{dc}$) From the DC offer. During this configuration solely 2 sources is employed. Thus

this technique of configuration is named as symmetrical construction electrical converter. The electrical converter level is set by each the modulation index and therefore the applied DC the electrical converter. By adjusting the various voltage level additionally ready to able to increase the amount of levels of the electrical converter. A DSPIC controller is employed for generating the PWM signals to the electrical converter circuit. The shift devices utilized in this Single-phase electrical converter area unit MOSFET (IRF840).

3.4 FIVE LEVEL ELECTRICAL CONVERTING OPERATING

This planned circuit consists of 2 full bridge electrical converter with 2 DC isolated power offer. By correct shift we are able to get the precise 5 level output voltage. The sequences area unit given below Table 3.1.

Table 3.1 Five Level electrical converter Tabulation

S11	S21	S12	S22	S32	S42	V1	V2	Vn
1	0	1	0	0	1	+Vdc	+Vdc	+2Vdc
1	0	1	0	1	0	+Vdc	0	+Vdc
1	0	0	1	1	0	+Vdc	-Vdc	0
0	1	1	0	0	1	-Vdc	+Vdc	0
0	1	1	0	1	0	-Vdc	0	-Vdc
0	1	0	1	1	0	-Vdc	-Vdc	-2Vdc

- Maximum positive output (2Vdc): S11,S41 is ON, connecting the load positive terminal to Vdc, and S12,S42 is ON, connecting the load negative terminal to ground. The switches S11, S41,S12,S42 area unit ON the voltage applied to the load terminals is 2Vdc.
- Positive output (Vdc): The switches S11, S41 are ON, the voltage applied to the load terminals is Vdc.
- Zero level: All the switches area unit off condition

- Negative output ($-V_{dc}$): The switches S31, S21 are ON, the voltage applied to the load terminals is $-V_{dc}$.
- Maximum negative output ($-2V_{dc}$): S31, S21 is ON, connecting the load positive terminal to V_{dc} , and S32, S22 is ON, connecting the load negative terminal to ground. The switches S31, S21, S32, S22 are unit ON the voltage applied to the load terminals is $-2V_{dc}$.

3.5 PWM GENERATION

The most common and standard technique of digital pure-sine wave generation is pulse dimension modulation. The PWM technique involves generation of a digital wave form, that the duty cycle is modulated specified the typical voltage of the wave form corresponds to a pure wave. The only manner of manufacturing the PWM signal is thru comparison of a low-power reference wave with a triangle wave. Multicarrier PWM ways uses high shift frequency carrier waves as compared to the reference waves to get a curved output wave. The Figure 3.3 shows multicarrier PWM wave form for cascaded construction electrical converter.

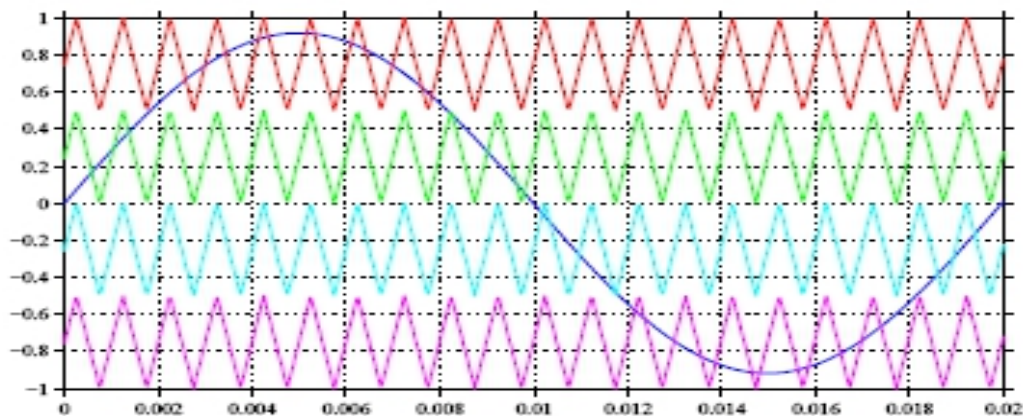


Figure 3.3 Multicarrier PWM generation for the electrical converter

Multicarrier PWM technique is simulated as per the circuit shown within the Figure 3.3. Normally electrical converter with m -level, $m-1$ carrier with same frequency f_c and same peak to peak amplitude A_c are unit disposed. The reference or modulation wave form has peak to peak amplitude A_r and

francium frequency f_r . The reference wave form is compared with carrier signals and if it's larger than a carrier signal then switch/device correspond to it carrier is switched on and if the reference is a smaller amount than carrier signals then device correspond to carrier is shifted. The curved pulse dimension modulation is often utilized in Industrial application. The francium frequency of reference signal f_r determines the electrical converter output frequency F_O and its peak amplitude A_r controls the modulated index M and so successively the rms output voltage V_o . Here the modulation index is outlined because the magnitude relation of amplitude of reference signal to the amplitude of carrier signal. The rms output voltage will varied by variable the modulation index M . If δ is that the dimension of every pulse then rms output voltage is found from $V_o = V_s \sqrt{((p\delta)/(\pi))}$.

Summary

The planned electrical converter has the advantage of exploitation less range of elements. 2 carrier signals the image of one {another} with an offset akin to the amplitude of the triangular carrier signal area unit accustomed generate PWM signals for the switches.

Some switches operate at harmonic et al operate at shift frequency. Operational principles with shift functions area unit analyzed.

CHAPTER 4

SIMULATION AND HARDWARE RESULTS

4.1 PLANNED SYSTEM SIMULATION

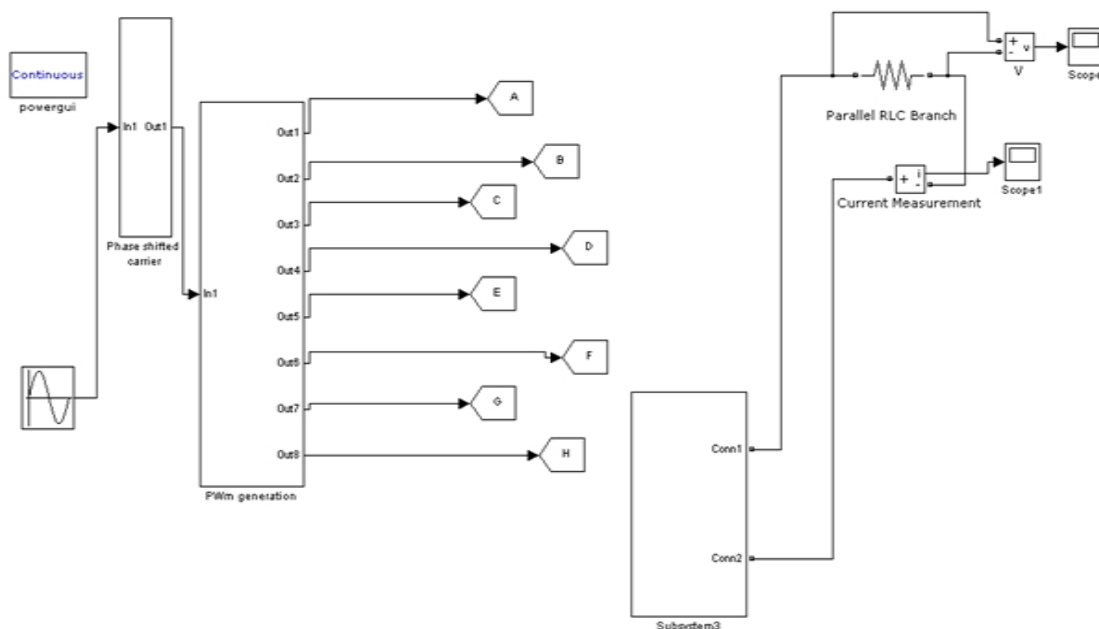


Figure 4.1 *Matlab simulation of fevel level cascade*

The 5 levels Cascaded H-Bridge structure electrical converter with and while not OTT filter is intended victimization Matlab-Simulink. Shows the heart beat generation for MLI circuit is obtained by comparison the curved undulation with triangular undulation and also the triangular wave adscititious with constant.

4.1.1 Simulation 5 Level Output Voltage

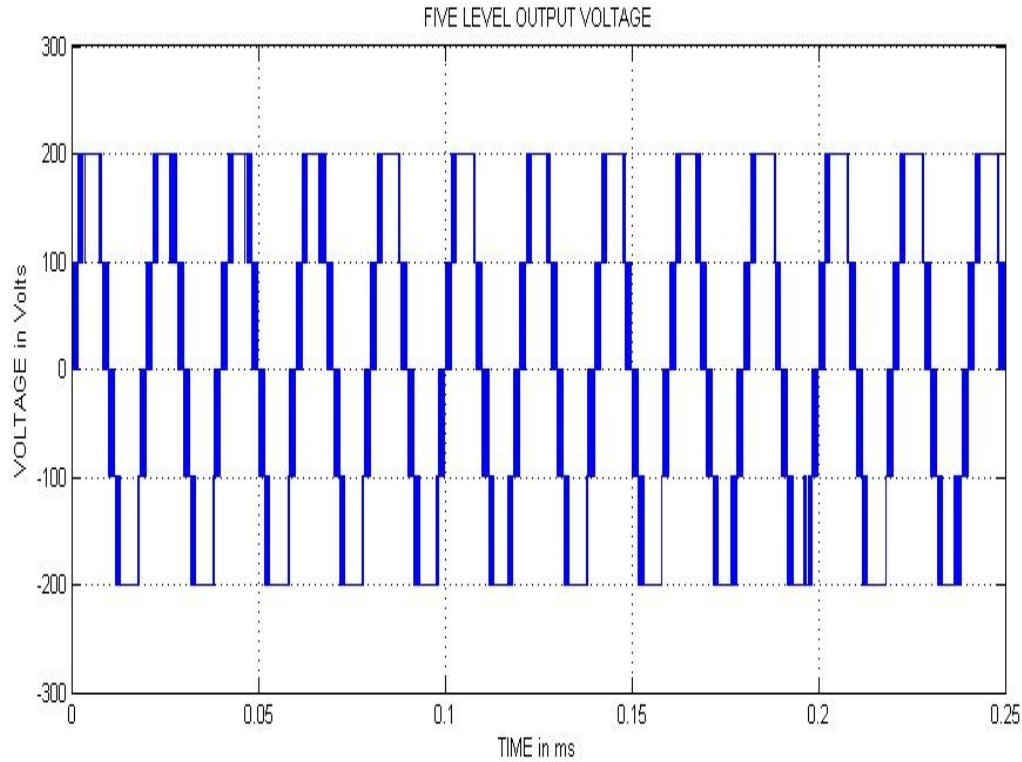


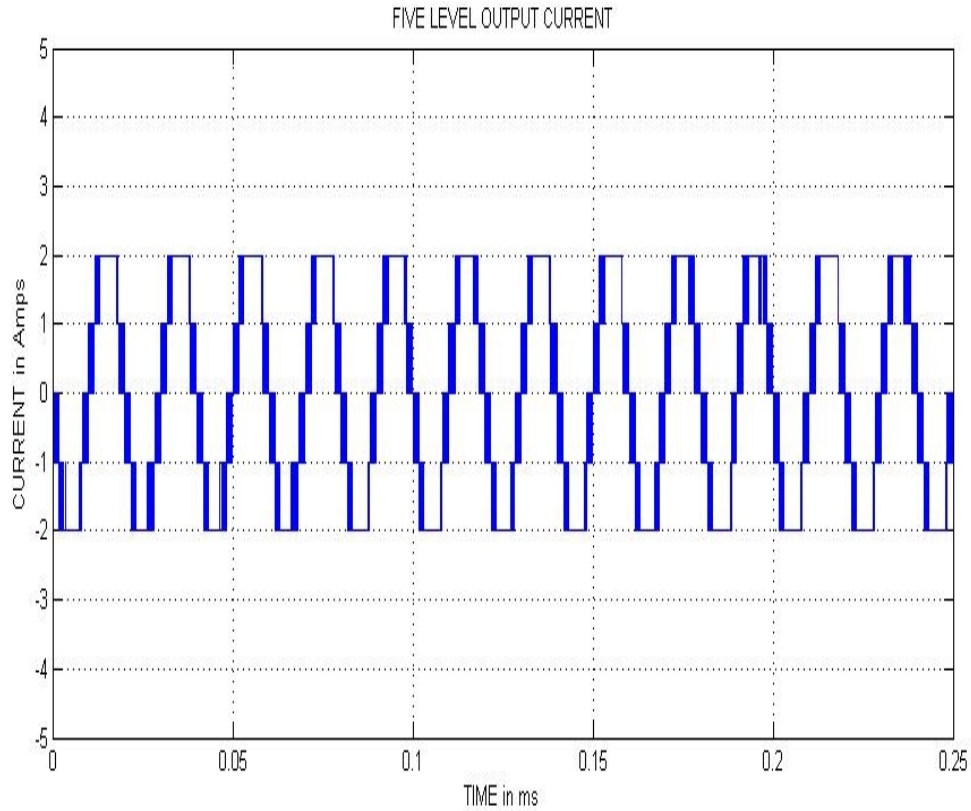
Figure 4.2 Five level output voltage

The heart beat generation to the switches Q1, Q2, Q5 and Q6, by comparison the carrier signal (Triangular waveform) and also the reference signal (Sinusoidal waveform). The heart beat to be generated by comparison 2 the 2 triangular wave with positive [*fr1] cycle of the curved undulation and also the remaining two triangular wave with negative [*fr1] cycle of the curved undulation.

The input curved voltage with 50Hz and also the angular frequency is used with amplitude voltage 200V.

Thus the input voltage is $V_s = V_m \sin \omega t$

4.1.2 Simulation Output Current Waveform



The output undulation is obtained within the pulse generation of assorted switches Q1, Q2, Q5 and Q6 is shown. The doctor's degree of the output AC voltage is zero.25 is obtained shows the pulses of the switches Q1, Q2, Q5 and Q6 and also the output voltage across R Load with OTT filter. Thus, pure curved output is obtained by victimization the OTT filter with reduced doctor's degree of zero.25.

Figure 4.3 Five level output current

4.2 HARDWARE VIEW

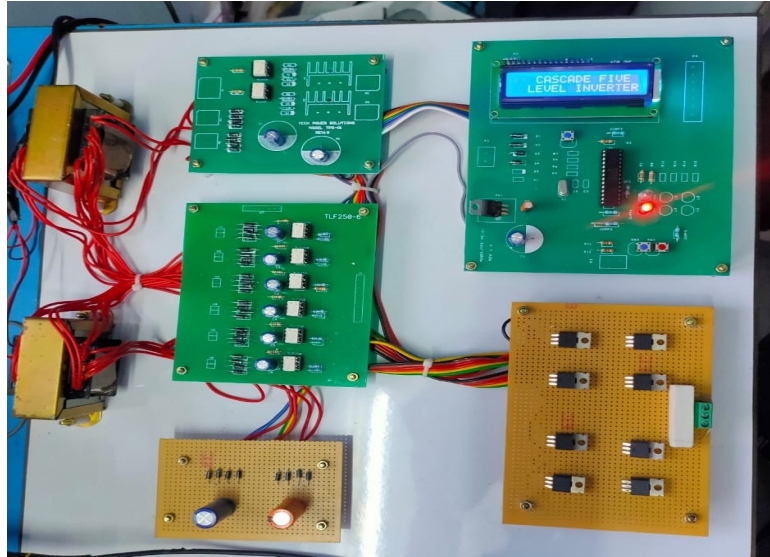


Figure 4.4 Five level cascade hardware view

In the hardware epitome a offer voltage of 230V is stepped all the way down to 12V employing a transformer, that is then remodeled to DC employing a diode bridge rectifier. The corrected voltage is then fed to the transformer IC, that regulates the voltage to 5V and it's fed to microcontroller as offer. The specified elements for hardware setup of electrical device, PIC microcontroller, bridge rectifier, transformer, H-bridge rectifier, optocouple.

4.2.1 Hardware Output Voltage Waveform

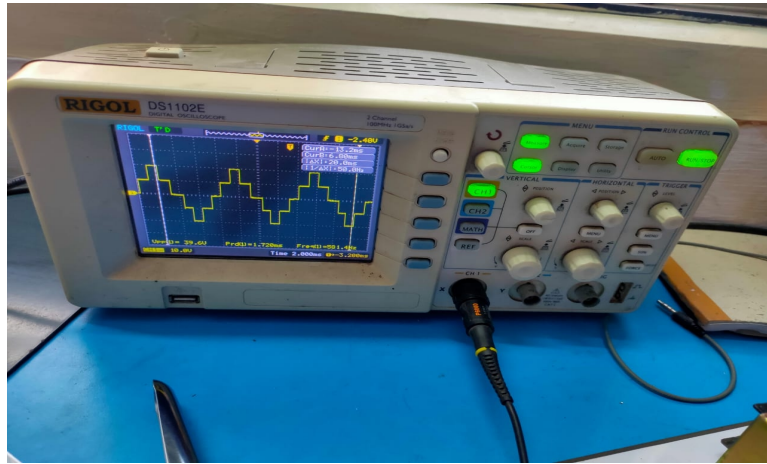


Figure 4.5 Five level output waveform

During this topology 5 level output voltage is obtained by reduced range of switches compared to it of typical cascaded H-Bridge structure electrical converter. Switches S1- S3 are change at the speed of the carrier signal frequency whereas S4 and S5 can operate at a frequency adore the basic frequency.

CHAPTER 5

HARDWARE IMPLEMENTATION

5.1 DSPIC302010 CONTROLLER

Microchip Technology's control & Power Conversion family of dsPIC Digital Signal Controllers provides AN easy-to-use answer for applications requiring control. The dsPIC family of Digital Signal Controllers options a fully-enforced digital signal processor (DSP) engine, thirty unit of measurement non-pipelined performance, compiler friendly style, and a well-recognized Microcontroller design and style surroundings. The twenty new dsPIC30F4011 devices type 3 product families targeting control and power conversion, sensor, and all-purpose applications. The dsPIC core may be a 16-bit (data) non-pipelined changed Harvard machine that mixes the management blessings of a superior 16-bit Microcontroller with the high computation speed of a totally enforced DSP to supply a tightly coupled, single-chip single-instruction stream answer for embedded systems styles. The initial 20-dsPIC30F4011 devices feature twelve Kbytes to one hundred forty four Kbytes of on-chip secure Flash program memory house and up to eight Kbytes

5.1.1 *Control PWM Module in DSPIC*

The DSPIC control PWM module is optimized for applications, like 3-phase AC induction motors, 3-phase brushless DC motors, and switched reluctance motors.

The control PWM module has either vi or eight output pins and three or four PWM generators, relying upon the device. The output pins could also be organized as complementary output pairs or as freelance outputs.

Essential PWM operative parameters, like output polarity, area unit programmed in non-volatile memory for safety. The non-volatile choices cut back the chance of putting the PWM outputs in a very state which may injury the ability devices connected to Peripheral.

5.2 DSPIC SMALL CONTROLLER OPTIONS

5.2.1 *High Performance Changed Architecture Computer Hardware*

- Modified Harvard design
- C compiler optimized instruction set design with versatile addressing modes
- 24-bit wide directions, 16-bit wide knowledge path
- 48 Kbytes on-chip Flash program area (16K Instruction words)
- 2 Kbytes of on-chip knowledge RAM
- 1 Kbytes of non-volatile knowledge EEPROM

5.2.2 *Control PWM Module Option*

- Six PWM output channels
 - Complementary or freelance Output modes
 - And Center Aligned modes
- Three duty cycle generators
- Dedicated time base
- Programmable output polarity
- Dead-time management for Complementary mode
- Manual output management
- Trigger for A/D conversions

5.2.3 *Peripheral Option*

- High current sink/source I/O pins: twenty five mA/25 mA
- Timer module with programmable presale
- Five 16-bit timers/counters; optionally combine
- 16-bit timers into 32-bit timer modules
- 16-bit Capture input functions
- 16-bit Compare/PWM output functions
- 2 UART modules with FIFO Buffers
- 1 will modules, 2.0B complain

5.2.4 *Input Capture Module*

This section describes the Input Capture module and associated operational modes. The options provided by this module area unit helpful in applications requiring frequency (Period) and Pulse mensuration.

5.2.5 *USART*

USART stands for the Universal Synchronous/Asynchronous Receiver/Transmitter. It's going to sound mysterious, however really, this can be the foremost frequent communication device used nowadays throughout the pc world: small controllers, (some) cell phones, barcode readers, PCs...First, allow us to see what all those words stand for:

- Universal implies that it is used with a large scope of devices
- Synchronous/Asynchronous shows whether or not the devices that communicate with Associate in Nursingother} need an external synchronization line (the clock). This device, gift in most PICs, will bang each ways in which. The Asynchronous mode (without the common

clock) is less complicated to implement, though it's typically slower than the synchronous

- Receiver/Transmitter implies that this device will receive and transmit (send) knowledge at the same time. It's additionally known as the two-way or duplex communication.

5.3 MOSFET

- This N-Channel sweetening mode Si gate power field result semiconductor device is a complicated power MOSFET designed, tested, and bound to face up to a fixed level of energy within the breakdown avalanche mode of operation.
- The invention of the ability MOSFET was part driven by the constraints of bipolar power junction transistors (BJTs), which, till recently, was the device of selection in power physical science applications.
- All of those power MOSFETs area unit designed for applications like change regulators, change converters, motor drivers, relay drivers, and drivers for prime power bipolar change transistors requiring high speed and low gate drive power.

5.3.1 *Features of MOSFET*

1. MOSFET has lower change losses however its on-resistance and physical phenomenon losses area unit additional.
2. MOSFET may be a voltage-controlled device.
3. MOSFET has positive temperature co-efficient for resistance. This makes simultaneous operation of MOSFET straightforward. If a MOSFET shares accumulated current at the start, it heats up quicker its resistance rises and this accumulated resistance causes this current to shift to different devices in parallel
4. In MOSFET secondary break down doesn't occur, as a result of it's positive temperature co-efficient.

5. MOSFET's in higher voltage ratings have additional physical phenomenon losses.

5.4 POWER SUPPLY

Here area unit many sorts of power offer. Most area unit designed to convert the Voltage AC Mains electricity to an acceptable low voltage offer for electronic Circuits and different Devices. An influence offer will by lessened into a series of blocks, every of that performs a specific operate. Here the AC offer main is given to the transformer. The electrical device having the various voltages.

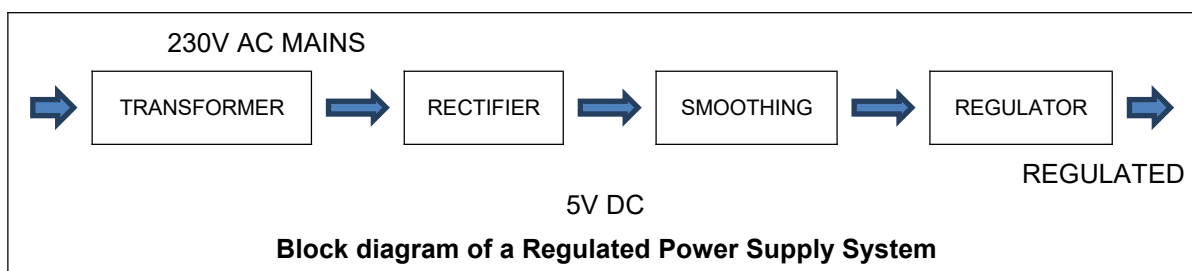


Figure 5.1: Diagram of regulated power offer

The output from the electrical device is given to the rectifier circuit. During this rectifier circuit the AC voltage is regenerate to DC voltages. The corrected DC voltage is given to the regulator circuit. The output of the regulator is relying upon the regulator IC chosen within the circuit.

5.4.1 Bridge Rectifier

A bridge rectifier is created victimisation four individual diodes, however it's additionally offered in special packages containing the four diodes needed. It's known as a rectifier. Smoothing is performed by an outsized price condenser connected across the DC offer to act as a reservoir, provision current to the output once the varied DC Voltage from the rectifier is falling.

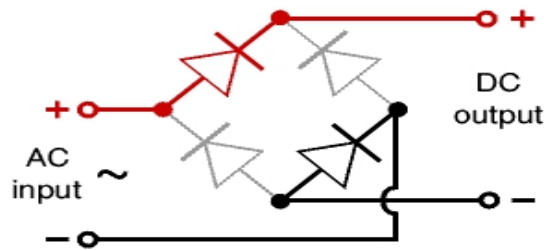


Figure 5.2 Bridge Rectifier

The Figure 5.2 shows the wrinkled DC, ironed DC by the filter capacitors. The electrical condenser charges quickly close to the height of the varied DC, and so discharges because it provides current to the output.

Note that smoothing considerably will increase the typical DC voltage to virtually the height price ($1.4 \times$ RMS value). As an example, 6V RMS AC is corrected to full wave DC of regarding four.6V RMS (1.4V is lost within the bridge rectifier), with smoothing this increase to virtually the height price giving $1.4 \times 4.6 = 6.4\text{V}$ swish DC. Smoothing isn't excellent because of the electrical condenser voltage falling a bit because it discharges, giving a little ripple voltage. For several circuits a ripple that is 100% of the availability Voltage is satisfactory and therefore the equation below provides the desired price for the Smoothing electrical condenser. a bigger electrical condenser can provide less ripple. The electrical condenser price should Be doubled once smoothing half-wave DC.

5.4.2 Regulator

Voltage regulators ICs square measure on the market with fastened (typically five, twelve and 15V) or variable Output voltages. They're additionally rated by the most current they'll pass. Negative Voltage regulators square measure on the market, in the main to be used in twin provides. Most regulators embrace some automatic protection from excessive current ('overload protection') and warming ('thermal protection').

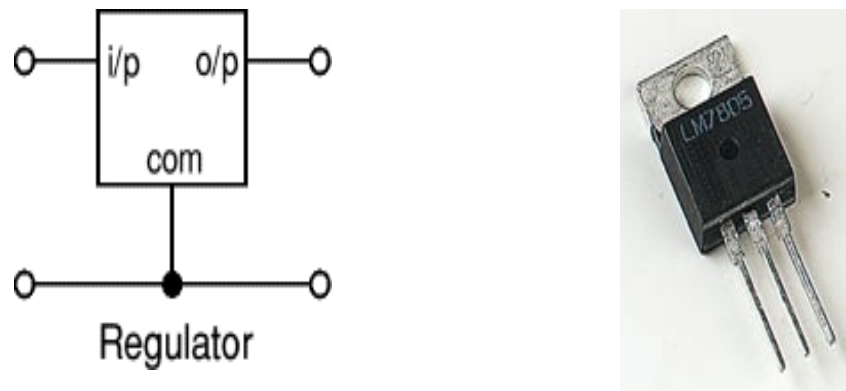


Figure 5.3 Regulator & IC

Many of the fastened transformer ICs has three leads and appearance like power transistors, like the 7805 +5V 1A regulator shown Figure 5.3 on the proper. They embrace a hole for attaching a conductor if necessary.

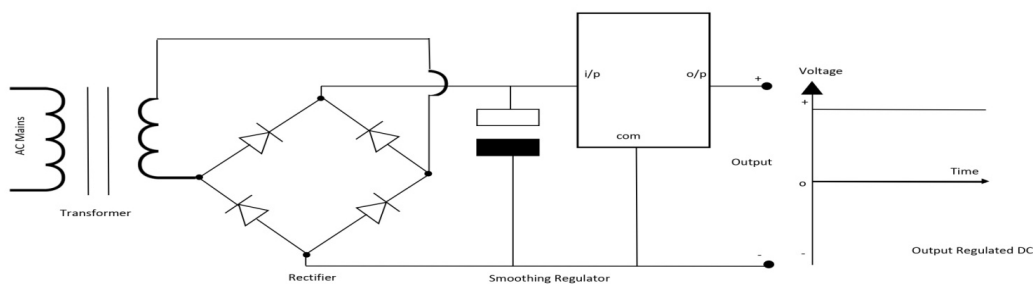


Figure 5.4: Rectifier circuit diagram and wave type

The higher than Figure 5.4 shows the rectifier circuit diagram and also the regulated output voltage. The regulated DC output is extremely swish with no ripple. It's appropriate for all electronic circuits. In typically there square measure 2 kinds of regulators square measure used. Specifically the positive and negative sort regulators. For positive sort regulators 78** series of regulators square measure used. For negative sort regulators 79** series of regulators square measure used. Depends upon the voltage and sort of the voltage the regulator IC is chosen.

5.4.3 Opto Isolator

The below fig 5.6 shows the driving force circuit diagram. IR2110 IC is employed to drive the MOSFET'S. The output of the opto-isolator is given to the IR2110 ic. There square measure 2 output signals square measure generated from the drive ic specifically each the output pulses square measure inverted to every different. The electrical phenomenon of the MOSFET is a lot of, that the signals that square measure given to the gate ought to be high gain for that the driving force ic is employed in MOSFET based mostly circuits.

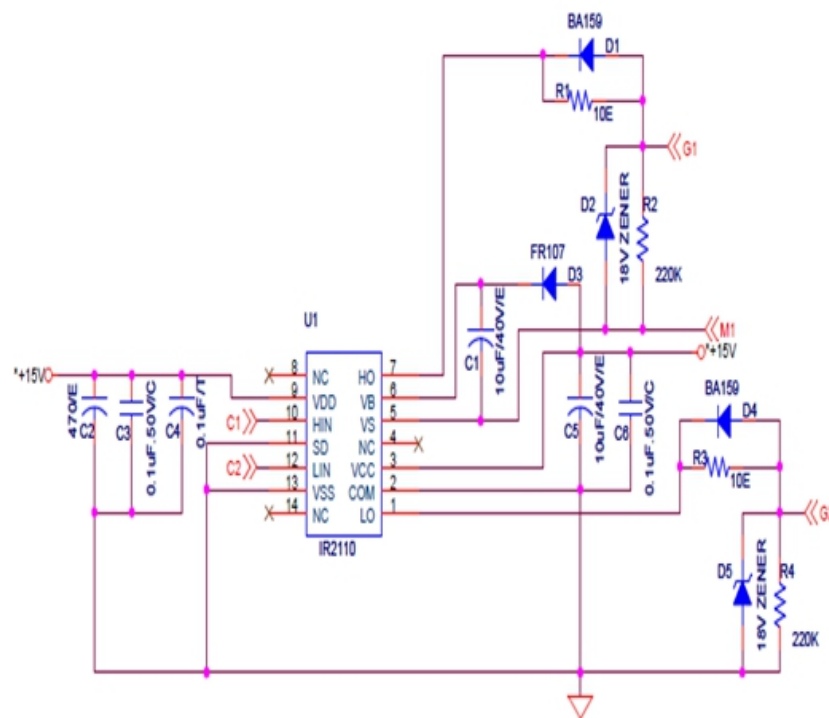


Figure 5.6 Driver circuit diagram

A MOSFET drive circuit is meant to attach the gate on to a voltage bus with no intervening resistance aside from the electrical phenomenon of the drive circuit switch. Gate driver acts as a high-energy buffer stage between the PWM output of the management device and gates of the first power shift MOSFET.

In this project the shift device used is MOSFET IRF 840. The voltage rating is 500v and also the current rating is eight A. Resistance and condenser (RC) snubber circuit is connected across the all the shift devices. This snubber circuits provide the protection to shift devices from the dv/dt and di/dt . One diode additionally connected across the shift devices , this diodes square measure flow

into the present at identical time reverse bias the reverse currents that is flows to the shift devices.

5.4.5 TLP240 Opto-Driver IC

The TLP240 is Associate in Nursing opto isolated gate driver. It options 8mA semiconductor diode drive current whereas the motive force is provided from 20V. This chip is appropriate for driving high speed switch apps, I tested the switch up to 1MHz. the motive force will approach to one.4A to confirm quick gate switch. If the high sides every has Associate in Nursing isolated provide and therefore the low sides have a provide the availability will go as high because the isolation can hold. Appropriate for speed management H-bridge applications. Provided by a 14V (suggested) regulated provide the motive force will switch open collector applications, that is power provides or switch mode power provides among others, however will switch very virtually something junction transistor driven.

Gate driver circuit is circuit integral a part of power physics converters that is employed to drive power semiconductor devices like BJT's, IGBT's and MOSFETs. Output of DC DC converters principally rely upon behavior of gate driver circuits. Its mean if gate driver circuit doesn't drive gate of MOSFET device properly, your designed DC DC device output won't be in step with your demand. So style of gate driver circuit is critically necessary in planning of power physics converters.



Figure 5.8 TLP 240

The on top of fig 5.8 TOSHIBA TLP240 consists of a lightweight emitting diode and a integrated icon detector. This unit is 8-lead DIP package.

TLP240 is appropriate for gate driving circuit of IGBT or power MOS junction transistor.

- Input threshold current: 4mA (max)
- provide current: 11mA (max)
- provide voltage: 10-34V
- Output current: $\pm 1.4A$ (max)
- switch time t_{pLH}/t_{pHL} : zero.4 μs (max)
- Isolation voltage: 2400Vrms (min)

The operate of Opto mechanical device is isolate to the feedback circuit from power circuit. Pulse dimension modulation signal (PWM one to PWM 12) comes from DSPIC Processor. This signal isn't directly fed through an influence circuit. Suppose feedback circuit (DSPIC) is connected to power circuit while not isolation circuit, the feedback circuit might get affected. Therefore we'd like to isolation circuit interface between power circuit and feedback circuit.

Table 5.1 Opto mechanical device Truth Table

INPUT	ENABLE	OUTPUT
H	H	L
L	H	H
H	L	H
L	L	H

CHAPTER 6

CONCLUSION

6.1 CONCLUSION

Multilevel inverters provide improved output waveforms and lower ThD. This project has bestowed a completely unique PWM switch theme for the projected construction electrical converter. During this project just one reference signal and is compared with a triangular wave signal to get the PWM signals. Here 2 DC voltage levels area unit utilized in these multi-level inverters. So, this technique of configuration is thought as symmetrical cascaded electrical converter. By dominant the modulation index and completely different levels of the output voltages achieved. While not victimization any extra passive components, the electrical converter can improve the performance parameters.

6.2 FUTURE SCOPE

As a future scope, construction electrical converter is analyzed for various output levels by dynamic modulation index and switch frequency. By planning appropriate, the full harmonic distortion will any be reduced on the output.

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