

ANALYSIS OF 8-BIT DATA COMPARATOR USING EFFICIENT PIPELINED ARCHITECTURE

Submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering
Degree in Electronics and Communication Engineering

by

S.MADHUMITHA– 37130228

D.MINISHA – 37130251



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION
ENGINEERING**

SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY (DEEMED TO BE UNIVERSITY)

Accredited with Grade “A” by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119

MARCH 2021



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)

Accredited with Grade “A” by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119

www.sathyabama.ac.in



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of S.MADHUMITHA (37130228) and D.MINISHA (37130251) who carried out the project entitled “**ANALYSIS OF 8-BIT DATA COMPARATOR USING EFFICIENT PIPELINED ARCHITECTURE**” under our supervision from September 2020 to March 2021.

Internal Guide

Dr.M.SUMATHI, M.E , Ph.D

Head of the Department

Dr. T. RAVI, M.E., Ph.D.

Submitted for Viva voce examination held on _____

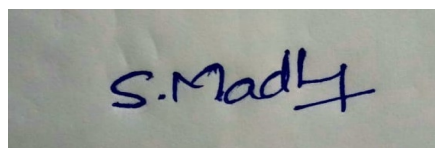
Internal Examiner

External Examiner

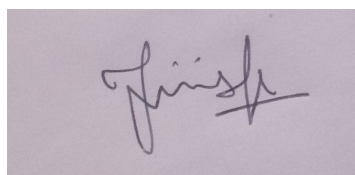
DECLARATION

We, **S.MADHUMITHA (37130228)** and **D.MINISHA (37130251)** hereby declare that the Project Report entitled “**ANALYSIS OF 8-BIT DATA COMPARATOR USING EFFICIENT PIPELINED ARCHITECTURE**” done by under the guidance of **Dr.M.SUMATHI, M.E , PH.D** is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

1)

A photograph of a handwritten signature in blue ink on a light-colored surface. The signature appears to be 'S. Madhumi'.

2)

A photograph of a handwritten signature in black ink on a light-colored surface. The signature appears to be 'D. Minisha'.

DATE: 17.04.2021

PLACE: Chennai

SIGNATURE OF THE CANDIDATES

ACKNOWLEDGEMENT

We are pleased to acknowledge our sincere thanks to Board of Management of **SATHYABAMA** for their kind encouragement in doing this project and for completing it successfully. We are grateful to them.

We convey our thanks to **Dr. N. M. Nandhitha, M.E, Ph.D**, Dean, School of Electrical and Electronics and **Dr. T Ravi, M.E. Ph.D**, Head of the Department, Dept. of Electronics and Communication Engineering for providing us necessary support and details at the right time during the progressive reviews.

We would like to express our sincere and deep sense of gratitude to our Project Guide **Dr.M.SUMATHI,M.E , Ph.D**, for her valuable guidance, suggestions and constant encouragement paved way for the successful completion of our project work.

We wish to express our thanks to all Teaching and Non-teaching staff members of the Department of **Electronics and Communication Engineering** who were helpful in many ways for the completion of the project.

ABSTRACTS

Modern technologies depend heavily on VLSI (Very Large Scale Integration). The first integrated circuit (IC) was developed in the early 1960s, and there were four generations of ICs have been developed since now: SSI (Small Scale Integration), MSI (Medium Scale Integration), LSI (Large Scale Integration), and VLSI (Very Large Scale Integration) . The most advanced ULSI (Ultra Large Scale Integration) is now on the horizon, with complexities exceeding 3 million devices on a single IC chip. Many digital systems, such as calculators, microprocessors, digital filters, and digital signal processors, rely heavily on data comparators.

To put it another way, the data comparator compares its inputs to produce differential output. This process necessitates a large number of hardware components and will also run at a slower tempo. The low-power two's complement 8 bit data comparator can be used in low-power applications such as ATM computers, processors, and DSP processors. To build the proposed model, the current data comparator will be restructured using pass transistor logic. In terms of power, delay, and power delay product, the design of an effective High speed data comparator will be compared to existing architecture.

The proposed data comparator will work more efficient than the existing data comparator. The existing model consumes more time to give output, so the delay value will be high but in proposed model it's more fast and easy. The power consumption also very high in the existing model when compared to the proposed. When the power, delay reduces then parallelly power delay product also reduces. The proposed model data comparator will be used in the ATM machines, processors, DSP processors.

TABLE OF CONTENTS

CHAPTER NO.	TITLE	PAGE NO.
	ABSTRACT	V
	LIST OF TABLES	VIII
	LIST OF FIGURES	IX
	LIST OF ABBREVIATIONS AND SYMBOLS	X
1	INTRODUCTION	1
	1.1. ADDERS	2
	1.1.1. HALF ADDER	3
	1.1.2. FULL ADDER	4
	1.2. MULTIPLEXER	6
	1.3. COMPARATOR	7
	1.4.AND GATE	8
	1.5.NOT GATE	9
	1.6.XOR GATE	11
	1.7. ORGANIZATION OF THE REPORT	13
2	LITERATURE SURVEY	14
	2.1. LITERATURE SURVEY AND OBJECTIVES	14
	2.2. LITERATURE SUMMARY	16
	2.3. PROBLEM DEFINITION	16
	2.4. OBJECTIVE OF THE PROJECT	16
3	PROCEDURE OF EXISTING SYSTEM	17
	3.1. EXISTING FULL ADDER	18
	3.2. MAIN FACTORS	19
	3.2.1. POWER	19
	3.2.2. DELAY	20
	3.2.3. POWER DELAY PRODUCT	20
4	PROPOSED DATA COMPARATOR	21

	4.1. OPERATION OF THE RESTRUCTURED FULL ADDER	21
	4.1.1. PASS TRANSISTOR	21
	4.1.2. PROPOSED FULL ADDER	22
	4.2. HSPICE SOFTWARE	22
	4.3. COSMOSCOPE	24
5	RESULTS AND DISCUSSION	26
	5.1. STIMULATION RESULT FOR NOT GATE	26
	5.2. STIMULATION RESULT FOR AND GATE	27
	5.3. STIMULATION RESULT FOR XOR GATE	28
	5.4. STIMULATION RESULT FOR MUX	29
	5.5. STIMULATION RESULT FOR FULL ADDER	30
	5.6. STIMULATION RESULT FOR COMPARATOR	31
	5.7. PERFORMANCE ANALYSIS	32
	5.7.1. PERFORMANCE ANALYSIS OF NOT GATE	32
	5.7.2. PERFORMANCE ANALYSIS OF AND GATE	33
	5.7.3. PERFORMANCE ANALYSIS OF XOR GATE	34
	5.7.4. PERFORMANCE ANALYSIS OF MUX	35
	5.7.5. PERFORMANCE ANALYSIS OF FULL ADDER	36
	5.7.6. PERFORMANCE ANALYSIS OF COMPARATOR	37
6	CONCLUSION	38
	REFERENCES	39

LIST OF TABLES

TABLE NO.	TITLE	PAGE NO.
1.1	TRUTH TABLE OF AND GATE	8
1.2	TRUTH TABLE OF NOT GATE	1
1.3	TRUTH TABLE OF XOR GATE	11
3.1	TRUTH TABLE OF FULL ADDER	18

DESIGN ANALYSIS

5.1	NOT GATE 130NM	32
5.2	NOT GATE 32NM	32
5.3	AND GATE 130NM	33
5.4	AND GATE 32NM	33
5.5	XOR GATE 130NM	34
5.6	XOR GATE 32NM	34
5.7	MUX 130NM	35
5.8	MUX 32NM	35
5.9	FULL ADDER 130NM	36
5.10	FULL ADDER 32NM	36
5.11	COMPARATOR 130NM	37
5.12	COMPARATOR 32NM	37

LIST OF FIGURES

FIGURE NO.	DESCRIPTION	PAGE NO.
1.1	ONE BIT HALF ADDER	4
1.2	ONE BIT FULL ADDER	5
1.3	DIAGRAM OF MULTIPLEXER	7
1.4	DIAGRAM OF COMPARATOR	7
1.5	SYMBOL OF AND GATE	8
1.6	TRANSISTOR LEVEL AND GATE	9
1.7	SYMBOL OF NOT GATE	9
1.8	TRANSISTOR LEVEL NOT GATE	10
1.9	SYMBOL OF XOR GATE	11
1.10	TRANSISTOR LEVEL XOR GATE	12
3.1	DATA COMPARATOR	17
3.2	EXISTING FULL ADDER	19
4.1	PASS TRANSISTOR LOGIC	21
4.2	PROPOSED FULL ADDER	22

LIST OF SYMBOLS AND ABBREVIATIONS

SYMBOLS	ABBREVIATIONS
VLSI	Very Large Scale Integration
IC	Integration Chip
ALU	Arithmetic & Logic Unit
CLA	Carry Look Ahead Adder
HA	Half Adder
FA	Full Adder
XOR	Exclusive or Gate
CMOS	Complementary Metal Oxide Semiconductor
RCA	Ripple Carry Adder
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ADC	Analog to Digital Converter
FPGA	Field Programmable Gate Array
MDF	Main Distribution Frame
TDF	Testis Determining Factor
AROF	Adaptive Rank Order Filter
MSB	Most Significant Bit
MOS	Military Occupational Specialty Code
HSPICE	Hewlett Stimulation Program with Integrated Circuit

CHAPTER 1

INTRODUCTION

The method of incorporating thousands of transistors into a single chip is known as VLSI design. VLSI design is primarily used to reduce the area of interconnecting fabrics. IC fabrication technology, designer efficiency, and cost are the key factors that restrict the production of smaller and more complex IC chips. Different performance aspects are relevant depending on the application. A processor's ALU is a crucial component. It is capable of performing both arithmetic and logic operations. The multiplier's efficiency determines how quick and accurate the process is. As a result, improving the multiplier's output improves the ALU's quality. To improve the output of a multiplier, we must improve the efficiency of the adder.

In an advanced computerized VLSI design, paired expansion is the most crucial and fundamental math include. The wave convey viper is the absolute first and most essential snake that can perform double number expansion. It isn't actually helpful since its inactivity is corresponding to the length of its info operands. The convey ahead viper is utilized to accelerate the expansion cycle. In contrast with conventional adders, equal prefix adders produce great execution. The viper with the huge, complex entryways would be excessively delayed for VLSI, so the plan is modularized by separating it into a tree of more modest, quicker adders. Thus, the postponement of pushing the help through the look-forward stages gets overwhelmed, and tree adders or equal prefix adders are utilized. To create the current entirety, rapid adders rely upon the past convey. Any decrease in deferral would bring about an increment in throughput in number expansion.

Equal prefix adders are reasonable for VLSI execution since the transfer on the utilization of straightforward cells and keep up ordinary association between them. We can characterize each prefix structure as

far as rationale levels, fan out and wiring tracks. Equal prefix adders give a decent hypothetical premise to make scope of configuration compromise regarding territory, force and deferral.

1.1. ADDERS

A snake, likewise called as a season, is a computerized circuit which is utilized to perform mathematical expansion. Adders are utilized in different spaces of the processor to figure table records, augmentation and decrement administrators ,addresses and different activities, just as in the math rationale systems(ALU) of certain PCs and different sorts of processors.

Adders can be developed for an assortment of mathematical portrayals, including parallel coded decimal and abundance 3, however paired numbers are the most well-known. It is easy to change over a snake into a viper subtractor when two's supplement or ones' supplement are utilized to address negative numbers. Other marked number portrayals require extra rationale notwithstanding the fundamental snake. Wave convey adders (RCA), for instance, to logarithmic - defer adders, for example, the convey look snake early, viper (CLA). There are a few other exhibition upgrading plans, for example, the convey increase snake and the Ling viper, that can improve the convey chain considerably more. In any case, since equal prefix trees have standard designs with logarithmic postponement, they are the most productive method of offering double expansion in Very Large Scale Integration (VLSI) advanced frameworks.

The initial phase in an equal prefix snake is to get the convey at each piece, and the subsequent advance is to register the absolute piece dependent on the convey bit. Prefix trees are more slow algorithmically than quick logarithmic adders like the convey spread adders, however their standard models permit them to outflank customary CLA adders. A convey look forward snake, which is utilized in one of Motorola's processors, causes this in VLSI structures. carries out the convey chain vertically as opposed to on a level plane, which seems to build wire

thickness and fan-in/out reliance. In spite of the way that logarithmic snake structures are perhaps the quickest viper algorithmically, the speed effectiveness of the convey look forward viper has been hampered by unavoidable losses because of fan-in and fan-out conditions, just as the substantial wire load dispersion the vertical way

1.1.1. Half Adder

A paired snake that adds two single parallel digits A_n and B is known as a half viper. Entirety (S) and convey (C) are the two yields (C). The convey signal demonstrates that a multi-digit expansion has flooded into the following digit. $2C + S$ is the estimation of the number. A full viper can be made by consolidating two half adders. The augends and numbers to be added pieces are the information factors of a half viper. The number and convey are the yield factors. Adders in VLSI advanced frameworks utilize parallel documentation, as recently expressed. At that point, utilizing Boolean conditions, add is done one small step at a time. Consider a twofold add with two n -cycle inputs $A;B$, the slightest bit convey in cin , and n -digit yields s .

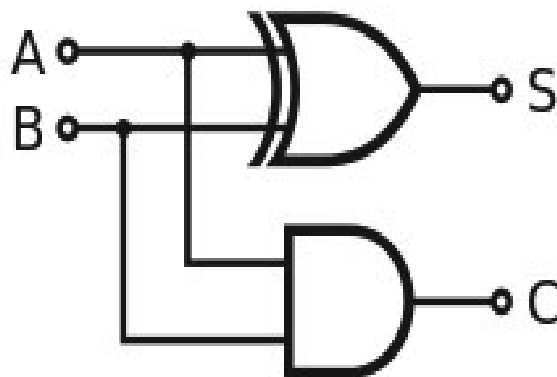


Figure 1.1.one bit half adder

$$S = A + B + cin.$$

where, $A = a_{n-1}, a_{n-2} \dots 0$, $B = b_{n-1}, b_{n-2} \dots 0$.

The in addition to in the above condition is the standard add activity. Be that as it may, in the twofold world, just Boolean polynomial math works. For add related tasks, AND, OR and Exclusive-OR (XOR) are required. In the accompanying documentation, a dab between signifies an OR b. Thinking about the situation of adding of two pieces, the entirety S and convey two factors (each with single piece), for example a.b means 'an AND b'. Essentially, a + b. c can be communicated utilizing Boolean activities

$$s_i = a_i \oplus b_i \oplus c_{i+1} = a_i \cdot b_i$$

The Equation can be carried out as demonstrated in Figure In the figure, there is a half snake, which takes just 2 information bits. Condition can be stretched out to perform full add activity, where there is a convey input.

$$s_i = a_i \oplus b_i \oplus c_i \quad c_{i+1} = a_i \cdot b_i + a_i \cdot c_i + b_i \cdot c_i$$

1.1.2. Full adder

A full snake adds parallel numbers and records for values conveyed in just as out. A the slightest bit total viper adds three the slightest bit numbers, now and again composed as A, B, and Cin; the operands are An and B, and Cin is a piece conveyed in from a past less huge point. The total viper is typically important for a course of adders that add paired quantities of 8, 16, 32, etc.

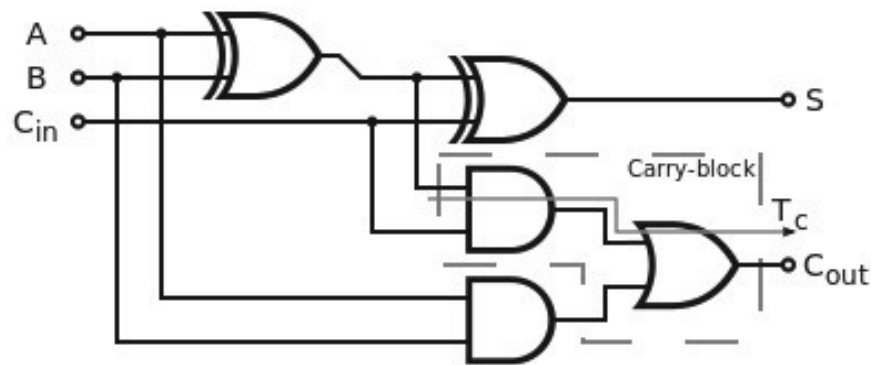


Figure 1.2.one bit full adder

an entire the slightest bit snake Equation can be utilized to construct a total viper. Figure shows the square outline of a 1-digit complete viper. For registering do, the total snake is comprised of two half adders and an OR entryway. Condition isn't expressly executed by the doors in Figure. The comparability can be handily shown utilizing Boolean algebra. Two paired literals are added to help in the calculation of the convey for each piece. They're known as convey produce and convey proliferate, and they're addressed by the letters gi and pi, individually. There's even an exacting considered impermanent total ti that is used. There is an association between these literals and the sources of info. $g_i = a_i; b_i p = a_i; b_i p = a_i; b_i p = a_i; b_i p = a_i; b_i p = a_i b_i = t_i$ With the help of the literals above, yield convey and aggregate at each piece can be composed as $c_{i+1} = g_i + p_i c_i$ $s_i = t_i c_i$ Carry-proliferate pi can be supplanted with transitory sum ti in certain literary works to diminish the quantity of rationale doors. These two words are separated here to make the definitions more clear. Just pi is utilized as convey engender in Ling adders, for instance. It is feasible to expand the single piece convey create/spread to bunch variant G and P. The inborn connections are appeared in the conditions underneath.

$$G_i : j + P_i : j = G_i : j + P_i : j \quad G_{j-1} : k \quad P_i : k = P_i : j = P_i : k = P_i : j = P_i : k$$

$$p_{j-1} \quad p_{j-1} \quad p_{j-1} \quad p_{j-1} \quad p_j$$

The gathering term from l to k is signified by $l \leq k$. Convey can be communicated in the accompanying condition utilizing bunch convey produce/engender.

$$c_{i+1} = G_{i:j} + P_{i:j}$$

▪

1.2.Multiplexer

The activity of communicating at least one simple or computerized signals over a typical transmission line at various occasions or rates is alluded to as multiplexing, and the framework we use to do so is alluded to as a multiplexer.

The multiplexer, truncated as "MUX" or "MPX," is a combinational rationale circuit that utilizes a control sign to change one of a few information lines over to a solitary regular yield line. Multiplexers work like extremely effective various area turning switches, connecting or controlling numerous info lines, alluded to as "channels," to the yield each in turn.

Multiplexers, otherwise called MUXs, are advanced circuits that convert computerized or paired information utilizing high velocity rationale entryways, or simple circuits that pass one of the voltage or current contributions to a solitary yield utilizing semiconductors, MOSFETs, or transfers.

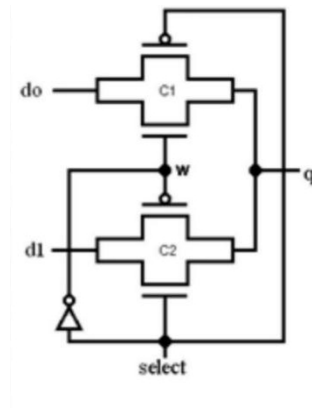


Figure 1.3:Diagram of Muxtipler

1.2. Comparator

A comparator is a gadget in hardware that analyzes two voltages or flows and yields a computerized signal demonstrating which is more prominent. There are two simple information terminals on it. A comparator is a high-acquire differential speaker with a specific plan. They're regularly utilized in simple to-advanced converters (ADCs) and unwinding oscillators, just as different instruments that figure and digitize simple signs.

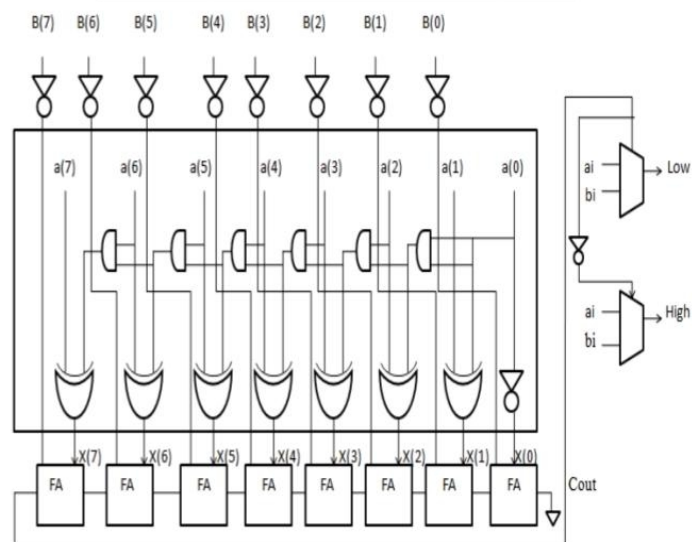


Figure 1.5: Diagram of Comparator

1.4.AND Gate

The AND gate is one of the fundamental computerized rationale entryway that executes intelligent combination; it works as per reality table . The AND entryway creates a HIGH yield in particular if the entirety of its data sources are HIGH (1).

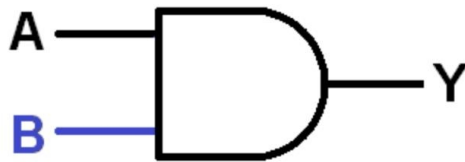


Figure 1.10: symbol of XOR GATE

1.1.TRUTH TABLE OF AND GATE:

B	A	Q
0	0	0
0	1	0
1	0	0
1	1	1

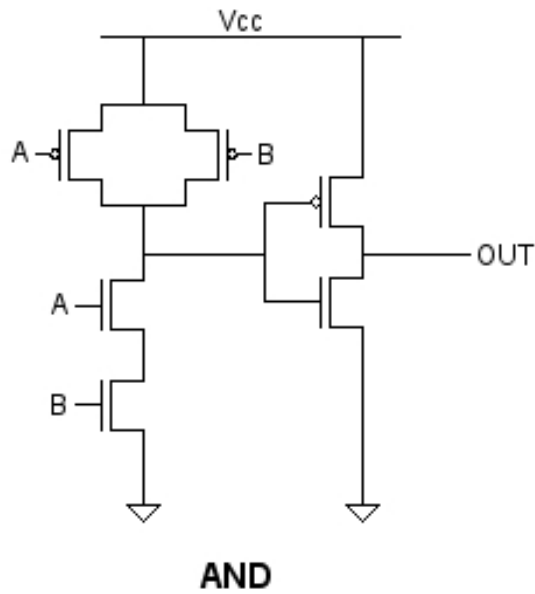


Figure 1.7:AND GATE (transistor level)

1.5.NOT GATE

Inverting NOT gates are single-input devices with an output level that is usually at logic level "1" and goes "LOW" to a logic level "0" when their single input is at logic level "1," in other words, they "invert" (complement) their input signal. When the input to a NOT gate is at logic level "0," the output returns "HIGH," giving us the Boolean expression: $A = \bar{Q}$.

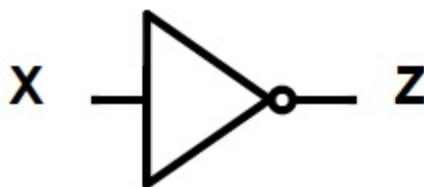


Figure 1.8:Symbol of NOT GATE

1.2.TRUTH TABLE OF NOT GATE:

INPUT	OUTPUT
0	1
1	0

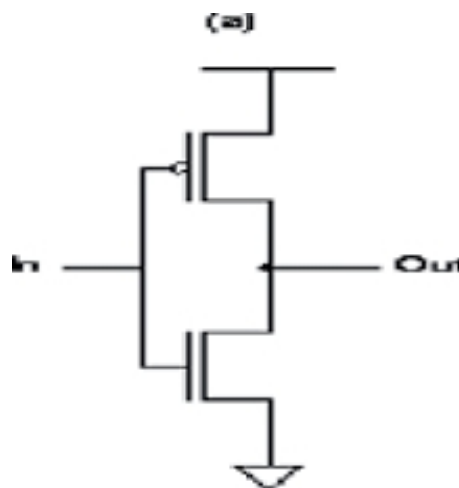


Figure 1.9:NOT GATE (transistor level)

1.6.XOR GATE:

When the number of true inputs is odd, the XOR gate (also known as EOR or EXOR and pronounced Exclusive OR) produces a true (1 or HIGH) output. An XOR gate implements an exclusive or, which means that a true output is produced if only one of the gate's inputs is true. A false output is

produced when both inputs are false (0/LOW) or both are real. The inequality function is represented by XOR, where the output is valid if the inputs are not alike and false otherwise. "Should have one or the other but not both" is a good way to note XOR.



Figure 1.10:symbol of XOR GATE

1.2.TRUTH TABLE OF XOR GATE:

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

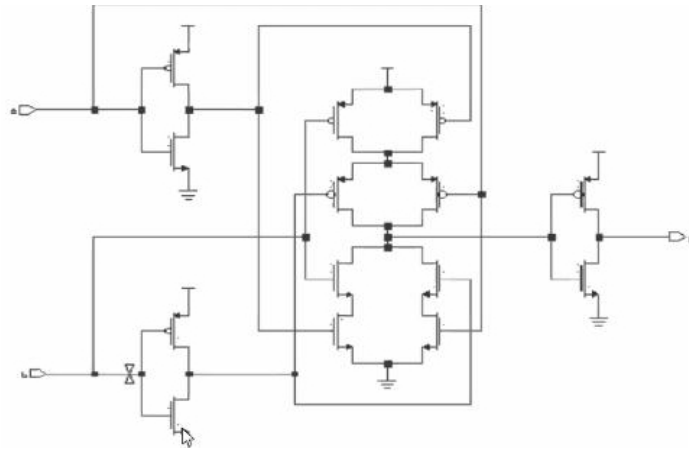


Figure 1.11:XOR GATE (transistor level)

1.7.ORGANIZATION OF THE REPORT

The undertaking report is coordinated into six sections

Section 1 examines the foundation of VLSI, inspiration, presentation of double adders. It additionally examines about the different multipliers and association of the undertaking work.

Section 2 conveys nitty gritty writing overview identified with the venture, writing outline, issue definition, targets of the undertaking.

Section 3 depicts the working and existing methods of information comparator,full adder,mux,AND gate,NOT gate,XOR door.

Section 4 examines the proposed full snake configuration utilizing pass semiconductor and Power Consumption.

Section 5 gives the recreation results and execution investigation of the current and proposed project work. It does a full similar examination on how the proposed work is in an ideal situation than the current plan.

Section 6 gives the end project work. It additionally gives the pattern of things to come work that is the manner by which the undertaking could be upgraded further. At long last, the references alluded to lead the venture are given in a nutshell.

CHAPTER 2

2.1.LITERATURE SURVEY AND OBJECTIVES

The literature survey and review are discussed in this chapter. It also provides a comprehensive description of the current comparator, mux, NOT, AND, XOR, and complete adder structures, as well as how they are synthesised.

Vasanth.k, Kavirajan A.A.F, Ravi.T, NirmalRaj.S(April 2014), "A Novel 8 Bit Digital Comparator for 3x3 Fixed Kernel Based Modified Shear Sorting," Indian Journal of Science and Technology, vol. 7, issue 4, pp. 452-462, April 2014. Any median filter that is good at removing impulse noise without degrading the image information requires an optimised field, speed, and power. The median's key function is Rank ordering. This introduces Snake-like sorting, a modern sorting technique. A parallel architecture is used to implement the proposed Sorting technique. Two architectures are proposed that are comparable to the standard 8 bit comparator and carry select comparator. The region occupied by parallel architecture for modified shear sorting median architecture is one tenth that of other 1D algorithms. The parallel architecture is found to have a lower delay and consumes less power. As a result, we propose a low-area, high-speed parallel pipelined architecture.

Vasanth, S.Karthik(2016) FPGA IMPLEMENTATION OF MODIFIED DECOMPOSITION FILTER 1K.1 Research Scholar, 2 Research Advisor 1Sathyabama University is a Tamilnadu university in Chennai, India. 2Cognizant Technology Solutions is an Indian company based in Chennai, Tamil Nadu. In this paper, a new area-minimized architecture for median filters is proposed, which is based on a modified decomposition algorithm. The complexity of current threshold decomposition algorithms, such as complex comparators, is replaced by the modified decomposition. Decomposition and recombination are the two steps of the proposed algorithm. In contrast to the TDF, which uses a large number of complex comparators and adders, the MDF uses simple comparators, buffers, and

adders. When opposed to TDF, the MDF algorithm occupies less space on the floor plan and in the routed FPGA. We recognise that the proposed algorithm necessitates fewer slices and a look-up table inside the FPGA. The proposed algorithm's timing and power are comparable to the current algorithm. As a result, for the Decomposition algorithm, an area-reduced architecture is proposed.

S. Karpagaabirami and P. Ramamoorthy, "An Efficient VLSI Architecture for Removal of Impulse Noise in Images," *International Journal of Computer Science and Mobile Computing*, Vol. 3, Issue 5, pp. 567–574 (May 2014). Impulse noise is a common cause of image corruption during image processing and transmission procedures. This paper proposes a VLSI implementation of the Adaptive Rank Order Filter (AROF) for the removal of impulse noise. The algorithm eliminates noise without compromising image quality. The simulation results show that the DTBDM VLSI Implementation takes up more space and is also more complex. When compared to DTBDM, the VLSI implementation of DROF uses less space and has a simpler architecture. For higher noise densities, the Adaptive Rank Order Filter outperforms other approaches in terms of filtering properties. The results of the experiments show that AROF-based restored images with higher noise densities have better visual quality than those obtained using other approaches.

VLSI Architectures for 8 Bit Data Comparators for Rank Ordering Image Applications by Sindhu. E and Vasanth. K The proposed work's main goal is to create a new Data comparator that provides a cost-effective solution for sorting / Rank ordering networks based on speed, power, and area. The proposed work entails the creation of six separate 8-bit comparators. The Xilinx 7.1i compiler tool was used to target the output of these six separate comparators for the XCV1000-4bg560. For the targeted computer XCV1000-4bg560, a different architecture for data comparators was designed using VHDL. The two cell sorters built were used on a pipelined architecture for modified shear sorting, and the architecture's output was calculated in terms of area speed and power. As a result, a variable architecture for image applications is proposed in the form of rank order applications.

2.2.LITERATURE SUMMARY

The Decoder-based comparator is used to control the flow of logic i.e data transfer. The proposed logic circuit compares MSB of first 8-bit with MSB of another 8-bit binary number and provides the output by performing basic XOR gate operation of X and Y respectively. The output of these is fed to decoder that operates when the bits are identical the decoder is disabled and when the bits be different from each other, the decoder is enabled and put them in the proper order.

2.3.PROBLEM DEFINITION

In order to improve the working efficiency of the existing comparator, a new proposed model has been developed to compare the proposed model with the existing model in terms of speed, power, power delay product and area. Pipelining design is a suitable VLSI architecture for decreasing the critical path, meanwhile it can reduce the speed. The basic operation of these architecture is performed by using clock (clk) sequence.

2.4.OBJECTIVE OF THE PROJECT

- 1.To increase the proficiency of the 8 cycle Data Comparator for Low Power applications.
- 2.To improve Efficiency Low Power Techniques will be applied in all Circuits.
- 3.To analyze, the qualities of MOSFET Technology regarding Power, Delay and Power Delay Product.
- 4.To recognize the Feasibility of 8 bit Data Comparator.

CHAPTER 3

PROCEDURE OF EXISTING SYSTEM

3.1.DATA COMPARATOR

Many digital systems, such as calculators, microprocessors, digital filters, and digital signal processors, rely heavily on data comparators. They're also used in discrete Fourier transform, correlation, and range measurement implementations. Since the comparison process is slow, the output of any digital device is normally calculated in terms of the used comparators. A comparator is an electronic circuit that compares two inputs and outputs the result of the comparison. To put it another way, the data comparator compares its inputs to produce differential output. This process necessitates a large number of hardware components and will also run at a slower tempo. Data Comparator and Sign Extension Tricks, Shift and Add, Reducing the Number of Partial Products The development of a high-speed data comparator that can handle both signed and unsigned numbers. There are 10 NOT gates, 6 AND gates, 7 XOR gates, 8 complete adder blocks, and 2 multiplexer blocks in this data comparator.

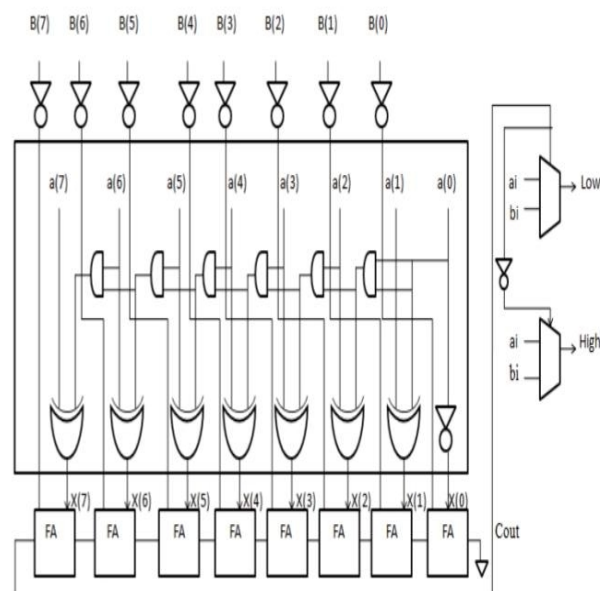


Figure 3.1.Data Comparator

3.2.Existing full Adder

The full viper is a snake that takes three information sources and yields two outcomes. The initial two sources of info are An and B, with the third being a C-IN input. The convey yield is marked C-OUT, while the typical yield is named S, which represents SUM. Numerous computerized circuits that perform expansion or deduction utilize a total viper circuit. It gets its name from the way that it adds two parallel digits in addition to a convey in digit to get a number and complete digit. It has three information sources and two yields subsequently. The snake blocks have 18 semiconductors (9 p-mos and 9 n-mos) and 2 NOT doors (c-mos inverter).

3.1.TRUTH TABLE FOR FULL ADDER

A	B	Cin	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

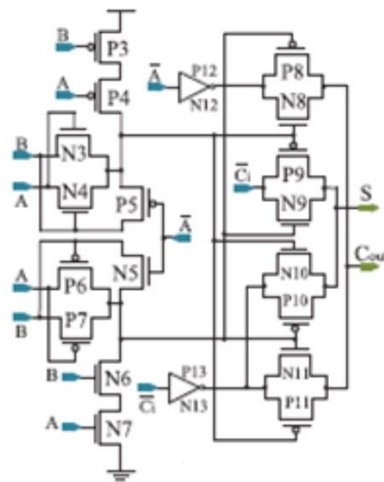


Figure 3.2.Existing Full Adder

MAIN FACTORS

- Power
- Delay
- Power Delay Product

POWER

Electric power is the rate at which electrical energy is transmitted by an electric circuit per unit of time. It is the pace at which work is completed. Electrical power is the rate at which electrical energy is transmitted by an electric circuit per unit time in terms of an electric circuit.

The unit of the Electric Power = Watt

$$\text{Power} = V \cdot I (\text{W})$$

$$I = Q/t$$

Where:

W=power in watts

V = potential in volts

I = current in amps

Q = charge in coulombs

t = time in seconds

DELAY

The time it takes for a signal to reach its destination is referred to as delay. The time it takes for the consequence of a shift in input to be noticeable at the output is known as the delay of a logic gate.

POWER DELAY PRODUCT

Power Delay Product is the product of the power and delay.

$$PDP = \text{Power} * \text{Delay}$$

CHAPTER 4

PROPOSED DATA COMPARATOR

In previous work, a Complete Adder with 18 transistors was used to design the Data Comparator. The Data Comparator in the proposed work is built using a modified Full Adder with 14 transistors, which consumes less power than the current design.

4.1.OPERATION OF THE RESTRUCTURED FULL ADDER

4.1.1.PASS TRANSISTOR

Unlike bipolar transistors, MOS transistors have an isolated gate that allows them to be used as switches in series with line carrying logic levels, similar to how relay contacts are used. The pass transistor and switching logic array is the name for this application of the MOS system.

ADVANTAGES OF PTL

1. As compared to CMOS, there are fewer devices needed to implement the logic functions.
2. Power consumption is low.

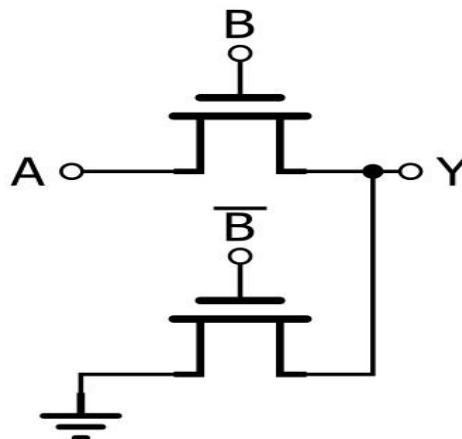


Figure 4.1 Pass Transistor Logic

4.1.2.PROPOSED FULL ADDER

The current complete adder is updated by reducing some transistors and redesigning it using the pass transistor logic. There are only 14 transistors in this proposed model (7 p-mos and 7 n-mos). The adder takes either a 0 or a 1 as input. When the input is 0, the p-mos is active; when the input is 1, the n-mos is active. As a result, the additional c-mos transistors are turned off at that time. It consumes more power and takes longer to complete, resulting in a delay and an increase in the power delay product. As a result, the power consumption and delay in this proposed model were minimised by reducing the transistors. As a result, it's a significant benefit of this proposed complete adder.

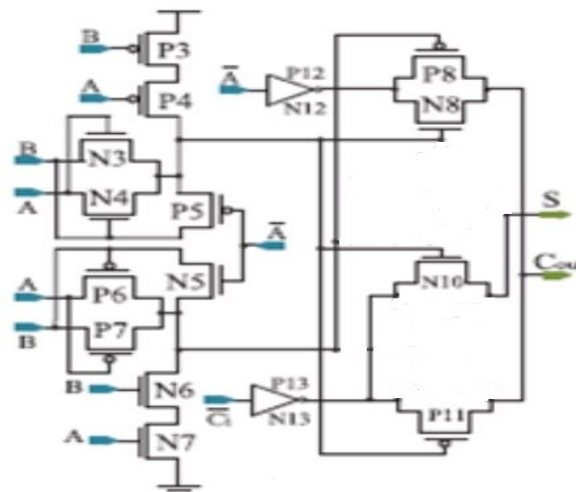
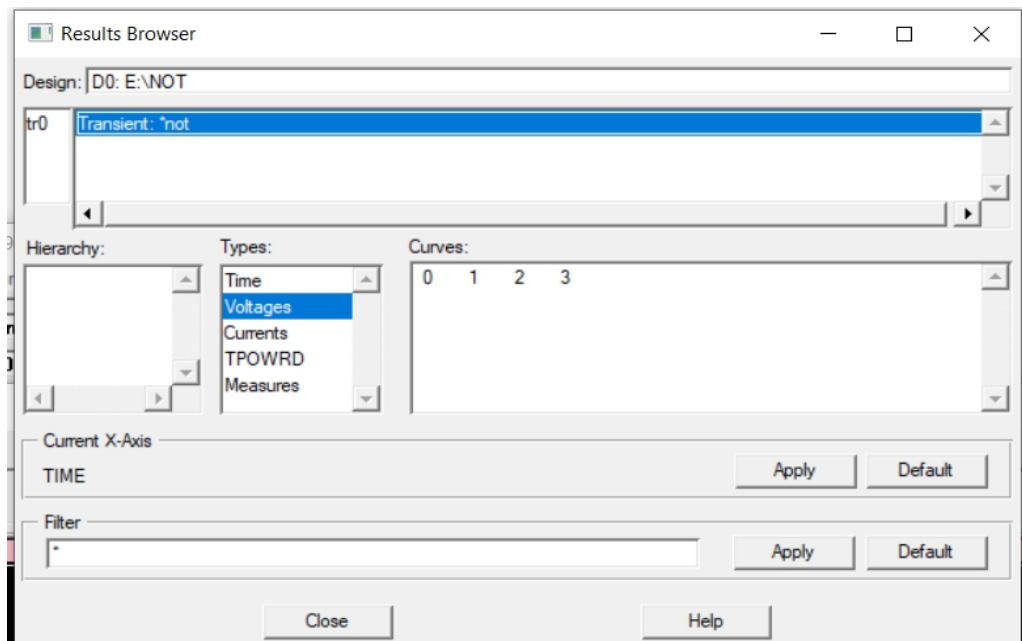
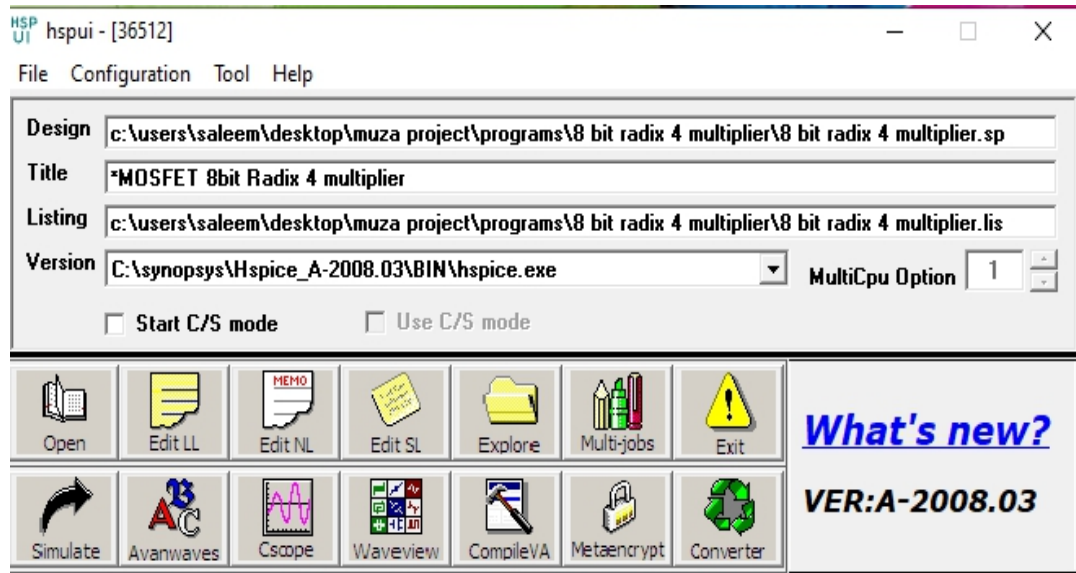


Figure 4.2 Proposed Full Adder

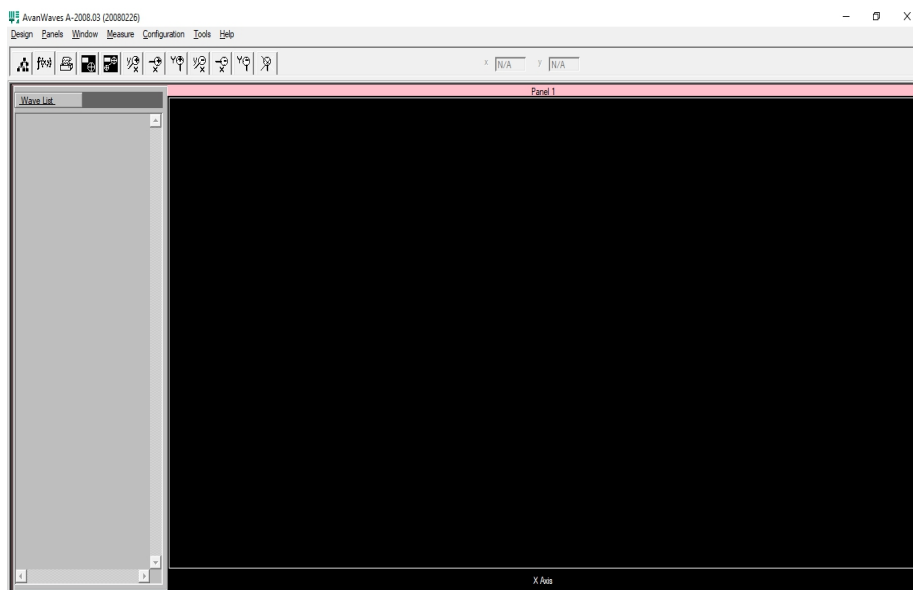
4.2.HSPICE SOFTWARE

Hewlett Simulation Program with Integrated Circuit is the full name of HSPICE. Unlike board-level designs made up of individual components, integrated circuits cannot be breadboarded before being manufactured. Furthermore, due to the high cost of photolithographic masks and other manufacturing requirements, it is critical to design the circuit to be as close to perfect as possible before it is designed. Until committing to producing an

integrated circuit, the industry-standard method of verifying circuit operation at the transistor level is to simulate the circuit with SPICE. It will, for example, draw circuits and model what happens when the circuits are powered up/ and how they act in various emergency situations.



4.2.1.STIMULATION SCREEN

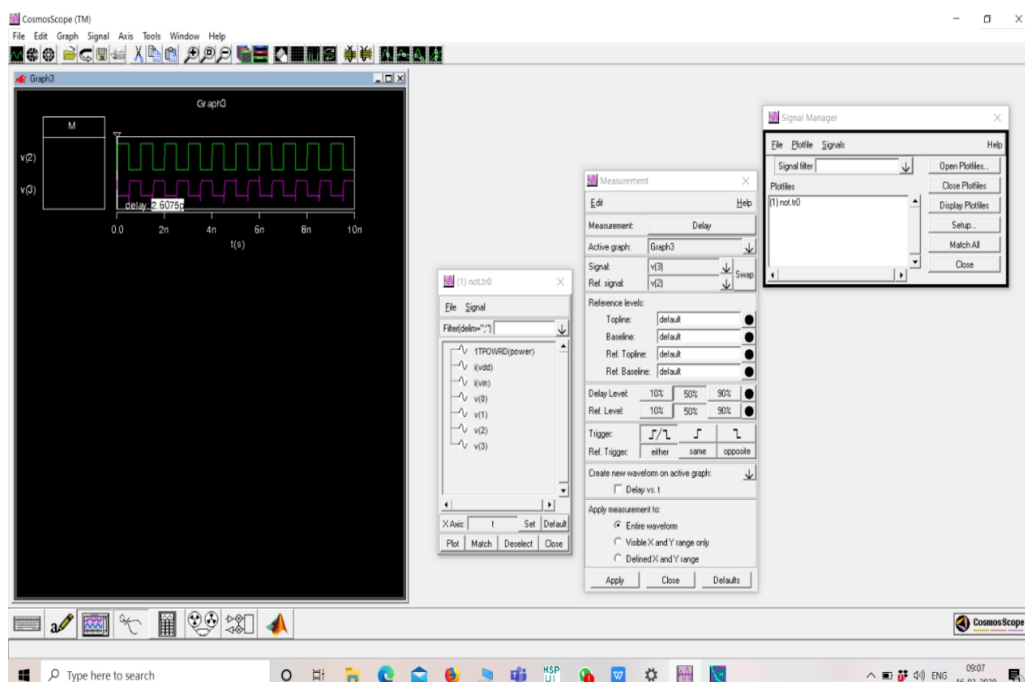


4.3.COSMOSCOPE

Cosmoscope is a software which is used to calculate the delay value.

Uses

- Simpleware 3D Modeling **Software**.
- Clinical **Applications** for 3D Images.
- Life Sciences **Applications** for 3D Images.



CHAPTER 5

RESULTS AND DISCUSSION

The existing and proposed architecture are simulated by using AvanWaves simulator. Output of the existing Data Comparator and proposed Data Comparator are analysed from the results and it is concluded that the proposed architecture reduces the power consumption compared with the existing system. The Synthesis is done using Hspice UI.

5.1 Simulation results for NOT Gate

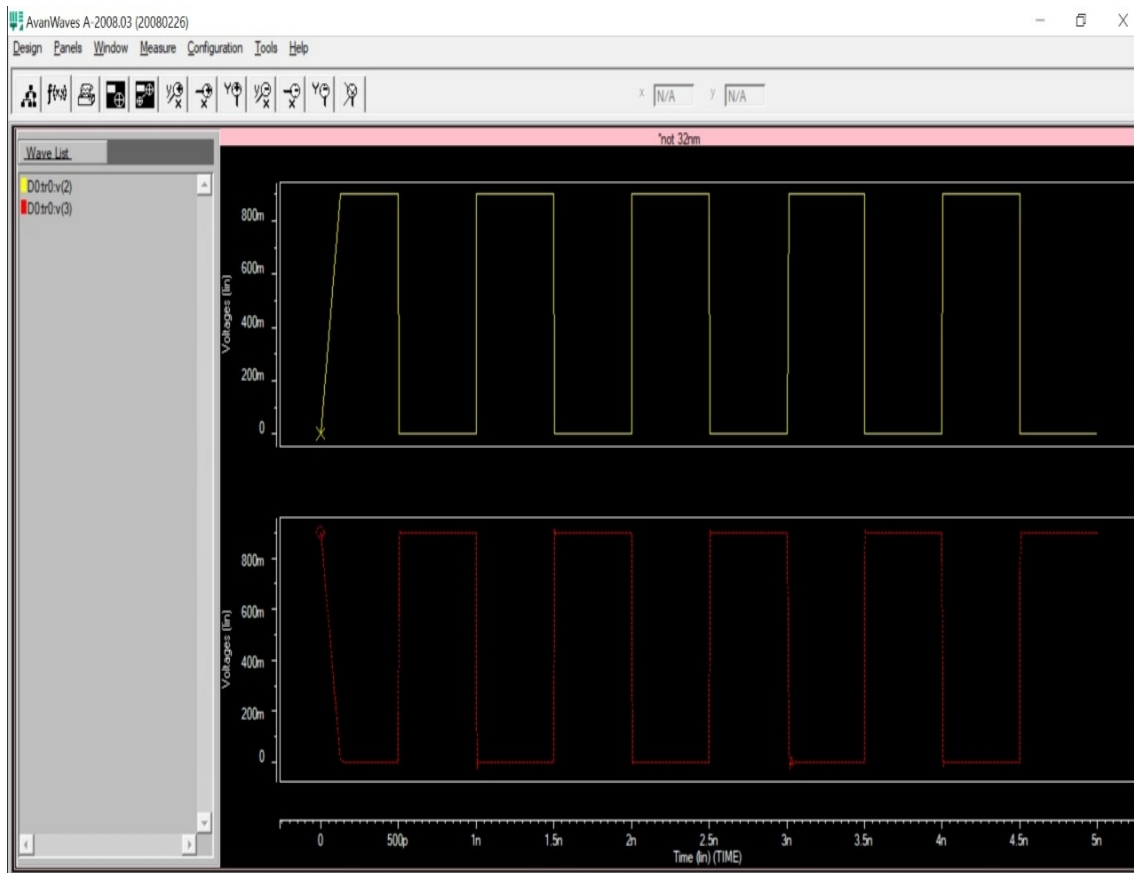


Figure 5.1: Simulation results for NOT Gate

Figure 5.1 shows the simulation output of a NOT gate. The inputs given was a and the output is taken by b.

5.2.Simulation results for AND Gate

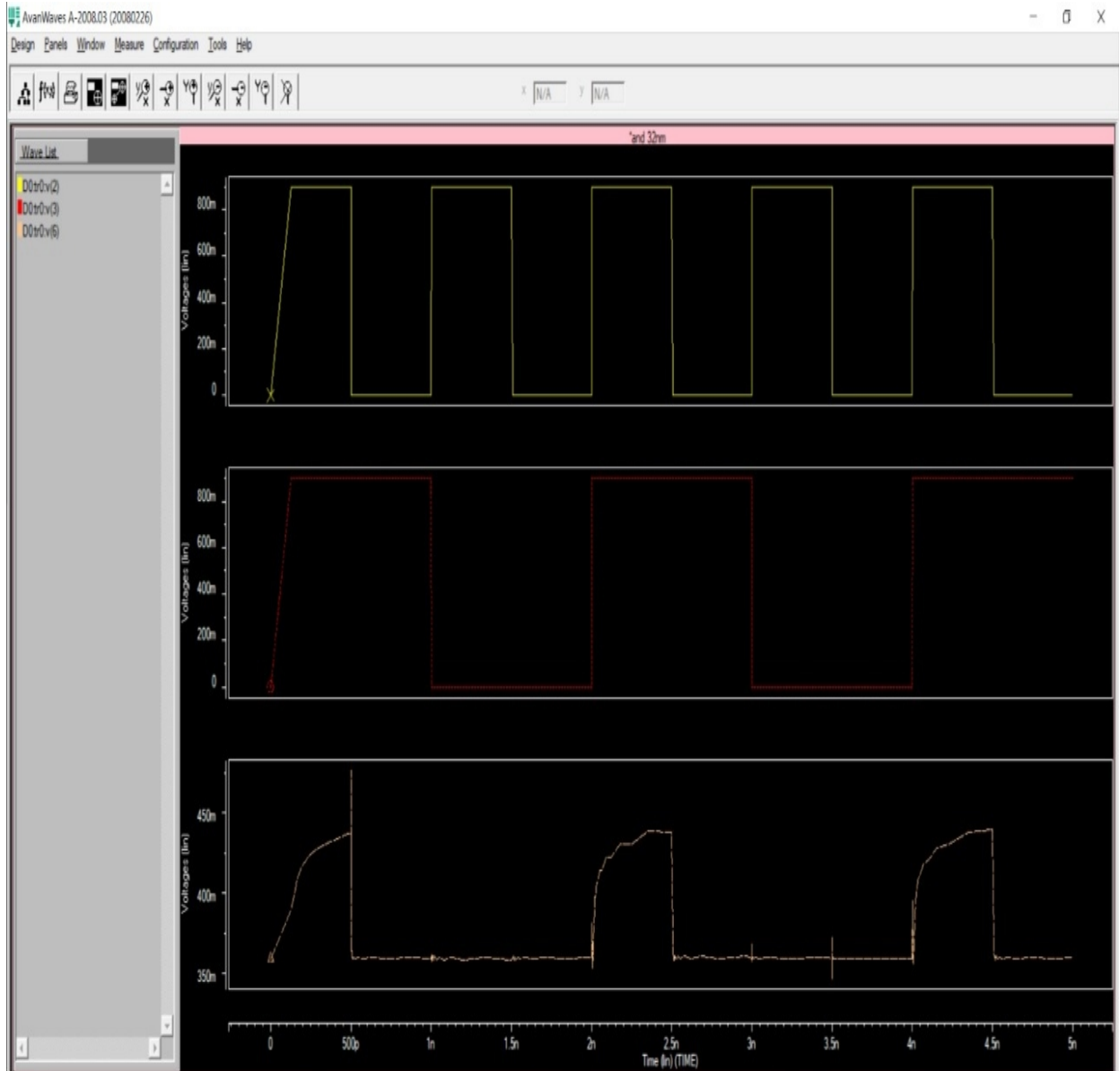


Figure 5.2: Simulation results for AND Gate

Figure 5.2 shows the simulation output of a AND gate. The inputs given were a, b and the output is taken by c.

5.3.Simulation results for XOR Gate

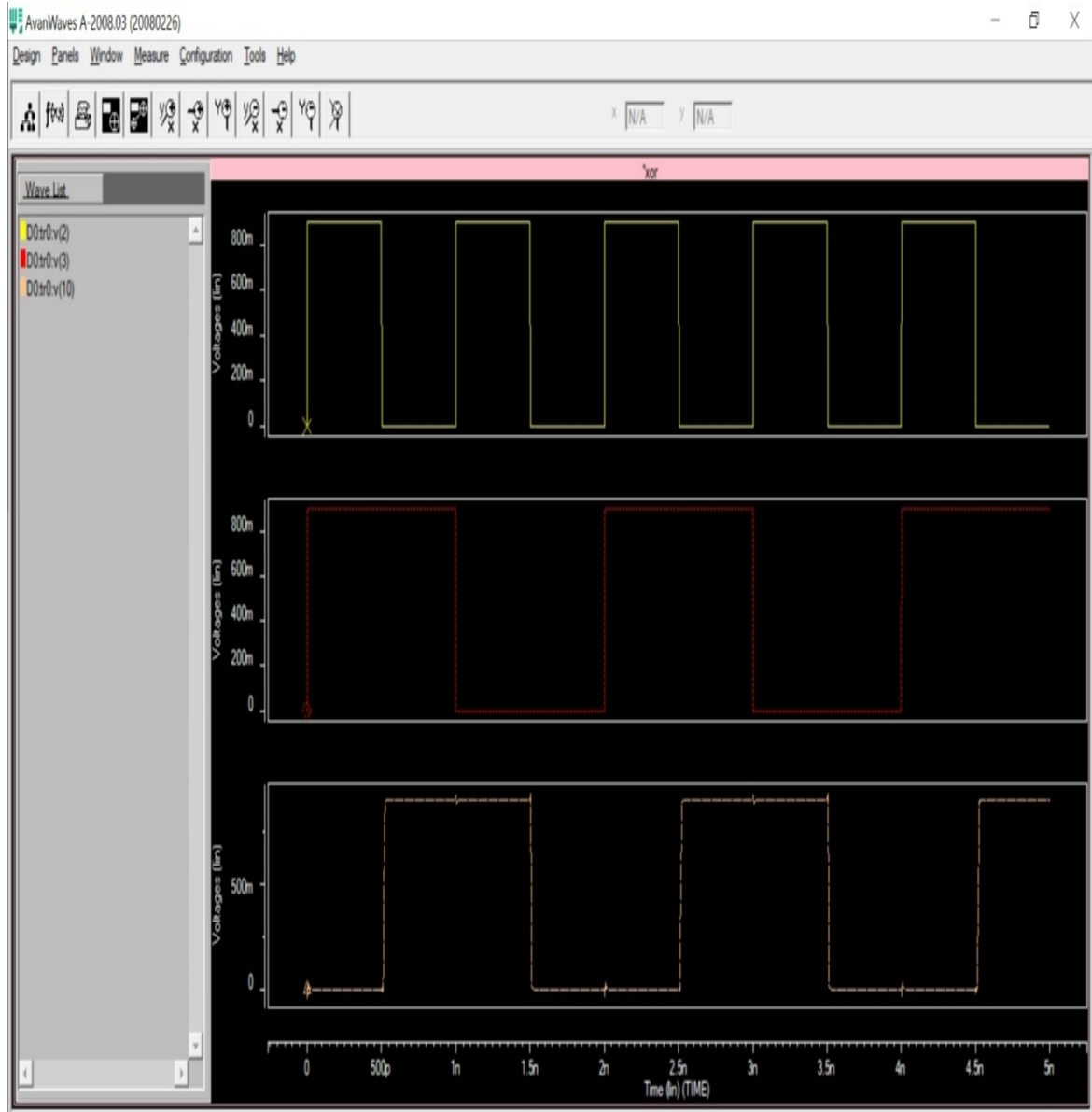


Figure 5.3: Simulation results for XOR Gate

Figure 5.3 shows the simulation output of a xor gate. The inputs given were a, b and the output is taken by c.

5.4.Simulation results for MUX Gate

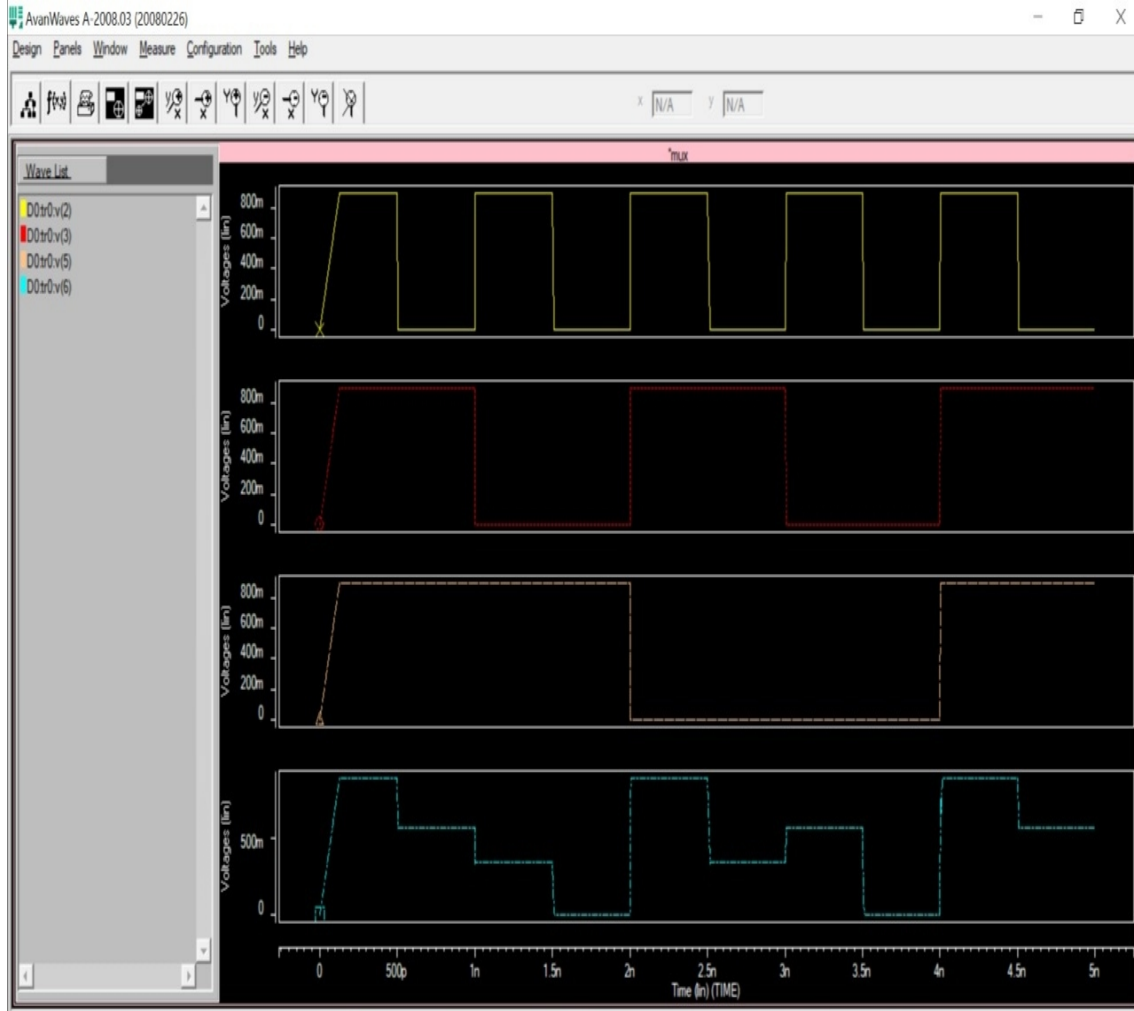


Figure 5.4: Simulation results for XOR Gate

Figure 5.4 shows the simulation output of a MUX gate. The inputs given were a, b,select and the output is taken by c.

5.5.Simulation results for Full Adder

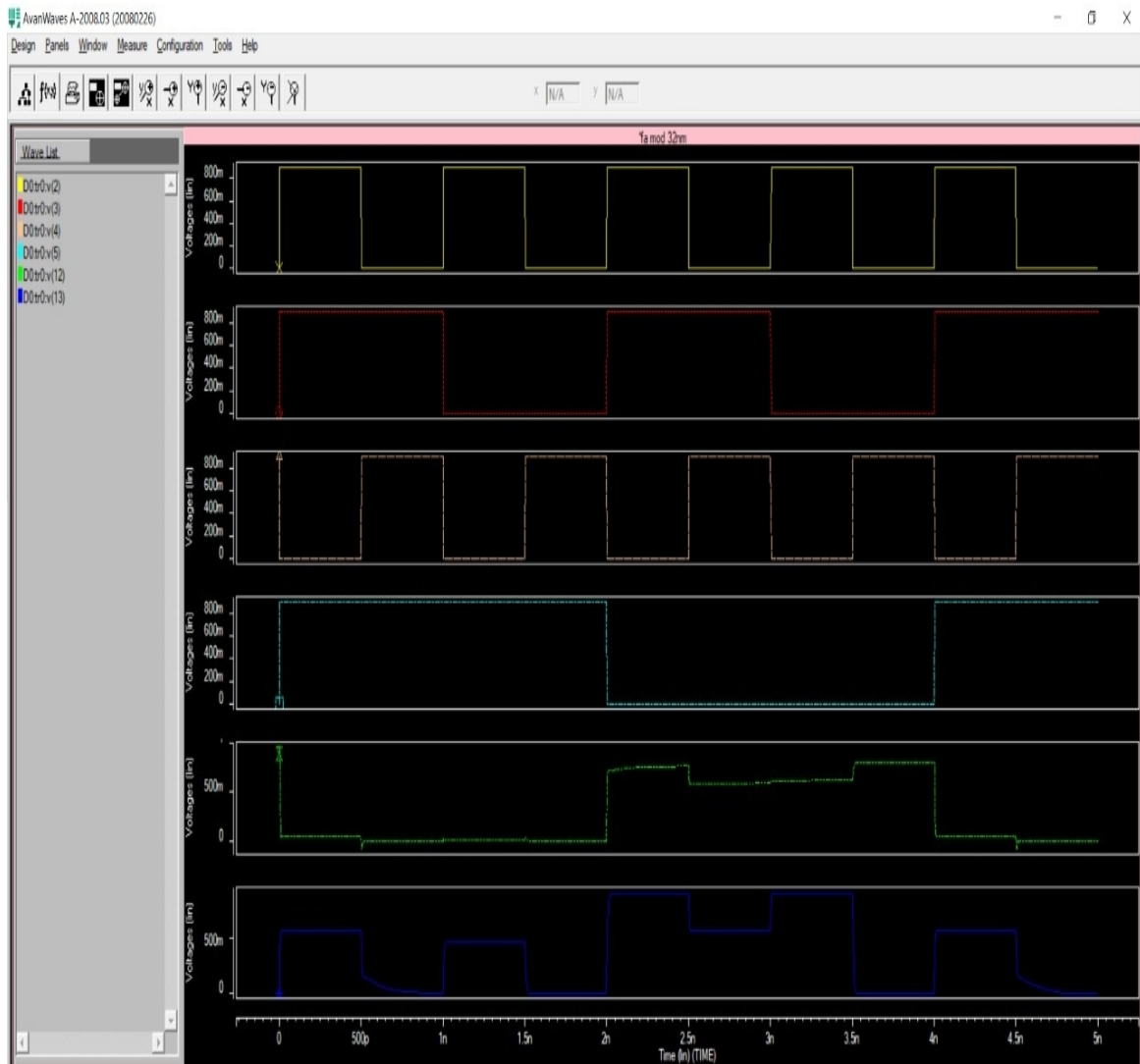


Figure 5.5: Simulation results for Full Adder

Figure 5.5 shows the simulation output of a Full Adder. The inputs given were a, b and the output is taken by c.

5.6.Simulation results for Data Comparator

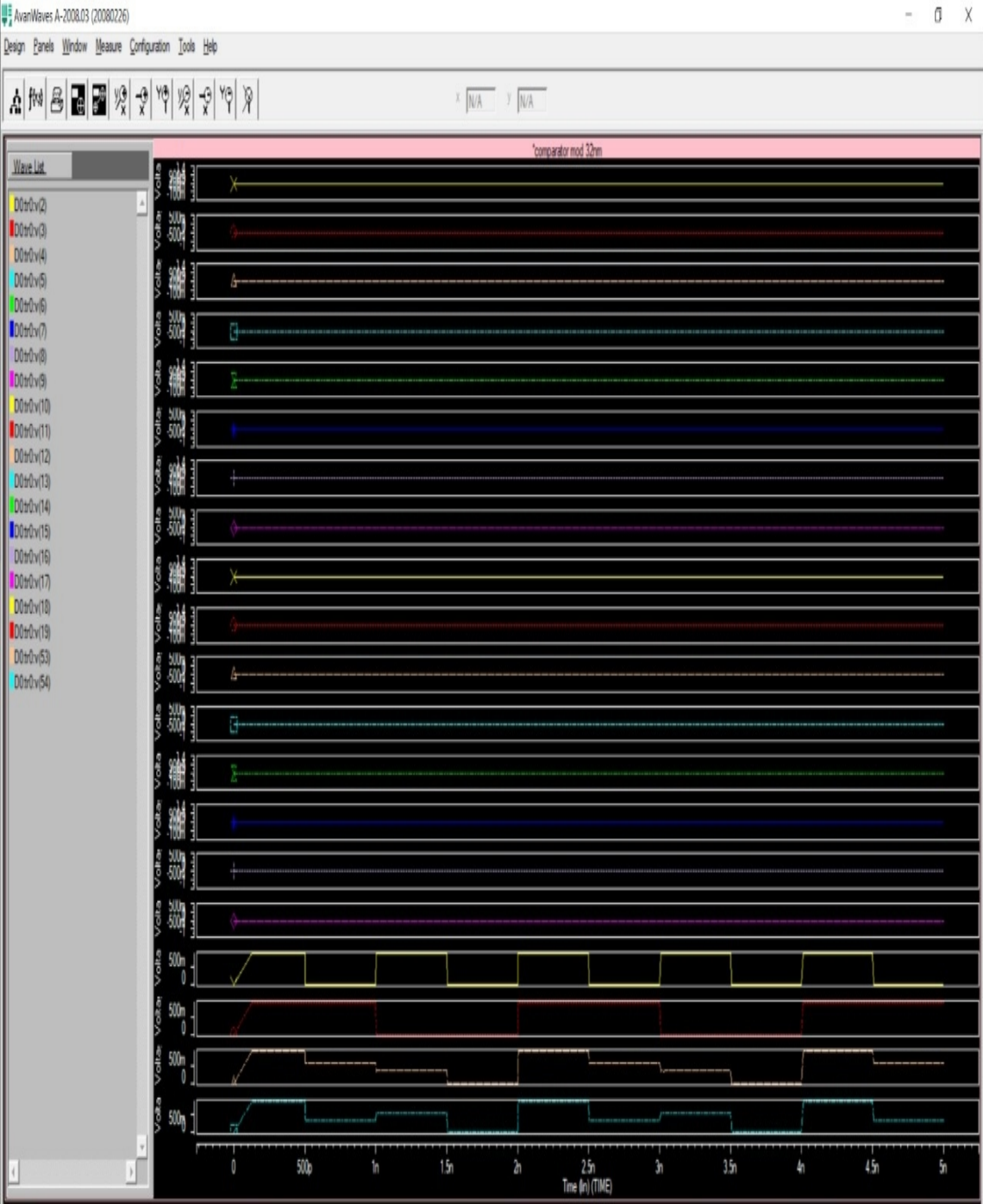


Figure 5.6: Simulation results for Data Comparator

Figure 5.6 shows the simulation output of a Data Comparator. The performance has been analysed.

5.7.PERFORMANCE ANALYSIS

The performance analysis of AND,NOT,XOR,Full Adder,Comparator in terms of power has been given below.

5.7.1.PERFORMANCE ANALYSIS OF NOT GATE

Table 5.1: Design analysis of 130NM NOT gate

NOT GATE (130NM) PARAMETERS	VALUES
POWER	$1.556 * 10^{-5}W$
DELAY	$46.594 * 10^{-12}s$
POWER DELAY PRODUCT	$72.5002 * 10^{-17}J$

Table 5.2: Design analysis of 32NM NOT gate

NOT GATE (32NM) PARAMETERS	VALUES
POWER	$4.849 * 10^{-8}W$
DELAY	558.58F s
POWER DELAY PRODUCT	$270.8554 * 10^{-7}J$

5.7.2.PERFORMANCE ANALYSIS OF AND GATE

Table 5.3: Design analysis of 130NM AND gate

AND GATE (130NM) PARAMETERS	VALUES
POWER	$8.052 * 10^{-6}W$
DELAY	2.0675 PFs
POWER DELAY PRODUCT	$16.6475 * 10^{-18}J$

Table 5.4: Design analysis of 32NM AND gate

AND GATE (32NM) PARAMETERS	VALUES
POWER	$4.849 * 10^{-8}W$
DELAY	558.58Fs
POWER DELAY PRODUCT	$270.8554 * 10^{-7}J$

5.7.3.PERFORMANCE ANALYSIS OF AND GATE

Table 5.5: Design analysis of 130NM XOR gate

XOR GATE (130NM) PARAMETERS	VALUES
POWER	$4.707 * 10^5 W$
DELAY	102.86 PFs
POWER DELAY PRODUCT	$484.1620 * 10^{-17} J$

Table 5.6: Design analysis of 32NM XOR gate

XOR GATE (32NM) PARAMETERS	VALUES
POWER	$4.776 * 10^7 W$
DELAY	16.293PF s
POWER DELAY PRODUCT	$77.8153 * 10^{-19} J$

5.7.4.PERFORMANCE ANALYSIS OF MUX

Table 5.7: Design analysis of 130NM MUX

MUX GATE (130NM) PARAMETERS	VALUES
POWER	$8.821 * 10^{-6}W$
DELAY	6.5677 PF s
POWER DELAY PRODUCT	$57.9336 * 10^{-18}J$

Table 5.8: Design analysis of 32NM MUX

MUX GATE (32NM) PARAMETERS	VALUES
POWER	$1.752 * 10^{-5}W$
DELAY	229.48PF s
POWER DELAY PRODUCT	$402.0489 * 10^{-5}J$

5.7.5.PERFORMANCE ANALYSIS OF FULL ADDER GATE

Table 5.9: Design analysis of 130NM Full Adder

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING FULL ADDER	$5.736 * 10^{-5}W$	11.417 PF s	$65.4879 * 10^{-17}J$
PROPOSED FULL ADDER	$3.997 * 10^{-5}W$	9.309 PF s	$36.0965 * 10^{-17}J$

Table 5.10: Design analysis of 32NM Full Adder

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING FULL ADDER	$5.026 * 10^{-5}W$	9.7557 PF s	$49.0396 * 10^{-17}J$
PROPOSED FULL ADDER	$3.951 * 10^{-5}W$	4.5131 PF s	$17.8312 * 10^{-16}J$

5.7.6.PERFORMANCE ANALYSIS OF COMPARATOR

TABLE 5.11:Design analysis of 130nm comparator

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING COMPARATOR	$1.918 * 10^{-4}W$	66.794 PF s	$128.1108 * 10^{-16}J$
PROPOSED COMPARATOR	$1.723 * 10^{-4}W$	46.804 PF s	$80.643 * 10^{-16}J$

TABLE 5.12:Design analysis of 32nm comparator

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING COMPARATOR	$4.160 * 10^{-4}W$	62.701 PF s	$260.8361 * 10^{-16}J$
PROPOSED COMPARATOR	$2.977 * 10^{-4}W$	62.695 PF s	$186.643 * 10^{-16}J$

CONCLUSION

The propose model data comparator with the restructured full adder block will be used in the low power applications like ATM machines,DSP processors.The power value has been calculated with the help of the HSPICE tool and avanwaves .Delay will be calculated by using the CosmosScope. The main objective of this project is to develop a comparator which should consume low power, the delay value should be low, the speed should be high and the area consumption should be less.The performance analysis of the proposed data comparator with the existing model clearly shows that the proposed model works efficiently that the existing model.By using the pass transistor logic,the existing data comparator is restructured.Whenever the input is 1 the Pmos is ON and Nmos will be OFF,where as whenever the input is 0 the Nmos will be ON and the Pmos will be OFF.In order to overcome these, a new proposed model has been developed.. The average power value for the existing data comparator $4.160 * 10^{-4}W$ which got reduced to $2.977 * 10^{-4}W$. It shows that power consumption got reduced to half,delay and power delay product also reduced .

REFERENCE

- [1] Karpagaabirami. S,P. Ramamoorthy, “ An Efficient VLSI Architecture for Removal of Impulse Noise in Images”, International Journal of Computer Science and Mobile Computing, Vol. 3, Issue. 5, pp 567 – 574, May 2014.
- [2] Aayisa Banu S, Ms. Divya R, Mr. Ramesh .K, “Design and Simulation of Low Power and High Speed Comparator using VLSI Technique”, International Journal of Advanced Research in Computer and Communication Engineering, Vol. 6, Issue. 1, pp 119 – 122, January 2017.
- [3] Bharat H. Nagpara, Godhakiya Santosh M, Nagar Jay V, “Design and Implementation of Different types of Comparator”, International Journal of Science, Engineering and Technology Research , Vol. 4, Issue. 5, pp 1321-1324 , May 2015.
- [4] Mehmood ul Hassan, Rajesh Mehra ,“ Design Analysis of 1-bit CMOS comparator”, Proceedings of International Journal of Scientific Research Engineering & Technology, Vol. , Issue. , pp 68 – 72, 14-15 March 2015
- [5] K.Vasanth, S.Karthik, S.Nirmal raj, Preetha mol. P, “FPGA implementation of optimized sorting networks for median filter”, International Conference on robotics and automation, INTERACT 2010, Sathyabama university, Tamilnadu, India, pages 253-258, 2010.
- [6] Keping CHAN, “ Bit-Serial Realizations of a Class of Nonlinear Filters Based on Positive Boolean Functions” , IEEE Transactions on Circuits and Systems, Vol 36,no 6,pp 785-795, JUNE 1989.
- [7] Vasanth.k, Kavirajan A.A.F, Ravi.T, NirmalRaj.S, “ A Novel 8 bit digital comparator for 3x3 fixed kernel based modified shear sorting”,

Indian journal of science and technology, vol 7 ,issue 4, pp 452- 462,
April 2014.

[8] K.Vasanth, V Elanangai, S Saravanan, G Nagarajan, "FSM-Based VLSI Architecture for the 3×3 Window-Based DBUTMPF Algorithm",
Proceedings of the International Conference on Soft Computing
Systems: ICSCS 2015, Springer, Vol no 2, pp 234- 245, 2015.

[9] K.Vasanth, "VLSI Architecture of Decision based Modified Selection
sort filter for Salt and pepper noise removal", International Journal on
Intelligent Electronic System, Vol 13,no.4, Pages 41-56, August 2014.

[10] K.Vasanth and S.Karthik, "FPGA implementation of modified
decomposition filter", International Conference on Signal and image
processing, ICSIP 2010, Chennai, Tamilnadu, India, pages 526-530.

[11] Keshab K. Parhi, "Low-energy CSMT carry generators and binary
adders", IEEE Transactions on Very Large Scale Integration (VLSI)
Systems, volume 21, issue 4, pp791, april 2013.

[12] <https://thunderwiring.wordpress.com/sorting-numbers/> [Accessed: 25-
FEB-2019]

analysis of 8 bit comparism

by kavin kishore

Submission date: 17-Apr-2021 06:26PM (UTC+0700)

Submission ID: 1561758437

File name: ANALYSIS_OF_8_BIT_COMPARATOR_report.docx (1.24M)

Word count: 5107

Character count: 26785

ANALYSIS OF 8-BIT DATA COMPARATOR USING EFFICIENT PIPELINED ARCHITECTURE

ABSTRACTS

Current innovations rely vigorously upon VLSI (Very Large Scale Integration). The initially incorporated circuit (IC) was created in the mid 1960s, and there were four ages of ICs have been created since now: SSI (Small Scale Integration), MSI (Medium Scale Integration), LSI (Large Scale Integration), and VLSI (Very Large Scale Integration) . The most developed ULSI (Ultra Large Scale Integration) is presently not too far off, with intricacies surpassing 3 million gadgets on a solitary IC chip. Numerous advanced frameworks, like number crunchers, chip, computerized channels, and advanced sign processors, depend vigorously on information comparators.

To put it another way, the data comparator compares its inputs to produce differential output. This process necessitates a large number of hardware components and will also run at a slower tempo. The low-power twos complement 8 bit data comparator can be used in low-power applications such as ATM computers, processors, and DSP processors. To build the proposed model, the current data comparator will be restructured using pass transistor logic. In terms of power, delay, and power delay product, the design of an effective High speed data comparator will be compared to existing architecture.

The proposed data comparator will work more efficient than the existing data comparator. The existing model consumes more time to give output, so the delay value will be high but in proposed model it's more fast and easy. The power consumption also very high in the existing model when compared to the proposed. When the power, delay reduces then parallelly power delay power also reduces. The proposed model data comparator will be used in the ATM machines, processors, DSP processors.

16 TABLE OF CONTENTS

CHAPTER NO.	TITLE	PAGE NO.
	ABSTRACT	V
	LIST OF TABLES	25 VIII
	LIST OF FIGURES	IX
	LIST OF ABBREVIATIONS AND SYMBOLS	X
1	INTRODUCTION	1
	1.1. ADDERS	2
	1.1.1. HALF ADDER	3
	1.1.2. FULL ADDER	4
	1.2. MULTIPLEXER	6
	1.3. COMPARATOR	7
	1.4. AND GATE	8
	1.5. NOT GATE	9
	1.6. XOR GATE	11
	1.7. ORGANIZATION OF THE REPORT	13
2	LITERATURE SURVEY	14
	2.1. LITERATURE SURVEY AND OBJECTIVES	14
	2.2. LITERATURE SUMMARY	16
	2.3. PROBLEM DEFINITION	16
	2.4. OBJECTIVE OF THE PROJECT	16
3	PROCEDURE OF EXISTING SYSTEM	17
	3.1. EXISTING FULL ADDER	18
	3.2. MAIN FACTORS	19
	3.2.1. POWER	19
	3.2.2. DELAY	20
	3.2.3. POWER DELAY PRODUCT	20
4	PROPOSED DATA COMPARATOR	21

	4.1. OPERATION OF THE RESTRUCTURED FULL ADDER	21
	4.1.1. PASS TRANSISTOR	21
	4.1.2. PROPOSED FULL ADDER	22
	4.2. HSPICE SOFTWARE	22
	4.3. COSMOSCOPE	24
5	RESULTS AND DISCUSSION	26
	5.1. STIMULATION RESULT FOR NOT GATE	26
	5.2. STIMULATION RESULT FOR AND GATE	27
	5.3. STIMULATION RESULT FOR XOR GATE	28
	5.4. STIMULATION RESULT FOR MUX	29
	5.5. STIMULATION RESULT FOR FULL ADDER	30
	5.6. STIMULATION RESULT FOR COMPARATOR	31
	5.7. PERFORMANCE ANALYSIS	32
	5.7.1. PERFORMANCE ANALYSIS OF NOT GATE	32
	5.7.2. PERFORMANCE ANALYSIS OF AND GATE	33
	5.7.3. PERFORMANCE ANALYSIS OF XOR GATE	34
	5.7.4. PERFORMANCE ANALYSIS OF MUX	35
	5.7.5. PERFORMANCE ANALYSIS OF FULL ADDER	36
	5.7.6. PERFORMANCE ANALYSIS OF COMPARATOR	37
6	CONCLUSION	38
	REFERENCES	39

LIST OF TABLES

TABLE NO.	¹⁴ TITLE	PAGE NO.
1.1	TRUTH TABLE OF AND GATE	8
1.2	TRUTH TABLE OF NOT GATE	1
1.3	TRUTH TABLE OF XOR GATE	11
3.1	TRUTH TABLE OF FULL ADDER	18

DESIGN ANALYSIS

5.1	NOT GATE 130NM	32
5.2	NOT GATE 32NM	32
5.3	AND GATE 130NM	33
5.4	AND GATE 32NM	33
5.5	XOR GATE 130NM	34
5.6	XOR GATE 32NM	34
5.7	MUX 130NM	35
5.8	MUX 32NM	35
5.9	FULL ADDER 130NM	36
5.10	FULL ADDER 32NM	36
5.11	COMPARATOR 130NM	37
5.12	COMPARATOR 32NM	37

LIST OF FIGURES

FIGURE NO.	DESCRIPTION	PAGE NO.
1.1	ONE BIT HALF ADDER	4
1.2	ONE BIT FULL ADDER	5
1.3	DIAGRAM OF MULTIPLEXER	7
1.4	DIAGRAM OF COMPARATOR	7
1.5	SYMBOL OF AND GATE	8
1.6	TRANSISTOR LEVEL AND GATE	9
1.7	SYMBOL OF NOT GATE	9
1.8	TRANSISTOR LEVEL NOT GATE	10
1.9	SYMBOL OF XOR GATE	11
1.10	TRANSISTOR LEVEL XOR GATE	12
3.1	DATA COMPARATOR	17
3.2	EXISTING FULL ADDER	19
4.1	PASS TRANSISTOR LOGIC	21
4.2	PROPOSED FULL ADDER	22

LIST OF SYMBOLS AND ABBREVIATIONS

SYMBOLS	ABBREVIATIONS
VLSI	Very Large Scale Integration
IC	Integration Chip
ALU	Arithmetic & Logic Unit
CLA	Carry Look Ahead Adder
HA	Half Adder
FA	Full Adder
XOR	Exclusive or Gate
CMOS	Complementary Metal Oxide Semiconductor
RCA	Ripple Carry Adder
²² MOSFET	Metal Oxide Semiconductor Field Effect Transistor
ADC	Analog to Digital Converter
FPGA	Field Programmable Gate Array
MDF	Main Distribution Frame
TDF	Testis Determining Factor
AROF	Adaptive Rank Order Filter
MSB	Most Significant Bit
MOS	Military Occupational Specialty Code
HSPICE	Hewlett Stimulation Program with Integrated Circuit

CHAPTER 1

INTRODUCTION

The method of incorporating thousands of transistors into a single chip is known as VLSI design. VLSI design is primarily used to reduce the area of interconnecting fabrics. IC fabrication technology, designer efficiency, and cost are the key factors that restrict the production of smaller and more complex IC chips. Different performance aspects are relevant depending on the application. A processor's ALU is a crucial component. It is capable of performing both arithmetic and logic operations. The multiplier's efficiency determines how quick and accurate the process is. As a result, improving the multiplier's output improves the ALU's quality. To improve the output of a multiplier, we must improve the efficiency of the adder.

In an advanced computerized VLSI design, paired expansion is the most crucial and fundamental math include. The wave convey viper is the absolute first and most essential snake that can perform double number expansion. It isn't actually helpful since its inactivity is corresponding to the length of its info operands. The convey ahead viper is utilized to accelerate the expansion cycle. In contrast with conventional adders, equal prefix adders produce great execution. The viper with the huge, complex entryways would be excessively delayed for VLSI, so the plan is modularized by separating it into a tree of more modest, quicker adders. Thus, the postponement of pushing the help through the look-forward stages gets overwhelmed, and tree adders or equal prefix adders are utilized. To create the current entirety, rapid adders rely upon the past convey. Any decrease in deferral would bring about an increment in throughput in number expansion.

Equal prefix adders are reasonable for VLSI execution since the transfer on the utilization of straightforward cells and keep up ordinary association between them. We can characterize each prefix structure as

far as rationale levels, fan out and wiring tracks. Equal prefix adders give a decent hypothetical premise to make scope of configuration compromise regarding territory, force and deferral.

1.1. ADDERS

A snake, likewise called as a season, is a computerized circuit which is utilized to perform mathematical expansion. Adders are utilized in different spaces of the processor to figure table records, augmentation and decrement administrators ,addresses and different activities, just as in the math rationale systems(ALU) of certain PCs and different sorts of processors.

Adders can be developed for an assortment of mathematical portrayals, including parallel coded decimal and abundance 3, however paired numbers are the most well-known. It is easy to change over a snake into a viper subtractor when two's supplement or ones' supplement are utilized to address negative numbers. Other marked number portrayals require extra rationale notwithstanding the fundamental snake. Wave convey adders (RCA), for instance, to logarithmic - defer adders, for example, the convey look snake early, viper (CLA). There are a few other exhibition upgrading plans, for example, the convey increase snake and the Ling viper, that can improve the convey chain considerably more. In any case, since equal prefix trees have standard designs with logarithmic postponement, they are the most productive method of offering double expansion in Very Large Scale Integration (VLSI) advanced frameworks.

The initial phase in an equal prefix snake is to get the convey at each piece, and the subsequent advance is to register the absolute piece dependent on the convey bit. Prefix trees are more slow algorithmically than quick logarithmic adders like the convey spread adders, however their standard models permit them to outflank customary CLA adders. A convey look forward snake, which is utilized in one of Motorola's processors, causes this in VLSI structures. carries out the convey chain vertically as opposed to on a level plane,

which seems to build wire thickness and fan-in/out reliance. In spite of the way that logarithmic snake structures are perhaps the quickest viper algorithmically, the speed effectiveness of the convey look forward viper has been hampered by unavoidable losses because of fan-in and fan-out conditions, just as the substantial wire load dispersion the vertical way

1.1.1. Half Adder

A paired snake that adds two single parallel digits A_n and B is known as a half viper. Entirety (S) and convey (C) are the two yields (C). The convey signal demonstrates that a multi-digit expansion has flooded into the following digit. $2C + S$ is the estimation of the number. A full viper can be made by consolidating two half adders. The augends and numbers to be added pieces are the information factors of a half viper. The number and convey are the yield factors. Adders in VLSI advanced frameworks utilize parallel documentation, as recently expressed. At that point, utilizing Boolean conditions, add is done one small step at a time. Consider a twofold add with two n -cycle inputs $A;B$, the slightest bit convey in cin , and n -digit yields s .

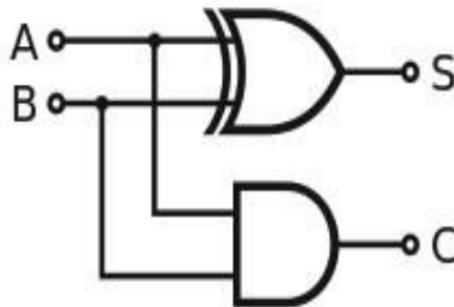


Figure 1.1.one bit half adder

Adders can be developed for an assortment of mathematical portrayals, including parallel coded decimal and abundance 3, however paired numbers are the most well-known. It is easy to change over a snake into a viper subtractor when two's supplement or ones' supplement are utilized to address negative numbers. Other marked number portrayals require extra rationale notwithstanding the fundamental snake. Wave convey adders (RCA), for instance, to logarithmic - defer adders, for example, the convey look snake early, viper (CLA).

The Equation can be carried out as demonstrated in Figure In the figure, there is a half snake, which takes just 2 information bits. Condition can be stretched out to perform full add activity, where there is a convey input.

1.1.2. Full adder

A full snake adds parallel numbers and records for values conveyed in just as out. A the slightest bit total viper adds three the slightest bit numbers, now and again composed as A, B, and C; the operands are A and B, and C is a piece conveyed in from a past less huge point. The total viper is typically important for a course of adders that add paired quantities of 8, 16, 32, etc.

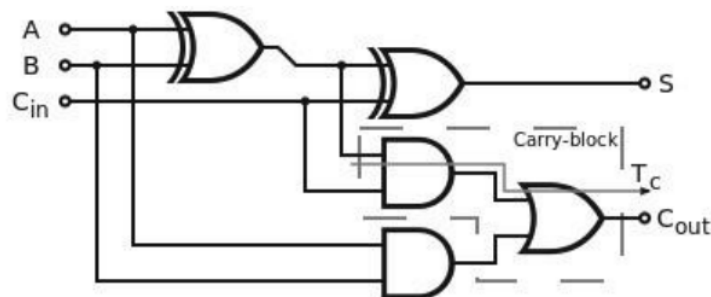


Figure 1.2.one bit full adder

an entire the slightest bit snake Equation can be utilized to construct a total viper. Figure shows the square outline of a 1-digit complete viper. For registering do, the total snake is comprised of two half adders and an OR entryway. Condition isn't expressly executed by the doors in Figure. The comparability can be handily shown utilizing Boolean algebra. Two paired literals are added to help in the calculation of the convey for each piece. They're known as convey produce and convey proliferate, and they're addressed by the letters g_i and p_i , individually. There's even an exacting considered impermanent total t_i that is used. There is an association between these literals and the sources of info. With the help of the literals above, yield convey and aggregate at each piece can be composed. Carry-proliferate p_i can be supplanted with transitory sum t_i in certain literary works to diminish the quantity of rationale doors. These two words are separated here to make the definitions more clear. Just p_i is utilized as convey engender in Ling adders, for instance. It is feasible to expand the single piece convey create/spread to bunch variant G and P. The inborn connections are appeared in the conditions underneath.

The gathering term from I to k is signified by I k. Convey can be communicated in the accompanying condition utilizing bunch convey produce/engender.

1.2.Multiplexer

The action of conveying in any event one basic or electronic signs over an average transmission line at different events or rates is suggested as multiplexing, and the structure we use to do so is implied as a multiplexer.

The multiplexer, shortened as "MUX" or "MPX," is a combinational reasoning circuit that uses a control sign to transform one of a couple

of data lines over to a single normal yield line. Multiplexers work like extremely effective various area turning switches, connecting or controlling numerous info lines, alluded to as "channels," to the yield each in turn.

Multiplexers, otherwise called MUXs, are advanced circuits that convert computerized or paired information utilizing high velocity rationale entryways, or simple circuits that pass one of the voltage or current contributions to a solitary yield utilizing semiconductors, MOSFETs, or transfers.

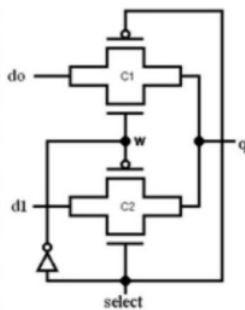


Figure 1.3:Diagram of Muxtipler

1.2. Comparator

A comparator is a gadget in hardware that analyzes two voltages or flows and yields a computerized signal demonstrating which is more prominent. There are two simple information terminals on it. A comparator is a high-acquire differential speaker with a specific plan. They're regularly utilized in simple to-advanced converters (ADCs) and unwinding oscillators, just as different instruments that figure and digitize simple signs.

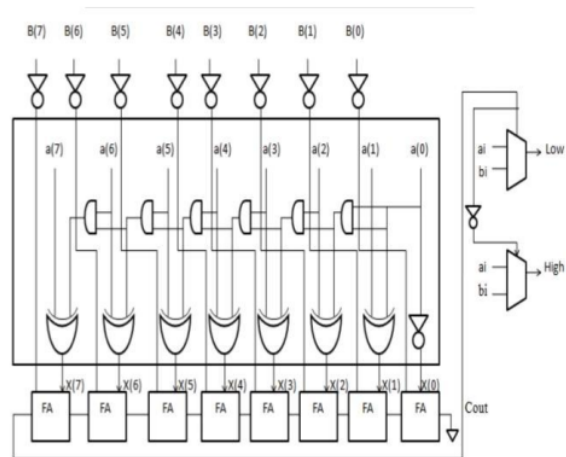


Figure 1.5: Diagram of Comparator

1.4.AND Gate

The AND gate is one of the ²¹ fundamental computerized rationale entryway that executes intelligent combination; it works as per reality table . The AND entryway creates a HIGH yield in particular if the entirety of its data sources are HIGH (1).



Figure 1.10: symbol of XOR GATE

⁵ 1.1.TRUTH TABLE OF AND GATE:

A	B	Q

0	0	0
0	1	0
1	0	0
1	1	1

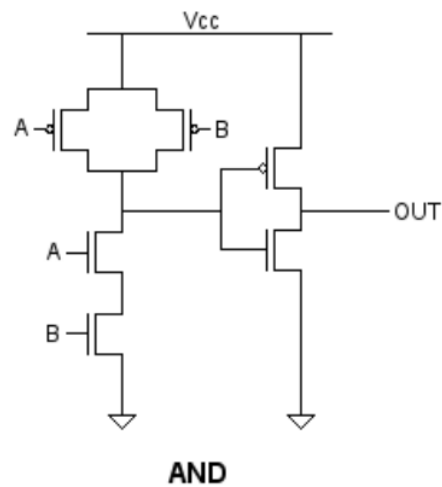
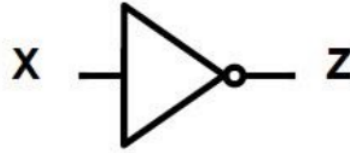


Figure 1.7:AND GATE (transistor level)

1.5.NOT GATE

NOT gate also called as inverter. It is a solitary information gadgets with a yield level that is for the most part at rationale level "1" and goes "LOW" to a rationale level "0" when their single info is at rationale level "1," as such, they "modify" (supplement) their info signal. At the point

when the contribution to a NOT entryway is at rationale level "0," the yield returns "HIGH," giving us the Boolean articulation: $A = Q$.



⁷ Figure 1.8: Symbol of NOT GATE

²⁰ **1.2. TRUTH TABLE OF NOT GATE:**

INPUT	OUTPUT
0	1
1	0

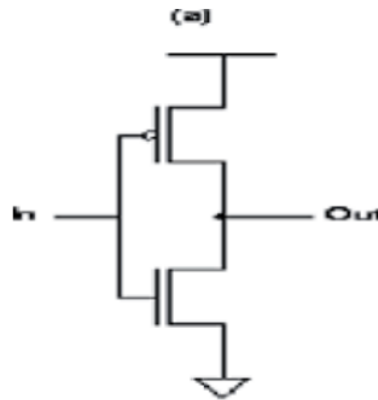


Figure 1.9: NOT GATE (transistor level)

1.6.XOR GATE:

When the number of true inputs is odd, the XOR gate (also known as EOR or EXOR and pronounced Exclusive OR) produces a true (1 or HIGH) output. An XOR gate implements an exclusive or, which means that a true output is produced if only one of the gate's inputs is true. A bogus yield is created when the two information sources are bogus (0/LOW) or both are genuine. The disparity work is addressed by XOR, where the yield is legitimate if the data sources are not the same and bogus in any case. "Ought to have either however not both" is a decent method to note XOR



Figure 1.10:symbol of XOR GATE

1.2.TRUTH TABLE OF XOR GATE:

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

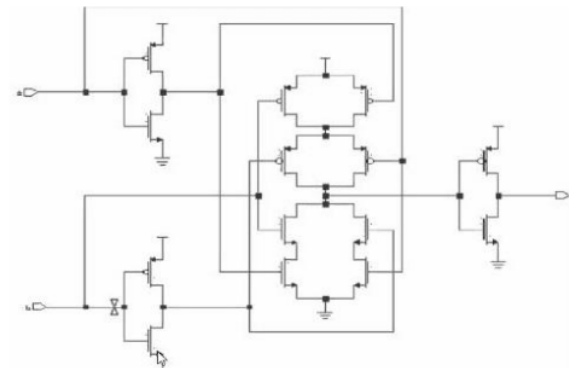


Figure 1.11:XOR GATE (transistor level)

1.7.ORGANIZATION OF THE REPORT

The undertaking report is coordinated into six sections

Section 1 examines the foundation of VLSI, inspiration, presentation of double adders. It additionally examines about the different multipliers and association of the undertaking work.

Section 2 conveys nitty gritty writing overview identified with the venture, writing outline, issue definition, targets of the undertaking.

Section 3 depicts the working and existing methods of information comparator,full adder,mux,AND gate,NOT gate,XOR door.

Section 4 examines the proposed full snake configuration utilizing pass semiconductor and Power Consumption.

Section 5 gives the recreation results and execution investigation of the current and proposed project work. It does a full similar examination on how the proposed work is in an ideal situation than the current plan.

Section 6 gives the end project work. It additionally gives the pattern of things to come work that is the manner by which the undertaking could be upgraded further. At long last, the references alluded to lead the venture are given in a nutshell.

CHAPTER 2

2.1.LITERATURE SURVEY AND OBJECTIVES

The writing overview and survey are talked about in this section. It additionally gives a thorough portrayal of the current comparator, mux, NOT, AND, XOR, and complete viper structures, just as how they are orchestrated.

⁴ Vasanth.k, Kavirajan A.A.F, Ravi.T, NirmalRaj.S(April 2014), "A Novel 8 Bit Digital Comparator for 3x3 Fixed Kernel Based Modified Shear Sorting," *Indian Journal of Science and Technology*, vol. 7, issue 4, pp. 452-462, April 2014. Any middle channel that is acceptable at eliminating motivation commotion without corrupting the picture data requires an enhanced field, speed, and force. The middle's key capacity is Rank requesting. This presents Snake-like arranging, a cutting edge arranging strategy. An equal design is utilized to execute the proposed Sorting procedure. Two models are recommended that are practically identical to the standard 8 digit comparator and convey select comparator. The area involved by equal design for changed shear arranging middle engineering is one 10th that of other 1D calculations. The equal engineering is found to have a lower delay and devours less force. Subsequently, we propose a low-territory, fast equal pipelined design.

Vasanth, S.Karthik(2016) *FPGA IMPLEMENTATION OF MODIFIED DECOMPOSITION FILTER 1K.1* ³³ Research Scholar, 2 Research Advisor 1Sathyabama University is a Tamilnadu college in Chennai, India. 2Cognizant Technology Solutions is an Indian organization situated in Chennai, Tamil Nadu. In this paper, another territory limited engineering for middle channels is proposed, which depends on a changed deterioration calculation. The intricacy of current limit disintegration calculations, for example, complex comparators, is supplanted by the adjusted deterioration. Deterioration and recombination

are the two stages of the proposed calculation. Rather than the TDF, which utilizes countless complex comparators and adders, the MDF utilizes basic comparators, cradles, and adders. When went against to TDF, the MDF calculation consumes less space on the floor plan and in the steered FPGA. We perceive that the proposed calculation requires less cuts and a look-into table inside the FPGA. The proposed calculation's planning and force are practically identical to the current calculation. Accordingly, for the Decomposition calculation, a region decreased design is proposed.

S. Karpagaabirami and P. Ramamoorthy, "An Efficient VLSI Architecture for Removal of Impulse Noise in Images," *International Journal of Computer Science and Mobile Computing*, Vol. 3, Issue 5, pp. 567–574 (May 2014). Motivation commotion is a typical reason for picture defilement during picture handling and transmission systems. This paper proposes a VLSI execution of the Adaptive Rank Order Filter (AROF) for the expulsion of drive commotion. The calculation disposes of commotion without bargaining picture quality. The reenactment results show that the DTBDM VLSI Implementation occupies more room and is likewise more complex. When contrasted with DTBDM, the VLSI execution of DROF utilizes less space and has a less complex design. For higher clamor densities, the Adaptive Rank Order Filter beats different methodologies regarding separating properties. The consequences of the examinations show that AROF-based reestablished pictures with higher clamor densities have preferred visual quality over those got utilizing different methodologies.

VLSI Architectures for 8 Bit Data Comparators for Rank Ordering Image Applications by Sindhu. E and Vasanth. K The proposed work's principle objective is to make another Data comparator that gives a savvy answer for arranging/Rank requesting networks dependent on speed, force, and region. The proposed work involves the formation of six separate 8-cycle comparators. The Xilinx 7.1i compiler device was utilized to focus on the yield of these six separate comparators for the

XCV1000-4bg560. For the focused on PC XCV1000-4bg560, an alternate engineering for information comparators was planned utilizing VHDL. The two cell sorters constructed were utilized on a pipelined design for adjusted shear arranging, and the design's yield was determined as far as region speed and force. Subsequently, a variable engineering for picture applications is proposed as rank request applications.

2.2.LITERATURE SUMMARY

The Decoder-based comparator is utilized to control the progression of rationale i.e information transfer. The proposed rationale circuit contrasts MSB of initial 8-digit and MSB of another 8-cycle double number and gives the yield by performing fundamental XOR door activity of X and Y respectively. The yield of these is taken care of to decoder that works when the pieces are indistinguishable the decoder is incapacitated and when the pieces be not the same as one another, the decoder is empowered and placed them in the legitimate request.

2.3.PROBLEM DEFINITION

To improve the functioning effectiveness of the current comparator, a new proposed model has been created to contrast the proposed model and the current model in terms of speed, power, power postpone item and region. Pipelining configuration is an appropriate VLSI design for diminishing the basic way, in the mean time it can lessens the speed. The fundamental activity of these engineering is performed by utilizing clock (clk) grouping.

2.4.OBJECTIVE OF THE PROJECT

1.To increase the capability of the 8 cycle Data Comparator for Low Power applications.

2.To improve Efficiency Low Power Techniques will be applied in all Circuits.

32 3.To examine, the characteristics of MOSFET Technology in regards to Power, Delay and Power Delay Product.

4.To perceive the Feasibility of 8 bit Data Comparator.

CHAPTER 3

PROCEDURE OF EXISTING SYSTEM

3.1.DATA COMPARATOR

Many digital systems, such as calculators, microprocessors, digital filters, and digital signal processors, rely heavily on data comparators. They're also used in discrete Fourier transform, correlation, and range measurement implementations. Since the comparison process is slow, the output of any digital device is normally calculated in terms of the used comparators. A comparator is an electronic circuit that compares two inputs and outputs the result of the comparison. To put it another way, the data comparator compares its inputs to produce differential output. This process necessitates a large number of hardware components and will also run at a slower tempo. Data Comparator and Sign Extension Tricks, Shift and Add, Reducing the Number of Partial Products The development of a high-speed data comparator that can handle both signed and unsigned numbers. There are 10 NOT gates, 6 AND gates, 7 XOR gates, 8 complete adder blocks, and 2 multiplexer blocks in this data comparator.

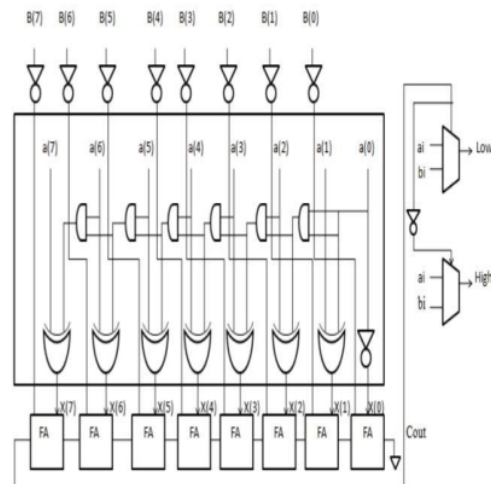


Figure 3.1.Data Comparator

3.2.Existing full Adder

The full snake is a snake that takes three data sources and yields two results. The underlying two wellsprings of information are An and B, with the third being a C-IN input. The pass on yield is checked C-OUT, while the average yield is named S, which addresses SUM. Various mechanized circuits that perform development or derivation use an all out snake circuit. It gets its name from the way that it adds two equal digits notwithstanding a pass on in digit to get a number and complete digit. It has three data sources and two yields thusly. The snake blocks have 18 semiconductors (9 p-mos and 9 n-mos) and 2 NOT entryways (c-mos inverter).

3.1.TRUE TABLE FOR FULL ADDER

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

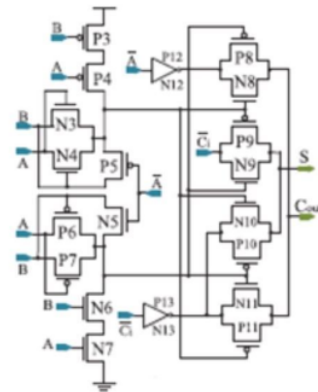


Figure 3.2.Existing Full Adder

MAIN FACTORS

- Power
- Delay
- Power Delay Product

CHAPTER 4

PROPOSED DATA COMPARATOR

In previous work, a Complete Adder with 18 transistors was used to design the Data Comparator. The Data Comparator in the proposed work is built using a modified Full Adder with 14 transistors, which consumes less power than the current design.

4.1.OPERATION OF THE RESTRUCTURED FULL ADDER

4.1.1.PASS TRANSISTOR

Unlike bipolar transistors, MOS transistors have an isolated gate that allows them to be used as switches in series with line carrying logic levels, similar to how relay contacts are used. The pass transistor and switching logic array is the name for this application of the MOS system.

ADVANTAGES OF PTL

1. As compared to CMOS, there are fewer devices needed to implement the logic functions.
2. Power consumption is low.

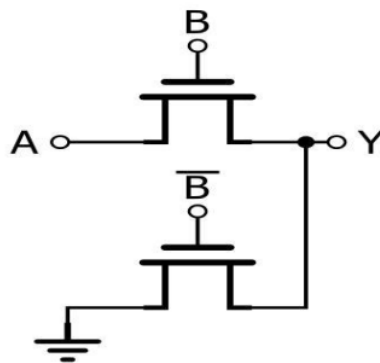


Figure 4.1 Pass Transistor Logic

4.1.2.PROPOSED FULL ADDER

The current complete adder is updated by reducing some transistors and redesigning it using the pass transistor logic. There are only 14 transistors in this proposed model (7 p-mos and 7 n-mos). The adder takes either a 0 or a 1 as input. When the input is 0, the p-mos is active; when the input is 1, the n-mos is active. As a result, the additional c-mos transistors are turned off at that time. It consumes more power and takes longer to complete, resulting in a delay and an increase in the power delay product. As a result, the power consumption and delay in this proposed model were minimised by reducing the transistors. As a result, it's a significant benefit of this proposed complete adder.

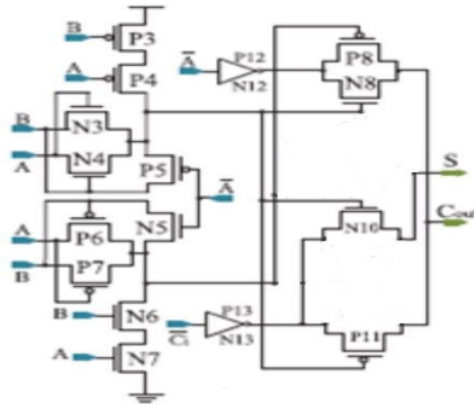
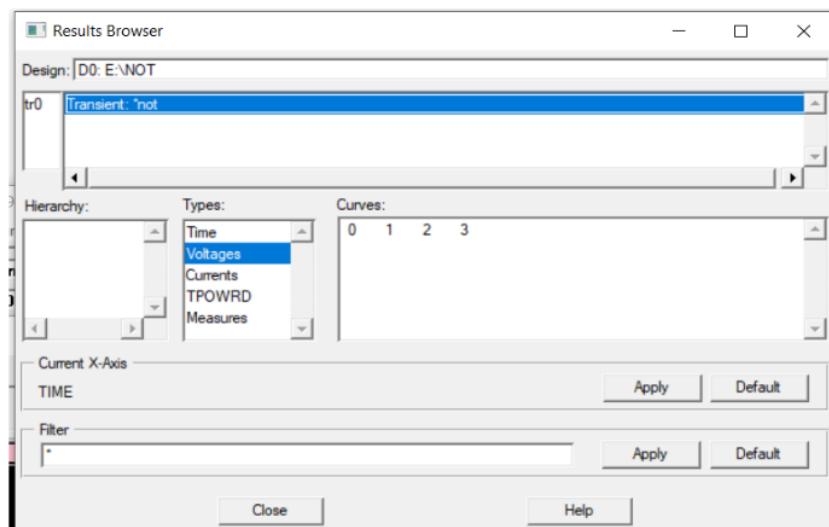
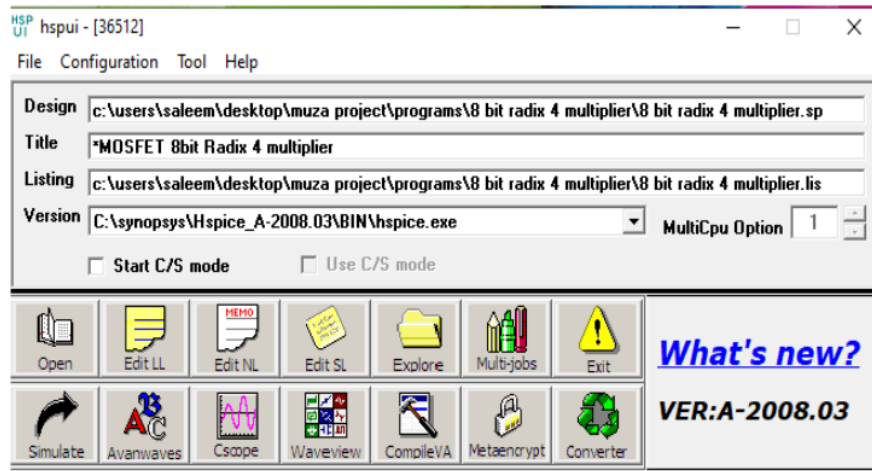


Figure 4.2 Proposed Full Adder

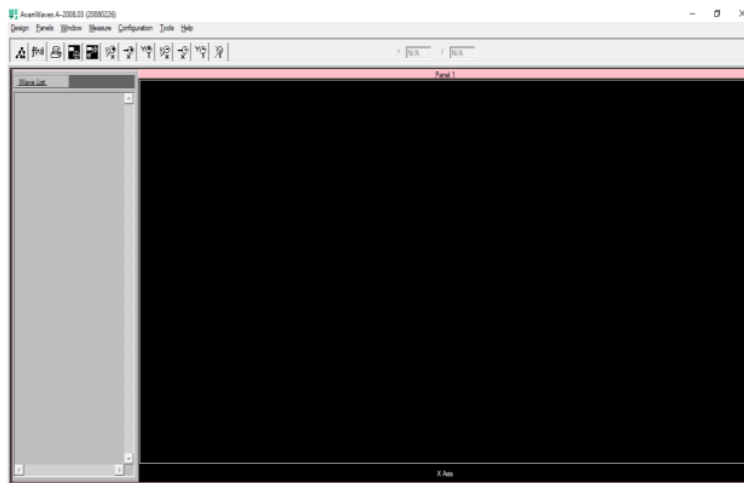
4.2.HSPICE SOFTWARE

Hewlett Simulation Program with Integrated Circuit is the complete name of HSPICE. Unlike block level plans made of individual segments, coordinated circuits can't be breadboarded prior to being

manufactured. Moreover, in view of the huge cost of photolithographic cover and other gathering necessities, it is essential to design the circuit to be anyway close to astounding as possible before it is by all accounts arranged. Until zeroing in on conveying a joined circuit, the business standard system for checking circuit action at the semiconductor level is to reenact the circuit with SPICE. It will, for example, draw circuits and model what happens when the circuits are controlled up/and how they act in various emergency conditions.



4.2.1.STIMULATION SCREEN

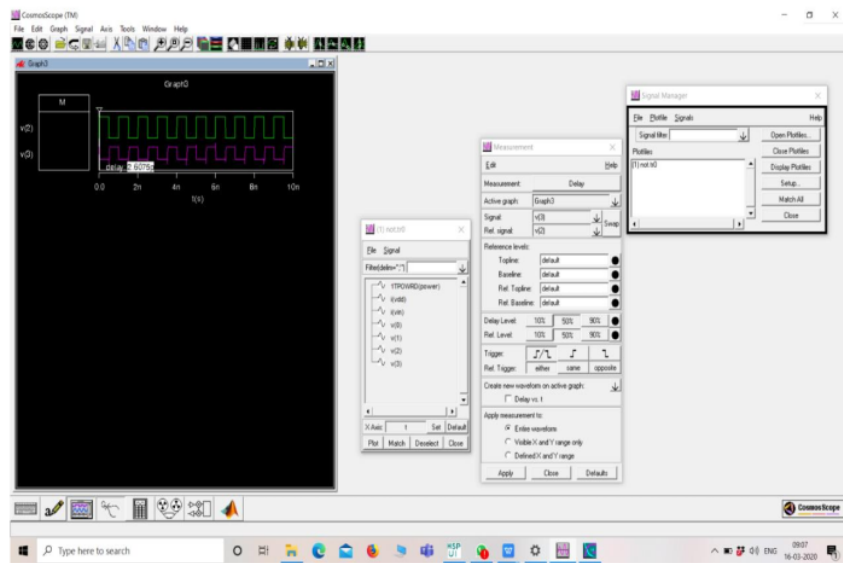


4.3.COSMOSCOPE

Cosmoscope is a software which is used to calculate the delay value.

Uses

- ¹⁷ Simpleware 3D Modeling **Software**.
- Clinical **Applications** for 3D Images.
- Life Sciences **Applications** for 3D Images.

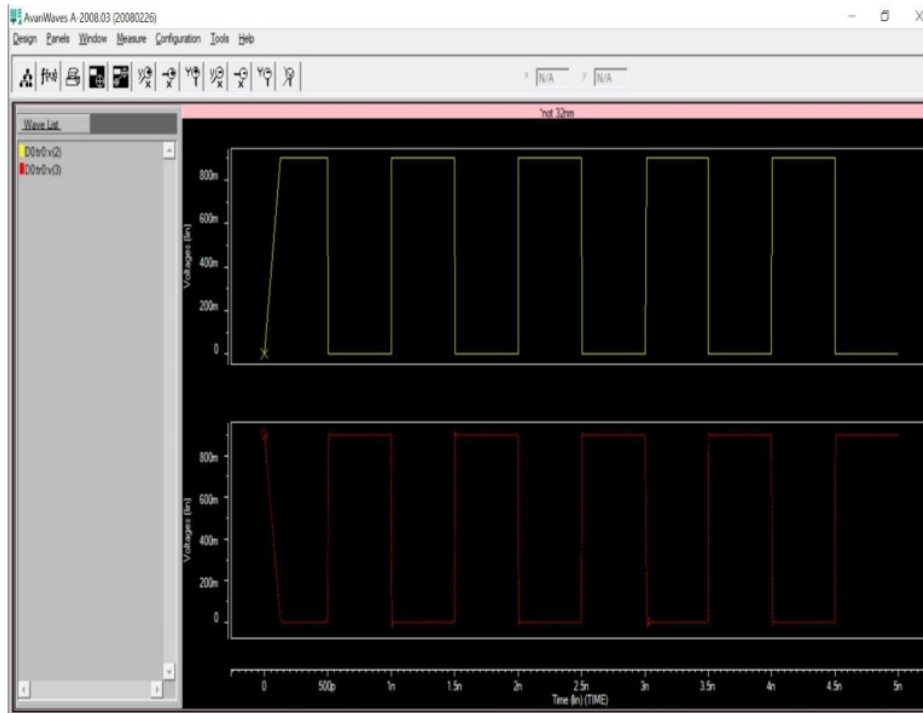


CHAPTER 5

RESULTS AND DISCUSSION

The existing and proposed architecture are simulated by using AvanWaves simulator. Output of the existing Data Comparator and proposed Data Comparator are analysed from the results and it is concluded that the proposed architecture reduces the power consumption compared with the existing system. The Synthesis is done using Hspice UI.

5.1 Simulation results for NOT Gate



19

Figure 5.1: Simulation results for NOT Gate

Figure 5.1 shows the simulation output of a NOT gate. The inputs given was a and the output is taken by b.

5.2.Simulation results for AND Gate

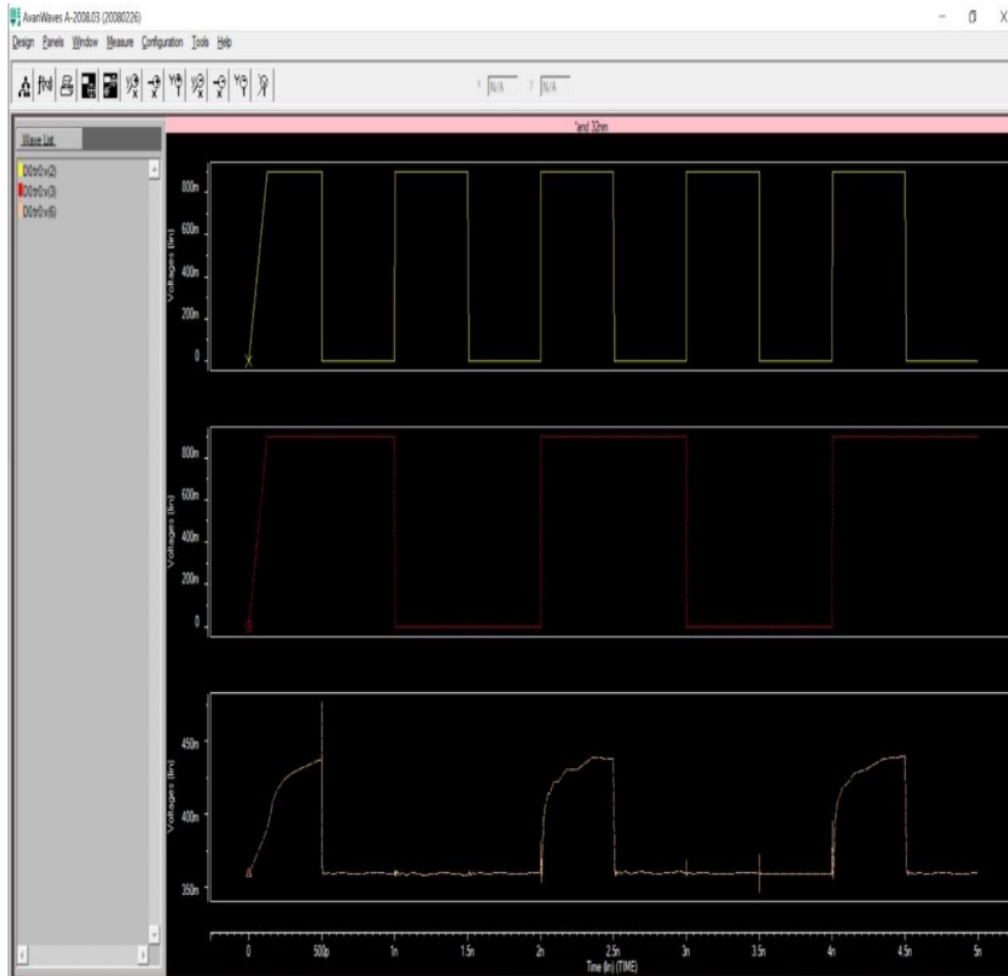


Figure 5.2: Simulation results for AND Gate

Figure 5.2 shows the simulation output of a AND gate. The inputs given were a, b and the output is taken by c.

5.3.Simulation results for XOR Gate

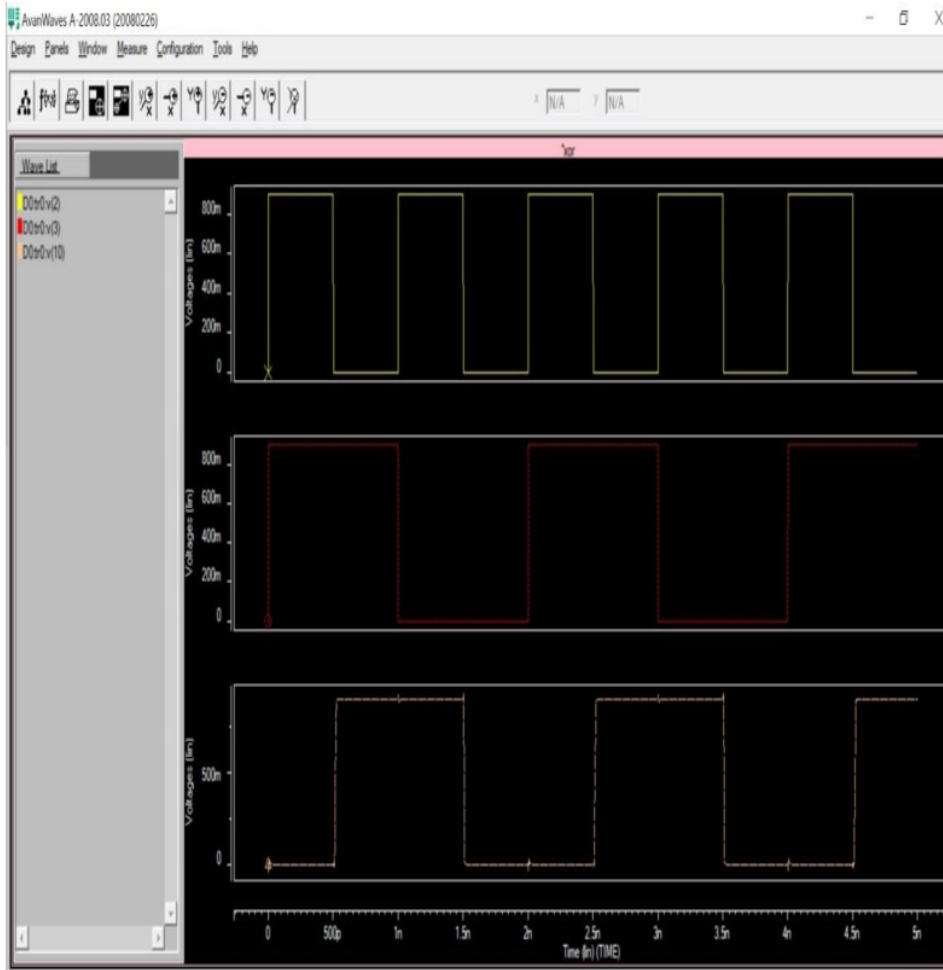


Figure 5.3: Simulation results for XOR Gate

Figure 5.3 shows the simulation output of a xor gate. The inputs given were a, b and the output is taken by c.

5.4.Simulation results for MUX Gate

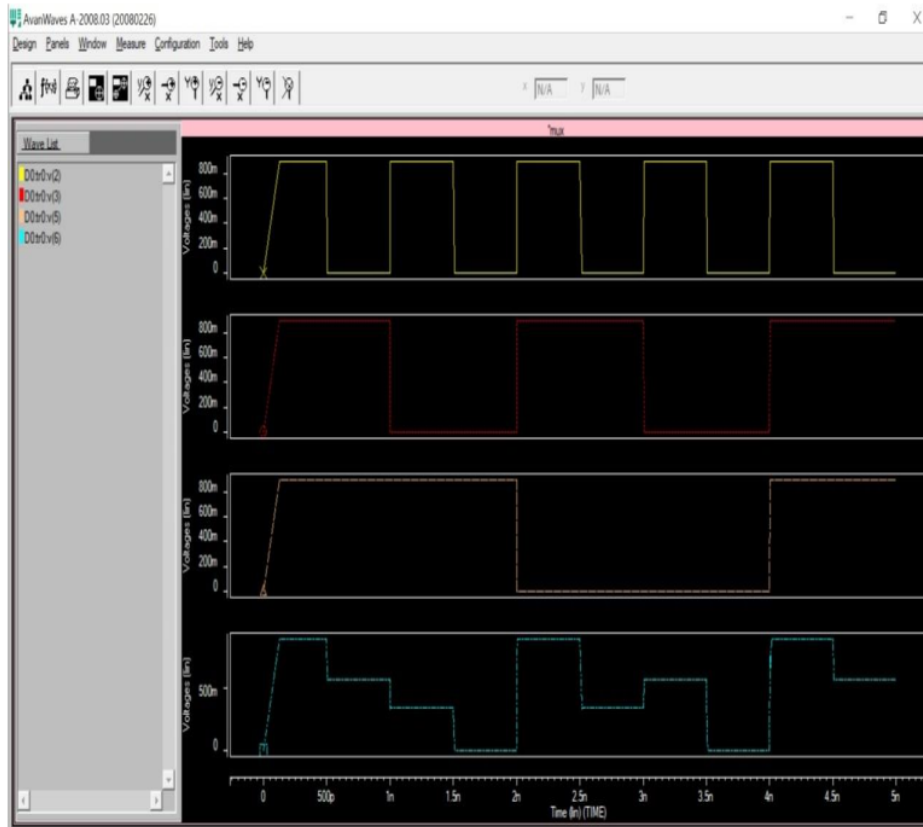


Figure 5.4: Simulation results for XOR Gate ¹⁵

Figure 5.4 shows the simulation output of a MUX gate. The inputs given were a, b,select and the output is taken by c.

29 5.5.Simulation results for Full Adder

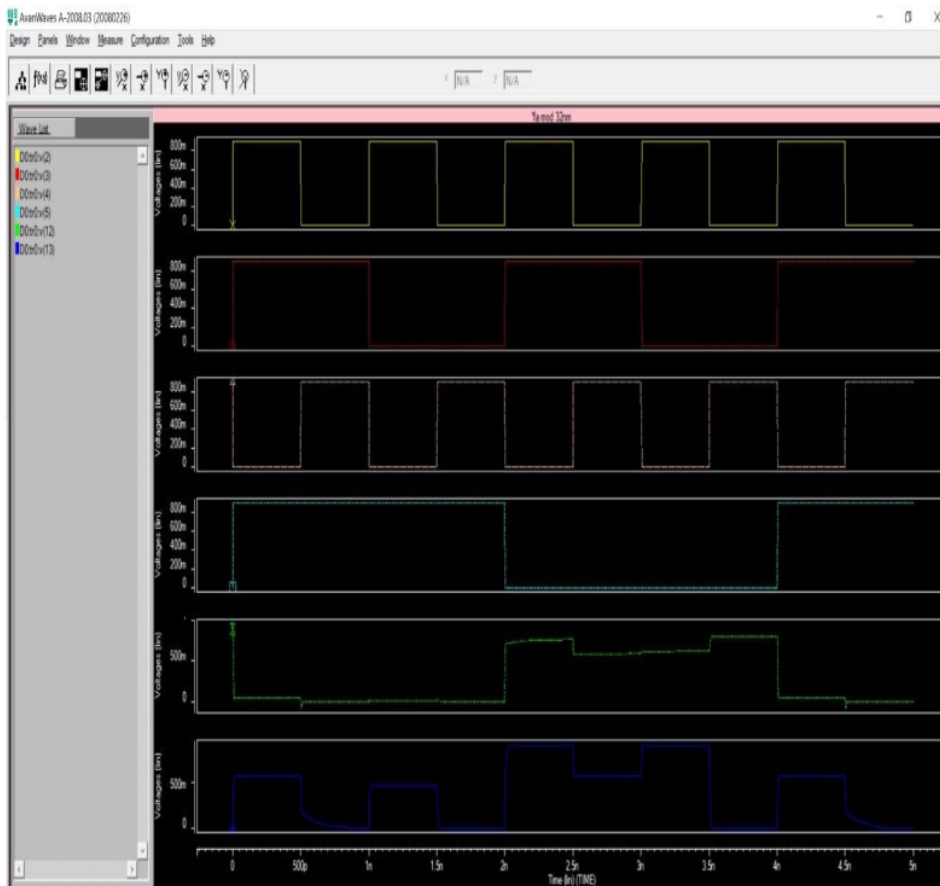


Figure 5.5: Simulation results for Full Adder

Figure 5.5 shows the simulation output of a Full Adder. The inputs given were a, b and the output is taken by c.

5.6.Simulation results for Data Comparator

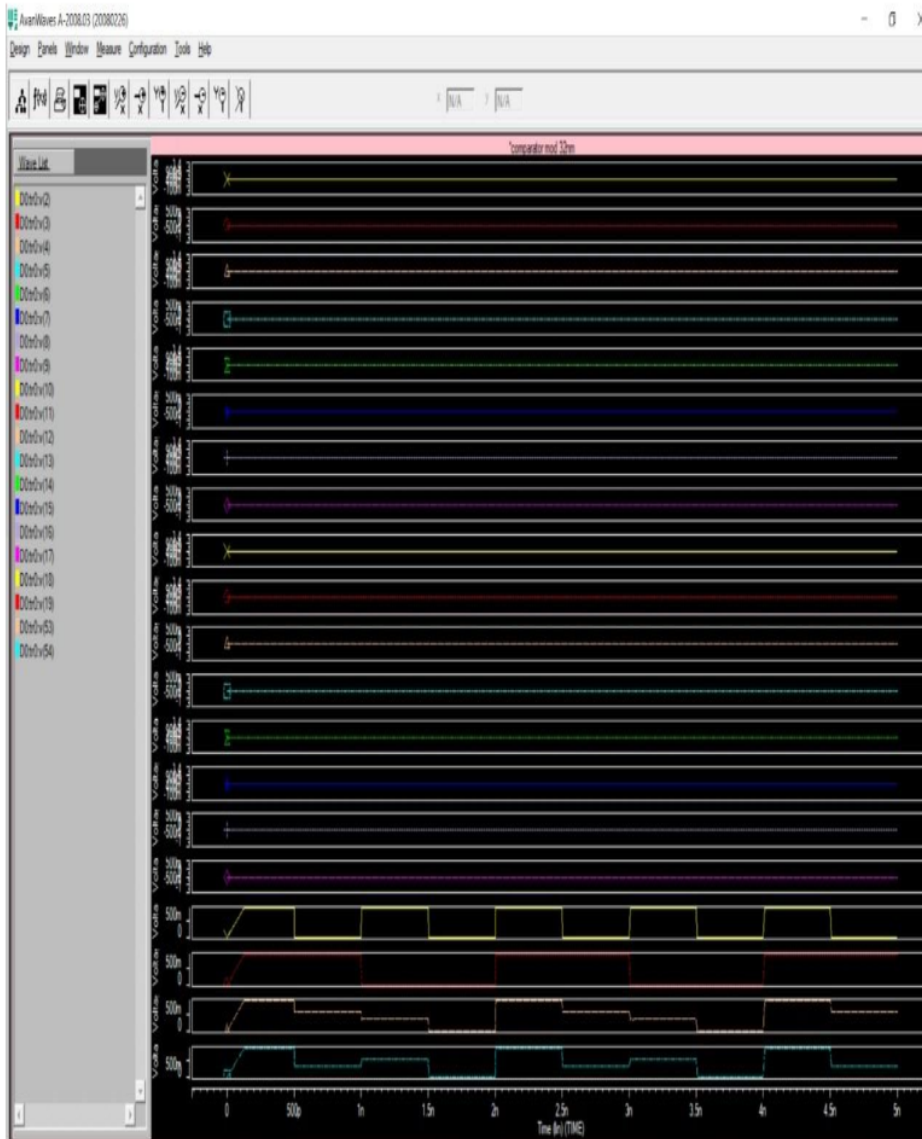


Figure 5.6: Simulation results for Data Comparator

Figure 5.6 shows the simulation output of a Data Comparator. The performance has been analysed.

5.7.PERFORMANCE ANALYSIS

The exhibition investigation of AND,NOT,XOR,Full Adder,Comparator regarding power has been given beneath.

5.7.1.PERFORMANCE ANALYSIS OF NOT GATE

Table 5.1: Design analysis of 130NM NOT gate

NOT GATE (130NM) PARAMETERS	VALUES
POWER	$1.556 * 10^{-5}W$
DELAY	$46.594 * 10^{-12}s$
POWER DELAY PRODUCT	$72.5002 * 10^{-17}J$

Table 5.2: Design analysis of 32NM NOT gate

NOT GATE (32NM) PARAMETERS	VALUES
POWER	$4.849 * 10^{-8}W$
DELAY	$558.58F s$
POWER DELAY PRODUCT	$270.8554 * 10^{-7}J$

5.7.2.PERFORMANCE ANALYSIS OF AND GATE

Table 5.3: Design analysis of 130NM AND gate

AND GATE (130NM) PARAMETERS	VALUES
POWER	$8.052 * 10^{-6}W$
DELAY	2.0675 PFs
POWER DELAY PRODUCT	$16.6475 * 10^{-18}J$

Table 5.4: Design analysis of 32NM AND gate

AND GATE (32NM) PARAMETERS	VALUES
POWER	$4.849 * 10^{-8}W$
DELAY	558.58Fs
POWER DELAY PRODUCT	$270.8554 * 10^{-7}J$

5.7.3.PERFORMANCE ANALYSIS OF AND GATE

Table 5.5: Design analysis of 130NM XOR gate

XOR GATE (130NM) PARAMETERS	VALUES
POWER	$4.707 * 10^5 W$
DELAY	102.86 PFs
POWER DELAY PRODUCT	$484.1620 * 10^{-17} J$

Table 5.6: Design analysis of 32NM XOR gate

XOR GATE (32NM) PARAMETERS	VALUES
POWER	$4.776 * 10^7 W$
DELAY	16.293PF s
POWER DELAY PRODUCT	$77.8153 * 10^{-19} J$

5.7.4.PERFORMANCE ANALYSIS OF MUX

**Table 5.7: Design analysis of 130NM
MUX**

MUX GATE (130NM) PARAMETERS	VALUES
POWER	$8.821 * 10^{-6}W$
DELAY	6.5677 PF s
POWER DELAY PRODUCT	$57.9336 * 10^{-18}J$

Table 5.8: Design analysis of 32NM MUX

MUX GATE (32NM) PARAMETERS	VALUES
POWER	$1.752 * 10^{-5}W$
DELAY	229.48PF s
POWER DELAY PRODUCT	$402.0489 * 10^{-5}J$

5.7.5.PERFORMANCE ANALYSIS OF FULL ADDER GATE

Table 5.9: Design analysis of 130NM Full Adder

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING FULL ADDER	$5.736 * 10^{-5}W$	11.417 PF s	$65.4879 * 10^{-17}J$
PROPOSED FULL ADDER	$3.997 * 10^{-5}W$	9.309 PF s	$36.0965 * 10^{-17}J$

Table 5.10: Design analysis of 32NM Full Adder

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING FULL ADDER	$5.026 * 10^{-5}W$	9.7557 PF s	$49.0396 * 10^{-17}J$
PROPOSED FULL ADDER	$3.951 * 10^{-5}W$	4.5131 PF s	$17.8312 * 10^{-16}J$

5.7.6.PERFORMANCE ANALYSIS OF COMPARATOR

TABLE 5.11:Design analysis of 130nm comparator

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING COMPARATOR	$1.918 * 10^{-4}W$	66.794 PF s	$128.1108 * 10^{-16}J$
PROPOSED COMPARATOR	$1.723 * 10^{-4}W$	46.804 PF s	$80.643 * 10^{-16}J$

TABLE 5.12:Design analysis of 32nm comparator

PARAMETERS	POWER	DELAY	POWER DELAY PRODUCT
EXISTING COMPARATOR	$4.160 * 10^{-4}W$	62.701 PF s	$260.8361 * 10^{-16}J$
PROPOSED COMPARATOR	$2.977 * 10^{-4}W$	62.695 PF s	$186.643 * 10^{-16}J$

CONCLUSION

The propose model data comparator with the restructured full adder block will be used in the low power applications like ATM machines,DSP processors.The power value has been calculated with the help of the HSPICE tool and avanwaves .Delay will be calculated by using the CosmosScope. The main objective of this project is to develop a comparator which should consume low power, the delay value should be low, the speed should be high and the area consumption should be less.The performance analysis of the proposed data comparator with the existing model clearly shows that the proposed model works efficiently that the existing model.By using the pass transistor logic,the existing data comparator is restructured.Whenever the input is 1 the Pmos is ON and Nmos will be OFF,where as whenever the input is 0 the Nmos will be ON and the Pmos will be OFF.In order to overcome these, a new proposed model has been developed.. The average power value for the existing data comparator $4.160 * 10^{-4}W$ which got reduced to $2.977 * 10^{-4}W$. It shows that power consumption got reduced to half,delay and power delay product also reduced .

analysis of 8 bit comparison

ORIGINALITY REPORT

13%

SIMILARITY INDEX

6%

INTERNET SOURCES

6%

PUBLICATIONS

8%

STUDENT PAPERS

PRIMARY SOURCES

1	E. Sindhu, K. Vasanth. "VLSI Architectures for 8 Bit Data Comparators for Rank Ordering Image Applications", 2019 International Conference on Communication and Signal Processing (ICCSP), 2019 Publication	2%
2	Submitted to BITS, Pilani-Dubai Student Paper	1%
3	ijarcse.com Internet Source	1%
4	www.ijareeie.com Internet Source	1%
5	Submitted to Guru Nanak Dev Engineering College Student Paper	1%
6	Submitted to The University of the South Pacific Student Paper	1%
7	Submitted to SASTRA University Student Paper	<1%

8	Submitted to Uxbridge College, Middlesex Student Paper	<1 %
9	Submitted to The Scientific & Technological Research Council of Turkey (TUBITAK) Student Paper	<1 %
10	Submitted to Universiti Tenaga Nasional Student Paper	<1 %
11	Submitted to Newport and District Group Training Association Student Paper	<1 %
12	Foroutan, Vahid, MohammadReza Taheri, Keivan Navi, and Arash Azizi Mazreah. "Design of two Low-Power full adder cells using GDI structure and hybrid CMOS logic style", Integration the VLSI Journal, 2013. Publication	<1 %
13	en.wikipedia.org Internet Source	<1 %
14	Submitted to Al Ain University of Science and Technology Student Paper	<1 %
15	Anil K. Maini. "Digital Electronics", Wiley, 2007 Publication	<1 %
16	www.coursehero.com Internet Source	<1 %

17	www.synopsys.com Internet Source	<1 %
18	Submitted to Lassiter High School Student Paper	<1 %
19	Submitted to University of East London Student Paper	<1 %
20	www.doctrionics.co.uk Internet Source	<1 %
21	Submitted to Middle East College of Information Technology Student Paper	<1 %
22	docplayer.net Internet Source	<1 %
23	Submitted to KDU College Sdn Bhd Student Paper	<1 %
24	Submitted to University of Leeds Student Paper	<1 %
25	ebookshelf.ust.hk Internet Source	<1 %
26	Submitted to VNR Vignana Jyothi Institute of Engineering and Technology Student Paper	<1 %
27	Submitted to Higher Education Commission Pakistan Student Paper	<1 %

28

N. Rajeswaran, S. Karpagaabirami, C. Gokilavani, R. Rajendran. "FPGA Based Denoising Method with T-Model Mask Architecture Design for Removal of Noises in Images", Procedia Computer Science, 2016

Publication

<1 %

29

Submitted to University of North Texas

Student Paper

<1 %

30

Sarah L. Harris, David Money Harris. "Digital Building Blocks", Elsevier BV, 2016

Publication

<1 %

31

documents.mx

Internet Source

<1 %

32

Chip-Hong Chang, Mingyan Zhang, Jiangmin Gu. "A novel low power low voltage full adder cell", 3rd International Symposium on Image and Signal Processing and Analysis, 2003. ISPA 2003. Proceedings of the, 2003

Publication

<1 %

33

Vasanth, K., and S. Karthik. "FPGA implementation of modified decomposition filter", 2010 International Conference on Signal and Image Processing, 2010.

Publication

<1 %

Exclude bibliography On