

MAXIMUM DEMAND CONTROL SYSTEM FOR SMART CITY USING WIRELESS COMMUNICATION

Submitted in partial fulfilment of the requirements for the award of Bachelor of
Engineering degree in Electronics and Communication Engineering

By

ALLAN DINO.J (37130018)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION

ENGINEERING

SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

Accredited with Grade “A” by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI,

CHENNAI - 600 119

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of ALLAN DINO.J (37130018) who have done the Project work as a team who carried out the project entitled "MAXIMUM DEMAND CONTROL SYSTEM FOR SMART CITY **USING WIRELESS COMMUNICATION**" under my supervision from December 2020 to March 2021.

Internal Guide

Dr.M.SUBRAMONIAM, M.E, Ph.D.

Head of the Department

Dr. T. RAVI M.E, Ph.D

Submitted for Viva voce Examination held on_____

DECLARATION

I, ALLAN DINO.J (37130018) hereby declare that the Project Report entitled “MAXIMUM DEMAND CONTROL SYSTEM FOR SMART CITY USING WIRELESS COMMUNICATION” done by us under the guidance of Dr. M. SUBRAMONIAM at Sathyabama Institute of Science and Technology is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

DATE:

PLACE:

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SIGNATURE OF THE CANDIDATE

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ABSTRACT

The Maximum Demand Controller is a system that meets the needs of the load management industries. When demand reaches a predetermined level, an alarm is sounded. This sequence is predetermined by the user and is programmed jointly by the user and the supplier of the device. The plant equipment's selected for the load management are stopped and restarted as per the desired load profile. Demand control scheme is implemented by using suitable control contactors. When the industrial cross the load limit the monitoring unit automatically identifies and gives alert system, then the industry must reduce the load applied, if they did decreases the load applied then the embedded system will automatically will remove the load and inform this information to the EB station using WPAN.

A network for the transmission of energy from sources to customers is an electrical grid. It consists of generating power plants, high-voltage transmission lines that transport energy from remote sources to demand centres and distribution lines connecting individual consumers. Power plants can be built near a source of combustible, at a dam site or to take advantage of renewable energy sources. Typically, they are very broad to use the economies of scale. The induced electrical power is increased to a higher voltage connecting it to the transmission network.

Tiny digitals built on the IEEE standard for wireless personal area networks, GSM are proprietary wireless protocols developed by Microchip technology used in small digital radios (WPANs). It is planned for low data transfer speeds and low-cost networks. If the industry passes the demand for load, the device reduces the load added automatically and informs the EB through the low data rate of RF transfer.

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CHAPTER – 1

INTRODUCTION

I. INTRODUCTION

The ongoing expansion and growth of the electric utility industry continuously introduce changes to a once predictable business. Electricity is being more and more regarded and treated as a commodity. This way, transmission systems are moved closer with the emphasis on power efficiency transmitted to their reliability and thermal limits.

Financial and business pressures will continue to require an efficient and more productive power system service with regard to the production, transmission and delivery in the changing utility setting. The safety and stability of electricity systems relies on advanced technology. It is apparent that more effective use and management of the current transmission system capacity is needed to achieve both operating efficiency and financial viability.

The use of advanced control technology improves the use of the current power grid. The Flexible AC Transmission Systems (FACTS) or power based electronic equipment have the validated technological solutions to tackle today's modern operational challenges. In comparison to the installation of new transmission lines, FACTS technology allows for better operations with limited capital expenditure, environmental effects and deployment times. As a cost-efficient alternative to the building of a new transmission line, FACTS systems provide advanced solutions. FACTS include the required transmission functional adjustments to make effective use of current transmission networks so that the difference between the stability and the thermal level is minimised.

CHAPTER - 2

LITERATURE REVIEW

The following IEEE papers are studied and reviewed and the limitations are observed and specified in this session and some of the concepts are used in formulating this system.

2.1 An evaluation method of maximum urban power supply capability based on dynamic voltage stability margin Xin Zhang; Huiling Li; Hongmei Luo; Xin Zhang; Xiuyue Yu; Feng Chen; Shu Liu IEEE 2019.

The maximum urban power supply potential is calculated using a formula based on a dynamic voltage stability margin (DVSM) (MUPSC). The aim is to optimise the power load while observing safety constraints on N-1. Restrictions include device stability limit, thermal stability limit, generator excitation current limit, voltage load limit, etc. In view of the dynamic response of the electrical power systems, this technique overcomes the limits of conventional approaches focused on static flow estimation. The results demonstrate that the MUPSC system is measured efficiently, the limiting variables of MUPSC and the failure points in the electricity grid are found. A true metropolitan grid is simulated.

2.2 Power-management strategies for a grid-connected PV-FC hybrid system Loc Nguyen IEEE 2019.

A way of running a hybrid device linked to the grid is presented in this article. A photovoltaic (PV) and Proton membrane fuel cell (PEMFC) hybrid system is considered. The PV array uses the MPPT technology to constantly provide full loading power as irradiation and temperature changes occur, which makes it an uncontrollable source. The hybrid device power output can be regulated in

synchronisation with PEMFC. The hybrid system can be operated in two operating modes, unit control mode (UPC) and feeder flow control (FFC). The synchronisation in the hybrid method of the two control modes, PV array coordination and PEMFC, and reference parameter determination are presented. The proposed operating strategy of modular mode change still works with full power in the PV array and PEMFC in its high efficiency range, thus improving system performance, enhancing system reliability and reducing the amount of operating mode changes.

2.3 Modelling and simulation of grid power management with modified fuzzy logic based MPPT tracking with hybrid power energy system Priyanka Ray; A. K. Sinha IEEE 2019.

As a replacement and as an alternative to massive traditional grid power plants, the rapid usage of the distributed energy resources has expanded. The inclusion of non-linear loads in the power grid will, however, potentially lead to the production of harmonic current and voltage, which in turn will impair the power efficiency of the entire power system. The utilities networks have recently been adapted to mixed energy, which leads to increasing uncertainties and different instabilities. The paper is focused on improved power efficiency with a combined wind and photovoltaic power production system. An enhanced MPPT based on the fumigated logic is applied for a hybrid system that delivers optimal power and contributes both to the load and the energy grid, which ensures a solid and efficient electricity generation system, enhancing both the consistent and complex behaviours. Given the challenges, it is suggested to maintain a grid-based control scheme that is based on the model of a hybrid system with massive system load parallel. Not only can the photovoltaic (PV) electricity be fully used but a synchronous voltage with fluctuating reagent charge can also be maintained. There are two separate P/Q inverter control topologies designed to provide the active and reactive power control loop for the hybrid device and to keep the power output of the grid synchronised accurately. Thus, the inverter can be used as a power converter to pump electricity from the clean energy supply into the grid and to

compensate for the disturbances in power efficiency and the demands of charge reactive power.

2.4 A note on demand side load management by maximum power limited load shedding algorithm for smart grids Cemal Keles; Baris Baykant Alagoz;Asim Kaygusuz IEEE 2019.

The deployment of DSLM enhances grid stability and supports sporadic use of renewable energies. In this research, we talk about the task of load limit algorithm to shedding power on domestic scales for DSLM applications. With this algorithm, domestic power usage is constrained by switching off low previous home electronics appliances, in relation to the volatile price and renewable energy generation stage (HEAs). Based on the power needs of HEA and the user priority pre-setting the planned load removal scheme. In the analysis, the algorithm for power-restricted load release is enhanced to take into account operational modes that include grid mode, island-mode and grid renewable energy mode (RE) and the impact of the proposed system on domestic consumption.

2.5 Design of a controller for grid bus power management with PV systemA. K. Sinha; Priyanka Ray IEEE 2019.

Renewable energy resources are one of the most important alternatives in this current scenario of globalisation, rather than traditional fossil fuels. In the presence of asymmetric load, this paper addresses the energy quality control of the grid bus system. The emergence of asymmetric load configuration in the power grid influences the supply voltage and current directly. Here, the PV feed system not only provides active power to the grid with MPP monitoring, but also offsets the impact of uneven load. Any of the inner unknown PV system parameters must be computed using known PV system parameters during Electric MPP Tracking. The PV system location and angle of the day MPP Tracking remains the same; it is only by setting inner parameters of the PV System for MPP Tracking that current can

only be changed for optimal. In this article, the simulation of an unbalanced bus with the controller is addressed to offset the unbalanced load effect on the PV system supplied utility grid. This paper presents the simulated representative effects of Matlab.

2.6 Echo State Network Based Power Control and Energy Management in Grid—Connected a Hybrid Wind—HydrogenPower Generation System HamzaBOUZERIA; Issam ABADLIA; Mohamed ADJABI IEEE 2019.

In terms of grid efficiency, the stability of the wind/solar hybrid system is a significant factor. A wind-solar hybrid energy system linked to the grid is presented in this article. It comprises four subsystems: generating wind turbines, PV, battery storage and loads. Either room has an AC bus or a DC bus connection. A programmable logic controller implements the energy storage and control system (PLC). Four operating modes are defined, that is ready, stand by, drive, stop. It uses an agent-based cooperative management strategy to reach optimum wind turbine and photovoltaic power point monitoring (MPPT) and operates in the best operating conditions. Experiments demonstrate that either grid-connected or stand-alone mode is available for this device. It has a nice GUI and a high-performance user interface.

2.7 Power control and energy management of a Lebanese smart micro grid Nizar Kfoury; Nazih Moubayed IEEE 2019.

A micro grid algorithm used in the Lebanese case is introduced in this article. The proposed microgrid is comprised of renewable and non-renewable electricity sources and supplies a residential load. PV and wind turbine are alternative energy sources. The PV and the wind turbine systems with maximum tracking power point (MPP) control units have a model and simulation effects with a perturbation controller and a PV algorithm and a fluctuating wind turbine logic controller. The PV/Wind hybrid system model and simulation effects with a storage system are also

treated. A converter and transformer connect this hybrid system to non-renewable sources of energy. These outlets are the Libyan grid and a diesel backup. Checking the inverter in the grid and off-grid situations is discussed in this article. Finally, an algorithm for energy conservation is proposed and tested.

2.6 Active Power Reserve Control for Grid-Forming PV Sources in Microgrids using Model-based Maximum Power Point Estimation **Zhe Chen; Robert H. Lasseter; Thomas M. Jahns IEEE 2019.**

Power reduction of PV (photovoltaic forming grid) sources to supply reserves is a promising way to address major challenges for survival in PV microgrids. It is presented a control scheme that is able to provide both the maximum energy point (MPP) estimate for grid-forming PV sources and the successful power reserve control. Model dependent MPP estimate to prevent the need for irradiance and temperature sensors is proposed. The control algorithm of this power reserve will have adjustable power reserves under various operating conditions. The accurate and quick response of the grid forming PV sources control scheme in island microgrids is illustrated by MATLAB/Simulink-based simulations and hardware in the loop (CHiL) controller emulation performance. In order to validate its efficacy in real-time settings, the experimental verification of the calculation of and control algorithms is also included with the installed outer PV array during networked operations.

2.7 An Online Smart Microgrid Energy Monitoring and Management System **Ahmed AbouArkoub; Mostafa Soliman; Zhen Gao; Sungbin Suh; Vincent D Perera IEEE 2019.**

In recent years the need for electricity has increased, and distributed generation and load management systems are key components of new micro grids (MG). Efficient and permanent grid control was a problem, and an online assessment is required to increase the efficiency of generation and delivery of loads.

This paper proposes a technique based on the Fuzzy LogicControl energy efficiency and management in an AC microgrid linked to the residential grid. A human-based management strategy designed to reduce the power changes in the grid and to increase the lifecycle of batteries. In addition to a battery pack, this device also uses PV cells, inverter cells and Max Power Point Tracing MPPT. The proposed approach controls the microgrid power flow and improves the efficiency of load control. The proposed scheme is tested and validated in an online fuzzy-logic control of various loads and battery charging conditions. Experimental trials are carried out. Results showed that the grid fluctuation profile was improved according to load/power generations.

2.8 Research on Demand Response Strategy of Electricity Market Based on Intelligent Power Consumption Han Jiarui; Xia Dong; Xu Jing; Liu Chen; Xu Ke; Cui Rongjing; Cui Chenlei IEEE 2019.

As the power system reform is gradually developing, the smart electricity is being directly confronted by the power user as an integral part of a powerful smart grid. The advancement of distributed generation, however, has made major improvements to the user's electricity demand properties. The reaction on the demand side is often more difficult. In this article, the solution approach on the energy market was debated according to peak valley use times tariffs and regulated load shipments, taking into account user electricity charges and distributed generation. In the first place, resident load reaction characteristics and dispersed photovoltaic power output characteristics were examined. Secondly, an optimization model for lower energy costs was suggested in view of the response to price demand. Finally, the suggested schemes for full absorption of dispersed generations were the synthesis of distributed power access, real-time dispatch policy and Advance Dispatching Techniques. This scheme has shown the ability to enhance the production of new energy waste and offers a potential foundation for the possible intelligent use of electricity.

CHAPTER – 3

INVESTIGATIONS

3.1 EXISTING SYSTEM

We may not have an automated power management system in the current system. The energy metre can be used to measure people's proximity. This is the method now in use and is discussed below.

- Demonstrate Bluetooth as a way of estimating proximity from face to face and proposes a near-estimation model with adequate smoothing and consideration of a wide range of standard settings. this method makes the following contributions:

- The relationship between the Bluetooth RSSI value and objective measurement-based distance and the theoretical effects of the radio propagation model. Explores the energy efficiency and accuracy of Bluetooth compared with Wi-Fi and GPS via real-life measurements.

- Deploy a "Phone Monitor" programme that gathers data on 196 Android based telephones such as Bluetooth RSSI values. On the basis of the data collection platform, we are willing, in many real-life scenarios, to use the model of proximity calculation to ensure the exact determination of the contact distance from person to person.

Any of such facilities' proposals provide little precision and cost of connectivity. Recently, a 3-D wireless-based solution based both on MI-WI and on triangulation technology has been suggested. It is also possible to use GPS to achieve relative distance between objects.

This device is hardware-friendly. It just requires a Bluetooth smartphone. A Bluetooth RSSI monitoring app has been developed. A Phone Monitor programme gathers Bluetooth data, including RSSI, MAC and Bluetooth de-tailed value (BTID).

When your phone senses other Bluetooth users, the data is stored in the SD card. In order to compare and refine closeness estimate, Bluetooth often collects data points from a number of other subsystems (light sensor, battery speed, etc.).

We monitor the light sensor results, to decide whether the phone is sheltered during the day (for example in a backpack or in a hand) and the environment (for example inside or outside building).

For comparison of energy use, the battery utilisation percentage is reported.

3.2 PROPOSED SYSTEM

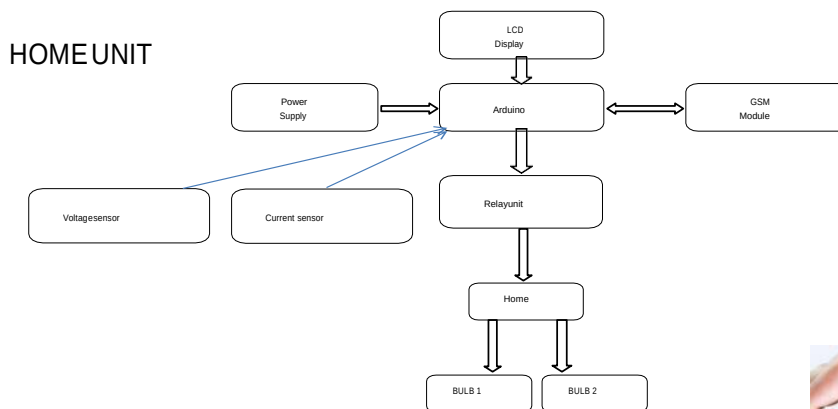
The power is measured by the energy metre until recently. However, no approach is optimal or adequate. This does not deter the plentiful use of power that leads to the final device deployment. These approaches are of no use. This system is therefore used for this region.

In this device, a wireless, protected area network is created to communicate. There are many nodes that can be linked to a vast network of communications. Any node can be mounted at our preferred location or area as a node and the show node in the eoffice. These nodes communicate around 2.4 GHz in the frequency spectrum.

Here, the real power used by the particular house is measured and tested in the EB office by its operation number. With respect to the signal received, the node travelling to or from the reference node is measured. In this scheme we introduce nodes in various places, called reference nodes, when we go to the destination.

The IEEE 802.15.4 RF Transceiver is known as the Gsm reference nodes. The controller monitors the shift in current. A serial peripheral network Bus – SPI connects the RF transceiver to the controller. The node display consists of an RF transceiver and RF signal from reference nodes is sent and received by it.

3.3 BLOCK DIAGRAM:



3.4 WORKING:

In this device, a wireless, protected area network is created to communicate. There are many nodes that can be linked to a vast network of communications. Any node can be mounted at our preferred location or area as a node and the show node in the eboffice.

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CHAPTER – 4

HARDWARE AND SOFTWARE

4.1 HARDWARE

Following are the hardware used to develop this system.

- ARDUINO Microcontroller
- LCD DISPLAY
- GSM 800C
- I2C
- Relay Unit
- Voltage Sensor
- Current Sensor

4.1.1 MICROCONTROLLER

HARDWARE DESCRIPTION

ARDUINO MICROCONTROLLER:

The Arduino Uno is an ATmega328-based microcontroller board (datasheet). It features 14 optical input/output pins (6 are used as PWM output), 6 analogue outputs, a ceramic 16 MHz resonator, USB, an ICSP header and a restart switch. It includes everything you need to help the microcontroller; just attach it to a device with a USB cable or power it to start with an AC-toDC adaptor or battery.

The Uno does not use the FTDI USB-to-serial chip from all previous boards. It is equipped with the Atmega16U2, configured as a USB-to-serial adapter (Atmega8U2 up to version R2).

Revision 2 of the Uno board has a resistor pulling the 8U2 HWB line to ground, making it easier to put into DFU mode.

Revision 3 of the board has the following new features:

pinout: adding SDA and SCL pins near the AREF pin and two additional pins close to the RESET pin, IOREF that make it possible to adjust the shields to the voltage supplied by the board. Shields will in future be compatibly with the 5V-based AVR board as well as the 3.3V-based Arduino Due board. The second is an unconnected screw, which is for potential use.

- Stronger RESET circuit.
- Atmega 16U2 replace the 8U2.

"No" in Italian means one and is designated to mark the next Arduino 1.0 update. The Uno and version 1.0 are Arduino's reference models, progressing. The Uno is the newest in a series of Arduino boards and the Arduino platform concept reference; see Arduino boards' index to be compared to previous models.

Table 4.1.1: TECHNICAL SPECIFICATIONS

Microcontroller	ATmega328P
Operating Voltage	5V
InputVoltage(recommended)	7-12V
Input Voltage (limit)	6-20V
Digital I/O Pins	14 (of which 6 provide PWM output)
PWM Digital I/O Pins	6
Analog Input Pins	6
DC Current per I/O Pin	20 Ma
DC Current for 3.3V Pin	50 Ma
Flash Memory	32KB(ATmega328P)
SRAM	2 KB (ATmega328P)
EEPROM	1 KB (ATmega328P)
Clock Speed	16 MHz
Length	68.6 mm
Width	53.4 mm
Weight	25 g

Design of scheme & reference

ALSO: [arduino-uno-reference-design.zip](#) EAGLE package. (NOTE: Eagle 6.0 and later works) [Arduo-uno-rev3-schematic.pdf](#): schematic:

Note: the reference version of Arduino may be Atmega8, 168 or 328, but the diagram shows an Atmega8, Current versions may be anATmega328. All three processors have the same pin configuration.

Power:

You can use the Arduino Uno via USB or an external power supply. Automatically selects the power source.

External (non-USB) power can be supplied by either a Wall-Wart adapter or battery. A 2.1mm center-positive connection into a power socket of the board allows the connector to be attached. The battery leads can be plugged into the POWER connector's Gnd and Vin pin headers.

An additional supply of 6 to 20 volts can be used by the assembly. The 5V pin can however supply less than five volts if supplied with less than 7V, and the panel may be unstable. The voltage control system will overheat and destroy the board if it uses more than 12V. The range of 7 to 12 volts is recommended.

The pins have the following power:

The Arduino board's input voltage while an external power source is used VIN (as opposed to 5 volts from the USB connection or other regulated power source). You can deliver voltage via this pin or you can reach it with this pin, whether you deliver voltage via the power port.

5V:

This pin releases a controlled 5V from the board controller. Either the DC jack (7-12V), a USB connector (5V), or the VIN pin on the board will supply the board with power (7-12V). A 5V or 3.3V voltage supply bypasses the controller and can destroy the board. We're not recommending it.

3V:

An on-board regulator 3.3 volt supply. The current drawing maximum is 50 mA.

GND:

Ground pins.

32 KB of the ATmega328 (with 0.5 KB used for the bootloader). There are also 2 KB SRAM and 1 KB EEPROM (which can be read and written with the EEPROM library).

Entry and Output

Any of the 14 Uno digital pins can be used as an input or output, using `pinMode()`, `digitalWrite()`. It is 5 volts in operation. Each pin has a maximum capacity of 40 mA and an internal pull-up resistor (unconnected).

(Standard) 20-50 kOhms. Norm. Furthermore, some pins have special functions:

Serial: 0 (RX) and 1 (TX). Used for receiving (RX) TTL serial data and transmitting (TX). The pins are wired to the relevant USB-to-TTL chip pins of ATmega8U2.

External interruptions: 2 and 3. The pins may be adjusted to cause a low value interrupt, an upward or a downward curve or a shift of value. For specifics see the feature `attachInterrupt()`.

PWM are three, five, six, nine, ten and eleven. Submit analogue `Write()` method for 8-bit PWM production.

SPI: 10 (SS), 11(MISO), 13 (SCK). SPI contact through the SPI library supports these pins.

LEDs : 13. An integrated LED with the digital pin 13 is available. If the pin is Up, the LED is on and if the pin is LOW, it is off.

The Uno has 6 analogue inputs numbered from A0 to A5, each with a resolution of 10 bits (i.e. 1024 different values). They scale from ground up to five volts by default, but the top end of their range can be adjusted by means of the AREF pin and by means of `analogReference()`. Furthermore, some pins have specialised functions:

TWI: A4 or SDA pin and A5 or pin SCL. The Wirelibrary supports TWI connectivity.

A few additional pins are on the board:

AREF. AREF. Analog data reference voltage. Reference used with `analog ()`.

Reset. Restart. Bring the microcontroller down to this LOW line. Used to connect shields to reset button blocking the one on the table.

See also the mapping between Arduino pins and ATmega328 ports. The Atmega8, 168 and 328 maps are the same.

Communication:

The Arduino Uno has a variety of monitor, other Arduino or other micro-controller communications facilities. ATmega328 delivers serial UART TTL(5V), usable on 0 (RX) and 1 optical stick (TX). This serial contact is transmitted via USB via an ATmega16U2 on the board and is a Virtual POT for computer applications. The 16U2 firmware uses USB COM basic controllers, without any extra driver. A.inf file is therefore available on Windows. Arduino programme consists of a serial display, which can be sent to and from the Arduino board with basic textual data. As data is

transferred via the USB chip and USB link to the device, the RX and TX LEDs in the board blow in (but not for serial communication on pins 0 and 1).

A serial software library enables serial communication on every digital pin of Uno.

I2C (TWI) and SPI connectivity is supported by the ATmega318. A wire library is available for simplifying the use of the I2C bus in the Arduino software; for information see the documentation. Using the SPI catalogue to communicate with the SPI.

Programming:

With Arduino Tools the Arduino Uno can be programmed (download). Choose "Tools Arduino Uno > Menu of the board (according to the microcontroller on your board).

The ATmega328 on Arduino Uno has a bootloader that lets you upload fresh code without using an external hardware programmer. This bootloader is provided. The initial protocol STK500 communication communicates (reference, C header files).

The bootloader can also be overwritten and the microcontroller can be programmed through the ICSP header; for further details, please see the instructions here.

There is a firmware source code for ATmega 16U2 (or 8U2 on the Rev1 and Rev2 boards). The DFU bootloader is loaded with the ATmega16U2/8U2 and can be turned on by:

On the rev1 boards: the solder jumper connected at the back of the board (close to Italy's map) and the 8U2 restarted.

On reversible or subsequent boards: the HWB line is pulled to the ground by a resistor which makes the DFU mode easy to use.

You can then download a new firmware via Atmel's FLIP (Windows) or a DFU programmer (Mac OS X and Linux). Or you can use an external programmer with ISP headers (overwriting the DFU bootloader). For more detail see this user-contributed guide.

Automatic (Software) Reset:

The Arduino Uno has been programmed to reset applications running on a connecting device, rather than require the physical press of the reset button before an upload is made. A reset line for the ATmega328 is attached through a 100 nanofarad condenser to one of the ATmega8U2/16U2 hardware flow control lines (DTR). The reset line fall long enough to reinstall the chip while this line is proclaimed (taken low). The programme Arduino uses this feature to upload code simply by pressing the Arduino Upload button. The bootloader can then have a shorter downtime since the DTR decrease can be coordinated well at the start of the upload. This configuration has other consequences. If Uno is attached to a Mac OS X or Linux device, it resets every time a programme connects to the computer (via USB). The bootloader is working on Uno for the next half-second or so. It will intercept the first bytes of data sent to the board after a link has opened while the programming ignores malformed data (i.e. something other than a new code upload). If a board sketch gets one-time initialization or other data as it begins first, make sure that the programme it communicates is waiting for a second after opening and before submitting the link.

A track can be cut to deactivate the self-setting of the Uno. The trace pads can be re-soldered on either side of the track. "RESET-EN" is numbered. The auto-reset can also be disabled by adding a 5V 110 ohm resistor to the reset line, and see the thread for this forum for information.

USB Overcurrent Protection:

The Arduino Uno has a resettable Polyfuse which provides shorts and overcurrent protection to your computer's USB ports. Although most machines provide their own internal security, the fuse adds an additional protection layer. The fuse immediately disrupts the link before a short connection or excess is eliminated, if more than 500 mA are added.

Physical Characteristics:

The full length and width for the Uno PCB is 2.7 and 2.1 inches, and the USB connector and power jack stretch beyond the previous size. The board may be fixed to a surface or case with four screw holes. Notice that there is a gap of 160 mil (0,16") between optical pins 7 and 8, not quite a multiple to the other 100 miles.

4.1.2 DEVICE FEATURES:

DEVICE FEATURES FOR THE PIC18F4XJ11 (44-PIN DEVICES)

Features	PIC18F44J11	PIC18F45J11	PIC18F46J11
Operating Frequency	DC – 48 MHz	DC – 48 MHz	DC – 48 MHz
Program Memory (Bytes)	16K	32K	64K
Program Memory (Instructions)	8,192	16,384	32,768
Data Memory (Bytes)	3.8K	3.8K	3.8K
Interrupt Sources	30		
I/O Ports	Ports A, B, C, D, E		
Timers	5		
Enhanced Capture/Compare/PWM Modules	2		
Serial Communications	MSSP (2), Enhanced USART (2)		
Parallel Communications (PMP/PSP)	Yes		
10-Bit Analog-to-Digital Module	13 Input Channels		
Resets (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow, MCLR, WDT (PWRT, OST)		
Instruction Set	75 Instructions, 83 with Extended Instruction Set Enabled		
Packages	44-Pin QFN and TQFP		

4.1.3 I/O PORTS:

Up to five ports are open, depending on the computer chosen and the features enabled. Any I/O pins are multiplied by alternating functions from the computer peripherals. Generally, this pin cannot be used as a general I/O pin when a peripheral is allowed.

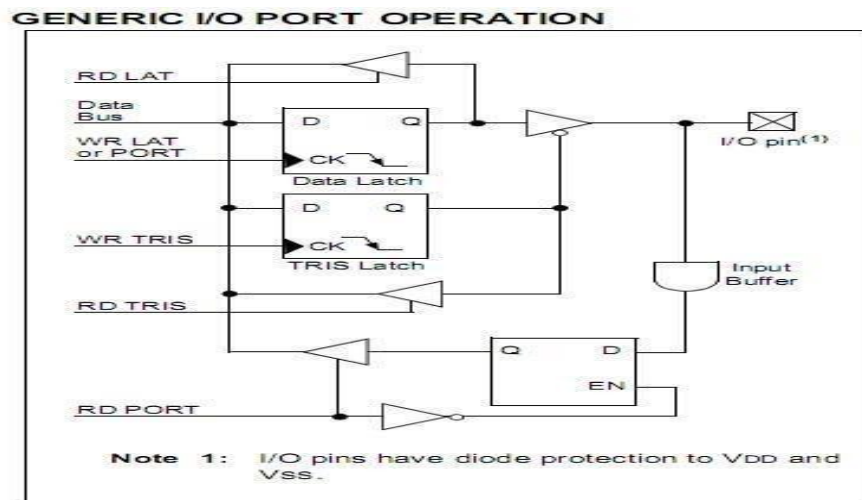


Figure: 4.1.3 I/O PORT OPERATION

Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT registers (Data Latch)

I/O Port Pin Capabilities:

The capacity of the port pins must be considered when designing an application. Outputs on some pins are more powerful than others. Any pins can also handle input values greater than VDD.

PIN OUTPUT DRIVE:

For groups of pins designed to satisfy requirements for a range of applications, the power output pin drives differ. PORTB and PORTC can drive

higher loads, for example LEDs. The other ports are usually only for small loads. The output capabilities are marked by Table9-1 sum-.

OUTPUT DRIVE LEVELS

Port	Drive	Description
PORTA	Minimum	Intended for indication.
PORTD		
PORTE		
PORTB	High	Suitable for direct LED drive levels.
PORTC		

OUTPUT DRIVE VALUES

INPUT PINS AND VOLTAGE CONSIDERATIONS:

The voltage resistance of the pins used as input device depends on the input feature of the pin. DC voltages up to 5.5V can also be handled for pins used as digital inputs; a standard level for digital logic circuits. Pins that also have some kind of analogue input will only handle VDD voltages.

PORTA, TRISA and LATA Registers:

PORTA is a two-way 7-bit port. Depending on the mode chosen, it acts as a 5-bit port. The PORTA pin would be an input if the TISA bit (= 1) is set (i.e., put the corresponding output driver in a high-impedance mode). When you clear a TRISA bit (= 0), the resulting PORTA pin will make a result (i.e., put the contents of the output latch on the selected pin).

The PORTA register reads the pins state, but the port latch is entered. Memory mapping is available even in the data lock (LATA) register. LATA register reads and writes the locked output value for PORTA for the read-modify-write

operation. Analog inputs, analogue VREF+ and VREF- inputs and the reference voltage are multiplexed by the other PORTA pins. The pin feature, RA< 3:0> and RA5, is selected as A/D converter inputs by clearing or setting the control bits in the ADCON1 Register. In the CMCON Register, pins, RA0 and RA3 can be used as input for the comparator as well. The comparators must also be turned off if RA<3:0> were to be used as a digital input.

The TTL levels and complete CMOS controls are given for any PORTA pin. And when it is used as analogue inputs, the TRISA register governs the orientation of the Port pins. When using them as analogue inputs, the user must ensure that the bits in the TRISA register are kept.

INPUT VOLTAGE LEVELS

Port or Pin	Tolerated Input	Description
PORTA<7:0>	VDD	Only VDD input levels tolerated.
PORTB<3:0>		
PORTC<2:0>		
PORTE<2:0>		
PORTB<7:4>	5.5V	Tolerates input levels above VDD, useful for most standard logic.
PORTC<7:3>		
PORTD<7:0>		

INPUT VOLTAGE VALUES

PORTB, TRISB and LATB Registers:

PORTB is a two-way, 8-bit port. The TRISB data management register is the corresponding one. The PORTB pin is an input by setting a TRISB (= 1) bit (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISB bit (= 0) makes a PORTB output for the respective pin (i.e., put the contents of the output latch on the selected pin). Memory is also mapped in the Data Llock Registry

(LATB). Read and write the latched output value for PORTB on the LATB Register. There is a poor inner pull-up of each PORTB screw.

All the pull-ups can be enabled by a single control bit. This is done with RBPU (INTCON2<7>) clearing bit. When the port pin is programmed as an output, the poor pull-up is automatically shut down. The sweeps are POR-deactivated. The interrupt-on-change function is present in four PORTB pins (RB<7:4>). This interrupt can only be caused by pins programmed as inputs.

The RB<7:4> input pins are identical to the latched old value on the last PORTB reading. RB<7:4> "miscellaneous" outputs are set to RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>). A flag piece, RBIF, still has a malfunction. PORTB can stop the flag, RBIF, after a delay instruction period and allow it to be cleared.

For the weakness of main depression and operations where PORTB can only be applied in the interrupt-on-change function, the interrupt-on-change functionality is recommended. PORTB polling during use of the interrupt-on-change function is not advised. The RB5 pin is multiplied to one of the RB5, KBI1/SDI1/SDA1/RP8 pin and with the feedback of the Timer0 modules clock.

PORTC, TRISC and LATC Registers:

PORTC is a two-way, 8-bit port. The TRISC data management register is the corresponding one. The PORTC Pin will be entered by setting a TRISC bit (= 1). (i.e., put the corresponding output driver in a high-impedance mode). When the TRISC bit is removed (= 0), the PORTC pin is an output (i.e., put the contents of the output latch on the selected pin). Memory is also mapped in the Data Look Registry (LATC). Please read and write latched PORTC output value for LATC record read-modify operations. PORTC has many peripheral features multiplexing. The pins have input buffers from Schmitt Trigger.

For each PORTC pin, you should ensure that the TRIS bits are defined for each peripheral feature. Some peripherals bypass the TRIS bit for a wire output and others override the TRIS bit to provide a pin for an entry. For additional details, the

user should refer to the relevant peripheral portion. In contrast to other PORTC pins, TRISC bits are not aligned with RC4 and RC5. They can only function as digital inputs as digital ports. When using an external transceiver RC4 and RC5 still function as transceiver inputs. The path of the data is defined by the operation performed by the module when the on-chip transceiver is used. Peripheral overrides influence the contents of the TRISC register. The TRISC reading returns the contents, though one or more pins can be overridden by a peripheral unit.

PORTD, TRISD and LATD Registers:

The PORTD is a two-way 8-bit port. The relevant TRISD data management register. The PORTD pin is an input by setting a TRISD bit (= 1). (i.e., put the corresponding output driver in a high-impedance mode). Clearing a TRISD bit (= 0) makes the PORTD pin the result (i.e., put the contents of the output latch on the selected pin).

Memory is also mapped to the Data Latch Register (LATD). Listen and write latched value for PORTD for read-modify-write operations on the LATD register. With Schmitt Trigger input buffers, all pins on PORTD are implemented. Each pin may be configured independently as an input or output. Each PORTD is weakly pulled internally. All the pull-ups can be enabled by a single control bit. This consists of the RDPU (PORTE<7>) setting-bit.

When the port pin is programmed as an output, the poor pull-up is automatically shut down. The sweeps are POR-deactivated. Please note that for all features like the pull-ups seen in PORTB pull-ups are possible.

PORTE, TRISE and LATE Registers:

PORTE is applied in two different ways depending on the actual PIC18F46J11 family interface chosen. PORTE is a 3-bit deep port for 44-pin computers. Three pins are individually adjustable as inputs or outputs (RE0/AN5/PMRD, RE1/AN6/PMWR and RE2/AN7/PMCS). The pins have input

buffers for Schmitt Trigger. These pins can read as '0's when chosen as analogue inputs.

The TRISE data management registry is the equivalent one. The subsequent PORTE pin is an input when you set a trise bit (= 1) (i.e., put the corresponding output driver in a high-impedance mode). The clearance of a TRISE bit (= 0) makes a PORTE production (i.e., put the contents of the output latch on the selected pin).

Though used as analogue inputs, TRISE governs the orientation of the RE pins. When using them as analogue inputs, the consumer must ensure the pins are programmed as inputs.

Memory also is mapped in the Data Latch Register (LATE). Read and write the latched output value for PORTE on the LATE register read and write. The PORTE pins each have a poor internal tension. All the pull-ups can be enabled by a single control bit. This is done by setup bit, PORTE<6>. This is done by setting bit. When the port pin is set as an output, the poor pull-up is automatically switched off. The sweeps are POR-deactivated. Please note that for all features like the pull-ups seen in PORTB pull-ups are possible.

Circumstances in the world of microcontrollers today have begun in the growth of integrated circuit technology. This has allowed hundreds of thousands of transistors to be stored in one chip. The first computers were generated by the addition of external peripherals such as memory or input-output lines, timers and others. Further rise in package volume and the design of integrated circuits. Both processor and peripherals is combined with those circuits. This is how a microcontroller was created as the first chip, or as a microcontroller.

4.1.4 Memory unit:

Memory is a component of the data-saving microcontroller. For any feedback we obtain the contents and it is all in a certain addressed memory position. We have two new concepts: addressing and place of memories. Memory is all places in memory, and the addressing is only one.

This means that, on the one hand, we have to pick the required memory location and, on the other, we have to wait for its contents. A memory must also be

used in addition to reading from a memory site. This is achieved by the provision of another line known as the control line. This line would be referred to as R/W (read/write). Control line is used as follows: if $r/w=1$ is read and if the other way around, the memory location is written.

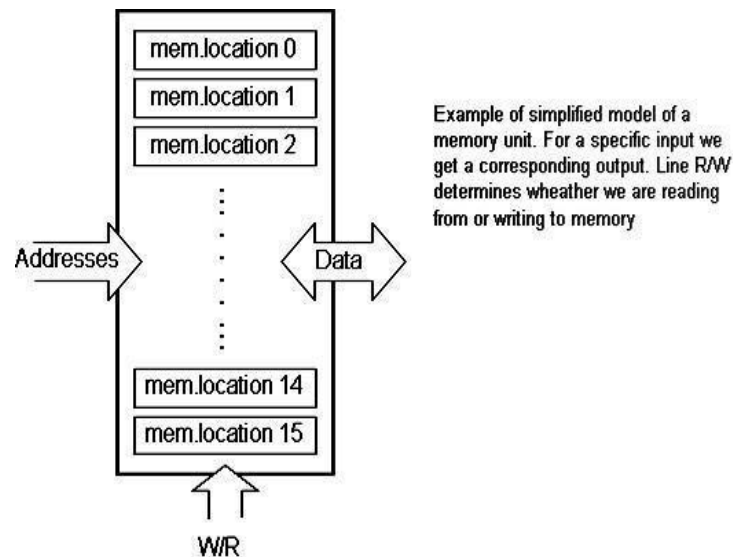


Figure 4.1.4: Block diagram of memory unit

4.1.5 Central Processing Unit:

Allow 3 additional memory sites to be added to a particular block that would be able to multiply, split, remove and transfer the contents from one place to another. The component which we have just integrated is the central processing unit (CPU). Registers are named their memory sites.

Therefore, registers are memory locations whose role is to assist with different math or other data operations anywhere data can be located. Look at what is happening now. We are bound to two separate entities (memory and CPU) so any data sharing and its features can be prevented.

Bus: That "way" is called "bus". It's physically an 8, 16, or more drum squad. Two kinds of buses are available: address and data bus. The first is as many lines as our memory and the second is as broad as data, in our case 8 bits or the link line. The first one is intended for CPU memory transmission and the second one for connecting all the microcontroller blocks.

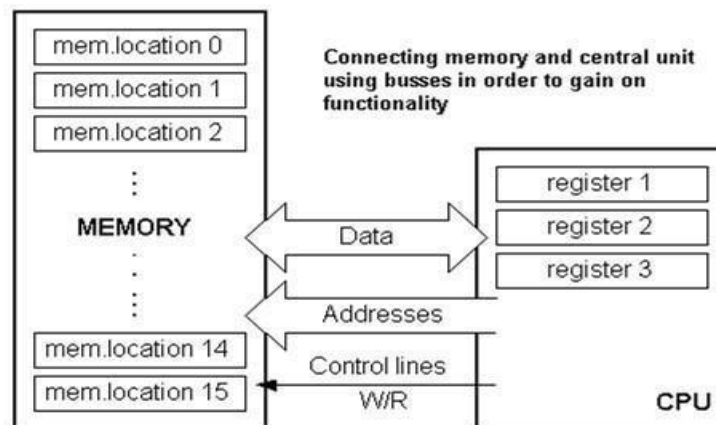


Figure 4.1.5: Representation of Bus

4.1.6 Input-output unit

We just applied "Ports" to some places. Input, exit or two-way ports are some kinds of ports. When dealing with ports, you first need to choose which port to use and then transfer the data to or from the port. The port serves as a memory spot while dealing with it. Anything is just entered or read from it and can be seen on the microcontroller pins.

4.1.7 Serial communication:

Although different lines are available for receipt and transmission, data can be received and send simultaneously (info). The serial communication block is called the full-duplex mode block which allows this type of communication. Unlike parallel transmission, data here travels bit by bit, or the term serial correspondence comes from a number of bits. Following receipt of the data from the receiving position we must read it and save it in the memory rather than send it to reverse the operation. We must set the data sharing rules to ensure that this works. The rules are known as the protocol. The data passes from the memory through the bus to the transmitting site, followed by the protocol to the receiver side.

4.1.8 Timer unit:

The timer block that can send us time, time, protocol, etc. stuff. This is a free-run clock that is actually a register whose numerical value increases by one interval such that we can calculate how long time has passed, taking its value in the T1 and T2 cycles and based upon its variance. The microcontroller requires a very

significant amount of time to realise this. Observer dog: Another thing is that we need to be aware of is the microcontroller's perfect operation over time.

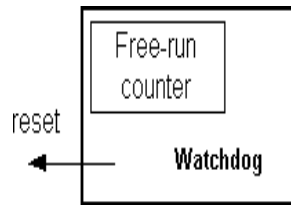


Figure 4.1.8: Watch dog timer

If our microcontroller ceases running the software or worse as a result of any interruption (often occurring in industry), it begins to function incorrectly. Naturally, we will resettlement it and it will run again when this happens in a device. We will push the microcontroller on and thus fix our dilemma. There is no reset button. We need to add another block, called the watchdog, to solve this challenge.

In truth, this block is another free-run counter where our programme must write a zero each time it runs properly. If the software is "stuck," zero does not occur and the clock alone resets the microcontroller until the maximum value is achieved. This would lead to the machine running again and this time around correctly.

4.1.9 Analog to Digital Converter:

Because microcontroller-conscious signals (zéro and one) normally vary considerably, they must be transformed into a pattern that a microcontroller understands.

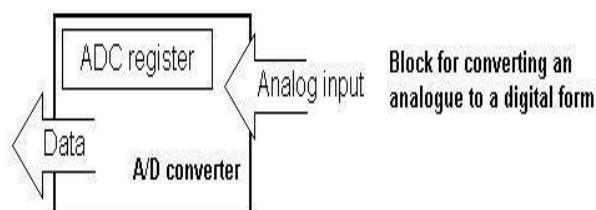


Figure 4.1.9: Analog to Digital converter

A block for analogue to digital conversion or an ADC is performed for this role. This block is responsible for converting an analogue to a binary number information and tracking it to CPU block for processing by the CPU block.

4.1.10 CISC and RISC:

Harvard is not a Von-Neumann design but a newer concept. It was because a microcontroller had to step up his work. Data bus and address bus are different for Harvard architecture. A bigger data flow through the central processing unit and, of course, a higher working speed is possible. The separation of a programme from the storage memory allows instructions not to be 8-bit words. It also is characterised by less instructions for Harvard architecture than von-Neumann, typically in one loop. Harvard architecture microcontrollers are sometimes branded "RISC."

RISC stands for computer set of reduced instructions. Von Neumann's architecture microcontrollers are referred to as 'CISC microcontrollers'

4.1.11 Memory organization:

Each of these PIC micro MCUs has three memory blocks. The memory of the programme and the data memory have individual buses to allow concurrent access.

4.1.12 Program memory organization:

A 13-bit programme counter for 8K x 14 programming space is provided for the PIC16F87X. The devices PIC16F877/876 have a FLASH memory of 8K x 14 words, and the devices PIC 16F873/874 have fourK x fourteen. A wrecking can be caused by accessing a place above the physically applied address. The vector of reset is 0000h and the vector of interrupt is 004h.

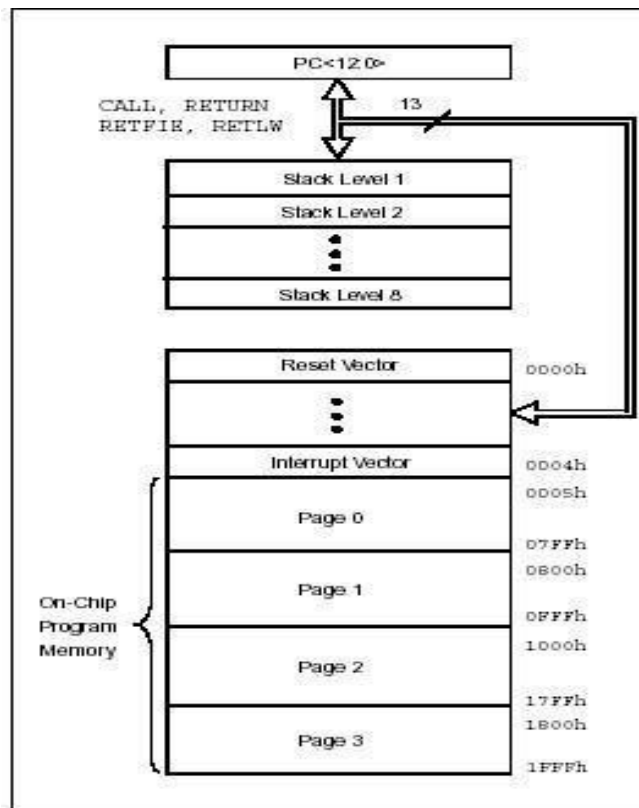


Figure 4.1.12: Program memory and Stack memory

4.1.13 Data memory organization:

The data memory is divided into several banks containing the Registers of General Purposes and the Specific Functions. The bank pick bits are the bits RP1 (STATUS<6>) and RP0 (STATUS<5>).

RP1:RP0	Bank
00	0
01	1
10	2
11	3

Figure4.1.13: Table Register bank selection

Any bank can reach 7Fh (128 bytes). For the special feature records, the lower sites of each bank are reserved. The general-purpose registers, implemented as static RAM, are above the special function registers.

General purpose register file: The file can be seen through the File Select Register FSR, directly or indirectly.

Special function registers:

The special function registers are registers that are used to monitor the intended output of the computer by the CPU and peripheral modules. These records are used as static RAMs. There are two types of special function registers: the main (CPU) and the peripheral.

Status register:

ALU arithmetic state, the RESET status and the dataspeed bits are included in the STATUS register. As for every other registry, the STATUS register may be the object of any instruction. The written name for these three bits is deactivated if STATUS Register is intended for a directive affecting bits Z, DC or C. These bits have been set or cleared by device logic. The TO and PD bits cannot be entered, so the outcome of a statement with the STATUS record may be different from the expected destination.

4.1.14 I²C Protocol:

Invented by Philips to fix low-speed peripherals to a chipset, an embedded processor or mobile phone, the I²C is a multi-masters serial computer bus. The designation is I-squared-C, and sometimes, wrongly, I-two-C, and is known as Inter Integrated Circuit. I²C only uses the Serial Data (SDA) and Serial Clock (SCL) open-drain bidirectional lines pulled up with the resistivity. The I²C architecture has a 7-bit address with 16 addresses reserved to communicate on a single bus, allowing a maximum of 112 node. Obviously, the overall number of nodes is constrained by the number of addresses and the total capacity of the bus of 400 pF. Philips has designed a simple 2 wire bi-directional bus for effective inter-IC control in order to improve hardware reliability and circuit simplicity. The bus is known as Inter IC or I²C. The on-chip interface allows all I²C-bus compliant systems to connect directly

with each other via the I2C bus. The multifaceted problems in the development of digital control circuits are solved by this design principle.

- Here are some of the features of the I²C -bus:
- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as mastertransmitters or as master-receivers.
- It's a true multi-master bus including collision detection and arbitration to prevent data corruption if two or more masters simultaneously initiate data transfer
- Serial, 8-bit oriented, bi-directional data transfers can be made at up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode, or up to 3.4 Mbit/s in the Highspeed mode
- On-chip filtering rejects spikes on the bus data line to preserve data integrity
- The number of ICs that can be connected to the same bus is limited only by a maximum bus capacitance of 400 pF.
- For 8-bit oriented digital control applications, such as those requiring microcontrollers, certain design criteria can be established.
- A complete system usually consists of at least one microcontroller and other peripheral devices such as memories and I/O expanders.
- The cost of connecting the various devices within the system must be minimized.
- A system that performs a control function doesn't require high-speed data transfer.
- Overall efficiency depends on the devices chosen and the nature of the interconnecting bus structure.

A serial bus configuration is needed to generate a system to meet these requirements. While serial buses have no parallel bus transmission capabilities, less cables and less IC connecting pins are necessary. However, a bus is not only a link wire; it encompasses all the communication formats and procedures in the system.

Devices operating on a serial bus should provide a protocol that prevents misunderstanding, lack of data and information blocking. Fast equipment must be able to coordinate with slow equipment. The machine does not depend on the

machines attached to it, or it would be difficult to change or upgrade. A procedure must also be conceived to determine which computer can operate the bus and when. And if various devices are connected to the bus with differing clock velocities, the bus clock source must be set. The specification of the I²C -bus involves all these requirements.

The I²C bus consists physically of two active cables and a ground link. Both active wires, such as SDA and SCL, are two-way. The serial line is SDA, and the serial line is SCL.

Each computer hooked to the bus has its own unique address or MCU, LCD, memory, or ASIC. Each unit has its own specific address. Depending on features, any of these chips will serve as a recipient and/or transmitter. Of course, an LCD driver is only a recipient and both a transmitter and the receiver may be a memory or I/O chip.

The Bus I²C is a Multinational Bus. This ensures that it can be linked to more than one IC that can initiate data transfer. The I²C protocol specifier specifies that a Bus Master is known to be the IC that initiates data transmission on the bus. Accordingly, all the other ICs are considered Bus Slaves at the moment.

- I²C -bus ICs enable a device design to move quickly from a practical block diagram to a prototype. Moreover, as the test device can be modified or updated directly to the I²C bus without any other external interface by clicking 'clicking' or not clicking the ICs to or from the bus. Here are some of the features of I²C -bus compatible ICs which are particularly attractive to designers:
- Functional blocks on the block diagram correspond with the actual ICs; designs proceed rapidly from block diagram to final schematic.
- No need to design bus interfaces because the I²C -bus interface is already integrated on-chip.
- Integrated addressing and data-transfer protocol allow systems to be completely software-defined
- The same IC types can often be used in many different applications
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I²C -bus compatible ICs

- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced
- Software development time can be reduced by assembling a library of reusable software modules.

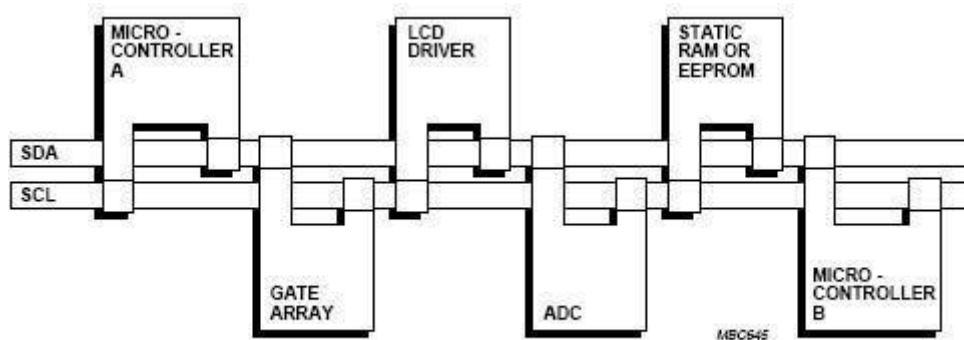
The I2C -bus supports all processes of IC production (NMOS, CMOS, bipolar). Included in the bus connecting systems are the two cables, SDA and Serial Clock (SCL). Each computer can act as either a transmitter and a receiver, and is known by a specific address (whether it is a microcontroller, LCD power, memory or a keyboard interface). An LCD driver is obviously just a receiver, although all data can be sent and received by a memory. Modules may also be called master or slave when doing data transfers as well as transmitters and receivers (see Table 1). Master is the mechanism that starts the transfer of data on the bus to produce clock signals to allow this transmission. Any unit is known to be a slave at that time.

Definition of I²C-bus terminology

TERM	DESCRIPTION
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by a master
Multi-master	More than one master can attempt to control the bus at the same time without corrupting the message
Arbitration	Procedure to ensure that, if more than one master simultaneously tries to control the bus, only one is allowed to do so and the winning message is not corrupted
Synchronization	Procedure to synchronize the clock signals of two or more devices

4.1.14 I²C-BUS TERMINOLOGY

The Multi-Master Bus is an I²C bus. This means that it can be wired to more than one system that can power the bus. If more than one microcontroller can be connected to the I²C -bus, more than one master can simultaneously attempt to initiate a data transfer. A protocol of arbitration has been designed to prevent the confusion that could result from such a case. This procedure depends on all I²C interfaces to be wired-AND connected to the I²C-bus. If two or more masters want to place details on the bus, one that creates a one will fail arbitration while the other generates a zero. The clock signals in arbitration are a sync combined with a wired-AND link to the SCL-line generated by the masters. It is always the responsibility of the master devices to produce clock signals on the I²C bus; when transmitting data on the bus, every machine generates its own clock signals. Except when extended by a slow-slave system holding down the clock line, or where arbitration happens by another master will a Bus clock signals of a master be changed.



Example of an I²C-bus configuration using two microcontrollers.

Figure4.1.15 : I²C BUS CONFIGURATION

SDA and SCL are two-directional lines connected by a current source or pull-up resistor to a positive supply voltage (see Fig.3). Both lines are HIGH when the bus is open. In order to execute the wired AD function, the output steps of devices attached to the bus must provide an open or open drain. I2C bus data can be transmitted in standard mode, in fast mode up to a speed of 100 kbit/s, up to 400 kbit/2s or in high speed mode up to three.4 mbit/s. Just depends on the bus capacity limit of 400 pF on the number of interfaces attached to the bus.

The I2C MSSP module completely implements all the main and slave functions (including general call support) and offers hardware interruptions to define a free bus on Start and Stop bits (multi-master function). The basic mode parameters and 7-bit and 10-bit addresses are implemented in the MSSP module.

Two pins are used for data transfer:

- Serial clock (SCL) – RC3/SCK/SCL
- Serial data (SDA) – RC4/SDI/SDA

The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

REGISTERS

The MSSP module has six registers for I²C operation.

These are:

- MSSP Control Register (SSPCON)

- MSSP Control Register 2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer Register (SSPBUF)
- MSSP Shift Register (SSPSR) – Not directly accessible
- MSSP Address

<u>Register</u> (SSPADD)	<u>Code</u> (Hex)	<u>Command to LCD Instruction Register</u>

SSPCON,

SSPCON2 and SSPSTAT are the control and status registers in I²C mode operation. Readable and writable are the SSPCON and SSPCON2 registers. The SSPSTAT is available in less than six bits. The top two bits are read/write in the SSPSTAT. SSPSR is the shift register for input or output transfer of data. SSPBUF is the buffer log that contains data bytes to or from which they are written. When the SSP has been setup in I2C Slave Mode, the SSPADD register stores the slave system address. The lower seven-bit SSPADD acts as the baudrate generator reload value while the SSP is initialised in the master mode.

4.2 LCD

Liquid crystal display (LCD) is a flat panel display that incorporates the light modulating properties of liquid crystals, an optical visual display or a video display. Light does not emit directly from Liquid Crystals.

LCDs can show random or fixed images, such as preset words, digits, and displays for seven segments such as the digital clock, as in a general computer display. They use the same simple hardware unless a wide range of tiny pixels are presented in random images when other displays have bigger components.

1	Clear display screen
2	Return home
4	Decrement cursor (shift cursor to left)

Arbitrary LCDs (as in the general computer display) or secret or visible fixed pictures like preset words, numbers and 7-segment displays like in a digital clock can be seen on or off the LCD. LCDs are available. They use the same general hardware, except that a	6	Increment cursor (shift cursor to right)
	5	Shift display right
	7	Shift display left
	8	Display off, cursor off
	A	Display off, cursor on
	C	Display on, cursor off
	E	Display on, cursor blinking
	F	Display off, cursor blinking
	10	Shift cursor position to left
	14	Shift cursor position to right
	18	Shift the entire display to the left
	1C	Shift the entire display to the right
	80	Force cursor to beginning of 1 st line
	C0	Force cursor to beginning of 2 nd line
	38	2 lines and 5x7 matrix

large number of small pixels consist of random images and some have large components.

Each pixel of an LCD usually consists of a sheet of molar alignment, which is perpendicular (in most cases) to one another, between two transparent electrodes and two polarising filters (parallel and perpendicular). The light that passes through the first filter will not be obstructed by the second without liquid crystal between the filters (crossed).

Prior to the use of the electric field, an arrangement of the electrode surfaces determines the position of the liquid crystal molecules. The surface orientation directions of both electrodes are perpendicular to each other in a twisted nematic

device, (which now is the most typical liquid-crystal device). The molecules then organise in a helical configuration or a torsion.

This causes the polarisation of the incident light to rotate, and the device becomes grey. The fluid crystal molecules in the middle of the layer are almost totally untwisted as the voltage is high enough and the polarisation of the occurrence light is not rotated when the fluid crystal layer crosses.

This light would then be polarised perpendicular to the second filter and blocked so that the pixel looks dark. By regulating the voltage applied across the fluid crystal layer in each pixel, various levels of grey may be passed by light in different quantities.

The ionic compounds contain both the liquid crystal material and the coordination layer. If a certain polarity electric field is used for a long time, so this ionic substance attracts to the surfaces and degrades the output of the instrument. Either an alternative current is applied or the polarity of the electric field is reversed when the mechanism has to be adjusted (the response of the liquid crystal layer is identical, regardless of the polarity of the applied field).

4.2.1 STEPS TO INTERFACE LCD WITH PIC MICROCONTROLLER:

STEP 1: Identify:

Identify your preferences LCD is available in all of the following flavours 16x1 16x2 , 20x2 in the AxB format in which A is the character number and B is the Rows number. 16x1 (lines) An LCD may be light back as well.

STEP 2: Connect:

Most of the LCD's follow the standard Hitachi Pin out which is simply...

TABLE – 4.2.1 PIN DESCRIPTION

Pin No	Name	Function	USE

1	Vss	Ground	
2	Vdd	+ve Supply	5v Volts Regulated DC
3	Vee	Contrast	This is used to set the contrast1
4	RS	Register Set	Register select signal "0":Instruction register (when writing) Busy flag & address counter (When reading) "1":Data register (when writing & reading)
5	R/W	Read / Write	Read/write select signal "0" for writing , "1" for reading
6	E	Enable	Operation (data read/write) enable signal
7	D0	Data Bit 0	
8	D1	Data Bit 1	
9	D2	Data Bit 2	
10	D3	Data Bit 3	
11	D4	Data Bit 4	
12	D5	Data Bit 5	
13	D6	Data Bit 6	
14	D7	Data Bit 7	
15	A	+4.2 for Back light	Positive supply for back light if available
16	K	Power supply Back light (0V)	

STEP 3: Interface:

RS, RW,E,D0 - D7 pins attach now to the micro controller pins Suppose, on port A or on port B, I link the databus, RS, RW, E. (You are able to save pins with the use of Nibble Mode LCD (4 data pins) (always in write mode). A smart LCD needs only a few commands and data for the LCD command set.

4.2.2 I2C:

I2C is a multimedia serial single-ended computer bus invented by Philips used to connect lowspeed peripherals to a cpu, embedded machine, mobile phone or another electronic unit..

The I2C uses only two bidirectional open-drain lines with resistors pulled up, Serial Data Line (SDA) and Serial Clock (SCL). Although systems with other voltages may be permitted, the typical voltage used is +5 V or +3.3 V.

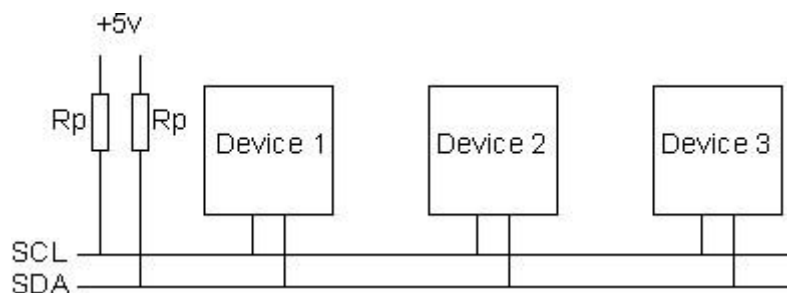


FIG 4.2.2 – I2C MASTER SLAVE CONNECTION WITH PULL UP RESISTORS

A 7-bit or 10-bit address space is available for I2C (depending on the computer used). [5] [5] [5] Common I2C Bus Speeds are 100 kbit/s and 10 kbit/s, but are arbitrarily allowed with low clock frequencies. I2C revisions will host additional nodes and run more quickly (400 kbit/s Fast mode, 1 Mbit/s Fast mode plus or Fm+ and High-Speed Mode 3.4Mbit/s). These speeds are used on embedded systems more commonly than on PCs. Additional features such as 16-bit addressing are also available.

The previous version is a bus with a 7-bit addressing of the clock (SCL) and data (SDA) row. The node bus has two roles: master and slave:

- Master Node — a clock node that starts slave correspondence.
- Slave node — node receiving the clock and answered if the master is specified.

The bus is a multi-master bus that allows you to have any number of master nodes. Master and slave functions in messages may also be modified (after a STOP is sent). There are four potential modes of operation for a given bus device, although most devices only use a single role and its two modes:

1. master transmit — master node is sending data to a slave
2. master receive — master node is receiving data from a slave
3. slave transmit — slave node is sending data to the master
4. slave receive — slave node is receiving data from the master

Initially, the master is in master transmission mode and is given a start bit followed by the slave's 7-bit message, which is followed by a single bit that shows whether it wants to write (0) to or read(1) from the slave. If the slave is present on the bus, it will react to the address with an ACK bit (active low for recognised).

The master then proceeds to send or receive the mode and the slave continues in his complementary mode, based on the reading/write bit sent (receive or transmit, respectively). The most important bit is sent to the address and data bytes. A high to low SDA transition with SCL high is the start bit; a low to high SDA transition with high SCL is the stop bit. The SCL low is used for all other SDA transformations.

If the master wants to write to the slave he gives the slave an ACK bit repeatedly byte. (In this case, the slave receives the master in master transmitter mode and the slave mode). The slave will receive repeated bytes from the slave if the master wants to read them, the master will give an ACK bit after the last byte. (The owner receives in master mode in this case, and the slave in slave transmission mode.) The master then either stops the transmission, or sends another START bit if he wants to maintain hold of the bus for a further switch (a "combined message"). I2C distinguishes fundamental categories of messages that each start with a START and end with a STOP:

- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.

- Combined messages, where a master issues at least two reads and/or writes to one or more slaves.

Each reading or writing starts with the START and the slave address in a combined letter. These often name repeated START bits after the first START in a merged post. Repeated START bits are not followed by STOP bits, because the slave knows that the next transmission is included in the same message.

Any slave can only answer to specific posts as specified by the documentation of its product.

Arbitrary message arrangements are supported by pure I2C frameworks. Nine of these systems, for example read N and write N, have SMBus limited by one slave.

PMBus expands the group's protocol to SMBus, enabling a combined message to be transmitted to several transactions such as SMBus. The STOP terminator shows when these clustered measures should be taken.

For instance, a PMBus operation might reconfigure three power supplies, and at the same time their new configurations will take effect: when they are receiving the STOP. No I2C nor SMBus defines message semantics, for example, the definition of the data bytes in communications with only a few exceptions.

Others are product-specific Message Semantics. Exceptions to those exemptions include messages to the I2C (0x00) general call address or SMBus alert response address; as well as messages to complex allocation and control in the SMBus Address Resolution Protocol (ARP).

4.2.3 SERIAL PERIPHERAL INTERFACE:

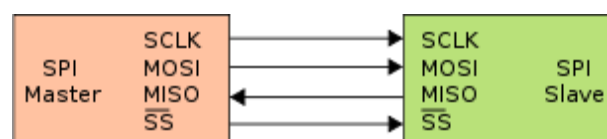


FIG 4.2.3– SINGLE MASTER SLAVE SPI

The Serial Peripheral Interface Bus or SPI bus is a synchronous, duplex serial data connection. Master/slave devices connect where the data-frame is initiated by the master computer. Multiple slave devices with single chip pick lines are permitted. SPI is often considered a four-wire serial bus, and is compared to 3-, 2- and 1-wire serial buses. SPI is usually called SSI (Synchronous Serial Interface).

The SPI bus specifies four logic signals:

- SCLK: serial clock (output from master);
- MOSI: master output, slave input (output from master);
- MISO: master input, slave output (output from slave);
- SS: slave select (active low, output from master).

With one master unit and one or more slave units, the SPI bus can be controlled. The SS pin can be set to the logic low if a single slave unit is used, if the slave allows.

Some slaves need a downward chip selecting signal to trigger an operation, for example the Maxim MAX1242 ADC, which initiates a high-low transfer conversion. A standalone SS signal is required for each slave device with several slave devices from the master.

Most systems with three-state outputs have a MISO signal (logically disconnected) that is highly impedant when the interface is not set. SPI bus segments cannot be shared by machines without tri-state outputs. One of the slaves can speak to the Master only and only the Chip selections can be turned on.

The bus master configures the clock first to start a conversation, using a frequency less than or equal to the slave device's maximum frequency. These frequencies are typically inside the 10-100-MHz range Then the master transmits

the chip's logic 0 over the pick chip side. A chip selector line is passed to a logic 0, which means the chip is a logic 1; a logical 0 is proclaimed.

If a waiting period is required (such as for analog-to-digital conversion), then the master must wait for at least that period of time before starting to issue clock cycles.

During each SPI clock cycle, a full duplex data transmission occurs:

The master sends a bit on the MOSI line;

The slave reads it from that same line;

The slave sends a bit on the MISO line;

The master reads it from that same line.

Not all transmission requires meaningful use of all four of these operations, however it is. Transmissions usually have two shifts, one of the master's and a single of the slave; they are bound in a loop, which are of some word size. Typically the data is moved first with the most meaningful bit when a new less important bit is shifted to the same register.

The master and slave have shared registry values since the register has been moved. Then any computer gets the value and does something, such as memory writing. When more data are exchanged, new data are loaded in the shift registers and processes are replaced.

There can be a lot of clock cycles involved in transmissions. The master stops toggling his clock if data is no longer to be passed on. Then it desecrates the slave usually. Transmissions often consist of 8-bit phrases, and if desired/needed a master will trigger several such transmissions. Other words sizes, however, are also

popular for Task-to-Analog or analogue to Digital Converters, such as 16-bit words for TSC2101, or 12-bit words for certain TSCs.

Any slave in the bus not activated on the chip-select-line should ignore the input clock and MOSI signals and not push MISO. Just one slave at a moment is to be selected.

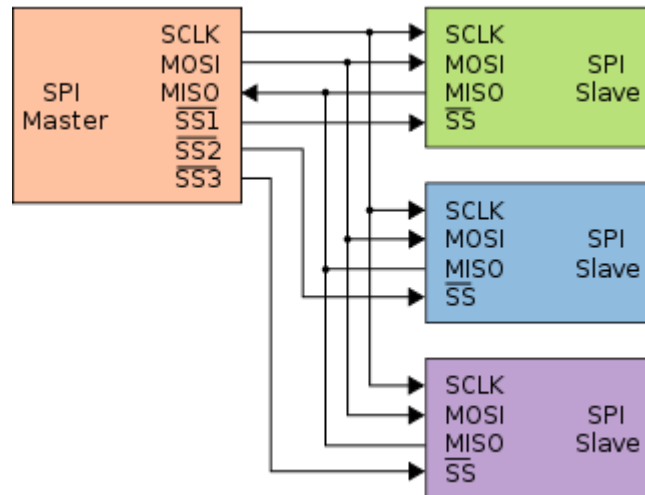


FIG4.2.4 –SPI BUS CONNECTING A MASTER WITH 3 SLAVES

4.3 RELAY UNIT:

4.3.1DESCRIPTION:

A complete height module that has four relay outputs is the 4-channel relay module. Any 4-Channel Modules can be mounted in any of the Rack Interface Module's slots to the right. Each 4- Channel Relay module output can be programmed separately to accomplish the required voting logic. The 4-channel relay provides "Alarm Drive Logic" for any relay that is used. AND and OR logic are used to configure the Warning Drive Logic. Alarming inputs from each monitoring channel or from some mixture of control channels in the rack can be used. This Alarm Drive Logic is designed to satisfy the basic needs of the application using the 3500 rack configuration software.

4.3.2 Characteristics:

On terminal lines, there are relay connections for normally closed (NC), normally open (NO), and common (C). There is consistency between NC and C when the relay is not energised (digital 0). There is consistency between NO and C when the relay is energised (digital 1).

4.3.3 Specifications:

Dimensions: 5.6 x 2.8 in (14.2 X 7 cm)

Power Requirements:

Single Board: 10 to 16 VDC @ 200 mA max.

4 Boards: 12 to 16 VDC @ 800 mA max.

Max Current Throughput: 1 A

Voltage: 5V

Relays:

Number of Channels 4

Contact Rating 10 A @ 120 VDC

8 A @ 30 VDC (resistive)

Max. Switching Capacity 1200 VA/240 W

Max. Operating Voltage 250 VAC/125 VDC

Max. Carrying Current 10 A (AC), 8 A (DC) (standard)

Relay Form Form C, Single-Pole Double-Throw (SPDT)

Output Terminals Normally Open (NO) , Normally Closed (NC)

Relay Life (mech.) 10 million operations minimum

Relay Life (load dependent) 100 thousand operations minimum

Operating Time 10 msec. max. (mean ~5.1msec.)

4.3.4 Sensors Array:

The sensor range consists of three sensors for air pollution, including carbon dioxide (CO₂), dioxide nitrogen (NO₂) and sulphide (SO₂). For emissions monitoring, the resolution of these sensors is enough. The above sensors each are equipped with a 4 mA–20 mA linear current scale. The production of 4 mA is null and 20 mA is the highest level of the gas. The 4 mA-20 mA range is converted to the 0-5 V by a simple signal conditioning circuit, which is consistent with the voltage range of the integrated analogue to digital converter in the microcontroller.

4.5 GSM Modem

For applications with synchronisation instead of fast data speeds, the GSM network used by mobile phones has a low cost, long-range wireless communication path. The GSM device can be attached to machinery such as industrial coolers and freezers, HVAC, vending machines, car operation, etc. This software explains how an AVR is used to power a GSM modem in a mobile phone. A textual protocol called the Hayes AT-Commands is the interface between modem and host. The commands allow for phone configuration, dialling, email, etc. This particular application uses a cellular RS232 data cable to link an AVR Butterfly and Siemens® M65.

4.6 Power Supply:

A mechanical unit providing electric energy for an electrical load is a power supply. A power supply's primary purpose is to transform one electrical energy to another, resulting in certain electrical power supplies being called electrical power transwers. While some electricity sources are individual independent units, others are configured in larger devices with their load. For example, power supplies used in computers on desktops and consumer products.

4.7 SOFTWARE USED:

Software used in this project are

- PROTEOUS IDE
- Hi-Tech Compiler
- C- Language

4.7.1 Proteus IDE:

Proteus is software for simulation of microprocessor, schematic recording, and PCB. The labcenter electronics is created.

The Micro Edition of XGameStation was developed with the schematic entrance and layout software of Labcenter's Proteus system.

In order to build up the PCB layout, many CAD users reject schematic capture as a must, but we have always contested this viewpoint. For a PCB interface that now automates the positioning of all components and the track routing, it also takes the most time to get the concept into the machine.

With this in mind, ISIS was created. Science and development have developed over 12 years and have been demonstrated by thousands of users around the world. Its strengths enable us to incorporate first traditional graph-based simulation into the design environment with the help of PROTEUS VSM. For the first time, a full circuit can be drawn from the same device to a micro-controller-based machine and then tested interactively. In the meantime, ISIS maintains a host of PCB-designer-driven features that allow the same design for development by ARES or other layout tools for PCBs.

ISIS also excels in the production of attractive schemes as you see in magazines for the educational user and author of engineering. In terms of line widths, filling types, colours and font, the drawing looks are completely regulated. Furthermore, you can describe the design of a house and copy the look of one picture to another using a templates scheme.

Other general features include:

- Runs on Windows 2k onwards.

- Automatic wire routing and dot placement/removal.
- Powerful tools for selecting objects and assigning their properties.
- Total support for buses including component pins, inter-sheet terminals, module ports and wires.
- Bill of Materials and Electrical Rules Check reports.
- Netlist outputs to suit all popular PCB layout tools.
- For the 'power user', ISIS incorporates a number of features which aid in the management of large designs. Indeed, a number of our customers have used it to produce designs containing many thousands of components.
- Hierarchical design with support for parameterized component values on sub-circuits.
- Design Global Annotation allowing multiple instances of a sub-circuit to have different component references.
- Automatic Annotation - the ability to number the components automatically.
- ASCII Data Import - this facility provides the means to automatically bring component stock codes and costs into ISIS design or library files where they can then be incorporated or even totaled up in the Bill of Materials
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4.7.2 ISIS & ARES:

Users of ARES, or indeed other PCB software will find some of the following PCB design specific features of interest:

- Sheet Global Net Properties which allow you to efficiently define a routing class for all the nets on a given sheet (e.g. a power supply needing POWER width tracks).
- Physical terminals which provide the means to have the pins on a connector scattered all over a design.
- Support for heterogeneous multi-element devices. For example, a relay device can have three elements called RELAY: A, RELAY: B and RELAY: C. RELAY: A is the coil whilst elements B and C are separate contacts. Each element can be placed individually wherever on the design is most convenient.
- Support for pin-swap and gate-swap. This includes both the ability to specify legal swaps in the ISIS library parts and the ability to back-annotate changes into a schematic.
- A visual packaging tool which shows the PCB footprint and its pin numbers alongside the list of pin names for the schematic part. This facilitates easy and error free assignment of pin numbers to pin names. In addition, multiple packagings may be created for a single schematic part.
- A full chapter is provided on how to use ISIS and ARES together.

ISIS & Simulation:

- For PROTEUS VSM, our groundbreaking immersive machine level simulator, ISIS offers the development environment. This product incorporates simulation of mixed circuit mode, micro-processor models and dynamic model components to simulate the full architecture of microcontrollers.

- ISIS offers first of all the means for entering the design, the framework for an immersive real-time simulation and a framework for the management of the source and software code for each project. Moreover, several graphic artefacts can be put on the schematic in order to allow traditional simulation of time, frequency and swept variables.

Major features of PROTEUS VSM include:

- True Mixed Mode simulation based on Berkeley SPICE3F5 with extensions for digital simulation and true mixed mode operation.
- Support for both interactive and graph based simulation.
- CPU Models available for popular microcontrollers such as the PIC and 8051 series.
- Interactive peripheral models include LED and LCD displays, a universal matrix keypad, an RS232 terminal and a whole library of switches, pots, lamps, LEDs etc.
- Virtual Instruments include voltmeters, ammeters, a dual beam oscilloscope and a 24 channel logic analyser.
- On-screen graphing - the graphs are placed directly on the schematic just like any other object. Graphs can be maximised to a full screen mode for cursor based measurement and so forth.
- Graph Based Analysis types include transient, frequency, noise, distortion, AC and DC sweeps and fourier transform. An Audio graph allows playback of simulated waveforms.
- Direct support for analogue component models in SPICE format.
- Open architecture for 'plug in' component models coded in C++ or other languages. These can be electrical., graphical or a combination of the two.
- Digital simulator includes a BASIC-like programming language for modelling and test vector generation.
- A design created for simulation can also be used to generate a netlist for creating a PCB - there is no need to enter the design a second time.

4.7.3 ISIS & Networks

ISIS is fully network compatible, and offers the following features to help Network Managers:

- Library files can be set to Read Only. This prevents users from messing with symbols or devices that may be used by others.
- ISIS individual user configuration in the windows registry. Since the registry determines the location of library files, it follows that users can have individual USERDVC.LIB files in their personal or group directories.

CHAPTER 5

RESULT& DISCUSSIONS

This project selects, studies and tests the hardware and empathises the software component. An algorithm must be created and flow charts planned according to the mission to be carried out by the machine. The programme shall be compiled and evaluated in a proteus according to the planned algorithm and flow map. For greater convenience and simple execution, the Program is written in C language. It can then be loaded into the microcontroller. The circuits are then provided in a breadboard to measure the result according to the block diagram and pin specification. PCB should be created for the previous circuit relation after verification of the effects and expected performance. The hardware is required to defend against external strength and injury. The system proposed should be tested and ready for use.

NORMAL CONDITION RESULT:

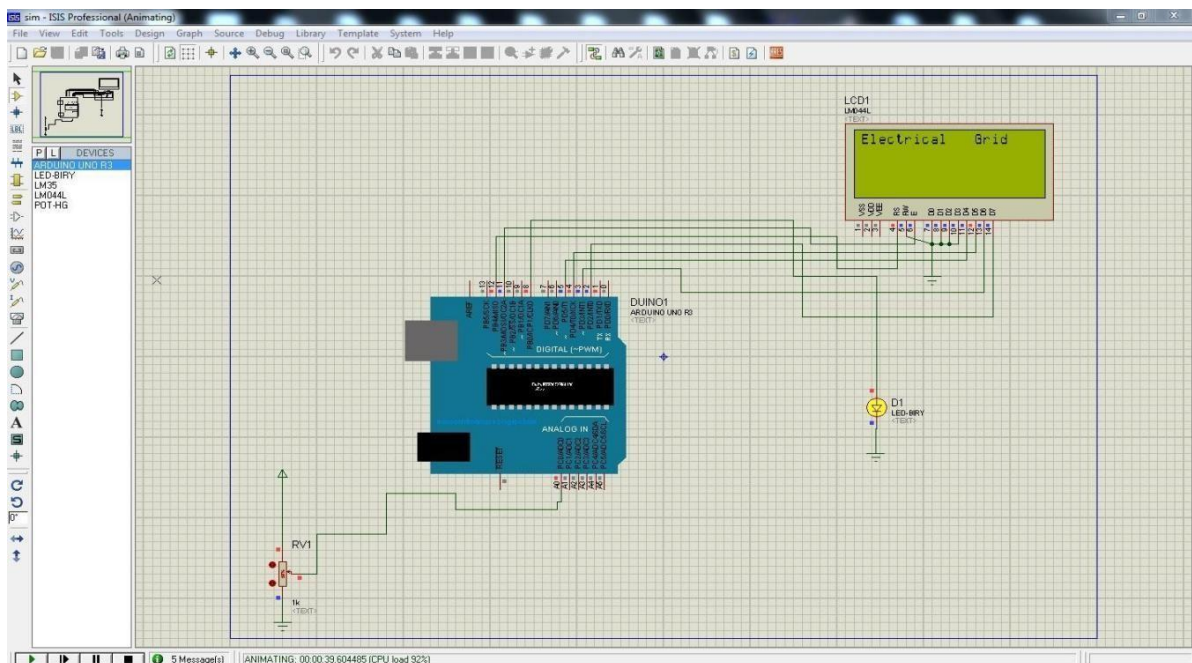


Fig:5.1

OVERLOAD CONDITION RESULT:

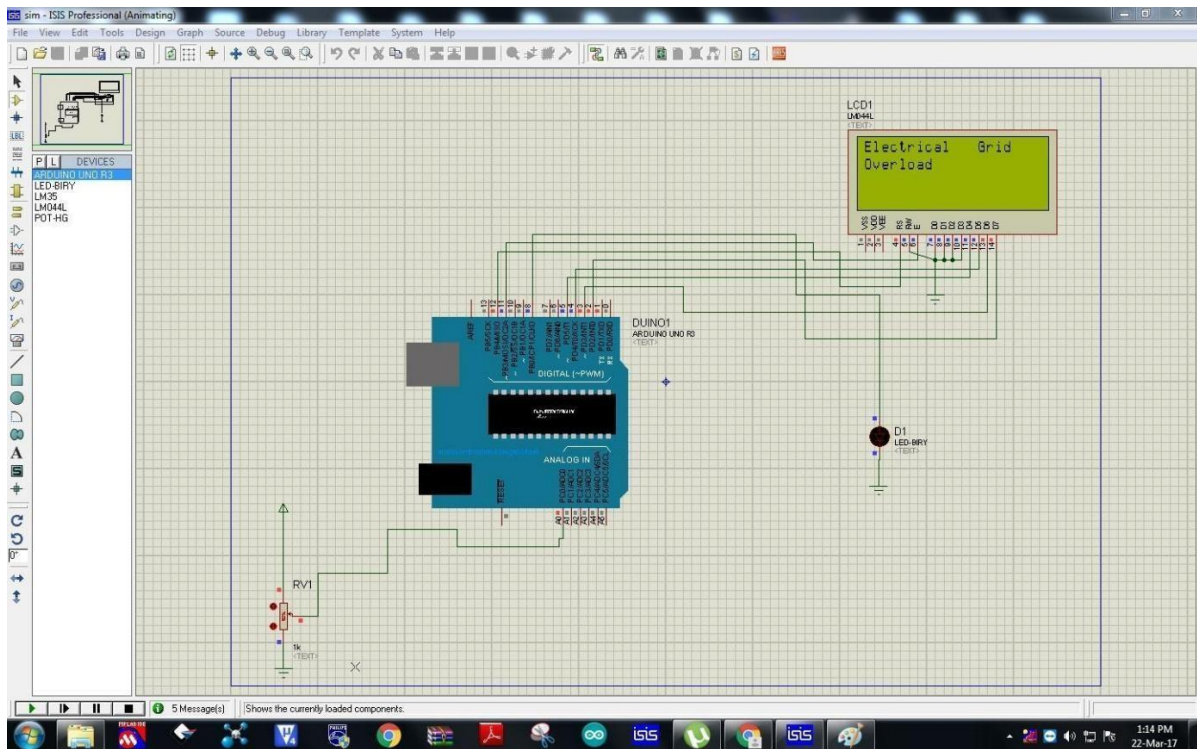


Fig:5.2

CHAPTER 6

CONCLUSION & SUMMARY

With proper integration of both the hardware and the software, a wireless electricity maximum power requirement Detection and monitoring system has also been planned. This machine offers a simple and efficient means of detecting electric robbery without any human interface. Usage of GSM allows the wireless network networks to achieve their many advantages. Theft simply circumvents the energy metre, but we have suggested the theft in our project by increasing the burden, and this approach is economic.

This specifically analyses the philosophy of the project and the literary analysis of the IEEE articles on this idea takes place. The method is revised and the system's concepts and shortcomings are identified. There is a detailed overview of the proposed structure and the block diagram and system architecture are created. The work of the system is explicitly clarified and in this process a project of the system is performed by the selection and testing of suitable hardware.

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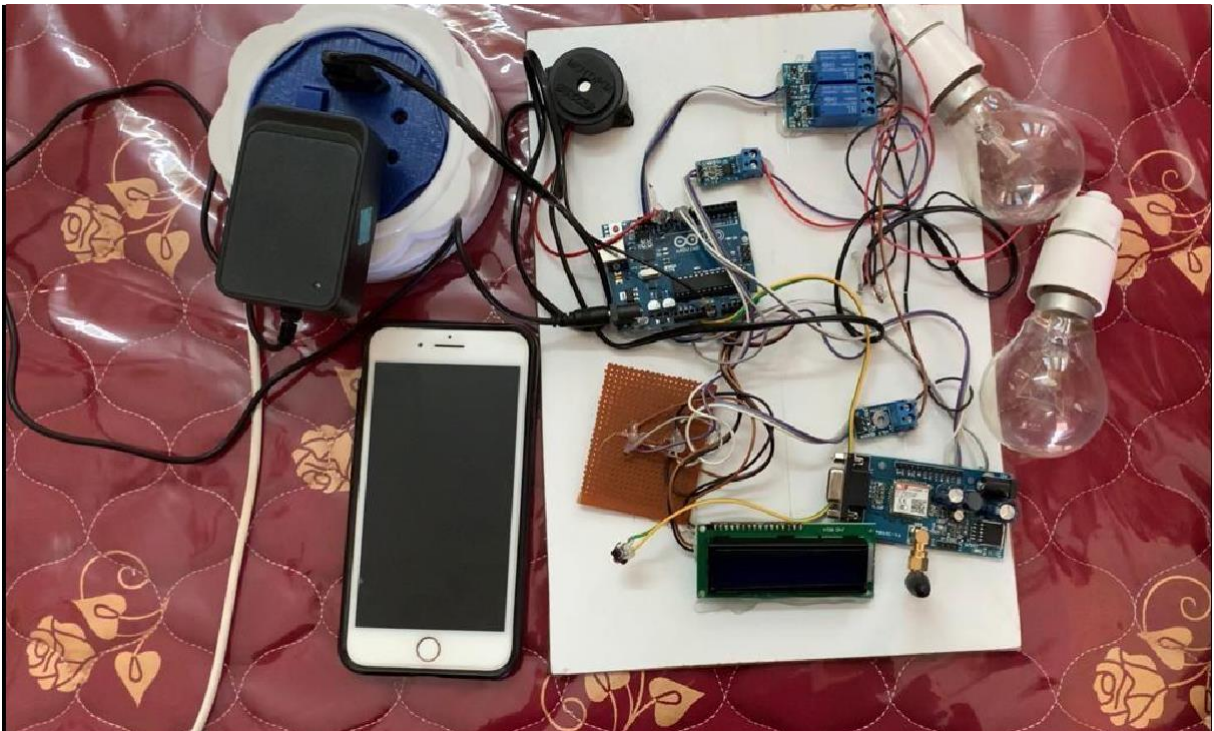
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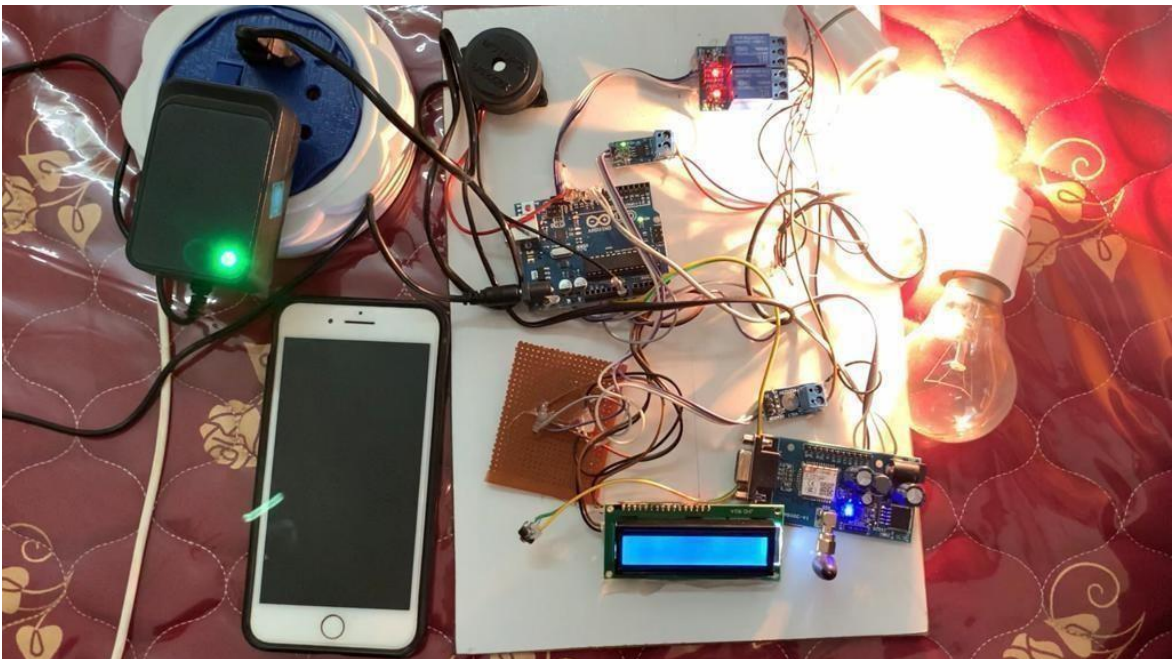
APPENDIX I

OUTPUT SCREENSHOTS

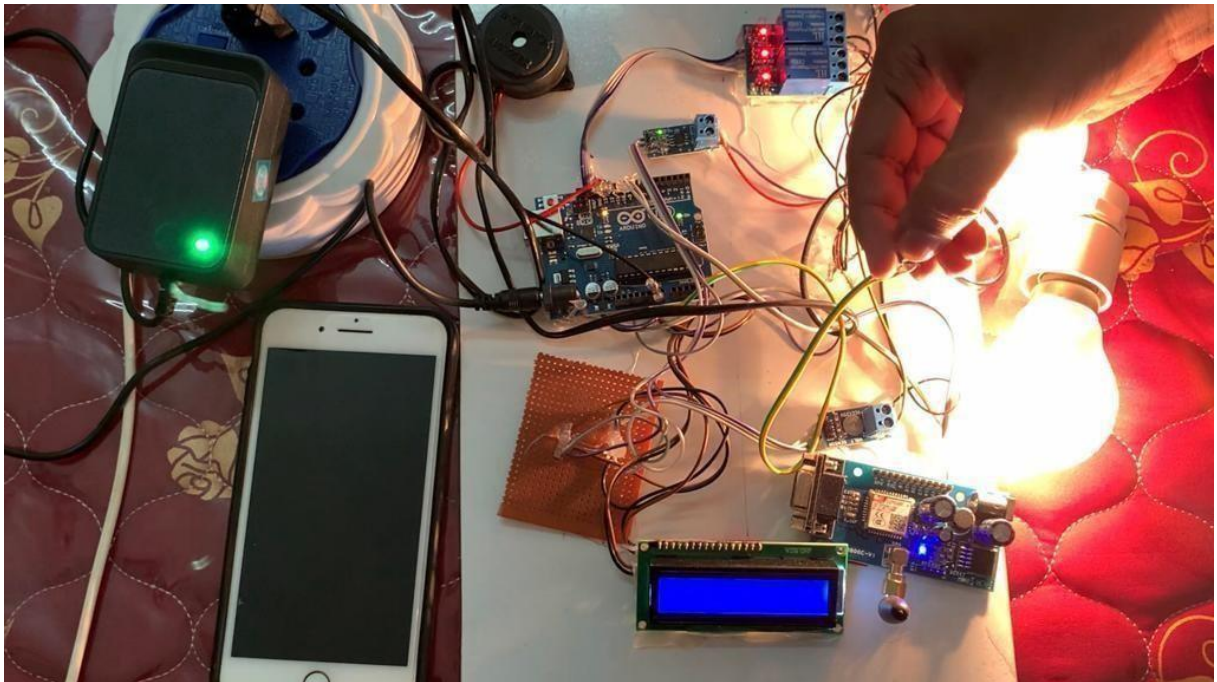
Entire setup:



Normal condition:



Power Exceed:



SMS generation:



APPENDIX II

SIMULATION CODING

```
#include<SoftwareSerial.h>
SoftwareSerial myserial(9,10);

void      send_sms();
#include<Wire.h>
#include <stdlib.h>

#include<LiquidCrystal_I2C.h>
#define smoke A0
LiquidCrystal_I2C
lcd(0x27,16,2);      int
card1_C;

void      setup()      {
myserial.begin(9600);
Serial.begin(9600); // put your setup code here, to run once:

pinMode(6,O
UTPUT);
pinMode(7,O
UTPUT);
digitalWrite(6,
HIGH);
digitalWrite(7,
LOW);
```

```

digitalWrite(1
3,LOW);
Wire.begin();
lcd.backlight()
; lcd.init();

lcd.setCursor(0,0);
lcd.print("NORMAL CONDITION");

}

void loop()
{

unsigned int x=0; float
AcsValue=0.0,Samples=0.0,AvgAcs=0.0,AcsVa
lueF=0.0; float v; v=analogRead(1);
lcd.setCursor(0,1); lcd.print("V:");
lcd.setCursor(2,1); lcd.print(v);

delay(2);

for (int x = 0; x < 150; x++){ //Get 150 samples
AcsValue = analogRead(2); //Read current
sensor values Samples = Samples +
AcsValue; //Add samples together delay (3); //
let ADC settle before next sample 3ms
}
AvgAcs=Samples/150.0;
AcsValueF = (2.5 - (AvgAcs * (5.0 / 1024.0)) )/0.100;

```

```

AcsValueF=Acs
ValueF/4;
Serial.print(Acs
ValueF);
lcd.setCursor(5,
1);
lcd.print("I:");
lcd.setCursor(7,
1); delay(2);

```

```

int
data2=analogRead(0)
; if(data2 > 100)
{
    Serial.print("enter the
loop");
digitalWrite(7,HIGH);
delay(3000);
digitalWrite(7,LOW);
send_sms2();

}

```

```

delay(2);

```

```

}

```

```

void send_sms2(){
    Serial.println("sms                function");
    myserial.println("AT+CMGF=1"); //Sets the GSM Module
in Text Mode delay(1000); // Delay of 1000 milli seconds
or 1 second

```

```
    myserial.println("AT+CMGS=\"+918610695239\\r"); // Replace x with
mobile number delay(1000);
    myserial.println("power excedded");// The SMS text
you want to send delay(100);
myserial.println((char)26);// ASCII code of CTRL+Z
delay(1000);

}
```



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