

Analysis of XOR-MUX Full Adder Based Computational Block For Low Power Architecture

Submitted in partial fulfillment of the requirements for the award of
Bachelor of Engineering degree in Electronics and Communication Engineering

by

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SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING**

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119

APRIL - 2021



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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of NAVANEETA SUTRADHAR (Reg.No: 37130281) and P.HEMA DHANA DEEPIKA (Reg.No: 37130329), who carried out the project entitled “**ANALYSIS OF XOR-MUX FULL ADDER BASED COMPUTATIONAL BLOCK FOR LOW ARCHITECTURE**” under my supervision from December 2020 to April 2021

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DECLARATION

We, NAVANEETA SUTRADHAR (Reg.No: 37130281) and P.HEMA DHANA DEEPIKA(Reg.No: 37130329) hereby declare that the Project Report entitled **ANALYSIS OF XOR-MUX FULL ADDER BASED COMPUTATIONAL BLOCK FOR LOW POWER AECHITECTURE** is done by us under the guidance of Mr. K.T.ILAYARAJAA, M.E.,(Ph.D) and at SATHYABAMA INSTITUTE OF SCIENCE AND TECHNOLOGY is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

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ABSTRACT

In this paper, we proposed three different accurate 4:2 compressor with using high speed gate level full adder design of XOR and Multiplexer circuit instead of conventional full adder design. Which have the flexibility of switching between the exact and approximate computing operating modes. In this approximate mode, these dual quality compressor provide high speed and low power consumptions at the cost of lower accuracy. Each of the compressor has its own level of accuracy in the approximation mode as well as different delay and power dissipations in the approximate and exact modes. Using these compressors in the Approximate multiplier, it will provide accuracies as well as the power and speed may change dynamically during the runtime operations. The proposed 4:2 compressor based approximate multiplier save few number of logic gates in partial product, and this proposed multiplier was evaluated in image processing application, such as image multiplication, image sharpening, and so on. This design was implemented in Verilog HDL, and synthesized in Xilinx S6LX9 FPGA and compared all parameters in terms of area, delay and power.

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CHAPTER 1

INTRODUCTION

1.1 MULTIPLEXER

Multiplexing is the generic term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called a Multiplexer. In electronics, a **multiplexer** (or **mux**; spelled sometimes as **multiplexor**), also known as a **data selector**, is a device that selects between several analog or digital input signals and forwards the selected input to a single output line. The selection is directed a separate set of digital inputs known as select lines. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output.

A multiplexer makes it possible for several input signals to share one device or resource, for example, one analog-to-digital converter for example, one analog-to-digital converter or one communications transmission medium, instead of having one device per input signal. Multiplexers can also be used to implement Boolean functions of multiple variables.

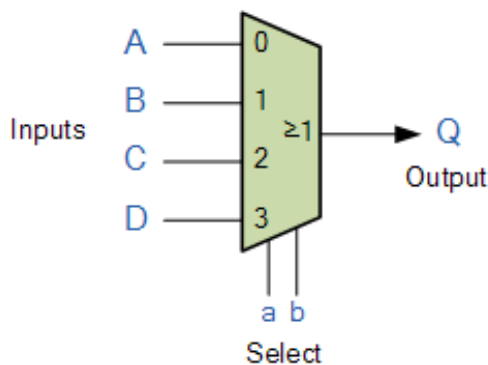


Fig:1.1:Symbolic Diagram of Multiplexer

Conversely, a demultiplexer (or demux) is a device taking a single input and selecting signals of the output of the compatible mux, which is connected to the single input, and a shared selection line. A multiplexer is often used with a complementary demultiplexer on the receiving end.

An electronic multiplexer can be considered as a multiple-input, single-output switch, and a demultiplexer as a single-input, multiple-output switch. The schematic symbol for a multiplexer is an isosceles trapezoid with the longer parallel side containing the input pins and the short parallel side containing the output pin. The schematic on the right shows a 2-to-1 multiplexer on the left and an equivalent switch on the right. The sel wire connects the desired input to the output.

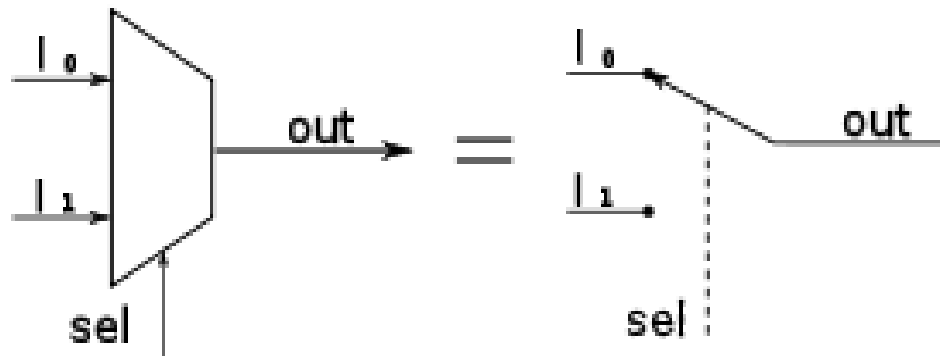


Fig:1.2:Schematic Of A 2-To-1 Multiplexer. It Can Be Equated To A Controlled Switch

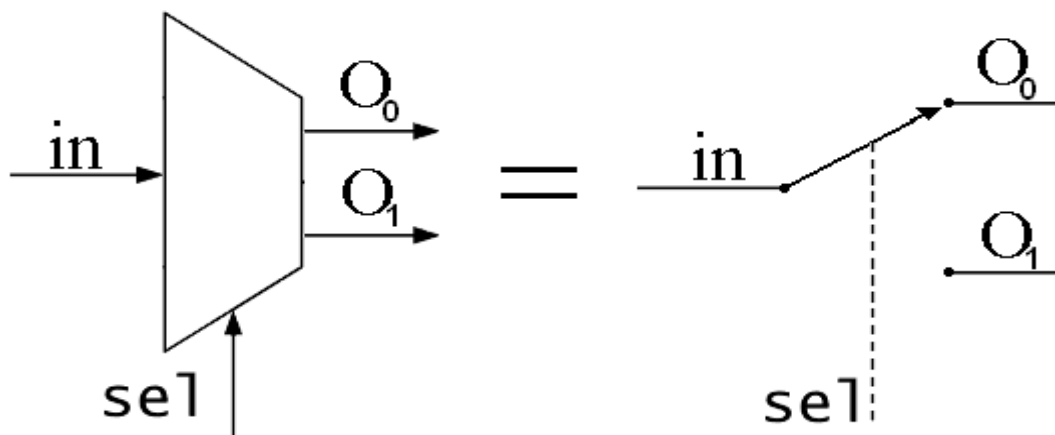


Fig:1.3:Schematic Of A 1-To-2 Demultiplexer. Like A Multiplexer, It Can Be Equated To A Controlled Switch.

1.2 DIGITAL MULTIPLEXER

In digital circuit design, the selector wires are of digital value. In the case of a 2-to-1 multiplexer, a logic value of 0 would connect to the output while a logic value of 1

would connect to the output. In larger multiplexers, the number of selector pins is equal to where is the number of inputs.

For example, 9 to 16 inputs would require no fewer than 4 selector pins and 17 to 32 inputs would require no fewer than 5 selector pins. The binary value expressed on these selector pins determines the selected input pin.

1.3 2*1 MULTIPLEXER

A 2-to-1 multiplexer has a boolean equation where A and B are the two inputs, S_0 is the selector input, and Z is the output:

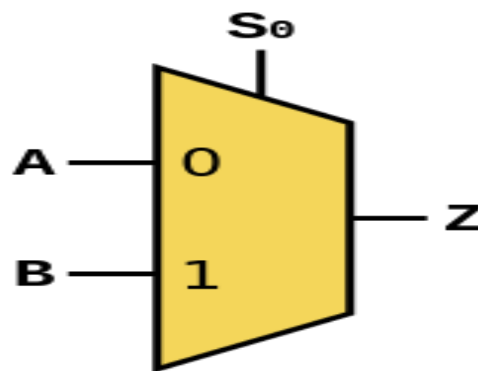


Fig:1.4:2*1 Multiplexer Pin Diagram

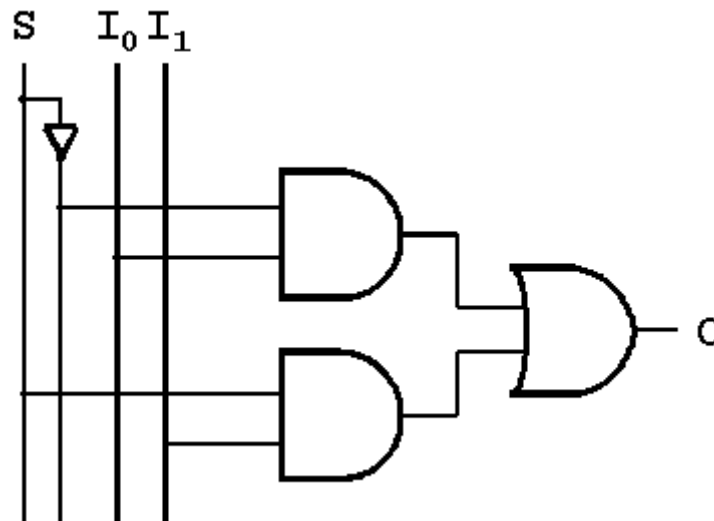


Fig:1.5:2*1 Multiplexer Circuit Diagram

1.4 4×1 MULTIPLEXER

4 x 1 mux need 4 AND and 1 OR and 2 NOT gates. Replace OR gate with Invert-input NAND , then above circuit will be replace with 2 NOT and 5 NAND , then 2 NANDS for 2 NOT's , then total 7 NAND gates required.

Output of 4*1mux is $A'B' + A'B + AB' + AB$. we can simplify this and we will get 1.

So i think we required 0 NAND gate.

$$A'B + AB' + AB$$

$$A'(B+B) + A(B'+B) = A' + A = 1$$

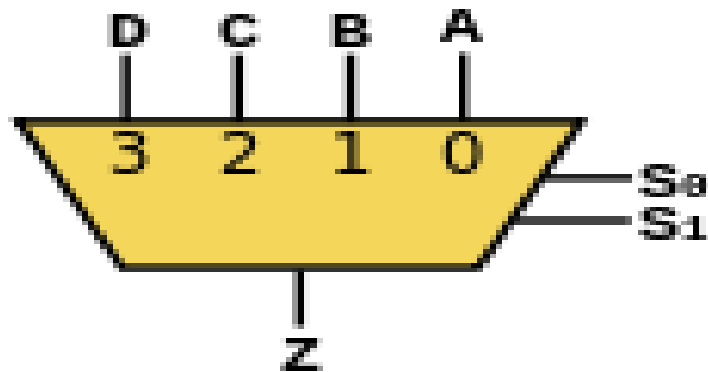


Fig:1.6:4*1 Multiplexer Pin Diagram

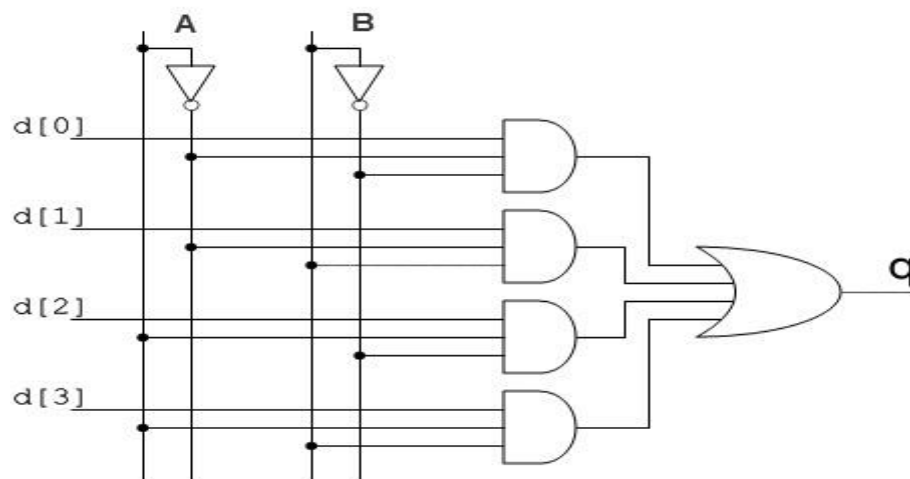


Fig:1.7:4*1 Multiplexer Circuit Diagram

Table:1.1:The Truth Table Of 4*1 Multiplexer

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

From the above truth table, we can write the output expressions as

If $S_1=0$ and $S_0=0$ then $Y = D_0$

Therefore, $Y = D_0 (S_1)^{\overline{}} (S_0)^{\overline{}}$

If $S_1= 0$ and $S_0=1$, the $Y = D_1$

Therefore, $Y = D_1 (S_1)^{\overline{}} S_0$

If $S_1=1$ and $S_0=0$, then $Y = D_2$

Therefore, $Y = D_2 S_1 (S_0)^{\overline{}}$

If $S_1=1$ and $S_0=1$ the $Y = D_3$

Therefore, $Y = D_3 S_1 S_0$

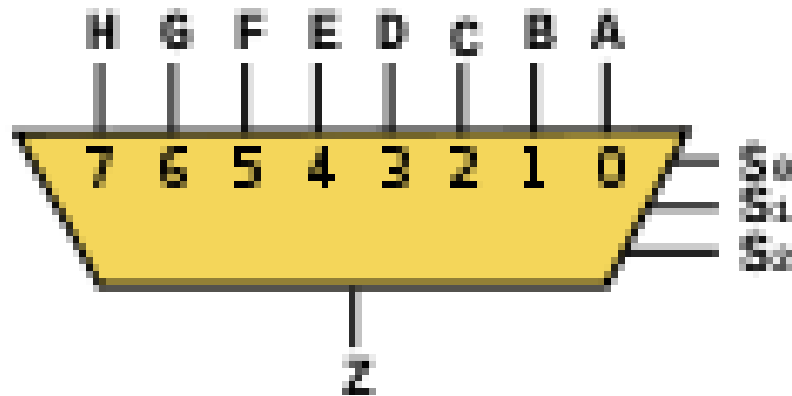
To get the total data output from the multiplexer, all these product terms are to be summed and then the final Boolean expression of this multiplexer is given as

$$Y = D_0 \overline{S_1} \overline{S_0} + D_1 \overline{S_1} S_0 + D_2 S_1 \overline{S_0} + D_3 S_1 S_0$$

1.5 8*1 MULTIPLEXER

An 8-to-1 multiplexer consists of eight data inputs D0 through D7, three input select lines S2 through S0 and a single output line Y. Depending on the select lines combinations, multiplexer decodes the inputs.

The below figure shows the block diagram of an 8-to-1 multiplexer with enable input that enable or disable the multiplexer. Since the number data bits given to the MUX are eight then 3 bits ($2^3=8$) are needed to select one of the eight data bits



*Fig:1.8:8*1 Multiplexer*

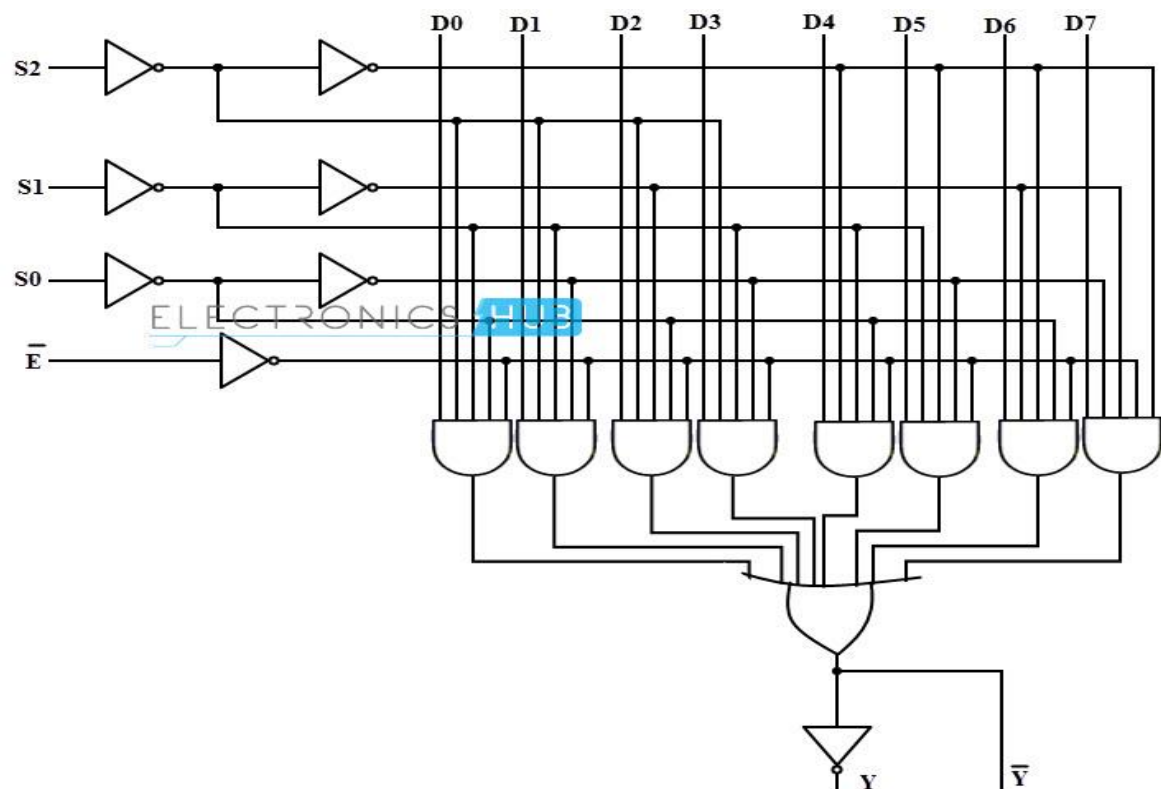


Fig:1.9:8*1 Multiplexer Circuit Diagram

The logic circuit diagram of an 8-to-1 multiplexer can be implemented by using 8 AND gates, 1 OR gate and 7 NOT gates as shown in below figure. In the circuit, when enable pin is set to one, the multiplexer will be disabled and if it is zero then select lines will select the corresponding data input to pass through the output.

Table1.2:Truth Table Of 8*1 Multiplexer

Select Data Inputs			Output
S_2	S_1	S_0	Y
0	0	0	D_0
0	0	1	D_1
0	1	0	D_2
0	1	1	D_3
1	0	0	D_4
1	0	1	D_5
1	1	0	D_6
1	1	1	D_7

1.6 LOGIC GATES

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

1.6.1 XOR Gate

XOR or Ex-OR gate is a special type of gate. It can be used in the half adder, full adder and subtractor. The exclusive-OR gate is abbreviated as EX-OR gate or sometime as X-OR gate. It has n input ($n \geq 2$) and one output.

$$Y = A \text{ XOR } B \text{ XOR } \dots N$$

$$Y = A + B + C + \dots N$$

$$Y = A$$

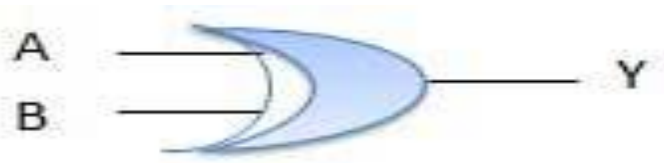


Fig:1.10 : Xor Logic Diagram

Table1.3 : Xor Truth Table

Inputs		Output
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

1.6.2 AND Gate

A circuit which performs an AND operation is shown in figure. It has n input ($n \geq 2$) and one output.

$$Y = A \text{ AND } B \text{ AND } C \dots N$$

$$Y = A.B.C \dots N$$

$$Y = ABC \dots N$$

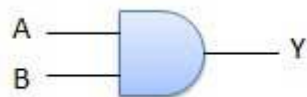


Fig:1.11 : And Logic Gate

Table1.4 : And Truth Table

Inputs		Output
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1

1.6.3 OR Gate

A circuit which performs an OR operation is shown in figure. It has n input ($n \geq 2$) and one output.

$$Y = A \text{ OR } B \text{ OR } C \dots N$$

$$Y = A + B + C \dots N$$



Fig:1.12 : Or Gate Logic Diagram

Table1.5 : Or Gate Truth Table

Inputs		Output
A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

This chapter discusses the about the literature survey and summary. It also gives a detailed idea on the existing Universal Shift Register and how their structures are synthesized

Table:2.1:Literature Survey

Title	Abstract	Contribution	Conclusion
Physical designing of MUX and XOR	By using pass gate logic with N & P MOS transistors, converted into MUX and XOR.	2:1 MUX, 2 inputs of XOR with builtin input signal inverters will be developed and added to CMOS logic gates.	Can design more complex logic gates where an optimized layout can be difficult to achieve.
MUX based on 1 bit Full Adder designing	2T mux is combined to get full adder that has output as sum & carry, resulting 1 bit full adder is of 16 transistors.	2T +MUX.	Shows efficiency of the design.
Designing of digital logic gates by using MUX	All the standard logical gates can be implemented with multiplexer.	Any kind of MUX can be used. For N input lines log or for 2n input lines, n selection lines are needed	Any Mux can be converted into logical gates.

2.1 LITERATURE SURVEY

Approximate computing has recently emerged as a promising approach to energy-efficient design of digital systems. Approximate computing relies on the ability of many systems and applications to tolerate some loss of quality or optimality in the computed result. By relaxing the need for fully precise or completely deterministic operations, approximate computing techniques allow substantially improved energy efficiency. This paper reviews recent progress in the

area, including design of approximate arithmetic blocks, pertinent error and quality measures, and algorithm-level techniques for approximate computing

.

2.2 PROBLEM DEFINITION

The occurrence of errors are inevitable in modern VLSI technology and to overcome all possible errors is an expensive task. It not only consumes a lot of power but degrades the speed performance. By adopting an emerging concept in VLSI design and test-error-tolerance (ET), we managed to develop a novel error-tolerant adder which we named the Type II (ETAI). The circuit to some extent is able to ease the strict restriction on accuracy to achieve tremendous improvements in both the power consumption and speed performance. When compared to its conventional counterparts, the proposed ETAI is able to achieve more than 60% improvement in the power-delay product (PDP). The proposed ETAI is an enhancement of our earlier design, the ETAI, which has problem adding small number inputs.

Low-power is an imperative requirement for portable multimedia devices employing various signal processing algorithms and architectures. In most multimedia applications, the final output is interpreted by human senses, which are not perfect. This fact obviates the need to produce exactly correct numerical outputs. Previous research in this context exploits error-resiliency primarily through voltage over-scaling, utilizing algorithmic and architectural techniques to mitigate the resulting errors. In this paper, we propose logic complexity reduction as an alternative approach to take advantage of the relaxation of numerical accuracy. We demonstrate this concept by proposing various imprecise or approximate Full Adder (FA) cells with reduced complexity at the transistor level, and utilize them to design approximate multi-bit adders. In addition to the inherent reduction in switched capacitance, our techniques result in significantly shorter critical paths, enabling voltage scaling. We design architectures for video and image compression algorithms using the proposed approximate arithmetic units, and evaluate them to demonstrate the efficacy of our approach. Post-layout simulations indicate power savings of up to 60% and area savings of up to 37% with an insignificant loss in output quality, when compared to existing implementations.

2.3 OBJECTIVE OF THE PROJECT

Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed. For applications related to human senses, approximate arithmetic can be used to generate sufficient results rather than absolutely accurate results. Approximate design exploits a tradeoff of accuracy in computation versus performance and power. However, required accuracy varies according to applications, and 100% accurate results are still required in some situations. In this paper, we propose an accuracy-configurable approximate (ACA) adder for which the accuracy of results is configurable during runtime. Because of its configurability, the ACA adder can adaptively operate in both approximate (inaccurate) mode and accurate mode. The proposed adder can achieve significant throughput improvement and total power reduction over conventional adder designs. It can be used in accuracy-configurable applications, and improves the achievable tradeoff between performance/power and quality. The ACA adder achieves approximately 30% power reduction versus the conventional pipelined adder at the relaxed accuracy requirement.

2.4 PROPOSED SYSTEM:

Adders are one of the key components in arithmetic circuits. Enhancing their performance can significantly improve the quality of arithmetic designs. This is the reason why the theoretical lower bounds on the delay and area of an adder have been analysed, and circuits with performance close to these bounds have been designed. In this paper, we present a novel adder design that is exponentially faster than traditional adders; however, it produces incorrect results, deterministically, for a very small fraction of input combinations. We have also constructed a reliable version of this adder that can detect and correct mistakes when they occur. This creates the possibility of a variable-latency adder that produces a correct result very fast with extremely high probability; however, in some rare cases when an error is detected, the correction term must be applied and the correct result is produced after some time. Since errors occur with extremely low probability, this new type of adder is significantly faster than state-of-the-art adders when the overall latency is averaged over many additions.

CHAPTER 3

AIM AND SCOPE OF PRESENT INVESTIGATION

3.1 PROPOSED METHODOLOGY

- Our proposed project focuses to reduce the amount of power that exists in the existing system
- The number of transistors used in designing of the existing system can be reduced in the proposed work
- The proposed system is more efficient in terms of power consumption

3.2 AREA OF THE PROPOSED WORK AND APPLICATION

A Multiplexer is used to increase the efficiency of the **communication** system by allowing the transmission of data such as audio & video data from different channels via cables and single lines. **Logic gates** perform basic **logical** functions and are the fundamental building blocks of digital integrated **circuits**. Most **logic gates** take an input of two binary values, and output a single value of a 1 or 0.

Full Adder is the **adder** which adds three inputs and produces two outputs. ... A **full adder** logic is designed in such a manner that can take eight inputs together to create a byte-wide **adder** and cascade the carry bit from one **adder** to the another.

3.3 FULL ADDER

Full adder is the basic block of arithmetic circuit found in microcontroller and microprocessor inside arithmetic and logic unit (ALU). Improvement of the adder is thus essential for upgrade the performance of those circuits where adder is employed. Full adders, till now, have been designed using wide range of structures for improvement of various parameters like power consumption, speed performance and structure size.

Full adder is a combinational circuit that performs the addition operation of 3 input bits. It basically consists three inputs and two outputs. The input variables are expressed by A, B and Cin. The two output variables are expressed by sum (S) and

carry (Cout) [4]. Fig. 1 shows the essential block diagram of full adder cell. The Boolean expression for full adder operation is defined below:

$$\text{SUM} = ((A \oplus B) \oplus \text{Cin})$$

$$\text{Cout} = AB + (A \oplus B)\text{Cin}$$

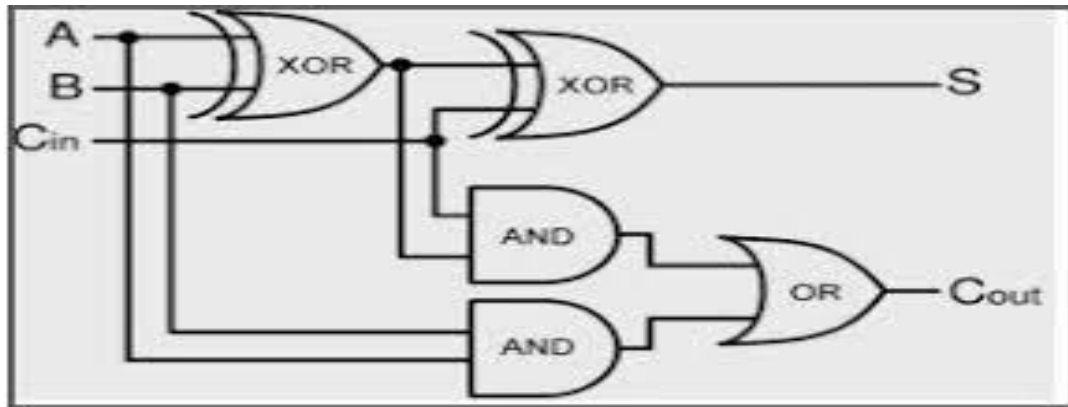


Fig:3.1:Full Adder Circuit Diagram

Table3.1:Truth Table Of Full Adder

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

A **full adder** circuit is central to most digital circuits that perform addition or subtraction. It is so called because it adds together two binary digits, plus a carry-in digit to produce a sum and carry-out digit.

Full Adder is the **adder** which adds three inputs and produces two outputs. The first two inputs are A and B and the *third* input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

Full adder includes two EX-OR **gates**, two OR **gates**, and two AND **gate**. The 'F283 is a **full adder** that performs the addition of two **4-bit binary** words. The sum (Σ) outputs are provided for each **bit** and the resultant carry (C4) output is obtained from the fourth **bit**.. End-around carry can be accomplished without the need for logic or level inversion.

3.3.1 Full Adder Has An Extensive Variety Of Application Are As Follows:-

- ALU- Arithmetic Logic Unit (one of the circuit is a full adder) to produce memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of this adder.
- For visuals correlated claims, wherever there is a actual considerable requirement of multifaceted calculations, the graphic processing unit uses optimized arithmetic logic unit which is made up of full adders, additional circuits as fine

3.3.2 Advantages Of Full Adder

- Low **power** consumption,
- High speed and robustness to supply voltage scaling, transistor sizing
- The disadvantage is that when used in a chain structure such as a ripple adder, the output drive capability is reduced.

3.3.3 The Disadvantages Of Full Adder:

- It does not incorporate (or take care of) previous carry for addition. Hence it is not
- It does not incorporate (or take care of) previous carry for addition. Hence it is not suitable for cascading for Multi-bit addition.
- To get rid of this problem, Full Adders are required which add three 1 bit.
- When Full Adders are used in a chain structure such as a Ripple Adder, the output drive capability is reduced.

3.4 Inverters

A **power inverter**, or **inverter**, is a **power electronic** device or circuitry that changes direct current (DC) to alternating current (AC). The input voltage, **output** voltage and frequency, and overall **power** handling depend on the design of the specific device or circuitry.

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An **inverter** converts the DC **electricity** from sources such as batteries or fuel cells to AC **electricity**. The **electricity** can be at any required voltage; in particular it can **operate** AC equipment designed for mains operation, or rectified to produce DC at any desired voltage



Fig:3.2:Inverter

An **inverter** converts the DC **electricity** from sources such as batteries or fuel cells to AC **electricity**. The **electricity** can be at any required voltage; in particular it can **operate** AC equipment designed for mains operation, or rectified to produce DC at any desired voltage.

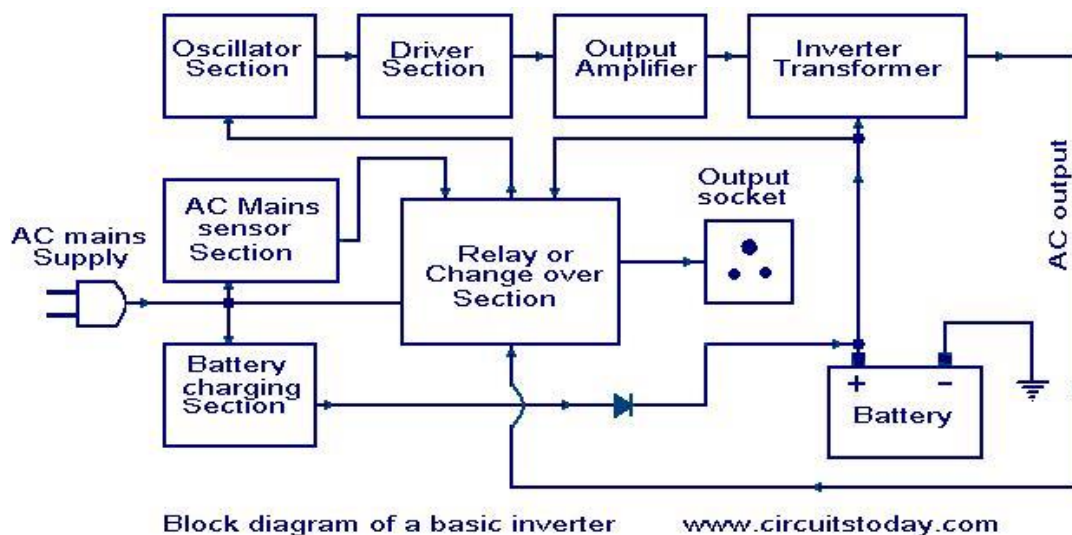


Fig:3.3:Basic Block Diagram Of Inverter

3.4.1 The Applications Areas Of Inverters Such As:

- Adjustable-speed ac motor drives.
- **Uninterrupted power supplies (UPS)**
- Running **appliances** of ac used in an automobile battery.power transmission industry such as reactive power controllers and adaptive power **filters**

3.4.2 According To The Output Characteristic Of An Inverter, There Can Be Three Different Types Of Inverters.

- Square Wave Inverter.
- **Sine Wave** Inverter.
- Modified **Sine Wave** Inverter.

3.5 XOR GATE

A **power** inverter, or inverter, is a **power** electronic device or circuitry that changes direct current (DC) to alternating current (AC). The input voltage, **output** voltage and frequency, and overall **power** handling depend on the design of the specific device or circuitry

XOR is a binary operation, it stands for "**exclusive or**", that is to say the resulting bit evaluates to one if only exactly one of the bits is set.

As I know, for **full adder** is required 6 **AND gate**,3 **OR gate** and 4 **NOT gate**.The **XOR** logic **gate** can be **used** as a one-bit **adder** that adds any two bits together to output one bit. ... Since the trailing sum bit in this output is achieved with **XOR**, the preceding carry bit is calculated with an **AND gate**. This is the main principle in Half **Adders**.

3.5.1 How Xor Gate Calculated

XOR is defined as exclusive or for two integers say a and b. To find **XOR**, we will first find the binary representation of both a and b. Lets do this also by example. Suppose a = 7 and b = 10

The **XOR gate** also called (Medulo Two Adder) , since it is used t give the sum of two binary numbers, it has been used in many arithmetic circuits (it will be explained in latter experiments). 2. Parity Checker: One of the **advantages** of using digital system, is it's capability of detecting and correction errors.

The main **disadvantage** of this implementation is that we need to use different types of **gates** to form a single **XOR gate**. By using only the **NAND gate**, we can implement the **Ex-OR gate** also. This is an easier way of producing **Ex-OR gate** functionality.

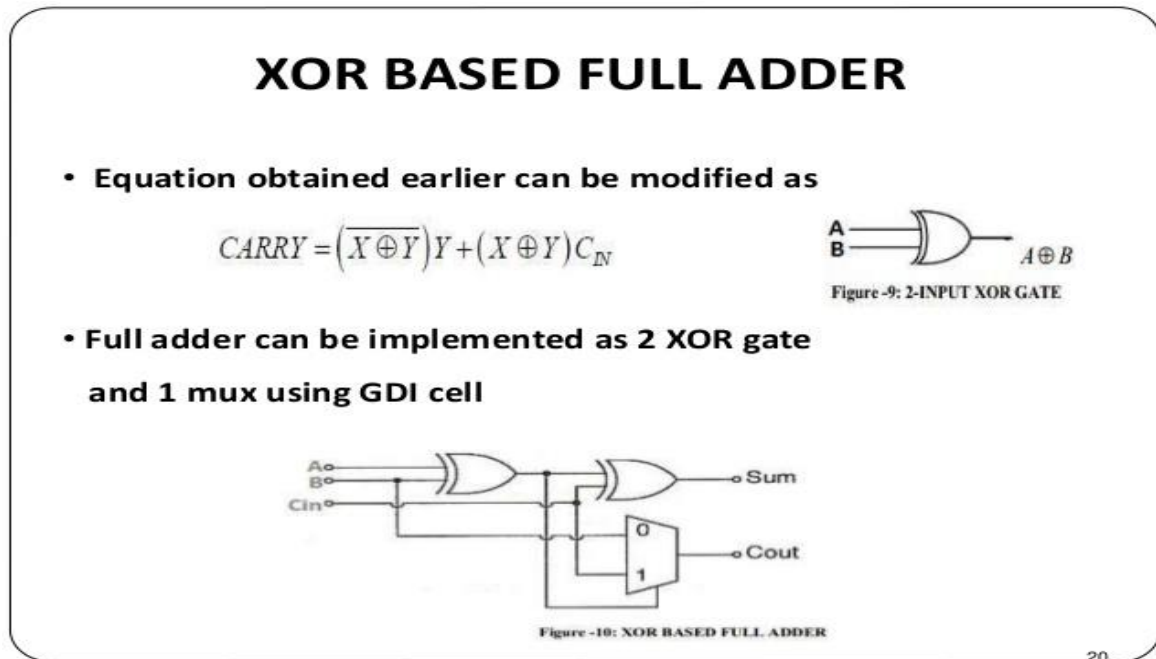


Fig:3.4:Xor Based Full Adder

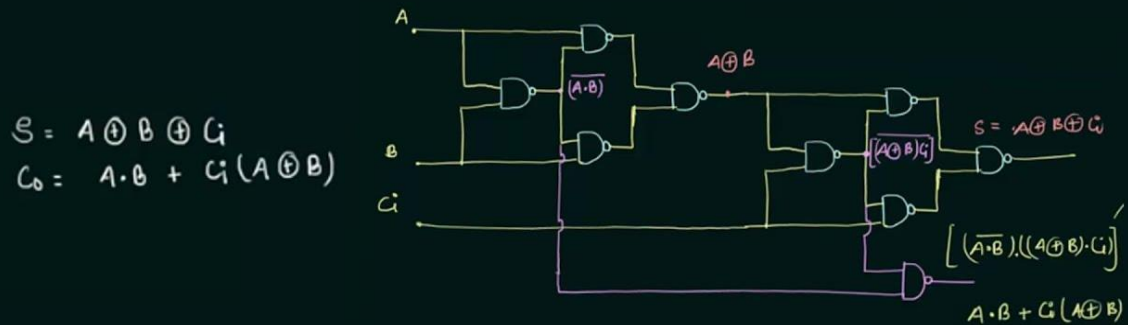
3.6 AND GATE

The **AND gate** is a basic digital logic **gate** that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results only if all the inputs to the **AND gate** are HIGH (1). If none or not all inputs to the **AND gate** are HIGH, LOW output results

The **AND gate** is so named because, if 0 is **called** "false" and 1 is **called** "true," the **gate** acts in the same way as the logical "and" operator. The output is "true" when both inputs are "true." Otherwise, the output is "false." In other words, the output is 1 only when both inputs one AND two are 1.

Logic gate circuit it given below, Here, **three NAND gates** are used to make an **OR gate**

Full Adder using NAND Gates



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Digital Electronics

Fig:3.5:Full Adder Using Nand Gates

Table3.2 : Two Input Truth Table Of Nand Gate

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Table3.3 :Three Input Nand Gate

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1

1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

3.6.1 Transistor NAND gate

A simple NAND gate can be constructed using transistors and resistors as shown in the figure below. The inputs of the NAND gate are directly connected to the transistor bases.

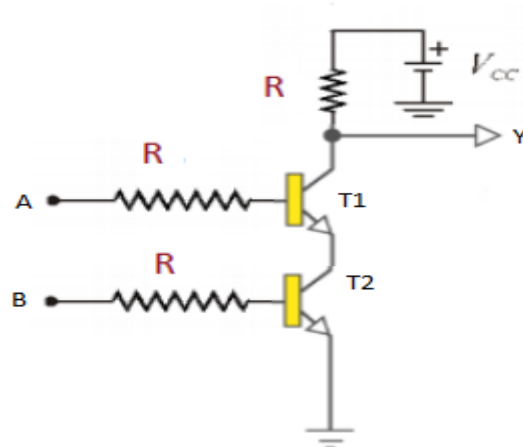


Fig:3.6:Basic Diagram Of Transistor In Nand Gate

3.7 OR GATE

The OR **gate** is a digital logic **gate** that implements logical disjunction it behaves according to the truth table to the right. A HIGH output (1) results if one or both the inputs to the **gate** are HIGH (1). If neither input is high, a LOW output (0) results

Full Adder is the **adder** which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM..

In another sense, the function of OR effectively finds the *maximum* between two binary digits, just as the complementary AND function finds the *minimum*.

OR gates are basic logic gates, and are available in TTL and CMOS ICs logic families. The standard 4000 series CMOS IC is the 4071, which includes four independent two-input OR gates. The TTL device is the 7432. There are many offshoots of the original 7432 OR gate, all having the same pinout but different internal architecture, allowing them to operate in different voltage ranges and/or at higher speeds. In addition to the standard 2-input OR gate, 3- and 4-input OR gates are also available. In the CMOS series, these are:

- 4075: triple 3-input OR gate
- 4072: dual 4-input OR gate

OR gate is used in many of our real life applications. One of its applications, “Alarm circuit for car door system” is explained below

The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation.

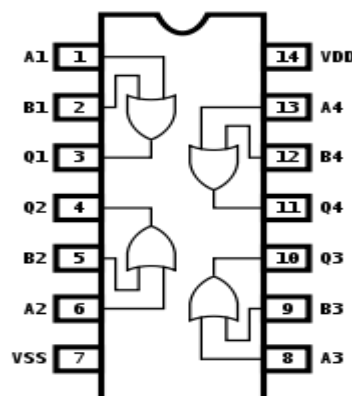


Fig:3.7:Basic Block Diagram Of Or Gate

3.7.1 APPLICATION OF OR LOGIC GATES

- The **OR gate Application** is a digital logic **gate** that implements logical disjunction – it behaves according to the adjacent truth table.
- A HIGH output (1) results if one or both the inputs to the **gate** are HIGH (1). If neither input is high, a LOW output (0) results

3.8 TRANSISTORS

A **transistor** is a semiconductor device used to amplify or switch electronic signals and electrical power. **Transistors** are one of the basic building blocks of modern electronics. It is composed of semiconductor material usually with at least three terminals for connection to an external circuit. A voltage or current applied to one pair of the transistor's terminals controls the current through another pair of terminals. Because the controlled (output) power can be higher than the controlling (input) power, a transistor can amplify a signal. Today, some transistors are packaged individually, but many more are found embedded in integrated circuits.

Austro-Hungarian physicist Julius Edgar Lilienfeld proposed the concept of a field-effect transistor in 1926, but it was not possible to actually construct a working device at that time. The first working device to be built was a point-contact transistor invented in 1947 by American physicists John Bardeen and Walter Brattain while working under William Shockley at Bell Labs. The three shared the 1956 Nobel Prize in Physics for their achievement. The most widely used type of transistor is the metal–oxide–semiconductor field-effect transistor (MOSFET), which was invented by Mohamed Atalla and Dawon Kahng at Bell Labs in 1959. Transistors revolutionized the field of electronics, and paved the way for smaller and cheaper radios, calculators, and computers, among other things.

Most transistors are made from very pure silicon, and some from germanium, but certain other semiconductor materials are sometimes used. A transistor may have only one kind of charge carrier, in a field-effect transistor, or may have two kinds of charge carriers in bipolar junction transistor devices. Compared with the vacuum tube, transistors are generally smaller and require less power to operate. Certain vacuum tubes have advantages over transistors at very high operating frequencies or high operating voltages. Many types of transistors are made to standardized specifications by multiple manufacturers.

The professor told us that in NMOS, the **source** is the small voltage, and the **drain** is the biggest voltage

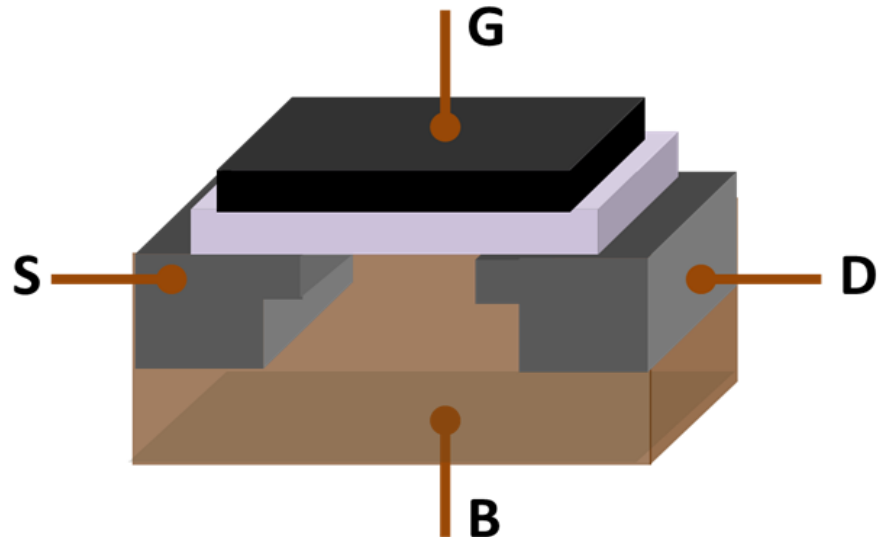


Fig:3.8:(MOSFET), Showing Gate (G), Body (B), Source (S) And Drain (D) Terminals. The Gate Is Separated From The Body By An Insulating Layer (Pink).

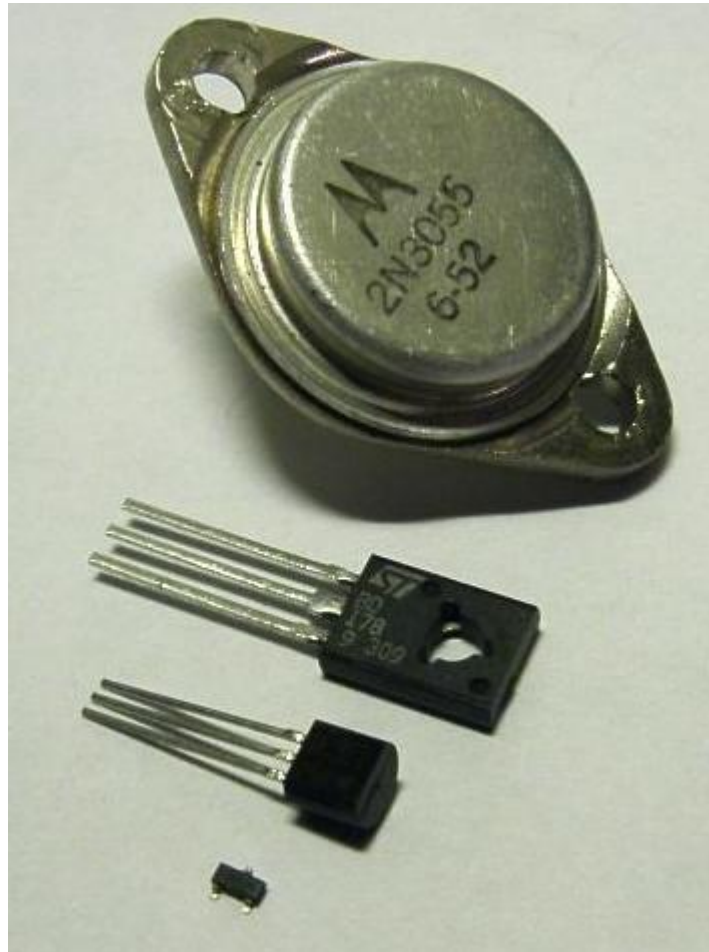


Fig:3.9:Assorted Discrete Transistors

3.8.1 Transistors Are Categorized

- Structure: MOSFET (IGFET), BJT, JFET, insulated-gate bipolar transistor (IGBT), "other types".
- Electrical polarity (positive and negative): n-p-n, p-n-p (BJTs), n-channel, p-channel (FETs).
- Maximum power rating: low, medium, high.
- Maximum operating frequency:
low,medium,high, radio (RF), microwave frequency (the maximum effective frequency of a transistor in a common-emitter or common-source circuit is denoted by the term f_T , an abbreviation for transition frequency—the frequency of transition is the frequency at which the transistor yields unity voltage gain)

- Application: switch, general purpose, audio, high voltage, super-beta, matched pair.
- Physical packaging: through-hole metal, through-hole plastic, surface mount, ball grid array, power modules (see Packaging).
- Amplification factor h_{FE} , β_F (transistor beta)^[76] or g_m (transconductance).

Hence, a particular transistor may be described as *silicon, surface-mount, BJT, n-p-n, low-power, high-frequency switch*.

3.8.2 Introduction To JFET

A popular way to remember which symbol represents which type of transistor is to look at the arrow and how it is arranged. Within an NPN transistor symbol, the arrow will Not Point iN. Conversely, within the PNP symbol, you see that the arrow Points iN Proudly

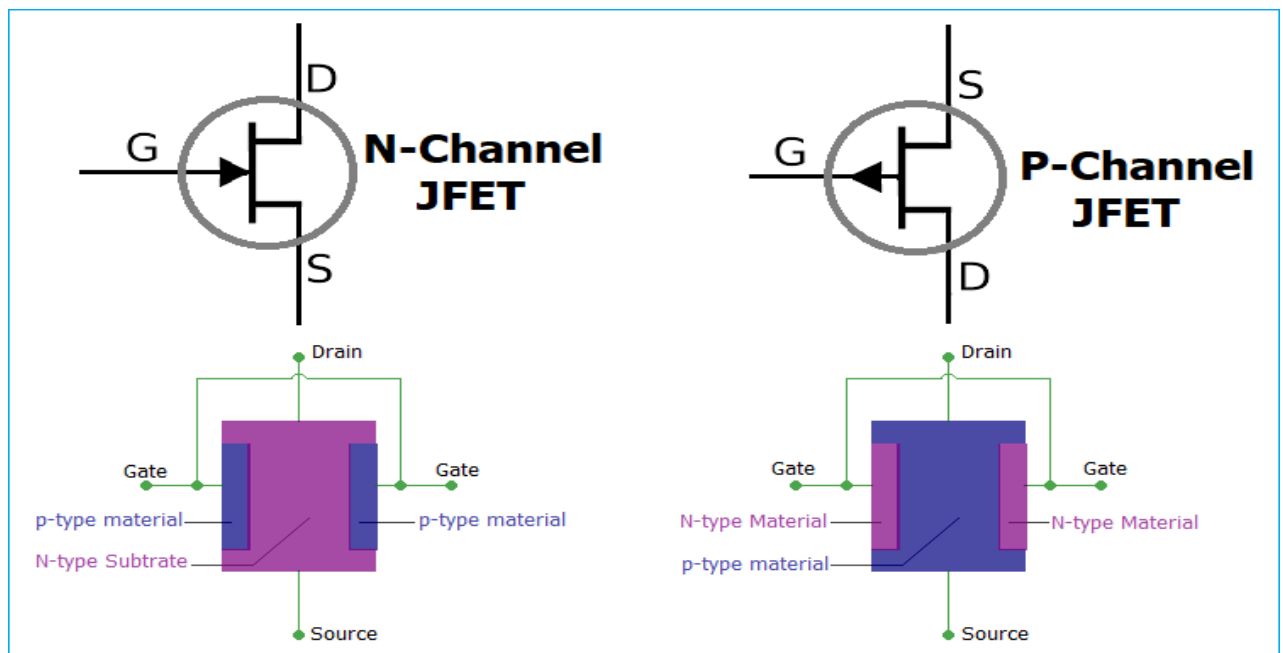


Fig:3.10:Construction ,Working And Biasing Block Diagram Of JFET

3.8.3 Introduction to BJT

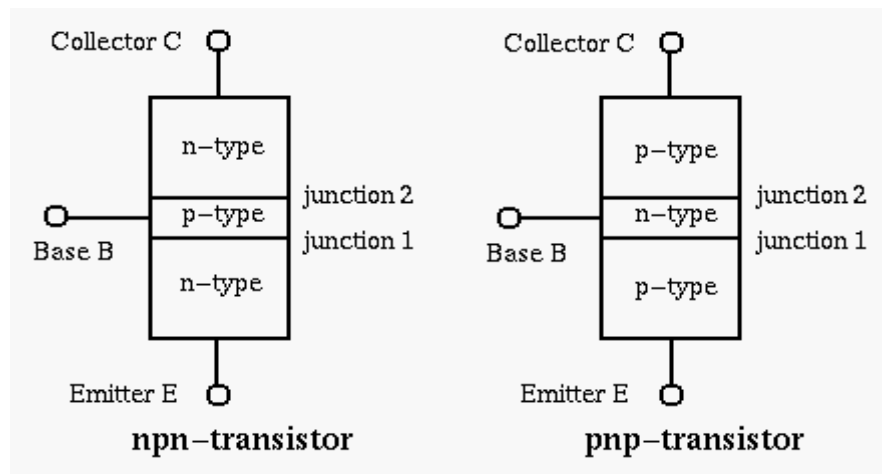


Fig:3.11:Block Diagram Of Bjt

It is an electronic component mainly used for amplification and switching purpose. As the name suggests, it is composed of two junctions called emitter-base junction and collector-base junction. Don't confuse BJT with regular transistors. A transistor is a semiconductor device, comes with three terminals that are used for external connection with electronic circuits. A transistor is termed as a trans resistor which is used as switch or gate for electronic signals. Small signals applied between one pair of its terminals are used to control much larger signals at the other pair of terminals. Actually, transistors are divided into two categories called unipolar transistor and a bipolar transistor. Bipolar junction transistor uses two charge carriers i.e. electrons and holes while unipolar transistor like FETs (Field Effect Transistors) uses only one charge carrier. I hope you are aware of another type of transistors called MOSFET. I'll try to cover each and everything related to this bipolar junction transistor, so you find all information at one place. Let's get started.

BJTs are divided into two types based on the nature and construction of the transistor. Following are two main types of the BJT.

- NPN(NEGATIVE POSITIVE NEGATIVE)
- PNP(POSITIVE NEGATIVE POSITIVE)

3.8.3.1 NPN(Negative Positive Negative)

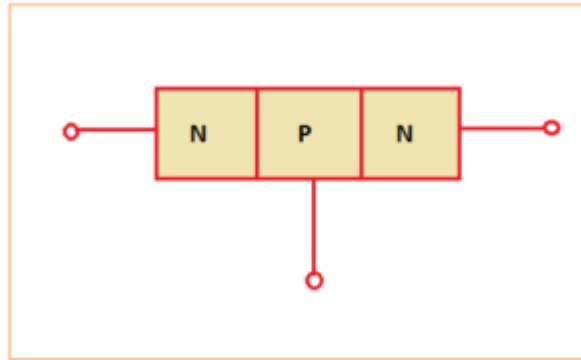


Fig:3.12:Basic Block Diagram Of Bjt-Npn

- NPN (negative-positive-negative) is a type of BJT where a P-doped layer of semiconductor exists between the two layers of N doped material.
- The P doped region represents the base of the transistors while other two layers represent emitter and collector respectively.
- NPN transistors are also called minority carrier devices because minority charge carriers at the base side are used to control large current at other terminals of the transistor.
- The current moves from an emitter to the collector where electrons act as a minority carrier at the base side.

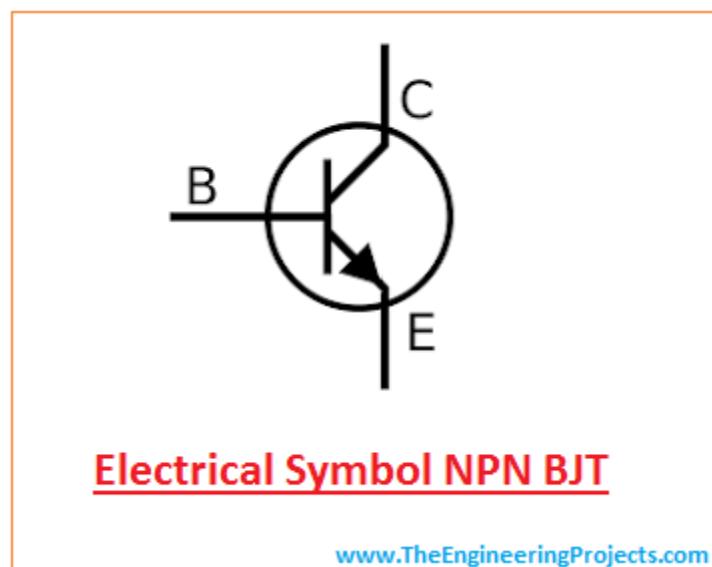


Fig:3.13:Electrical Symbol Of Npn-Bjt

3.8.3.2 PNP(Positive Negative Positive)

- PNP (positive-negative-positive) transistor is a type of BJT where N doped semiconductor layer which acts as a base, is housed between the two layers of P doped material.
- The base uses small base current and negative base voltage to control large current at the emitter and collector side and voltage at the collector side is larger than the voltage at the base side.
- In PNP transistor current direction and voltage polarities are reversed as compared to NPN transistors.

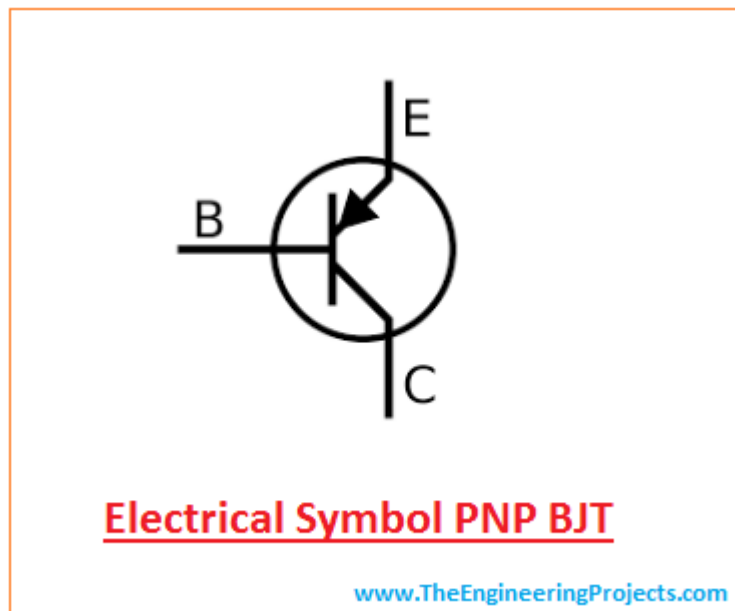


Fig:3.14:Electrical Symbol Of Pnp-Bjt

- PNP transistors work in a similar way like NPN transistor with some exception i.e. holes are diffused through the base from an emitter and are collected by the collector.
- This transistor is rarely used for applications as conduction carried out by the movement of electrons is considered fast and holds more value as conduction by movement of holes.

3.8.4 Mosfet(Metal Oxide Semiconductor Field Effect Transistor)

The metal–oxide–semiconductor field-effect transistor (MOSFET, MOS-FET, or MOS FET), also known as the metal–oxide–silicon transistor (MOS transistor, or MOS), is a type of field-effect transistor that is fabricated by the controlled oxidation of a semiconductor, typically silicon. It has an insulated gate, whose voltage determines the conductivity of the device. This ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. The MOSFET is by far the most common transistor, and the basic building block of most modern electronics. The MOSFET accounts for 99.9% of all transistors in the world.

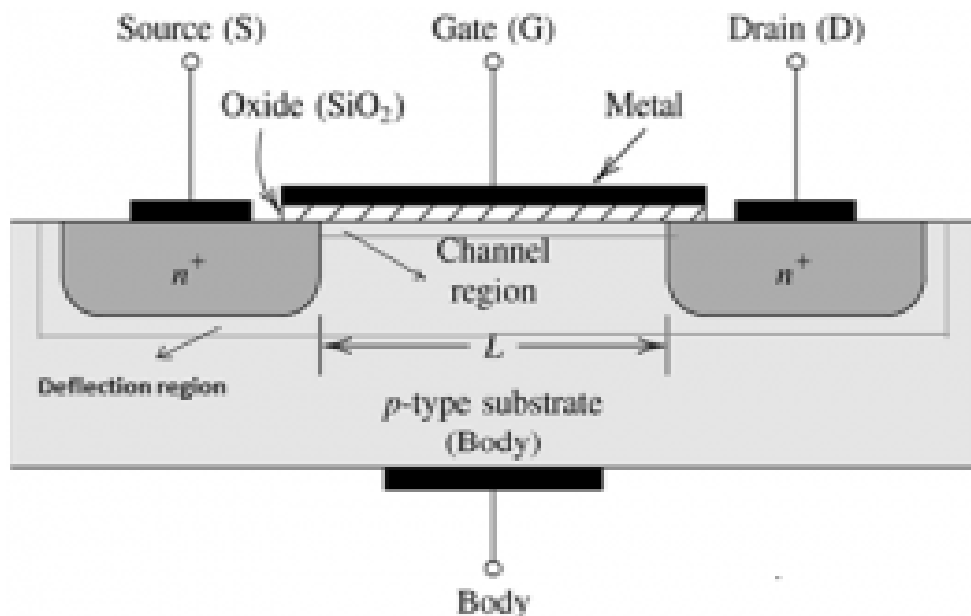


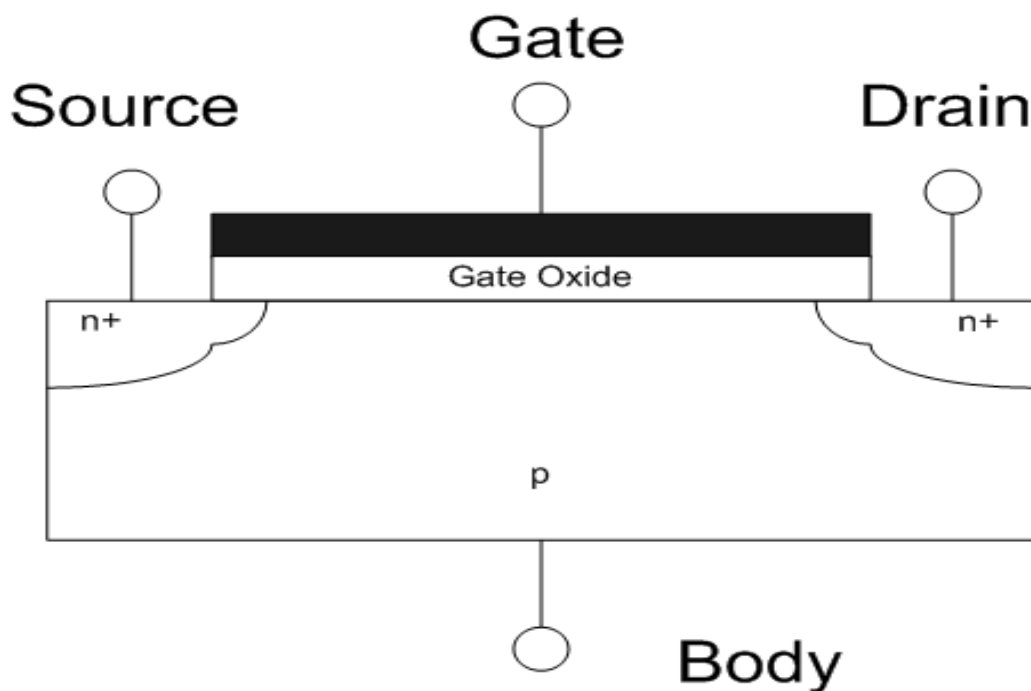
Fig:3.15:Basics Working Principle Of Mosfet

3.8.4.1 FET(Field Effect Transistor)

FETs are devices with three terminals: source, gate, and drain. FETs control the flow of current by the application of a voltage to the gate, which in turn alters the conductivity between the drain and source. FETs are also known as unipolar transistors since they involve single-carrier-type operation. The very basics are that the gate, source and drain are terminals of a Field Effect Transistor (FET), as opposed to the bipolar transistor where the equivalent terminals are the emitter, base and collector.

The gate is the terminal that is used to control the flow of current through the FET. A small gate current can control a much larger current through the device, resulting in amplification.

The source and drain are the terminals used to connect the FET to the power supply.



**FIG:3.16 : Cross-Sectional View Of A Field-Effect Transistor,
Showing Source, Gate And Drain Terminals**

3.8.5 Advantages

The key advantages that have allowed transistors to replace vacuum tubes in most applications are

- No cathode heater (which produces the characteristic orange glow of tubes), reducing power consumption, eliminating delay as tube heaters warm-up, and immune from cathode poisoning and depletion.
- Very small size and weight, reducing equipment size.

- Large numbers of extremely small transistors can be manufactured as a single integrated circuit.
- Low operating voltages compatible with batteries of only a few cells.
- Circuits with greater energy efficiency are usually possible. For low-power applications (for example, voltage amplification) in particular, energy consumption can be very much less than for tubes.
- Complementary devices available, providing design flexibility including complementary-symmetry circuits, not possible with vacuum tubes.
- Very low sensitivity to mechanical shock and vibration, providing physical ruggedness and virtually eliminating shock-induced spurious signals (for example, microphonics in audio applications).
- Not susceptible to breakage of a glass envelope, leakage, outgassing, and other physical damage.

3.8.6 Limitations

Transistors have the following limitations:

- They lack the higher electron mobility afforded by the vacuum of vacuum tubes, which is desirable for high-power, high-frequency operation — such as that used in over-the-air television broadcasting.
- Transistors and other solid-state devices are susceptible to damage from very brief electrical and thermal events, including electrostatic discharge in handling. Vacuum tubes are electrically much more rugged.
- They are sensitive to radiation and cosmic rays (special radiation-hardened chips are used for spacecraft devices).
- In audio applications, transistors lack the lower-harmonic distortion — the so-called tube sound — which is characteristic of vacuum tubes, and is preferred by some.

CHAPTER 4

EXPERIMENTAL OR MATERIALS AND METHODS;ALGORITHMS

In the existing work the USR is designed using a Logic gates and 4*1 multiplexer. In the proposed work the USR is designed using a modified 2*1 multiplexer

Addition forms the basis of digital computer systems. Three novel gate level full adder designs, based on the elements of a standard cell library are presented in this work: one design involving XNOR and multiplexer gates (XNM), another design utilizing XNOR, AND, Inverter, multiplexer and complex gates (XNAIMC) and the third design incorporating XOR, AND and complex gates (XAC). Comparisons have been performed with many other existing gate level full adder realizations. Based on extensive simulations with a 32-bit carry-ripple adder implementation; targeting three process, voltage and temperature (PVT) corners of the high speed (low Vt) 65nm STMicroelectronics CMOS process, it was found that the XAC based full adder is found to be delay efficient compared to all its gate level counterparts, even in comparison with the full adder cell available in the library. The XNM based full adder is found to be area efficient, while the XNAIMC based full adder offers a slight compromise with respect to speed and area over the other two proposed adders.

4.1 CONVENTIONAL FULL ADDER

Which has lesser delay compared to the existing design minimum sum-of-products (MSOP) form of a Boolean function can be obtained using a standard two-level logic minimize Espresso Though the logic realization corresponds to an AND-OR two-level logic format, inverting buffers required for the primary inputs have to be separately accounted for. A 1-bit full adder, based on MSOP forms for sum and carry outputs, is shown in . A traditional full adder implementation based on two half adder modules is shown in . The full adder design incorporating logic sharing, as described in is depicted by . A slight modification is done, in that the NOR gate followed by the NOT gate to realize the sum output in the original circuit has been replaced by an OR gate. A binary full adder realization mainly employing 4:1 MUX is highlighted in . Due to the non-availability of appropriate inverted input MUX cells to directly implement the XOR

functionality, inverters were used in addition to the standard MUX cells to facilitate XOR logic realization. Excepting this, the rest of the full adder logic appears similar to that of , as shown in . A full adder design employing two stages of XNOR gates for the sum logic, while that employing two successive stages of XOR gates for the sum logic is depicted by . The centralized full adder design mentioned in and is portrayed by . The design of a gate level binary full adder , based on Shannon's decomposition theorem and multiplexing control input technique for the carry and sum outputs, is given in . The internal details of the full adder cell, which forms a part of the commercial library, could not be commented upon in this article and so only the block schematic of the same is given below in. The inputs and outputs are listed therein. Three full adder designs are proposed in this work. The first design employs only XNOR gates and 4:1 MUX. However, one of the two non-inverting 2:1 MUX has an inverted input. This design is portrayed by and shall be referred to as XNM based full adder. The second design employs XNOR, AND, NOT, inverted input 4:1 MUX and complex gates (XNAIMC based full adder), as shown in . The complex gate used is the AO12 cell, which performs the function, $f = xy + z$, where 'x' and 'y' are the inputs to the AND logic and 'z' is the separate input to the OR logic. The last adder design is a refinement of the full adder design mentioned, in that, the AND gate of the second half adder module and the OR gate associated with the carry output are replaced by a single complex gate, namely AO12 cell. This design, referred to as XAC based full adder, is shown in . Amongst all the other gate level full adders, the XAC based full adder realization was found to be the fastest. This is substantiated by the maximum operating speed values, highlighted in . The expressions for the sum and carry outputs of the XAC based full adder are as follows. The Boolean product term, $(a \oplus b) \cdot c_{in}$ in (4), has been implemented by the complex gate, AO12

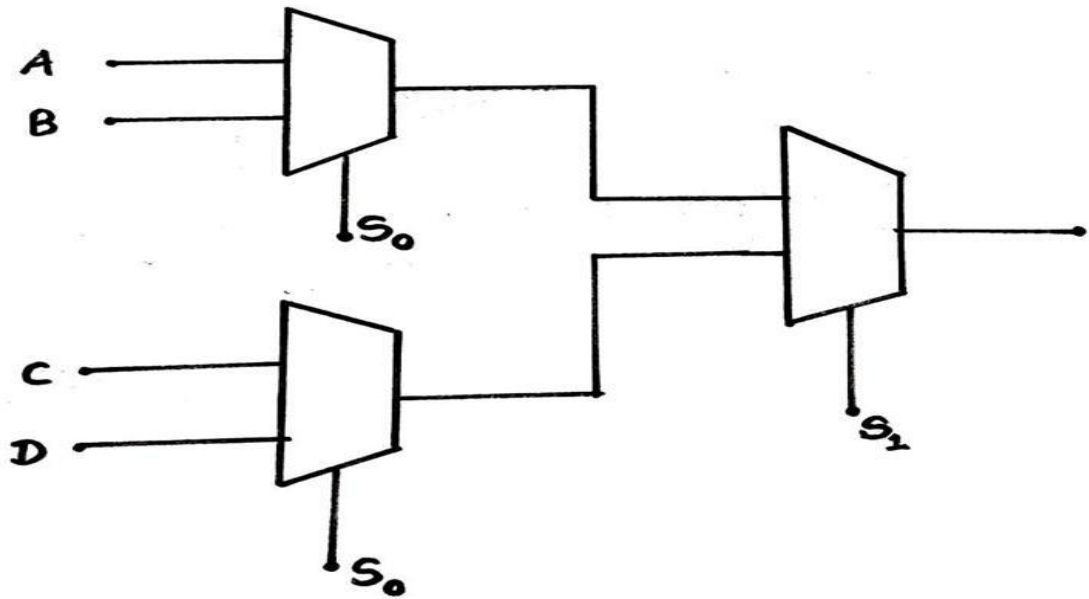


Fig:4.1:Conventional Full Adder

4.2 FULL ADDER BASED EXOR

The existing multiplexer will be modified, such that the proposed architecture will be more efficient in terms of average power, speed and energy consumption. Proposed 4×1 multiplexer has been designed GDI technique. Gate Diffusion Input (GDI) a new technique for low power combinational digital circuit design is defined. The existing Universal Shift Register has been designed and analysed using conventional Logic Gates and conventional 4×1 multiplexer.

The proposed low power 4×1 multiplexer using GDI Technology along with proposed low power Full Adder has been used in the proposed Universal Shift Register to analyse its performance. In this proposed architecture of 4×1 Multiplexer using GDI Technology and low power Full Adder which has been used to reduce the power and delay of the Universal Shift Register

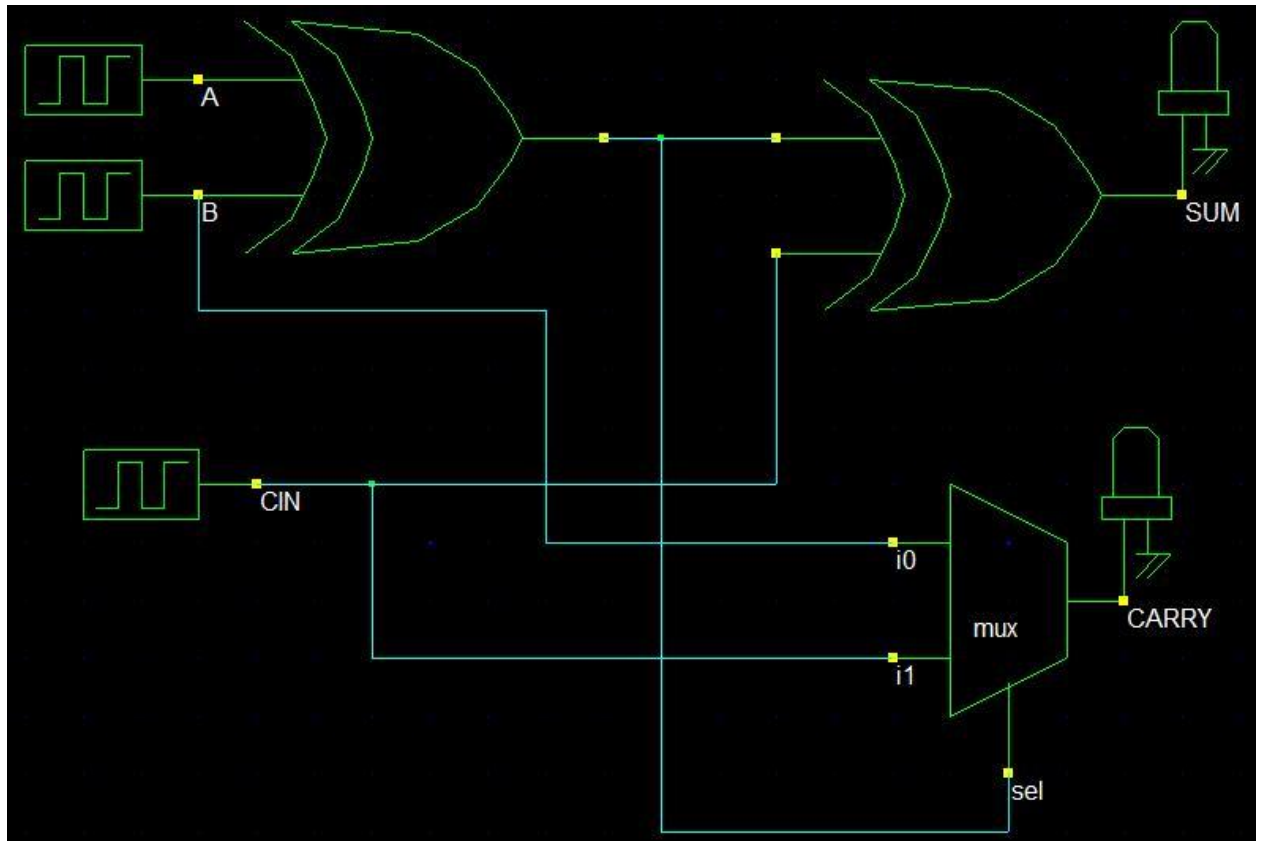


Fig:4.2:Exor-Mux Fulladder

4.3 GDI BASED EXOR-MUX FULL ADDER

There are various low power technique were present nowadays in which GDI is also one of them. Nowadays a GDI is the most commonly used technique for the reduction of power as it reduces the switching of output. Also a GDI technique is used to reduce the number of transistor for the reduction in area of chip. The most commonly cell in a GDI technique is an inverter cell which is formed by the combination of a single PMOS and NMOS. Here a single input is provided to the gate terminal of both and then output is taken out. As shows in the basic 4×1 multiplexer formed by the help of GDI technique

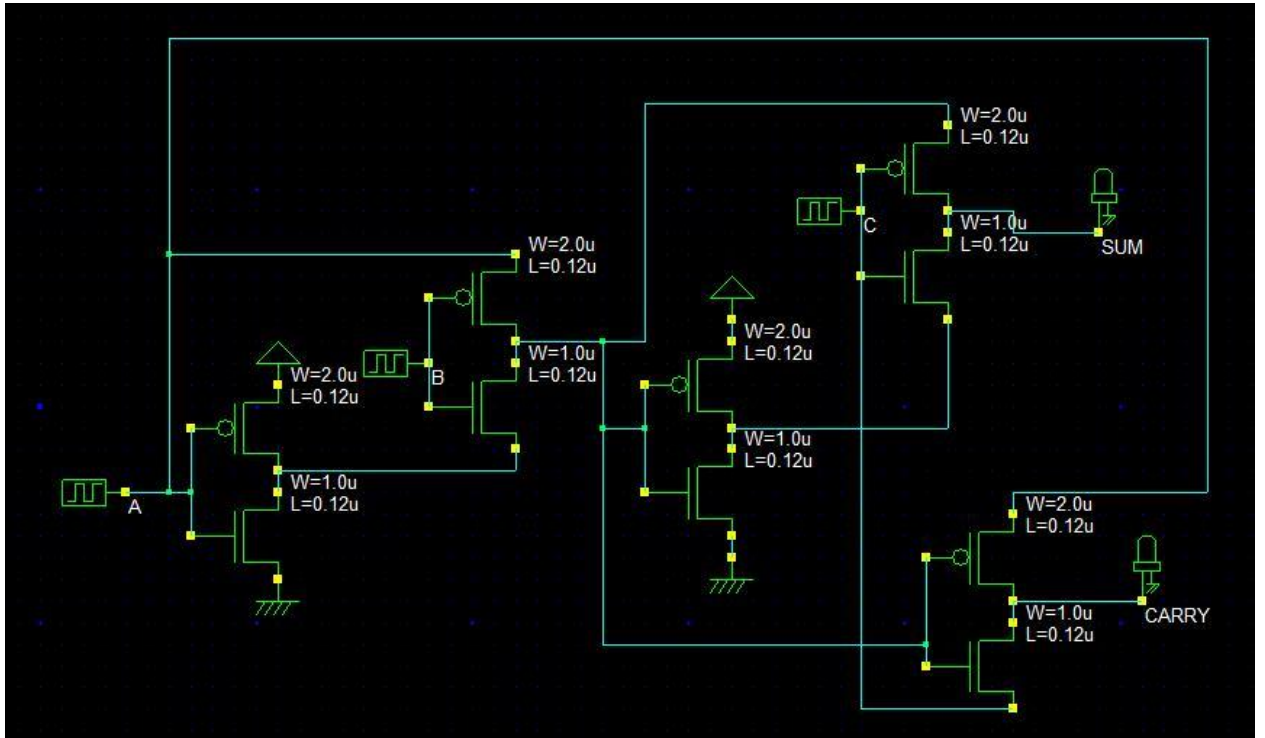


Fig:4.3:Gdi Based Exor-Mux Fulladder

This technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. Performance comparison with traditional CMOS techniques is presented, with respect to the, delay and power dissipation, showing advantages of GDI as compared to other methods. A variety of logic gates have been implemented in 130 nm technology to compare the GDI technique with CMOS. This modified 4×1 multiplexer using GDI technique is used for the 4×1 multiplexer. Now, the modified 4×1 multiplexer .

CHAPTER 5

RESULTS AND DISCUSSION ,PERFORMANCE ANALYSIS

The existing and proposed architecture are simulated by using H-spice simulator. Output of the existing USR and proposed USR are analysed from the results and it is concluded that the proposed architecture reduces the delay compared with the existing system. The existing and proposed design are simulated in synopsis H-spice tool.

The design has been evaluated in 130 nanometer technology. The spice code of the schematic design can be viewed in edit NL in H-spice tool. It is simulated. If there is any error, it shows job aborted which then can be even modified. The avanwaves in H-spice tool shows the simulated output waveforms

5.1 CONVENTIONAL FULL ADDER

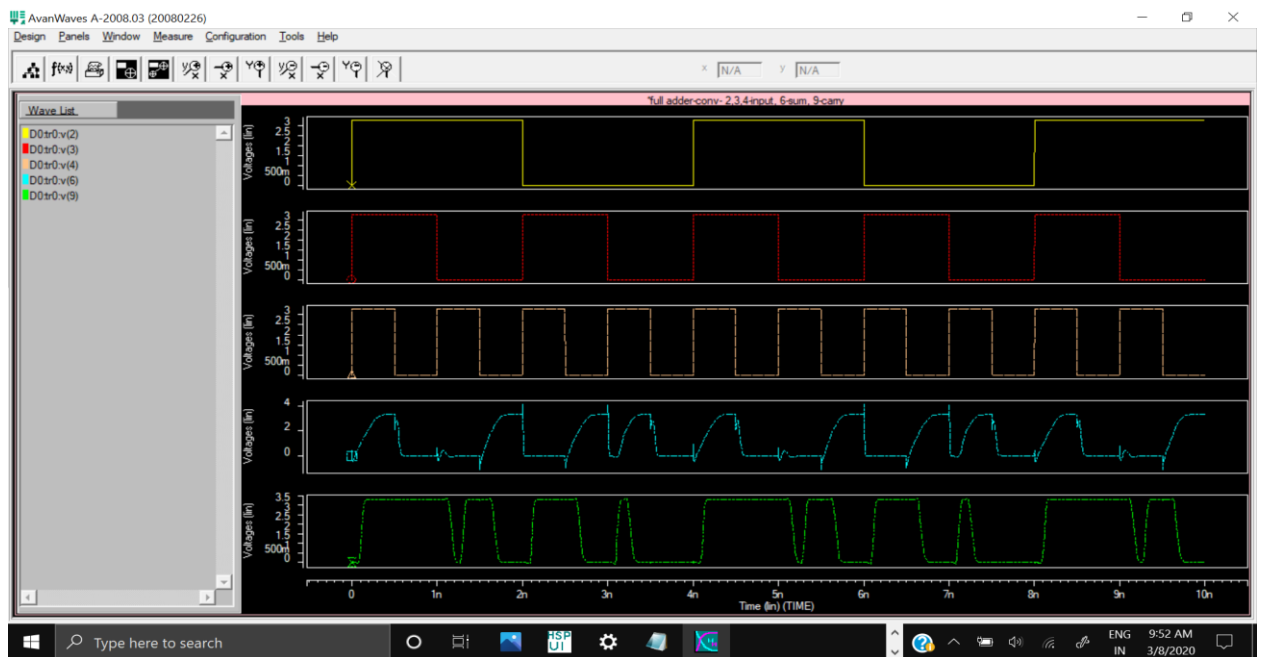


Fig:5.1:Graph of Conventional Full Adder

From here we got,

avgpower	peakpower	temper	alter#
1.276e-04	1.949e-02	25.0000	1.0000

5.2 GDI BASED XOR MUX

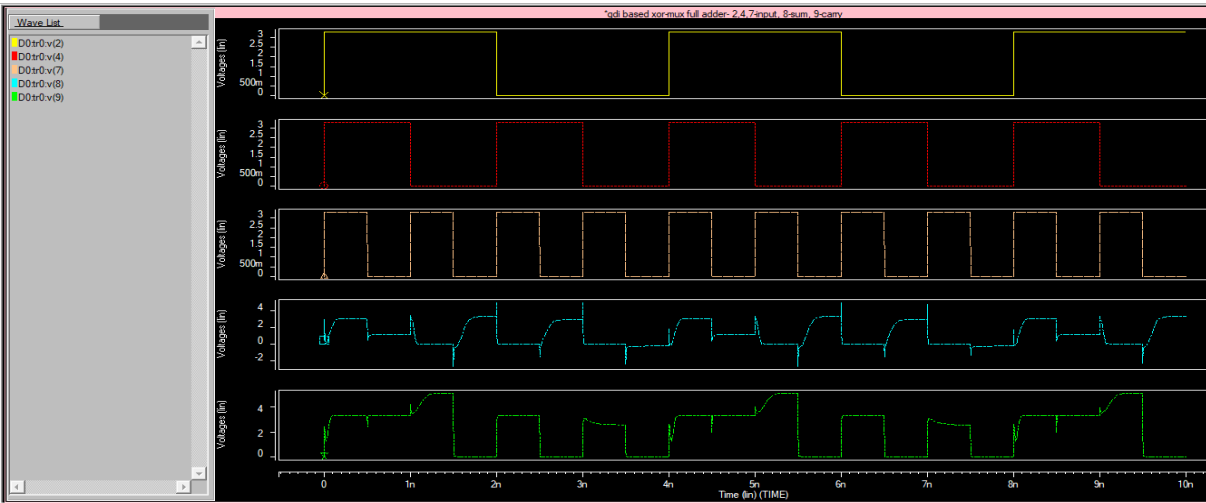


Fig:5.2:GDI Based XOR-MUX Full Adder

From here we got,

avgpower	peakpower	temper	alter#
4.049e-03	2.277e-05	25.0000	1.0000



Fig:5.3:Proposed XOR MUX

avgpower	peakpower	temper	alter#
2.705e-02	1.327e-04	25.0000	1.0000

Table : 5.1 : Average power,Peak Power,Temper

S.No.		Avg Power	Peak Power	Temper
1	CONVENTIONAL FULL ADDER	1.276e-04	1.949e-02	25.0000
2	GDI BASED EXOR-MUX FULLADDER	2.277e-05	4.049e-03	25.0000
3	EXOR-MUX FULLADDER	1.327e-04	2.705e-02	25.0000

Table5.2 : GDI Based Exor-Mux Fulladder

CIRCUIT	AVERAGE POWER (μW)	DELAY (pS)	PDP (aJ)
Conventional full adder	132.7	117.53	15,596.23
Proposed-1 (CMOS Xor-mux full adder)	127.6	114.34	14,589.78
Proposed-2 (GDI xor-mux fulladder)	22.7	37.76	857.15

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

We have proposed a new efficient Universal Shift Register using low power XOR-MUX Full adder based computational block for low power architecture and modified 4×1 multiplexer, which gives better response in terms of speed in comparison to the conventional Universal Shift Register. We have achieved a design of a proposed Universal Shift Register which is faster and has reduced the delay of the conventional USR considerably. Since our objective was to reduce the delay of the USR and it has been reduced, hence we achieved our objective. So, we practically saw that the proposed USR with modified multiplexer (using gdi technology) is much more efficient.

6.2 FUTURE SCOPE

Shift register can be used for the storage or the transfer of binary data. So, improving its performance can improve the overall efficiency of the system. Future work can be concentrated on area efficiency of the Logic gates and multiplexer and can obtain better efficiency in terms of area. This proposed universal shift register can be implemented and can obtain better efficiency.

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