

CMOS TRANSCONDUCTANCE LNA INTEGRATION OF VITAL SIGN PROCESSING RECEIVER WITH CLUTTER ELIMINATION USING SC CHEBYSHEV LPF

Submitted in partial fulfillment of the requirements for the award of
Bachelor of Engineering degree in Electronics and Communication Engineering

By

KALICHETI SAI NANDHAN REDDY(37130179)



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING**

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119

APRIL - 2021



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JEPPIAAR NAGAR, RAJIV GANDHI SALAI,

CHENNAI- 600119

www.sathyabama.ac.in



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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of KALICHETI.SAI NANDHAN REDDY(37130179) , who carried out the project entitled“**CMOS TRANSDUCTANCE LNA INTEGRATION OF VITAL SIGN PROCESSING RECEIVER WITH CLUTTER ELIMINATION USING SC CHEBYSHEV LPF**” under my supervision from September 2019 to April 2020.

Internal Guide

Mr. K.T ILAYARAJAA, M.E.,(Ph.D)

Head of the Department

Dr.T.RAVI, M.E.,Ph.D

Submitted for Viva voce Examination held on_____

Internal Examiner

External Examiner

DECLARATION

I, KALICHETI.SAI NANDHAN REDDY(Reg.No: 37130179) hereby declare that the Project Report entitled **CMOS TRANSCONDUCTANCE LNA INTEGRATION OF VITAL SIGN PROCESSING RECEIVER WITH CLUTTER ELIMINATION USING SC CHEBYSHEV LPF** is done by me under the guidance of Mr. K.T.ILAYARAJAA, M.E.,(Ph.D) and at SATHYABAMA INSTITUTE OF SCIENCE AND TECHNOLOGY is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

DATE:

1.

PLACE:

SIGNATURE OF THE CANDIDATES

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ABSTRACT

This project is about a critical signal processing circuit with no automatic signal processing or ultra-wideband (UWB) pulse-based radar algorithm for simultaneous dc/near-dc exclusion and out-of-band interference removal. As a secure and balanced pseudo resistor applied under a servo feedback mechanism in a critical signal receiver of the sensing radar, the proposed inherent self-balancing MOS diode (SBMD) operates as High-Pass Filter (HPF) with minimal corner frequency below 0.5 Hz which suppresses undesired clutters of reflected signals and input dc-offset voltages from underlying circuit offsets. A third-order switched-capacitor (SC) Chebyshev low-pass filter (LPF) with trans-conductance low-noise amplifier (LNA) and leap-frog topology was embraced as the next step to remove out-band noise, create an integrated band-pass response vital-sign transmission circuit and incorporate it into a radar module to verify its viability. This study was finally established at 130 nm and 45 nm CMOS Technology in Tanner EDA.

1. INTRODUCTION

1.1 Objective

This archive contains VLSI reference data, as well as project and programming execution.

1.2 References

- RTL hardware design utilizing VHDL coding for Efficiency and Portability and also Adaptability
- circuit Designing with VHDL Volnei A. Pedroni
- spartan-6 family overview
- Model sim User's manual software version 6.5 b

1.3 Abbreviations

VLSI	very large scale integrated circuits
HDL	hardware description language
VHDL	vhisc hardware description language
VHISC	very high speed Integrated circuits
IEEE	institute of electrical and electronic engineers
VITAL	VHDL initiative towards ask libraries
RTL	Register Transfer Level
WAVES	waveform and vector exchange to support the design and test verification
PLA	Programmable Logic Array
PAL	Programmable Array Logic
CPLD	complex programmable logic devices
CLB	configurable logic blocks
ISE	Integrated Software Environment
EDA	electronic design automation
FPGA	Field-programmable gate array

2. Introduction to VLSI design:

2.1 What is VLSI?

"Very Large Scale Integration" is the abbreviation for "Very Large Scale Integration." In this area, it entails cramming ever-increasing numbers of logic devices into ever-smaller spaces. Circuits that would have taken up a lot of room on a board can now be squeezed into a compact space just a few millimetres across thanks to VLSI! VLSI circuits are being used in computers, cars, digital cameras, and cell phones, among other things. All of this necessitates great knowledge on a variety of levels.

Working with VLSI Circuits

The way common blocks like latches & gates are implemented varies from what students have already seen, but the behaviour remains the very same. All of this downsizing necessitates a new set of considerations. Actual implementations, as well as architecture, necessitates great knowledge and consideration.

Circuit Delays: Large complex circuits operating at higher frequencies face a major challenge: signal propagation delays across gates and wire, even for areas as small as a few micrometers across, the processing speed is so fast that by the time the delays accumulate, they can also match the clock speeds.

Power: Increased power consumption is an other effect of higher operation frequencies. This has two effects: devices consume batteries more quickly, and heat dissipation rises. Heat, when combined with the fact that surface areas have shrunk, poses a serious challenge to the circuit's stability.

Layout: Circuit part layout is a task that is common to all branches of electronics. What makes our case unique is that we have several options for doing so: vast layers of different materials on the same Silicon(Si), various configurations regarding smaller parts for the same portion, and much more ,the decision among those two will be made based

on how the circuit components are laid out. Layout may also influence VLSI chip fabrication, making it easier or more difficult to implement components on silicon.

Introduction to VHDL

A digital framework can be approached from a variety of perspectives and abstraction levels. At the desired level of abstraction, an HDL should faithfully and accurately model and define a circuit, whether it is already designed or under construction, from either the structural or behavioural perspectives. Since HDLs are modelled after hardware, they have completely different semantics and applications than conventional programming languages.

Limitations of traditional programming languages

Nowadays, there are many computer programming languages available, ranging from Frontend to C to Java. Regrettably, they are insufficient to design digital hardware. Examining the evolution of a language will help you understand their limits. The syntax as well as the semantics of a programming language define it. The semantics is the "context" associated with language constructs, while the syntax includes the grammatical rules used to write a programme. When creating a new programming language, the designers first research the characteristics of the underlying processes before creating syntactic constructs and related semantics to model and express these features.

A sequential method is modelled in most common general-purpose programming languages, such as C. Operations are carried out in this method in a sequential order, one at a time. Since the outcome of one operation always depends upon the outcome of another operation, the order in which operations are carried out cannot be changed at will. The sequential process model has two significant advantages. At a high stage, it aids the human thought process in the generation of a step-by-step algorithm. The sequential method resembles the operation of a simple computer model at the implementation stage, allowing for efficient translation from an algorithm to machine instructions.

Digital hardware, conversely, has somewhat different characteristics than sequential hardware. Smaller parts make up a standard digital device, with custom wiring connecting the input as well as output ports of these parts. When a signal changes, the sections that are attached to it are activated, and a new set of operations is started as a result. These operations are carried out in parallel, and each one takes a certain amount of time, which represents the propagation delay of a particular part, to complete. After each component is finished, the value of respective output port is updated. If the value is modified, the output signal activates all associated components, triggering a new round of operations. The relations of components, concurrent operations, and the principle of propagation delay and timing are all highlighted in this overview of digital systems. Traditional programming languages' sequential model are not able to get the features of the digital hardware, necessitating the use of special languages (e.g., HDL etc) that are developed to design the digital hardware.

VHDL provides facilities for explaining the logical structure and operation of digital systems at various levels of abstraction, from device to gate. It's designed to be used as a modelling language for specification and simulation, among other things. If we limit ourselves to a subset that can be automatically converted into hardware, we can also use it for hardware synthesis.

The very high speed integrated circuits (VHSIC) software of the US government gave birth to VHDL. Throughout the curriculum, it has become clear that a common or standard language for providing the structure and functions of integrated circuits was needed (ICs). The Vhisc hardware description language shortly (VHDL) is created as a result. It was later improved under the direction of the institute of electrical and electronic engineers that is (IEEE) and acquired as IEEE standard 1076, standard VHDL language reference manual, in the year 1987. VHDL-87 is the name given to the first standard edition of the language.

Following the initial release, a number of extensions were created to help with different design and modelling needs. Several IEEE standards describe these enhancements:

- i. IEEE standard 1076.1-1999, VHDL analog and mixed signal extensions (VHDL-AMS): gives the extension for analog and mixed-signal modeling.
- ii. VHDL mathematical or arithmetical packages, IEEE standard 1076.2-1996, include additional mathematical functions for real as well as complex numbers.
- iii. IEEE standard 1076.3-97, synthesis sets, which offers arithmetic operations over a set of bits.
- iv. ASK libraries initiative in VHDL (VITAL), IEEE standard 1076.4-1995 it specifies a method for adding enhanced timing information to ASIC cells.
- v. IEEE standard 1076.6-1999, VHDL Register transfer level shortly (RTL) synthesis: defines a subset that is applicable for synthesis.
- vi. IEEE standard 1164 was published in 1993. (std-logic1164) Multivalve logic framework for VHDL model interoperability: specifies new data types for multivalve logic architecture.
- vii. VHDL waveform and vector exchange to aid design and test verification (WAVES): explains how to exchange data or information in a simulation environment using VHDL (IEEE standard 1029.1-1998).

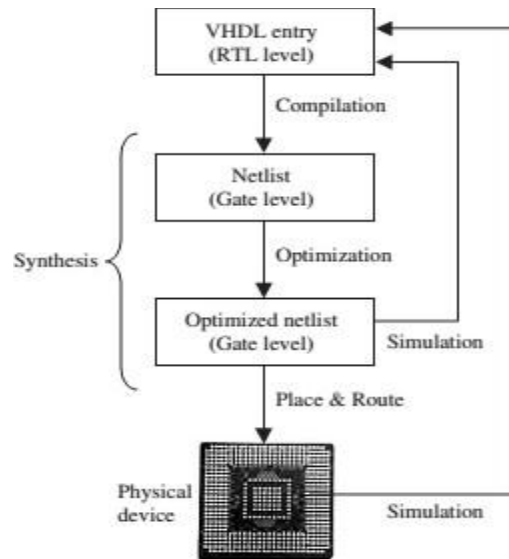


Fig.1: Flow of VHDL design

Electronic Design Automation

VHDL circuit synthesis, implementation, and simulation can be done with a variety of EDA also known as (Electronic Design Automation) methods. Some tools (e.g., Altera's Quartus II, which enables the synthesis of VHDL code onto Altera's CPLD/FPGA chips, or Xilinx's ISE suite, for Xilinx's CPLD/FPGA chips) are ordered as part of a vendor's design suite. Other instruments (for example, synthesizers) may be offered by specialist EDA companies in addition to being ordered as part of design suites (Mentor Graphics, Synopsis, Simplicity, etc.). Leonardo Spectrum is an example of the above category (a synthesiser from mentor graphics), simplify (a synthesiser from simplicity), as well as Model sim (a simulator software from model technology, a mentor graphics company). The designs which are published in the book are synthesised on Altera or Xilinx CPLD/FPGA devices (appendix A). ISE was used in conjunction with ModelSim, and MaxPlus II was used in conjunction with Advanced.

Quartus II or Synthesis Software Leonardo Spectrum was occasionally used as well. We agreed to standardize the visual presentation of all simulation graphs, despite the fact that a variety of Tanner EDA tools have been used for executing and evaluating the

examples provided in the design. The waveform editor in MaxPlus II was used because of its clean appearance. Newer simulators, such as ISE modelsim simulator and quartus II simulator, have a much wider range of features, allowing for more refined timing analysis, for example. As a result, certain methodologies have been used to verify the detailed points of each design.

Field programmable gate array

The Field programmable gate array shortly (FPGA) is a type of semiconductor based system that can be programmed after manufacturing by the consumer or designer so the term "field programmable." To programme an FPGA, one should use a logic circuit or use a source code in hardware description language shortly(HDL) environment to describe how they want that chip to operate (HDL). FPGAs can perform any logical feature that an application specific integrated circuit also called as ASIC can, but for certain applications, the ability to customize the functionalities after shipping is beneficial.

FPGA's have programmable logical blocks as well as a reversible hierarchy of interconnections that allow those blocks being "wired together," similar to an one chip programmable breadboard. Complex combinational functions can be performed with logic blocks, or simple logical gates namely AND as well as XOR gates can be used. The logic blocks in most FPGAs often contain memory elements, which are usually flip-flops or larger memory blocks.

FPGAs are typically slow than their fixed ASIC counterparts of any given semiconductor operation. They often consume more energy and have less functionality for the same circuit complexity. Short time to market, opportunity to re program in the field itself to correct bugs, and lower non-recurring engineering costs are among their benefits. Vendors may take a middle ground by building their hardware on standard FPGAs but manufacturing the final version so that it can't be changed until the design is committed.

Xilinx has launched a field programmable gate array also called as (FPGA) systems in the mid-1980s. They are designed for the implementation of high-performance, large-size circuits and differ from CPLDs in architecture, storage technology, number of built-in features, and cost.

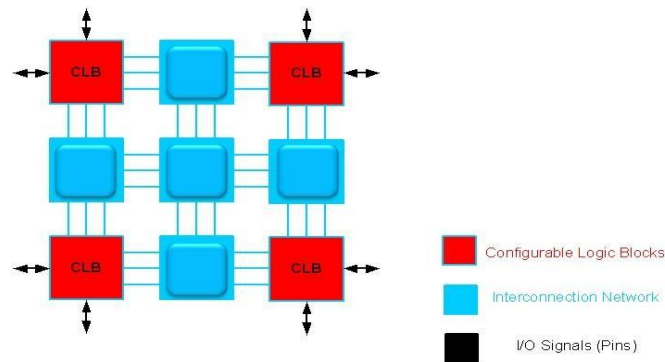


Figure 1 : FPGA Architecture

Figure 2 gives the fundamental architecture of an FPGA. It is made up of a matrix of CLBs (Configurable Logic Blocks) linked by a switch matrix array.

A CLB's internal architecture differs from that of a PLD. First, rather than using AND gates followed by OR gates (as in SPLDs), SOP expressions are usually implemented using a LUT (lookup table). Furthermore, the number of flip-flops in an FPGA is much higher than in a CPLD, allowing for the development of more complex sequential circuits. FPGA chips provide SRAM memory, clock multiplication (PLL or DLL), PCI interface, and other characteristics in comparison to JTAG support and interface to various logic levels. Multipliers, DSPs, and microprocessors are all dedicated blocks on some chips.

Another significant distinction between an FPGA and a CPLD is the interconnect storage. Though CPLDs are non-volatile (they use antifuse, EEPROM, Flash, and other technologies), most FPGAs use SRAM and are therefore volatile. Since FPGAs have a higher number of programmable interconnections, but need an external ROM, this approach saves space and reduces chip cost. Non-volatile FPGAs (with antifuse) are available, which may be beneficial when reprogramming is not needed.

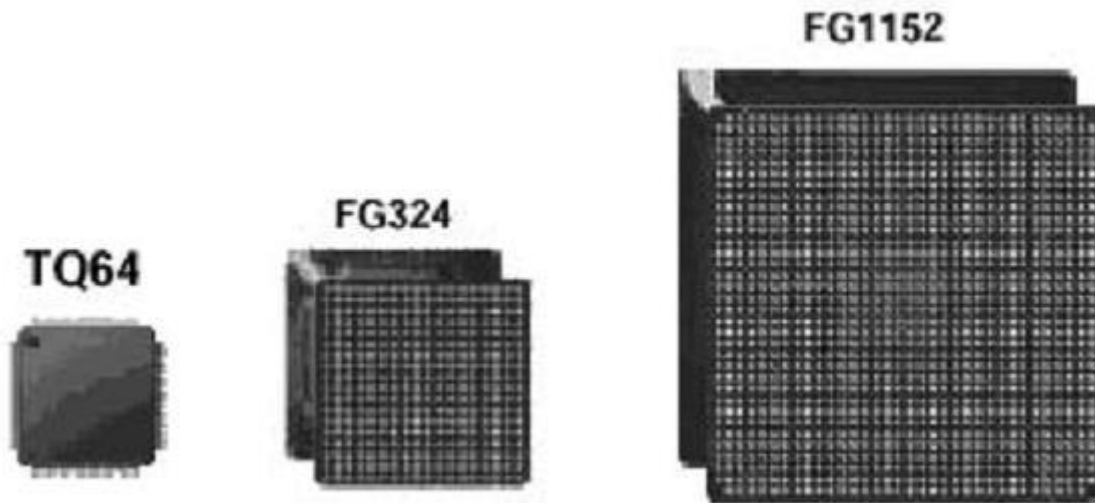


Figure 2 : Examples of FPGA Packages

FPGAs can be extremely complex. Chips having nine copper layers also over 1,000 I/O pins made with state-of-the-art 0.09mm CMOS technology are currently available. Figure A6 depicts a few examples of FPGA packages, including one of the smallest (64 pins) on the left, a medium-size package (324 pins) in the centre, and a massive package (1,152 pins) on the right. FPGAs are made by a number of firms, including Xilinx, Actel, Altera, and Fast Logic. Since all Xilinx FPGAs store the interconnects in SRAM, they are reprogrammable but volatile (thus requiring external ROM). Actel FPGAs, conversely, are basically non-volatile (they use anti-fuse) but not reprogrammable (except one family, which uses Flash memory). Since each solution having its own advantages and drawbacks, the specific application will determine which chip design is best.

3. Project

3.1 Base Paper Abstract:

The Ultra Wideband shortly (UWB) pulse based radar system, this brief provides a crucial sign processing circuit for the synchronous dc as well as near dc removal and out of band interference elimination without any digital signal processing shortly DSP or an algorithm assistance. In an imperative sign beneficiary of the detecting radar, an inherent self adjusted MOS diode shortly (SBMD) is proposed as a steady and adjusted pseudo resistor is applied under a servo feedback circle to go about as a high-pass channel (HPF)

with a ultralow corner recurrence lesser than 0.5 Hertz for taking out undesired messes of the reflected signals and information dc-counterbalance voltages from inborn circuit balances. To smother out-band clamors, a third order exchanged capacitor (SC) Chebyshev low-pass channel (LPF) with leap frog methodology was utilized as the subsequent step, resulting in an integrated vital-sign processing circuit with band pass frequency response and its incorporation into a radar module to verify its viability.

3.2 Literature survey:

- • “A CMOS transceiver with a 1.1-mW-RX-81.4-dBm sensitivity for Bluetooth low energy,” IEEE Trans. Microw.Theory Techn., J. Masuch and M. Delgado-Restituto, A completely integrated low power 130nm CMOS transceiver customised to the Bluetooth low energy (BLE) standard is presented in this paper. The receiver uses a zero-IF passive front-end architecture that is powered directly by a quadrature voltage controlled oscillator shortly (QVCO) with no buffering level. The QVCO uses a passive RC network embedded in a fractional-N phase-locked loop (PLL) to cancel the parasitic magnetic coupling between those two cores and keep the quadrature phase error below 1.5° . The PLL has a 1 MHz loop bandwidth, which is adequate to minimise frequency pulling effects caused by nearby interferers. Tiny PMOS based cells increase the signal output of one of those QVCO's cores in the transmitter's direct modulation Gaussian Frequency shift keying scheme. To generate the necessary phase rotations in the base band section the transceiver makes use of a 4-bit phase domain ADC based on non linear combiner topology. The suggested combiner operates in the present domain and doesn't use resistors, resulting in a demodulator that is both power and area efficient. The full receiver has sensitivity upto - 81.4 dBm and meets the BLE's interference blocking specifications. It draws 1.1 milliwatt from a 1.0 V supply and also has a power quality comparable to recent super-regenerative receivers, which are more vulnerable to interference. The transmitter produces 1.6 dBm output power to a differential of 100 and consumes 5.9 mW, implying a 24.5 percent total efficiency.

- • “A game-theoretic approach to optimal energy management using wireless sensor networks and energy harvesting technologies,” IEEE Wireless Communications, IEEE Wireless Communications, IEEE Wireless Communications, IEEE Wireless Communications, IEEE Wireless Communications V. K. Bhargava, D. Niyato, E. Hossain, M. M. Rashid, and D. Niyato, E. Hossain, E. Hossain, E. Hossain, E. Hossain For autonomous sensor networks, the energy gathering methodologies are needed because using a limited utility or undynamic battery recharging is not feasible . A energy harvesting model (such as a solar cell) transforms various types of environmental energy into electricity, which is then delivered to a sensor node. However, since a sensor node can only produce a finite amount of energy, energy-saving mechanisms are important for lowering energy consumption. We provide a glimpse of the various energy harvesting technologies and energy saving mechanisms about wireless sensor networks in this article. The related research details on sensor network energy efficiency using energy harvesting methodology are then addressed. To that end, we give an ideal energy management policy for a solar powered sensor node that employs an energy-saving sleep and wakeup strategy. The problem of deciding the probability of sleeping and waking up is conceived as a bargaining game. The Nash equilibrium is employed as the game's solution.
- • “To remove storage capacitor, a switched capacitor energy harvester based on a single-cycle criterion for MPPT,” IEEE Trans, X. Liu, K. Ravichandran, and E. Sánchez-Sinencio, Feb. 2018. In the energy gathering method for the Internet of All, a single cycle criterion maximum power point tracking shortly(MPPT) technique is advised to eradicate the need for bulky on chip capacitors (IoE). The traditional time-domain MPPT consumes very little power, but it does require a nano farad level capacitor for fine time resolution. The advised maximum power monitoring relies on a logical criteria that is easily calculated by a finite-state machine, with the

maximum PV power occurring at the minimum conversion ratio and maximum switching frequency. The magnitude of output power is determined using the single cycle criterion. The proper configuration of the reconfigurable switched capacitor power converter addresses practical issues such as self-starting and self-sustaining capabilities. In IoE applications a hysteretic control not only controls the output, but also suppresses the loading state. Without using a storage capacitor, this harvester simultaneously tackles the challenges of self-starting, self-sustaining capacity, and controlled performance. As compared to other PV cells, the power conversion efficiency peaks at 72 percent and stays above 60 percent over a large range of harvesting voltage and power. The processor is just 0.552 mm² in size.

- • T. Sano et al., in IEEE ISSCC Dig. Tech. Papers, Feb. 2015, “13.4 A 6.3 mW BLE transceiver On-chip matching network is used to embed RX image-rejection filter and TX harmonic-suppression filter.” Solutions to the BLE requirements, such as using the sliding IF (SIF) architecture in the RX [1,2] and a Class-D amplifier with HD2 calibration, have been widely discussed in previous research to achieve lower current consumption. [4] in the TX. The SIF architecture, on the other hand, includes RF image blocking without any exception rule or by the use of off chip filters. Meanwhile, the calibration on the TX has a flaw in terms of the offset problem. Furthermore, there is no way to make the RF port have "zero" external components. A BLE transceiver with a reconfigurable filter is introduced in this document, which is integrated into an on-chip matching network with no external components.
- • O. U. Khan and D. D. Wentzloff, “8.1 nJ/b 2.4 GHz short-range contact receiver in 65 nm CMOS,” IEEE Trans, July 2015. The IEEE 802.15.4 is a standard that is supported by an 8.1 nanoJoules/bit 2.4 GHz receiver with integrated digital baseband system that supports O-QPSK DSSS modulation for short-range Internet of Things applications (IoTs). In general, a wireless communication receiver's sensitivity is proportional to its power consumption. This receiver takes advantage of the trade off to achieve an

approximate total power consumption of 2.02 mW, which includes ADCs and digital baseband processing, while maintaining a sensitivity of -52.5 dBm at rate of 250 Kbps. So the radio frequency (RF) front-end alone is nearly 2x more energy efficient than the prior art. The receiver was made in 65 nm CMOS with a 0.86 mm² area.

- “A 0.6-V zeroIF/low-IF receiver for 2.4-GHz ISM-band applications with an integrated fractional-N synthesiser,” IEEE J., Mar. 2010. A. Balankutty, S.-A. Yu, Y. Feng, and P. R. Kinget. The design of analogue, RF, as well as the mixed mode circuits has become increasingly difficult as supply voltages have been reduced as a result of process scaling. The design of a ultra low voltage, low power, and heavily integrated dual mode receiver for 2.4-GigaHertz ISM band type applications is presented in this paper. The receiver works reliably between 0.55-0.65 V and is compliant with industry standards including Bluetooth and ZigBee. We address the architectural and circuit level design strategies used to solve design problems at low voltage supplies, such as restricted f_T for transistors and higher nonlinearities due to limited usable signal swing. The highly integrated receiver prototype chip was fabricated in a typical digital 90nm CMOS also known as complementary MOS process and it rises a gain of 67 dB, noise figure of 16 dB, IIP3 of -10.5 dBm, synthesiser phase noise of - 127 dBc/Hz at 3MHz offset will consume about 32.5 mW from 0.6 V, and occupies an active area of 1.7 mm².

3.3 Existing System:

Noncontact and direct conversion are used to identify vital signals. Long-term physiological tracking relies heavily on Doppler radar. The dc offset caused by clutter signals and circuit imbalances, on the other hand, is a critical problem that often degrades the sensitivity of physiological data reception. There are a few options for dealing with the dc-offset issue. The first is to use arctangent demodulation in a quadrature radar architecture to remove congestion and sensing blind zones, but this increases circuit complexity and takes up a significant amount of space. In the second method,

compensation is done by use of a traditional calibration technique involving equal amplitude but out-of-phase clutter signals. Nonetheless, a clutter canceller in the RF front-end circuit with an adjustable phase-shifter and a programmable gain amplifier (PGA) posed some questions about the volatility of incoming RF signals and the complexity of the device.

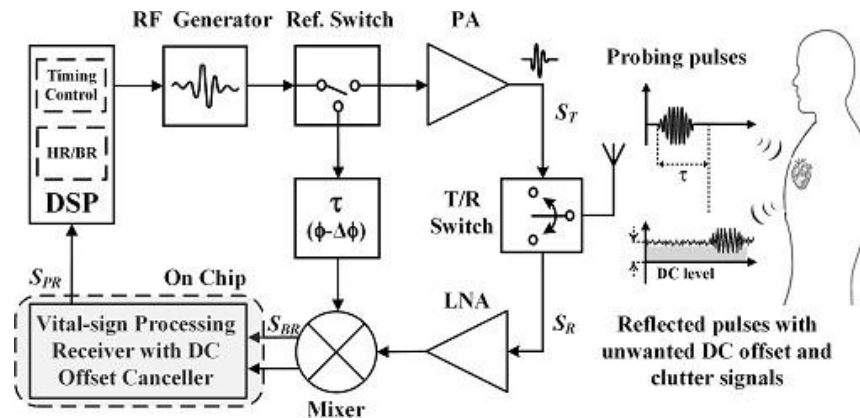


Figure 3 : Architecture of a pulse based radar system with dc offset and clutter elimination

Instead of using the pre-calibration method, a dual-tuning voltage-controlled oscillator (VCO) in a self-injection locked mode which is used to detect vital signs with dc-offset elimination. Another way to directly manage the down-converted information and feed the necessary compensation voltages to the demodulator to calibrate the dc offset is to use an adaptive dc compensation circuit in the analogue receiver. To form a high-pass response and avoid any dc residue, a servo loop feedback configuration can be used. However, maintaining the ideal vital signs necessitates an ultra low corner frequency, which is extremely difficult to achieve due to unrealizable high feedback resistance or capacitance. In the feedback direction of a biomedical instrument amplifier (IA), a MOS diode working in the sub threshold region as a pseudo resistor with ultrahigh resistance is mainly used for input bias. However, when phase and voltage as well as temperature (PVT) variations occur, the pseudo resistor's small dynamic range and high sensitivity reduce its stability and applicability. In a sub threshold region as a pseudo resistor, the input and also output swing variations (V_{gs}/V_{gd}) applied at the two terminals of a traditional MOS diode will deviate the desired resistance. A stable bias scheme at the

gate of a MOS diode is also needed to counteract process variation. A stable bias scheme at the gate of a MOS diode is also needed to counteract process variation. Furthermore, the dc offset occurs not only in the reflected pulses but also in each sub circuit mismatched offset of a receiving chain, which should all be rejected in terms of device integration. Because of its high-gain property (60–80 dB), a small input offset can saturate the following stages in the processing circuit, lowering detection sensitivity.

The mechanism for removing intrinsic input-referred offsets caused by circuit imbalances in the receiver chain is commonly considered for the overall radar system's stability.

3.4 Disadvantages:

- Having more logic area, and power consumptions.
- Having more noise and dc-offset
- Instability in radar system

3.5 Proposed System:

This brief describes a vital sign processing circuit for the ultra wideband (UWB) pulse-based radar system with no automated signal processing or algorithm support for synchronized dc/near-dc omission and out-of-band disturbance elimination. In a vital-sign receiver of a sensing radar, an intrinsic self-balanced MOS diode (SBMD) was proposed to serve as a stable and balanced pseudo resistor implemented under a servo feedback loop to minimise undesired clutters of reflected signals and input dc-offset voltages from intrinsic circuit offsets as a High-Pass Filter (HPF) with an ultra-low corner frequency smaller than 0.5 Hz as a stable servo feedback. To remove out-band noises, a third-order switched-capacitor (SC) Chebyshev low-pass filter (LPF) with trans-conductance low noise amplifier (LNA) and leap-frog topology was used as the next step, followed by the creation of an integrated band pass frequency response vital-sign processing circuit and its testing in a radar module. Finally, Tanner EDA was used to improve this work at 130 nm and 45 nm CMOS technology.

Trans-conductance LNA:

The transconductance LNA serves two purposes: first, it must transform the input voltage signal to an output current signal with the least amount of noise possible. Second, it should be able to match inputs. Figure 2 contrasts the topologies of transconductance LNAs as a survey of the prior art. Figure 2 depicts a common-source LNA (a). It has a fair transconductance but does not provide any input matching, whereas figure 2b shows a common-source LNA with inductive degeneration (b). Though providing narrowband matching, its G_m is independent of transistor transconductance.

The single-ended common-gate LNA is shown in Figure 2(c). It provides wideband matching and the cross-coupling improves the transistors g_m .

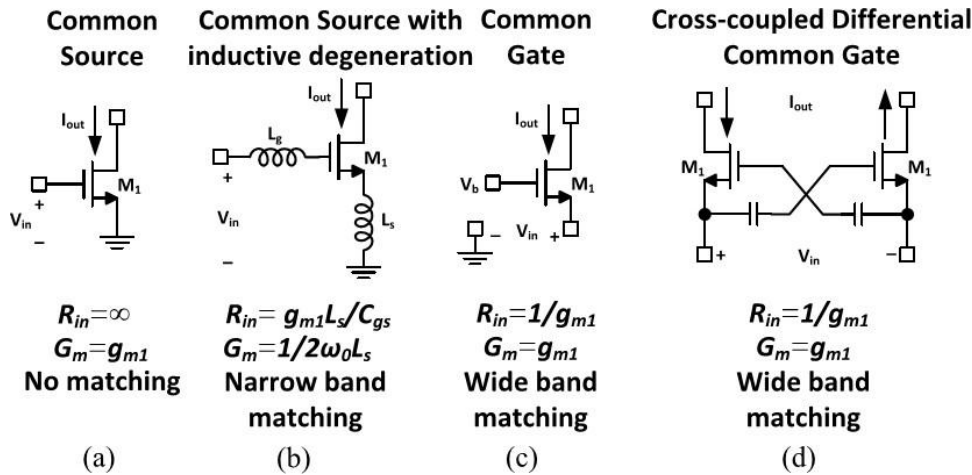


Figure 4 : Transconductance LNA topologies. (a) Common source. (b) Common source with inductive degeneration. (c) Single-ended common gate. (d) Cross-coupled differential common gate.

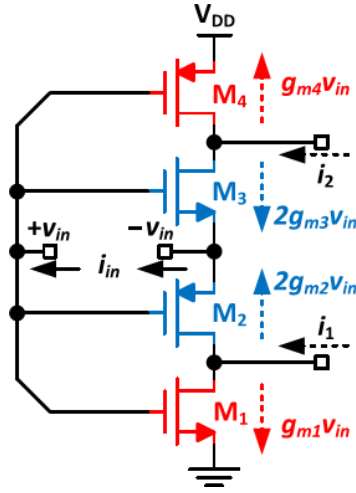


Figure 5 : Proposed transconductance LNA concept

A common-gate LNA has the disadvantage of requiring a large current to provide input matching. Figure 3 depicts the basic principle of the proposed transconductance LNA as a solution. In contrast, input matching is provided by complementary CMOS transistors (M2 and M3).

To increase the transconductance by a factor of two, the input voltage (negative input voltage) is applied at the gate (source) of both transistors. M1 as well as M4 have been included to boost the overall transconductance. Current i_1 is given by

$$i_1 = g_{m1}v_{in} + 2 \times g_{m2}v_{in} \quad (1)$$

while i_2 is given by

$$i_2 = g_{m4}v_{in} + 2 \times g_{m3}v_{in}. \quad (2)$$

The output currents can be summed together and the total output current will be

$$i_{out} = i_1 + i_2 = (g_{m1} + 2g_{m2} + 2g_{m3} + g_{m4}) v_{in}. \quad (3)$$

Assuming $g_{m1} = g_{m3} = g_{mn}$ and $g_{m2} = g_{m4} = g_{mp}$, the total transconductance is given by

$$G_m = i_{out}/v_{in} = 3(g_{mn} + g_{mp}). \quad (4)$$

The input current is given by

$$i_{in} = 2(g_{mn} + g_{mp})v_{in} \quad (5)$$

and the input impedance becomes

$$Z_{in} = v_{in}/i_{in} = 1 / 2(g_{mn} + g_{mp}). \quad (6)$$

To provide matching, the following condition should be satisfied:

$$R_S = Z_{in} = 1 / 2(g_{mn} + g_{mp}) \quad (7)$$

R_S denotes the source impedance (antenna impedance). Matching can be accomplished with less power consumption by stacking four transistors, and total transconductance can be increased by adding transistors. The differential and complete implementation of the proposed transconductance LNA are shown in Fig. 4. Capacitors are used to integrate the output currents at the output and for ac coupling at the input. While Equations (1)–(7) could theoretically be used to model the proposed LNTA in Fig. 4, the nonidealities in the implementation seem to necessitate that we have an expression for input impedance with nonidealities.

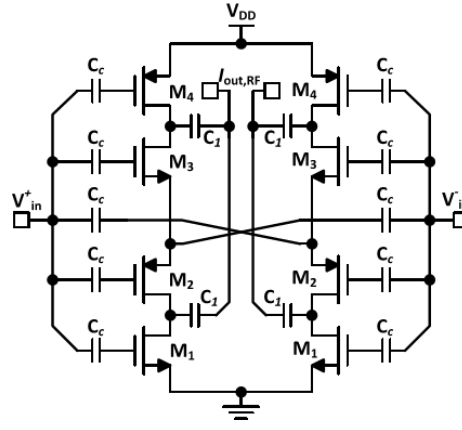


Figure 6 : Fully differential implementation of the proposed transconductance LNA

Third Order SC Chebyshev LPF :

The third-order SC Chebyshev LPF, as shown in Fig. 5, helped increase the overall SNR by suppressing out-of-band noises. To achieve high stability and low-impact PVT variations, the LPF was configured in a leap-frog configuration. The bandwidth of the SC LPF could be changed from 50 Hz to 20 kHz by adjusting the sampling rate using interval sample-and-hold (S/H) clocks ($f_{BW} = f_{S/H}/50$).

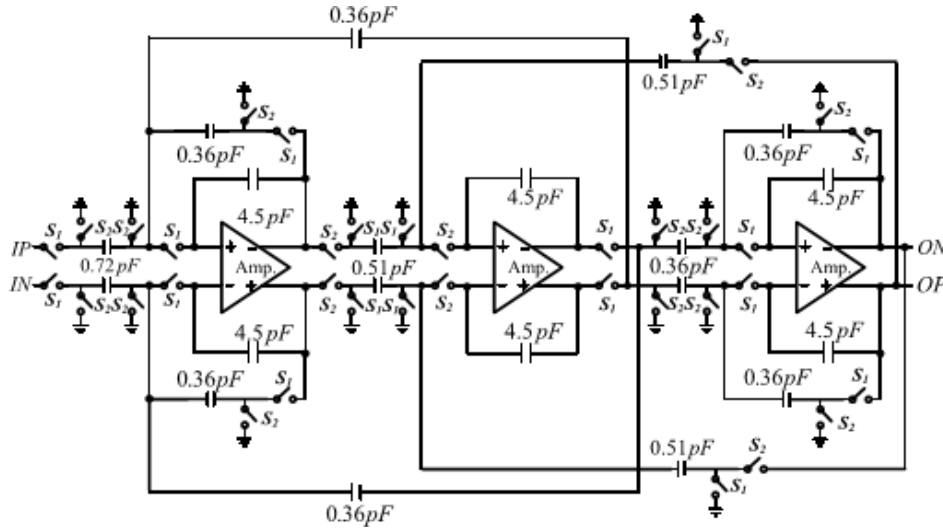


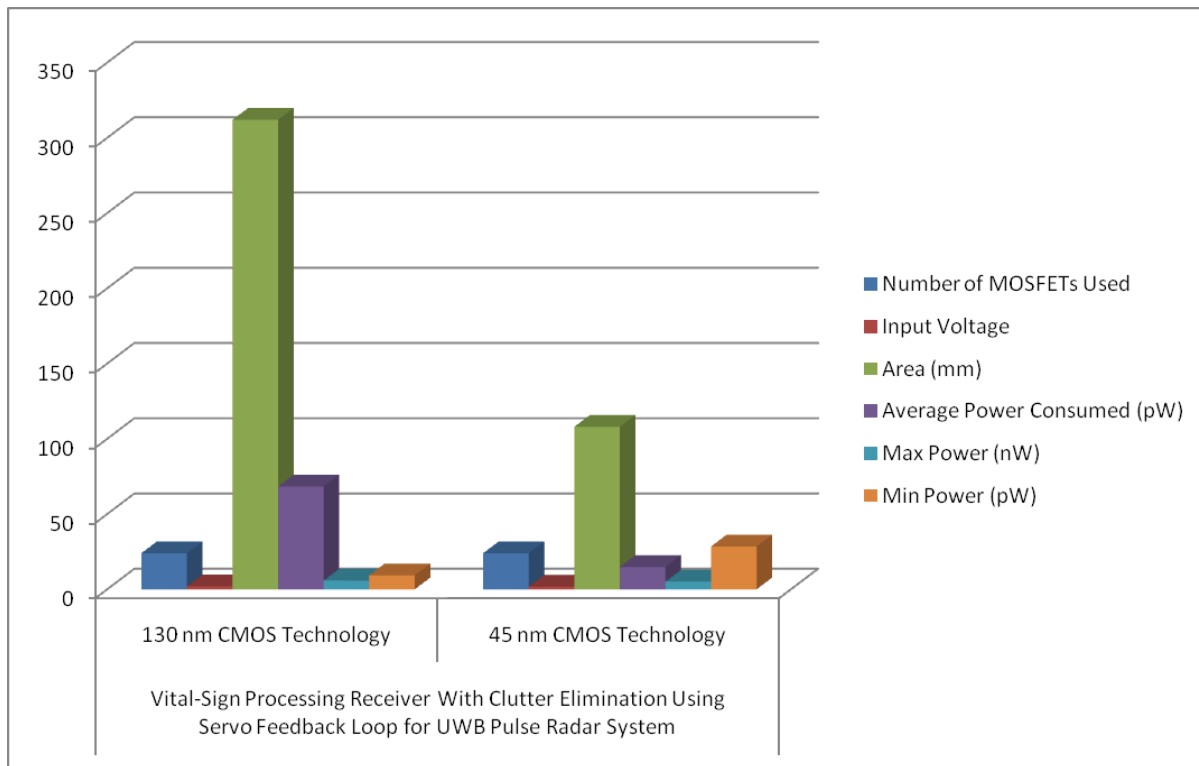
Figure 7 : Schematic of the third-order SC Chebyshev LPF

3.6 Advantages:

- Requires less logic area, and less power consumptions
- Dc-offset cancellation and low noise
- Increased stability in Radar System

4. Comparison

	Vital-Sign Processing Receiver With Clutter Elimination Using Servo Feedback Loop for UWB Pulse Radar System	
	130 nm CMOS Technology	45 nm CMOS Technology
Number of MOSFETs Used	24	24
Input Voltage	2.0	1.8
Area (mm)	312.0	108.0
Average Power Consumed (pW)	68.28263	14.88633
Max Power (nW)	5.7938	5.0694
Min Power (pW)	9.322886	28.4779



5. Software Requirement

Tanner is a Spice Analogue Integrated Circuits Computer Analysis Program. The Engine Machines in the Tanner Tool are as follows:

1. S-EDIT (To edit the schematic)
2. T-EDIT (Simulation Edit)
3. W-EDIT (Waveforms Edit)
4. L-EDIT (Layout Edit)

Spice software uses these engine tools to enable users to design and simulate new ideas in Analogue Integrated Circuits before committing to the time-consuming and expensive process of chip fabrication.

5.1 Schematic edit tool (s-edit)

S-Edit is a file, module, and page hierarchy. Symbol and schematic modes are introduced. S-Edit has a feature that allows you to:

1. Implementing a design.
2. Viewing, drawing & editing of objects.
3. Design connectivity.
4. Properties, net lists & simulation.

Instance & browse schematic & symbol mode.

Beginning a design:

It explains the design process in detail in terms of file module operation and module.

Browser:

A working knowledge of the S-Edit design hierarchy of files and modules is needed for effective schematic design. Modules make up S-Edit template files. A module, such as a transistor, a gate, or an amplifier, is a functional unit of design.

Module contains of two components:

1. Primitives: Geometrical objects created by using drawing tools.
2. Instances refer to various other modules in file. The instanced module is often the original.

S-Edit has two viewing modes:

1. Schematic Mode: to create or view a schematic, we operate in schematic mode.
2. Symbol Mode: it represents symbol of a larger functional unit such as operational amplifier.

5.2 T-spice pro circuit analysis

An overview of the T- Spice Pro circuit analysis suite's integrated components:

S- Edit" Schematic Editor displays and edits schematic data files (.sdb) that describe the circuits to be analysed in graphical form.

T- Spice" Circuit Simulator uses simulation input files (.sp) to describe the circuits to be studied in textual form for editing and simulation.

The numerical results of the circuit analyses, shape manipulation, and show by W- Edit" Waveform Viewer are stored in simulation output files (.out).

Circuit simulator (t-spice)

Individual points in a circuit can be specified and analysed using T-Spice Pro's waveform probing function, which combines S- Edit, T- Spice, and W- Edit. The following are some examples of analyses: The input file is at the heart of T-process. Spice's (also known as the circuit description, the net list &the input deck). This is a plain text file containing the T-Spice device statement and simulation commands for creating a model of the circuit to be simulated using the SPICE circuit description language. Any text editor can be used to build and modify input files. T-Spice is a programme that simulates circuits. It gives the facility of

1. Design Simulation and
2. Simulation Commands
3. Device Statements
4. User-Designed External Models
5. Small Signal & Noise Models

To solve circuit problems, T- Spice employs Kirchhoff's Current Law (KCL). A circuit in T- Spice is a set of devices connected to nodes. The circuit state is represented by the voltage at all nodes. T-Spice finds a range of node voltages that satisfy the KCL constraint (implying that sum of the currents flowing into each of the node is zero). T-Spice

calculates and adds up all the currents flowing out of each system into nodes connected to it in order to determine if a collection of node voltages is a solution (its terminals). The circuit model for a resistor of resistance R determines the relationship between voltages at device terminals and currents across the terminal that is

$$I=\Delta V/R$$

Where, ΔV represents the voltage difference across the device. A few analyses are discussed below:

DC Operating Point Analysis

The steady-state condition of a circuit is found using DC operating point analysis, which is obtained (in theory) after the input voltages have been applied for an infinite amount of time. T- Spice reads the contents of the model file for NMOS and PMOS transistor evaluation with the include instruction. MOSFET model parameters for both n and p-type devices are assigned values in the technology file. These parameters are read from the input file and used to test MOSFET model equations, with the results being used to construct internal tables of current and charge values. In the computations needed by the simulation, values read or interpolated from these tables are used. Following each transistor name are the names of its terminals. Drain-gate -source -bulk is the appropriate order of terminal names. The model name (in this case, NMOS or PMOS) and physical characteristics including length and width are then defined. The op command calculates DC operating points and saves the results to the file defined in the Simulate > Start Simulation dialogue box. The DC operating point information for the circuit mentioned in the input file is listed in the output file.

DC Transfer Analysis

The voltage or current at one set of points in a circuit is studied as a function of the voltage or current at another set of points using DC transfer analysis. Sweeping the source variables over specified ranges and recording the output accomplishes this. The `.dc` command is followed by a list of sources to be swept and the voltage ranges over which the sweeps are to be performed, suggesting transfer analysis. The following is how the transition study will be carried out: `Add` will be set to 5 volts, and `vin` will be swept over its defined range; `vdd` will then be incremented, and `vin` will be swept over its range; and so on, until `vdd` reaches its upper limit. The `.dc` order disregards the values assigned to the voltage sources `vdd` and `vin` in the voltage source statements, but they must also be declared in those statements. The `print dc` command reports results for nodes in and out to the designated destination.

Transient Analysis

The results of a transient study show how circuit elements change over time. There are three modes in the simple T-Spice command for transient analysis. The DC operating point is calculated in the default mode, and T-Spice uses it as beginning point for transient simulation. The command defines the parameters of the transient analysis that will be run.

AC Analysis

AC analysis characterizes the circuit's behaviour dependence on small-signal input frequency. It includes three steps:

- (1) Calculating the DC operating point;
- (2) Linearizing the circuit and
- (3) Solving the linearized circuit for each frequency.

When an ac voltage source is used, the DC voltage difference between the two nodes is set to -0.0007 volts; the AC magnitude is 1 volt, and the AC phase is 180 degrees. An AC analysis is performed with the `.ac` order. The `.ac` keyword is followed by details about the frequencies that will be swept during the study. If the frequency is to be swept logarithmically by decades (DEC), the norm is to have 5 data points per decade. The two

print commands output the node's voltage magnitude (in decibels) and phase (in degrees) to the specified file, respectively.

The .ac model command writes the small- signal model parameters and operating point voltages and currents for all the circuit devices.

Noise Analysis

Tiny, random variations in voltage and current levels are unavoidable in real circuits. The impact of noise in a circuit can be simulated and recorded in T- Spice alongside AC research. The aim of noise analysis is to determine how noise from various circuit devices affects an output voltage or voltages as a function of frequency. Noise analysis is done in tandem with AC analysis; if the .ac command is absent, the noise command is skipped. The noise command allows noise analysis to be conducted at the same frequencies while the .ac command is present. The noise command accepts two arguments: the output at which noise effects should be calculated and the input at which the noise should be considered concentrated for calculating the equivalent noise spectral density. Printing results is done with the print command.

Waveform edit

When it comes to testing, understanding, and improving VLSI circuits, the ability to visualize the complex numerical data generated by simulation is crucial. W-Edit is a waveform viewer that provides flexibility, control, and speed in a graphical data representation context. W-Edit has a number of advantages:

1. T-spice, Tanner EDA's circuit level simulator, is tightly integrated. Without modifying the output text data files, W-Edit can chart data produced by T spice directly. Data can also be dynamically charted as it is generated during the simulation process.
2. Charts can be modified automatically based on the type of data being presented.
3. Charts can automatically be configured according to the type of data being presented.
4. W-Edit treats data as a unit known as a trace. Multiple traces from various output files can be viewed in a single or multiple windows at the same time; traces can be

copied and transferred between charts and windows. Existing traces can be used to generate new ones using trace arithmetic.

5. Chart views can be viewed back & forth and zoomed in & out, including specifying the exact X-Y co-ordinate range.
6. Properties of axes, traces, rides, charts, text & colors can be changed at any time. W-Edit accepts numerical data in the form of plain or binary text files. T-header Spice's and comment related information is used for automated chart configuration. W-Edit can be linked to a running simulation in T-Spice to upgrade results in real time. With the WDB, W-Edit saves data with map, trace, axis, and environment settings in files (W-Edit Database).

5.3 Layout (l-edit):

It's a method that describes the masks used in integrated circuit fabrication. Files, cells, and mask primitives are used to define a layout design. The component parameters at the layout level are completely different from those at the schematic level. As a result, it allows the consumer to evaluate the circuit's response before proceeding to the time-consuming and expensive fabrication process. There are rules for designing a schematic circuit layout diagram that allow the user to compare the output response to the anticipated one.

L- Edit: An Integrated Circuit Layout Tool

Layers in L- Edit are linked to masks used in the fabrication process. Different colours and patterns may be used to reflect different layers. In terms of files, cells, instances, and mask primitives, L- Edit defines a layout design. You can put as many files into memory as you want. A file may have any number of cells in it. A file may have any number of cells in it. These cells can be linked in a hierarchical way, as in a traditional design, or they can be completely separate, as in a library file. Mask primitives and instances of other cells may be found in any number or mixture of cells.

Cells: The Basic Building Blocks

The basic building block of the integrated circuit design in L- Edit is a cell. Designing layout happens within cells. A cell can:

1. Contain part or all of the entire design.
2. Be referenced in other cells as a sub- cell, or instance.
3. Be made up entirely of instances of other cells.
4. Contain original drawn objects, or primitives.
5. Be made up entirely of primitives or a combination of primitives and instances of other cells.

Hierarchy

L- Edit allows you to create entirely hierarchical masks. It is possible for cells to produce instances of other cells. An instance is a reference to a cell; if you modify the instanced cell, it will affect all instances of that cell. Since an instance does not need to store any of the data inside the instanced cell, only a reference to the instanced cell is stored, along with details about how the instance may be rotated and mirrored, instances simplify the process of updating a template and minimise data storage requirements.

In L-Edit, there is no such thing as a "separated" hierarchy: instances and primitives can coexist in the same cell at any stage. The design files themselves are self-contained. A cell in an instance's pointer often points to another cell in the same design file. To keep the destination file's self-contained nature, L- Edit copies through any cells that are instanced by the copied cell when cells are copied from one file to another.

Design Rules

Manufacturing constraints can be defined in L- Edit as design rules. Layouts can be verified against these design rules.

Design Features

L- Edit is a mask editor that allows you to create completely custom masks. Because of L Edit's user-friendly gui, manual layout can be completed faster. Furthermore, special systems can be designed to use a technology without having to worry about problems caused by automated transformations. In CMOS- Bulk technology, phototransistors, guard bars, vertical and horizontal bipolar transistors, static structures, and Schottky diodes, for example, are as simple to build as traditional MOS transistors.

Floor plans

L- Edit is a floor-planning method that requires manual input. You may choose to display instances as an outline with only a name, or as completely fleshed-out mask geometry. When you view your design in outline mode, you can quickly and easily rearrange the cells in your design to achieve the required floor plan. Instances at any stage in the hierarchy can be managed using the same graphical move/pick operations or rotation/mirror commands as you use on primitive mask geometry, with insides hidden or displayed.

Memory Restrictions

L- Edit allows users to make their design files as wide as they want, as long as they have enough RAM and disc space.

Hard Copy

The ability to print a hard copy of the template is provided by L- Edit. Very large plots can be printed to a small scale on multiple 8 1/2 x 11 inch pages using the multi age option. On inkjet plotters, an L- Edit macro is available to allow large-format, high-resolution colour plotting.

Variable Grid L-Edit's grid options supports lambda- based design as well as micron-based and mil- based designs.

Error Recovery L-Edit's error- trapping mechanism finds system errors and in most cases provides a means to recover without losing or damaging the data.

1. L- Edit Modules
2. L- Edit TM: a layout editor
3. L- Edit $\square$ Extract TM: a layout extractor

4. L- Edit [®] DRC TM: a design rule checker

L- Edit is a high-performance, interactive, graphical mask layout editor with a lot of features. L- Edit creates layouts quickly and easily, allows for an infinite number of layers, cells, and hierarchy levels, and supports completely hierarchical designs. It supports 90°, 45°, and all-angle drawing modes and contains all major drawing primitives.

L- Edit Extract converts L- Edit templates into SPICE-compatible circuit net lists. It can identify active and passive devices, sub circuits, and the most common device parameters, such as resistance, capacitance, device length, width, and region, as well as device source and drain area.

L- Revision DRC manages minimum width, exact width, minimum space, minimum surround, non-exist, overlap, and extension rules and has user-programmable rules. It is capable of handling both full chip and region-only DRC. For quickly and easily cycling through rule-checking errors, DRC provides Error Browser and Object Browser functions.

6. Output Screen Shots

130 nm Screenshots:

Power Report:

The screenshot shows the TSPice simulation output window. The title bar indicates the file path is "TS Third_Order_SC_Chiebyshew_LPFoot (-AppData\Local\Temp) - GVIM". The menu bar includes File, Edit, Tools, Syntax, Buffers, Window, and Help. The toolbar contains various icons for file operations and simulation control. The main text area displays the following content:

```

h. 853437e-005 1.1690e+000 1.1481e+000 2.1019e+000 2.8981e+000
h. 863437e-005 1.1691e+000 1.1482e+000 2.1217e+000 2.8786e+000
h. 873437e-005 1.1692e+000 1.1484e+000 2.1430e+000 2.8570e+000
h. 883437e-005 1.1693e+000 1.1485e+000 2.1657e+000 2.8343e+000
h. 893437e-005 1.1695e+000 1.1487e+000 2.1897e+000 2.8103e+000
h. 903437e-005 1.1696e+000 1.1488e+000 2.2149e+000 2.7851e+000
h. 913437e-005 1.1698e+000 1.1490e+000 2.2413e+000 2.7587e+000
h. 923437e-005 1.1699e+000 1.1491e+000 2.2686e+000 2.7314e+000
h. 933437e-005 1.1701e+000 1.1493e+000 2.2969e+000 2.7031e+000
h. 943437e-005 1.1703e+000 1.1495e+000 2.3260e+000 2.6740e+000
h. 953437e-005 1.1704e+000 1.1497e+000 2.3558e+000 2.6442e+000
h. 963437e-005 1.1706e+000 1.1499e+000 2.3861e+000 2.6139e+000
h. 973437e-005 1.1708e+000 1.1501e+000 2.4169e+000 2.5831e+000
h. 983437e-005 1.1710e+000 1.1502e+000 2.4481e+000 2.5519e+000
h. 993437e-005 1.1712e+000 1.1504e+000 2.4794e+000 2.5206e+000
5. 000000e-005 1.1713e+000 1.1506e+000 2.5000e+000 2.5000e+000

* BEGIN NON-GRAPHICAL DATA

Power Results
UDDD from time 0 to 5e-005
Average power consumed -> 6.828263e-011 watts
Max power 5.793837e-009 at time h.50344e-005
Min power 9.322886e-012 at time 2.26344e-005

* END NON-GRAPHICAL DATA
*
* Parsing 0.00 seconds
* Setup 0.01 seconds
* DC operating point 0.00 seconds
* Transient Analysis 0.07 seconds
* Overhead 1.53 seconds
* -----
* Total 1.62 seconds

* Simulation completed with 1 Warning

* End of T-Spice output file
  
```

The status bar at the bottom right shows "576,43" and "Bot".

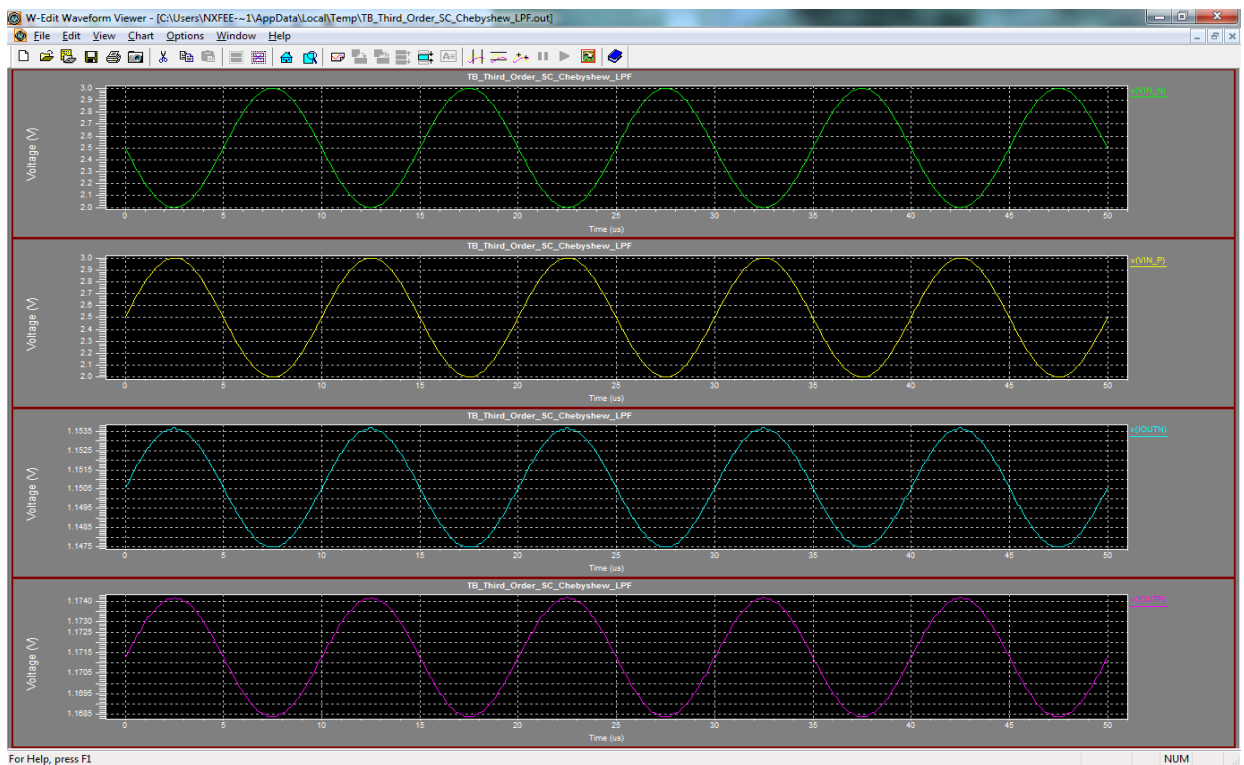
Area Report:

```
TB_Third_Order_SC_Chebyshev_LPF.out (-\AppData\Local\Temp) - GVIM
File Edit Tools Syntax Buffers Window Help
[Icons]

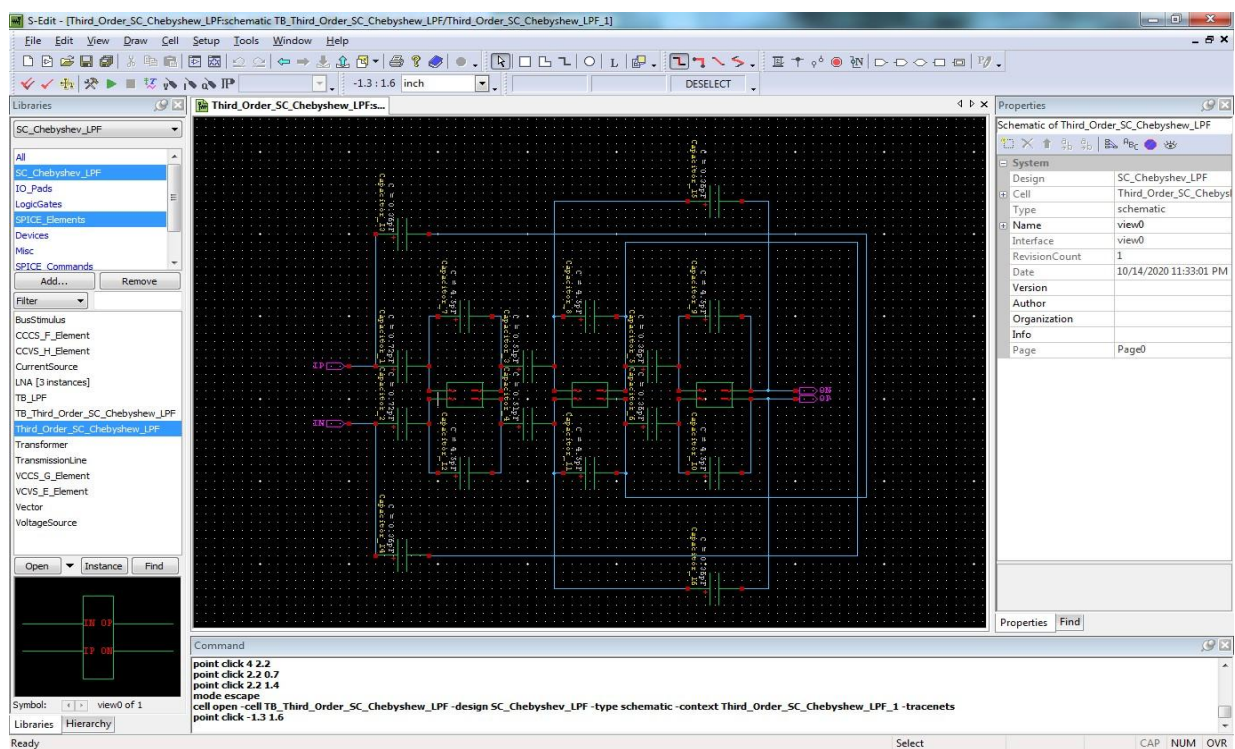
*SEdit: Alter blocks = 0
*
* Accuracy and Convergence options:
*   dctest = 100      numndset|dchold = 100
*
* Timestep and Integration options:
*   relq|relchgtol = 0.0005
*
* Model Evaluation options:
*   dcap = 2          defnrb = 0 [sq]          defnrd = 0 [sq]
*   defnrs = 0 [sq]   tnom = 25 [deg C]
*
* General options:
*   temp = 25 [deg C]  threads = 4
*
* Output options:
*   acout = 1          ingold = 0
*
*
* Device and node counts:
*   MOSFETs - 24      MOSFET geometries - 4
*   BJTs - 0          JFETs - 0
*   MESFETs - 0       Diodes - 0
*   Capacitors - 55   Resistors - 0
*   Inductors - 0     Mutual inductors - 0
*   Transmission lines - 0   Coupled transmission lines - 0
*   Voltage sources - 3    Current sources - 0
*   UCUS - 0           UCCS - 0
*   CCUS - 0           CCCS - 0
*   U-control switch - 0  I-control switch - 0
*   Macro devices - 0     External C model instances - 0
*   HDL devices - 0
*   Subcircuits - 0       Subcircuit instances - 4
*   Independent nodes - 51  Boundary nodes - 4
*   Total nodes - 55
*
* *** 1 WARNING MESSAGE GENERATED DURING SETUP
*
*SEdit: Alter=0
*SEdit: Analysis types DCOP 0 ACHODEL 0 AC 0 TRANSIENT 1 TRANSFER 0 NOISE 0
*
*SEdit: .tran 5e-008 5e-005
TRANSIENT ANALYSIS
Time(s)      v(IOUTP)<U>  v(IOUTN)<U>  v(VIN_P)<U>  v(VIN_N)<U>
0.000000e+000 1.1713e+000 1.1506e+000 2.5000e+000 2.5000e+000
3.125000e-009 1.1713e+000 1.1506e+000 2.5010e+000 2.4990e+000

42,70 1%
```

Output waveform:



LPF Design:



Power Report:

35

Area Report:

```

TB_Third_Order_SC_Chebyshev_LPF.out (~\AppData\Local\Temp) - GVIM
File Edit Tools Syntax Buffers Window Help
[Icons]

* T-Spice 13.00 Simulation Thu Oct 15 17:15:11 2020 C:\Users\HXFEE~1\AppData\Local\Temp\TB_Third_Order_SC_Chebyshev_LPF.sp
* Command line: tspice -o C:\Users\HXFEE~1\AppData\Local\Temp\TB_Third_Order_SC_Chebyshev_LPF.out C:\Users\HXFEE~1\AppData\Local\Temp\TB_Third_Order_SC_Chebyshev_LPF.s
P
* T-Spice Win32 13.00.20080321.01:01:33
* Warning : T-Spice has detected a subcircuit with no DC path to ground,
* : due to capacitors being treated as open circuits
* : during the DC operating point computation.
* : DCstep will be set to 100 in order to prevent non-convergence.
* : To override the automatic setting of dcstep, you may add the option:
* : .option dcstep=0

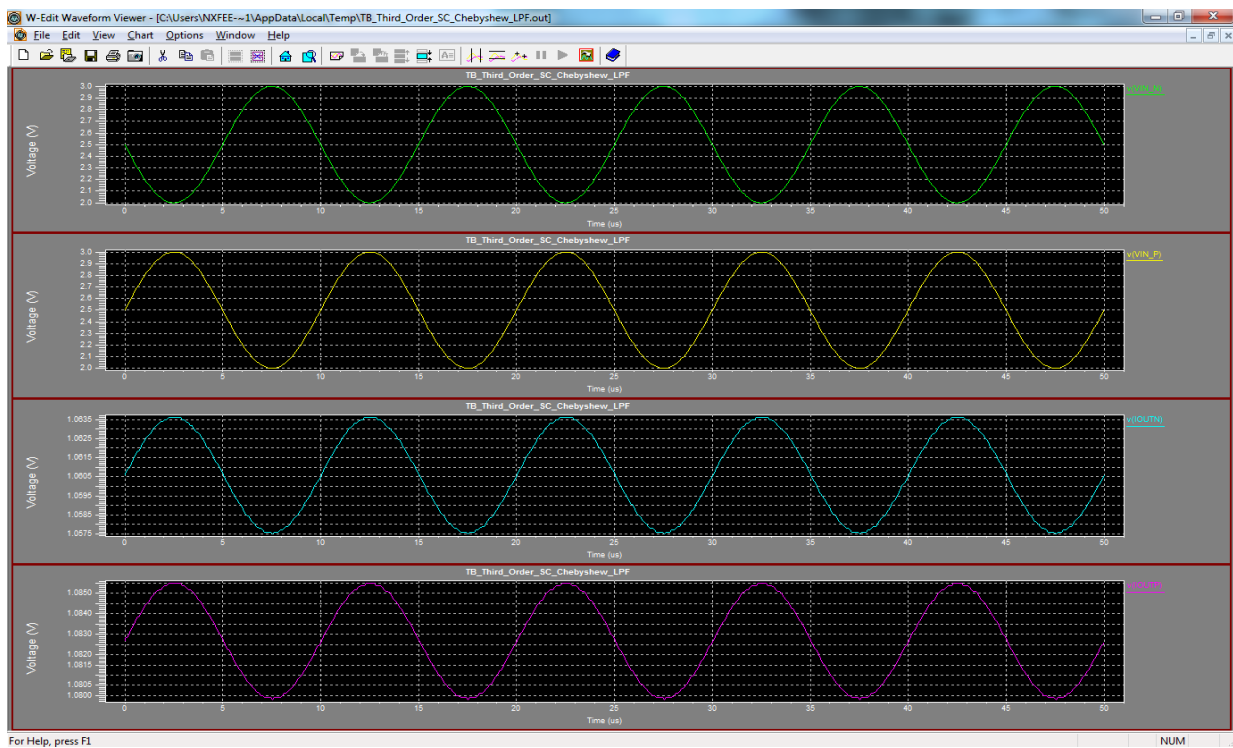
*SEEDIT: Alter blocks = 0

* Accuracy and Convergence options:
* dcstep = 100 numndset[dchold = 100
*
* Timestep and Integration options:
* relq[relchgtol = 0.0005
*
* Model Evaluation options:
* dcap = 2 defnrb = 0 [sq] defnrd = 0 [sq]
* defnrs = 0 [sq] tnon = 25 [deg C]
*
* General options:
* temp = 25 [deg C] threads = 4
*
* Output options:
* acout = 1 ingold = 0
*
*
* Device and node counts:
* MOSFETs - 24 MOSFET geometries - 4
* BJTs - 0 JFETs - 0
* MESFETs - 0 Diodes - 0
* Capacitors - 55 Resistors - 0
* Inductors - 0 Mutual inductors - 0
* Transmission lines - 0 Coupled transmission lines - 0
* Voltage sources - 3 Current sources - 0
* UCUS - 0 UCES - 0
* CCUS - 0 CCES - 0
* U-control switch - 0 I-control switch - 0
* Macro devices - 0 External C model instances - 0
* HDL devices - 0
* Subcircuits - 0 Subcircuit instances - 4
* Independent nodes - 51 Boundary nodes - 4
* Total nodes - 55

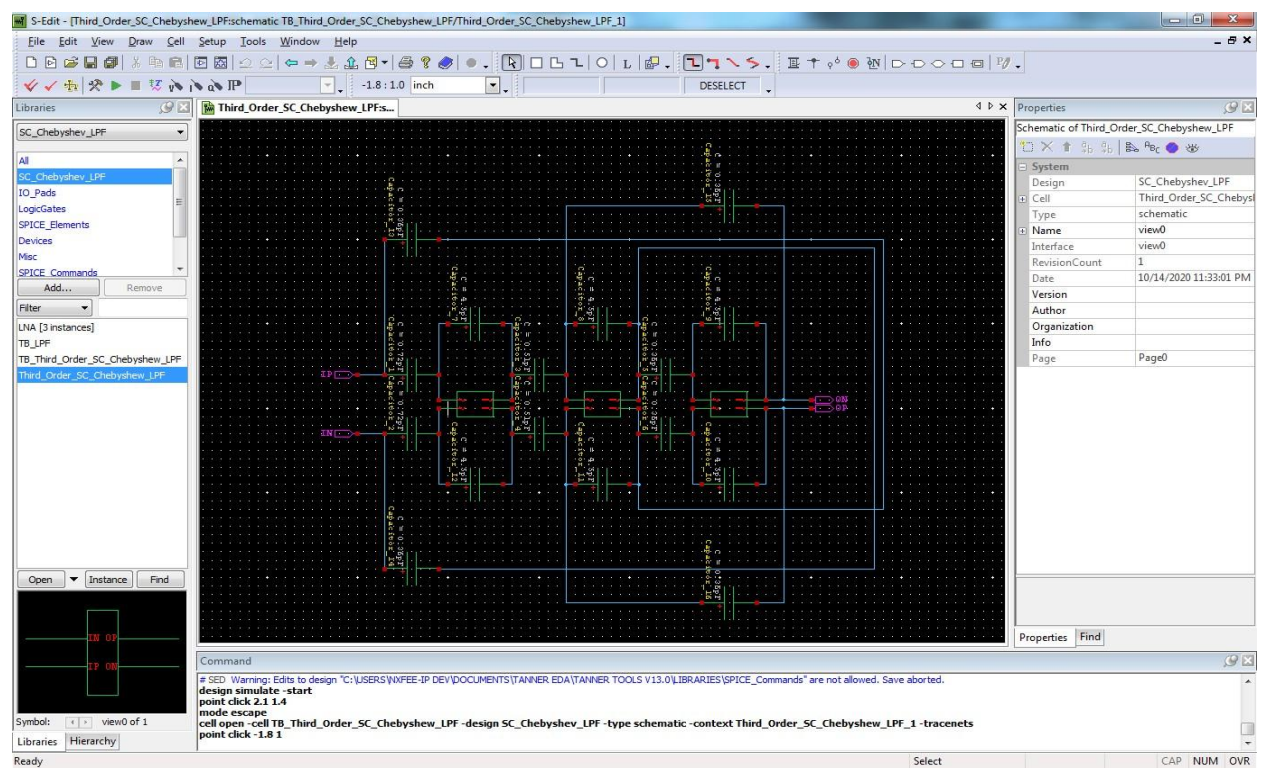
* *** 1 WARNING MESSAGE GENERATED DURING SETUP
40,47 Top

```

Output waveform:



LPF Design:



7. Reference

- [1] B.-K. Park, O. Boric-Lubecke, and V. M. Lubecke, "Arctangent demodulation with DC offset compensation in quadrature Doppler radar receiver systems," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 5, pp. 1073–1079, May 2007.
- [2] H.-C. Kuo et al., "A fully integrated 60-GHz CMOS direct-conversion Doppler radar RF sensor with clutter canceller for single-antenna noncontact human vital-signs detection," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1018–1028, Apr. 2016.
- [3] P.-H. Wu et al., "Phase- and self-injection-locked radar for detecting vital signs with efficient elimination of DC offsets and null points," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 685–695, Jan. 2013.
- [4] Z.-P. Yang and Y.-C. Chiang, "Vital signal radar with adaptive compensation circuits to effectively eliminate DC offsets," *IEEE Microw. Wireless Compon. Lett.*, vol. 28, no. 1, pp. 88–90, Jan. 2018.
- [5] P.-I. Mak, S.-P. U, and R. P. Martins, "On the design of a programmable gain amplifier with built-in compact DC-Offset cancellers for very low voltage WLAN systems," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 2, pp. 496–509, Mar. 2008.
- [6] A. M. Sodagar, G. E. Perlin, Y. Yao, K. Najafi, and K. D. Wise, "An implantable 64-channel wireless microsystem for single-unit neural recording," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2591–2604, Sep. 2009.

- [7] R. R. Harrison and C. Charles, "A low-power low noise CMOS amplifier for neural recording applications," *IEEE J. Solid state Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
- [8] R. Puddu et al., "A precision Pseudo Resistor bias scheme for the design of very large time constant filters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, no. 7, pp. 762–766, Jul. 2017.
- [9] W.-P. Hung, C.-H. Chang, and T.-H. Lee, "Real-time and noncontact impulse radio radar system for μm movement accuracy and vital-sign monitoring applications," *IEEE Sensors J.*, vol. 17, no. 8, pp. 2349–2358, Apr. 2017.
- [10] D. Zito et al., "SoC CMOS UWB pulse radar sensor for contactless respiratory rate monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 503–511, Dec. 2010.
- [11] C. Gu et al., "Accurate respiration measurement by using DC-coupled continuous-wave radar sensor for motion-adaptive cancer radiotherapy," *IEEE Trans. Biomed. Eng.*, vol. 59, no. 11, pp. 3117–3123, Nov. 2012.