

EVALUATION OF AN EFFICIENT DUAL STAGE COMPRESSOR FOR HIGH SPEED MULTIMEDIA APPLICATIONS

Submitted in partial fulfilment of the requirements for the award in
Bachelor of Engineering degree in
Electronics and Communication Engineering

By

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SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)

Accredited with Grade "A" by NAAC

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **SEETHA LAKSHMI.G.M (Reg No:37130365)** and **SINDHUMANI.B (Reg No:37130382)** who carried out the project entitled **EVALUATION OF AN EFFICIENT DUAL STAGE COMPRESSOR FOR HIGH SPEED MULTIMEDIA APPLICATIONS** under our supervision from December 2020 to April 2021.

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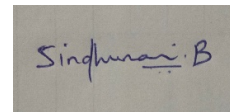
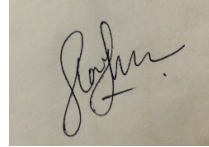
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DECLARATION

We, **SEETHA LAKSHMI.G.M (Reg No: 37130365)** and **SINDHUMANI.B (Reg No: 37130382)** hereby declare that the Project Report entitled **EVALUATION OF AN EFFICIENT DUAL STAGE COMPRESSOR FOR HIGH SPEED MULTIMEDIA APPLICATIONS** done by me under the guidance of **Mr.MATHAN.N., M.Tech.,(Ph.D)** at is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

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ABSTRACT

The overhead on computation units in a processor to deliver high performance and execution efficiency can be leveraged by introducing approximation. Speed of operation which is inversely proportional to the delay of the system requires immense parallel operations that incur huge hardware and power dissipation. Energy and area efficient systems can be realised by relaxing the precision and reliability of the system. In order to maintain the balance between delay, area and power, approximate computing has emerged as a promising solution. Approximate application is a common operation used in approximate computing methods for high performance and low power computing. These applications deliver high performance at the cost of reduction in accuracy. Furthermore, such implementations reduce the complexity of the system architecture, delay and power consumption. Power efficient circuits for approximate multiplication can be realized with an approximate 4:2 compressor. This paper proposes a novel design that uses a modification of a previous approximate 4:2 compressor design and adds an error recovery module, delay and power with comparable accuracy when compared with the existing architecture. The proposed design, even with the additional error recovery module, is more accurate requires less hardware, and consumes less power than previously proposed 4:2 compressor – based approximate multiplier design. These designs are implemented using 130nm CMOS technology and efficiency of the proposed designs have been extensively verified and projected on scales of area, delay, power, Power Delay Product (PDP). A novel high speed, area – efficient, low power 4:2 compressor architecture is proposed. The proposed compressors are utilized to implement in multipliers. The analysis is further will be extended for high speed applications.

TABLE OF CONTENTS

ABSTRACT		v
LIST OF FIGURES		ix
LIST OF TABLES		xi
CHAPTER NO		PAGE NO
1	INTRODUCTION	1
	1.1 Compressor	1
	1.1.1 4:2 Compressor	2
	1.2 Multiplexer	3
	1.2.1 Types of Multiplexers	4
	1.3 Gates	8
2	LITERATURE SURVEY AND OBJECTIVES	12
	2.1 Literature Survey	12
	2.2 Literature Summary	15
3	Existing System	16
	3.1 2*1 Mux	17
	3.2 OR Gate	18

	3.3 XOR Gate	18
	3.5 NOR Gate	20
	3.6 AND Gate	21
4	MODIFIED DUAL STAGE 4:2 COMPRESSOR USING STACK TECHNIQUE	22
	4.1 Stack Technique	22
	4.2 Modified Dual Stage 4:2 compressor using stack technique	23
	4.3 2*1 Mux using Stack Technique	24
	4.4 OR Gate using Stack Technique	24
	4.5 AND Gate using Stack Technique	25
	4.6 XOR Gate using Stack Technique	26
5	RESULTS AND DISCUSSION	27
	5.1 Simulation Results	27
	5.1.1 4:2 Compressor Simulation Output	27
	5.1.2 2*1 Mux Simulation Output	28
	5.1.3 OR Gate Simulation Output	29
	5.1.4 AND Gate Simulation Output	29

5.1.5 XOR Gate Simulation Output	30
5.1.6 Simulation results of 2:1 Multiplexer	30
5.1.7 Simulation results of modified 4:2 compressor	31
5.1.8 Simulation results of multiplier using 4:2 compressor	31
5.2 Performance Analysis	32
5.2.1 Performance Analysis of 130nm Compressor	32
5.2.2 Performance Analysis of 130nm modified Compressor using P Stack	32
5.2.3 Performance Analysis of 130nm modified Compressor using N Stack	33
5.2.4 Performance Analysis of 130nm modified Compressor using Full Stack	33
5.2.5 Performance Analysis of 32nm Compressor	34
5.2.6 Performance Analysis of 32nm modified Compressor using P Stack	34
5.2.7 Performance Analysis of 32nm modified Compressor using N Stack	35
5.2.8 Performance Analysis of 32nm modified Compressor using Full Stack	35
6 CONCLUSION AND SUMMARY	36
REFERENCES	37

LIST OF FIGURES		
FIGURE NO.	DESCRIPTION	PAGE NO
Fig 1.1	4:2 Compressor	2
Fig 1.2	Multiplexer	3
Fig 1.3	2*1 Mux Multiplexer	4
Fig 1.4	4*1 Multiplexer	6
Fig 1.5	8*1 Multiplexer	7
Fig 1.6	8*1 Multiplexer Circuit	8
Fig 1.7	AND Gate	9
Fig 1.8	OR Gate	10
Fig 1.9	XOR Gate	11
Fig 3.1	Basic Block of Dual Stage 4:2 Compressor	16
Fig 3.2	2*1 Mux using Transmission Gate	17
Fig 3.3	OR Gate using Transmission Gate	18
Fig 3.4	XOR Gate using Transmission Gate	19
Fig 3.5	NAND Gate using Transmission Gate	20

Fig 3.6	NOR Gate using Transmission Gate	21
Fig 3.7	AND Gate using Transmission Gate	21
Fig 4.1	Stack Diagram	23
Fig 4.2	2*1 MUX using Stack Technique	24
Fig 4.3	OR Gate using Stack Technique	25
Fig 4.4	AND Gate using Stack Technique	25
Fig 4.5	XOR Gate using Stack Technique	26
Fig 5.1	4:2 Compressor Simulation Output	27
Fig 5.2	2*1 Mux Simulation Output	28
Fig 5.3	OR Gate Simulation Output	29
Fig 5.4	AND Gate Simulation Output	29
Fig 5.5	XOR Gate Simulation Output	30
Fig 5.6	Simulation results of 2:1 Multiplexer	30
Fig 5.7	Simulation results of modified 4:2 compressor	31
Fig 5.8	Simulation results of multiplier using 4:2 compressor	31

LIST OF TABLES		
TABLE NO	DESCRIPTION	PAGE NO
1.1	2*1 MUX TruthTable	5
1.2	4*1 Mux Truth Table	6
1.3	8*1 Mux Truth Table	8
5.1	Performance Analysis of 130nm Compressor	30
5.2	Performance Analysis of 130nm modified Compressor using P Stack	30
5.3	Performance Analysis of 130nm modified Compressor using N Stack	31
5.4	Performance Analysis of 130nm modified Compressor using Full Stack	31
5.5	Performance Analysis of 32nm Compressor	32
5.6	Performance Analysis of 32nm modified Compressor using P Stack	32
5.7	Performance Analysis of 32nm modified Compressor using N Stack	33
5.8	Performance Analysis of 32nm modified Compressor using Full Stack	33

CHAPTER 1

INTRODUCTION

Dual stage 4:2 compressor helps in efficient performance and the main benefit we gain is consuming less power. In MOSFET technology, the use of multipliers has been increased which made developers to concentrate more on the performance of multipliers that consumes low power and minimum delay. This dual stage 4:2 compressor will make the work faster and the speed of operation which is inversely proportional to the delay of the system requires immense parallel operations that incur huge hardware and power dissipation. In dual stage 4:2 compressor, operation results in faster systems with different design complexity and consumption of power. Due to this changes in the designs it will not affect or reduce in accuracy and mainly it does not affect the normal operation for machine learning and multimedia applications. The importance of using dual stage 4:2 compressor it helps to detect variation and reduced the error of tolerance. It is used to design approximate arithmetic circuits for AI and DSP applications.

By introducing a module for error recovery, the proposed 4:2 approximate compressor that reduces the error profile of the compressor. The novel design for 4:2 compressor with an error rate of 12.5% was achieved by relaxing the constraints on area, delay and power. The proposed 4:2 compressor improves the image quality and the efficiency in image processing with 25% error rate. Energy and area efficient systems can be realised by relaxing the precision and reliability of the system. The dual stage compressor can be used for digital systems. The proposed compressors are utilized to implement in multipliers. Since we include more transistors it will not affect the area efficiency.

1.1 COMPRESSOR

The compressor is a useful element that is widely used in VLSI circuits and systems. It is generally used as a processing element. In this work, a 4:2 compressor has been designed with XOR-NOR module and multiplexer module.

The XOR-XNOR module is consists of six transistors and the multiplexer is consists of transmission gate. The compressor has been designed and simulated in Synopsystool by using 90nm CMOS technology. Average power dissipation, worst case delay and power delay product are computed. The same has been observed by varying the supply voltage. A study of the performance comparison has been carried out with existing compressors. It is found that the proposed compressor has low power consumption and the best Power Delay Product (PDP).

1.1.1 4:2 COMPRESSOR

A compressor circuit is denoted by the m-n compressor, where m and n represent inputs and outputs bits, respectively. It is also denoted as m:n. A 4-2 compressor is one of the popular compressors that are widely used in VLSI circuits and systems. It is used multiplier circuit to reduce partial products. Thus, it can reduce four partial products into two. Along with the 4 inputs and 2 outputs, 4-2 compressor has a carry input (Cin) from the previous operation and a carry output (Cout) to propagate. The block diagram is shown in Fig. 1. The inputs are A, B, C, D and Cin. The outputs are Sum, Carry and Cout.

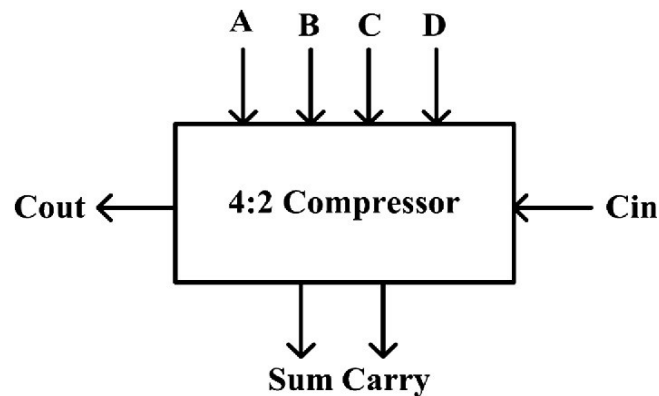


Fig 1.1 4:2 Compressor

It shows a conventional architecture of the 4-2 compressor by using XOR gates and MUX. It has more number of XOR gates that increase delay and power consumption. To address the delay and power consumption, a modified architecture has been designed as shown based on XOR-XNOR module and MUX.

1.2MULTIPLEXER

The multiplexer is a combinational logic circuit designed to switch one of several input lines to a single common output line. Multiplexing is the term used to describe the operation of sending one or more analogue or digital signals over a common transmission line at different times or speeds and as such, the device we use to do just that is called a Multiplexer. Multiplexers, or MUX's, can be either digital circuits made from high speed logic gates used to switch digital or binary data or they can be analogue types using transistors, MOSFET's or relays to switch one of the voltage or current inputs through to a single output.

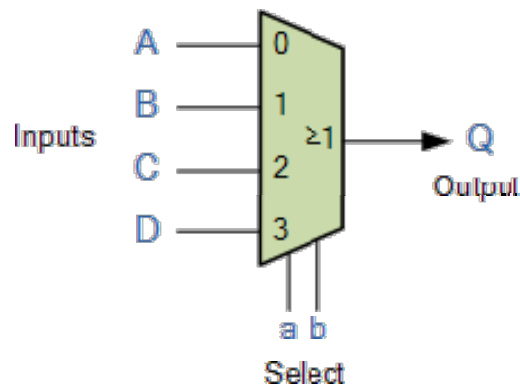


Fig 1.2 Multiplexer

Multiplexers are not limited to just switching a number of different input lines or channels to one common single output.

There are also types that can switch their inputs to multiple outputs and have arrangements or 4 to 2, 8 to 3 or even 16 to 4 etc. configurations and an example of a simple dual channel 4 input multiplexer. A multiplexer based design approach is used to generate SUM.s

1.2.1 Types of Multiplexer

Multiplexers are classified into four types

1. 2-1 multiplexer (1select line)
2. 4-1 multiplexer (2 select lines)
3. 8-1 multiplexer(3 select lines)
4. 16-1 multiplexer (4 select lines)

2-to-1 Multiplexer

A 2-to-1 multiplexer consists of two inputs D0 and D1, one select input S and one output Y. Depends on the select signal, the output is connected to either of the inputs. Since there are two input signals only two ways are possible to connect the inputs to the outputs, so one select is needed to do these operations.

If the select line is low, then the output will be switched to D0 input, whereas if select line is high, then the output will be switched to D1 input. The figure below shows the block diagram of a 2-to-1 multiplexer which connects two 1-bit inputs to a common destination.

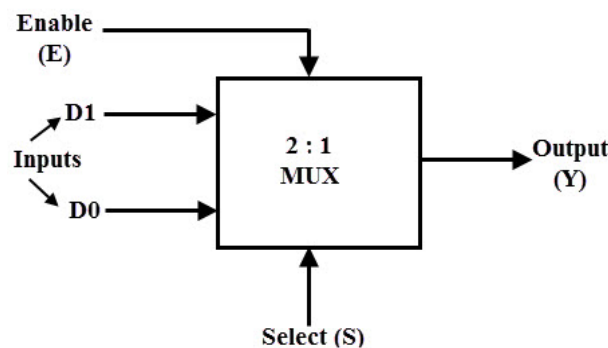


Fig 1.3 2-1 Multiplexer

The truth table of the 2-to-1 multiplexer is shown below. Depending on the selector switching the inputs are produced at outputs, i.e., D0, D1 and are switched to the output for S=0 and S=1 respectively. Thus, the Boolean expression for the output becomes D0 when S=0 and output is D1 when S=1.

Table 1.1 2*1 Mux Truth Table

Select	Inputs		Output
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

4-to-1 Multiplexer

The 4X1 multiplexer comprises 4-input bits, 1- output bit, and 2- control bits. The four input bits are namely 0, D1, D2, and D3, respectively; only one of the input bits is transmitted to the output. The output 'q' depends on the value of control input AB. The control bit AB decides which of the input data bit should transmit the output. The following figure shows the 4X1 multiplexer circuit diagram using AND gates. For example, when the control bits AB =00, then the higher AND gates are allowed while remaining AND gates are restricted. Thus, data input D0 is transmitted to the output 'q'.

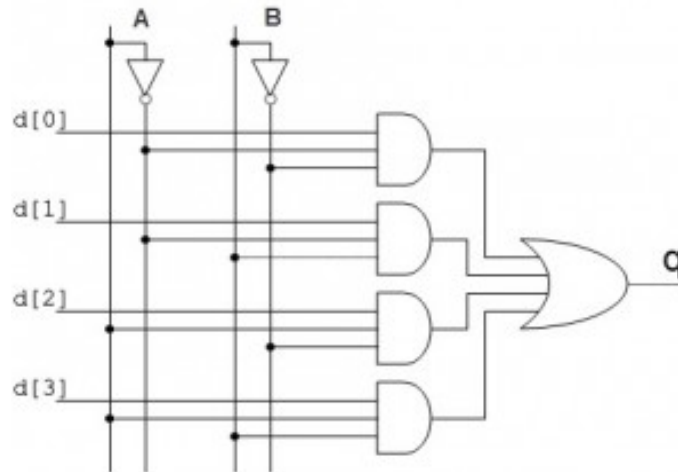


Fig 1.44-1 Multiplexer

If the control input is changed to 11, then all gates are restricted except the bottom AND gate. In this case, D3 is transmitted to the output, and $q = D_0$. If the control input is changed to $AB = 11$, all gates are disabled except the bottom AND gate. In this case, D3 is transmitted to the output, and $q = D_3$. The best example of a 4X1 multiplexer is IC 74153. In this IC, the output is the same as the input. Another example of a 4X1 multiplexer is IC 45352. In this IC, the output is the compliment of the input. The truth table of a 4-to-1 multiplexer is shown below in which four input combinations 00, 10, 01 and 11 on the select lines respectively switches the inputs D0, D2, D1 and D3 to the output. That means when $S_1=0$ and $S_0=0$, the output at Y is D0, similarly Y is D1 if the select inputs $S_1=0$ and $S_0=1$ and so on.

Table 1.2 4-1 Mux Truth Table

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

8-to-1 Multiplexer

The 8-to-1 multiplexer consists of 8 input lines, one output line, and 3 selection lines.

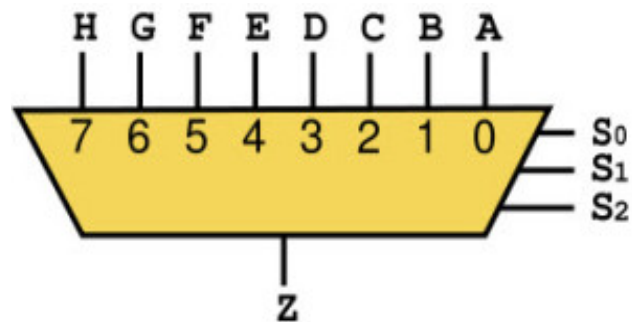


Fig 1.58-1 Multiplexer

8-1 Multiplexer Circuit

For the combination of a selection input, the data line is connected to the output line. The circuit shown below is an 8*1 multiplexer. The 8-to-1 multiplexer requires 8 AND gates, one OR gate, and 3 selection lines. As an input, the combination of selection inputs is giving to the AND gate with the corresponding input data lines. In a similar fashion, all the AND gates are given connection. In this 8*1 multiplexer, for any selection line input, one AND gate gives a value of 1 and the remaining all AND gates give 0. And, finally, by using OR gates, all the AND gates are added; and, this will be equal to the selected value.

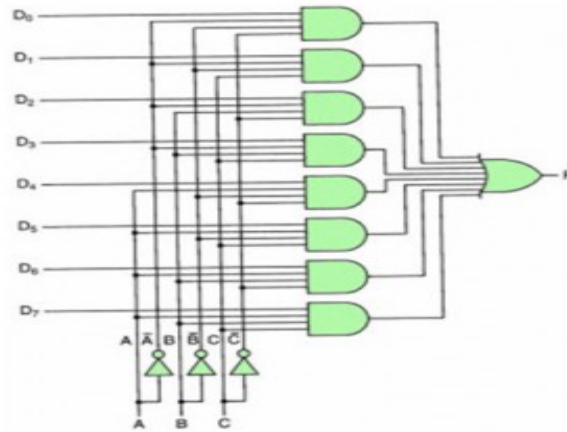


Fig 1.6 8-1 Multiplexer Circuit

The truth table for an 8-to1 multiplexer is given below with eight combinations of inputs so as to generate each output corresponds to input. For example, if $S_2 = 0$, $S_1 = 1$ and $S_0 = 0$ then the data output Y is equal to D_2 . Similarly the data outputs D_0 to D_7 will be selected through the combinations of S_2 , S_1 and S_0 as shown in below figure.

Table 1.3 8-1 Mux Truth Table

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

1.3GATES

A logic gate is a basic building block of a digital circuit that has two inputs and one output. The relationship between the input and the output is based on a certain logic. These gates are implemented using electronic switches like transistors, diodes. But, in practice, basic logic gates are built using CMOS technology, FETS, and MOSFET (Metal Oxide Semiconductor FETs). Logic gates are used in microprocessors, microcontrollers, embedded system applications, and in electronic and electrical project circuits.

The basic logic gates are classified into seven types: AND gate, OR gate, XOR gate, NAND gate, NOR gate, XNOR gate, and NOT gate. The truth table is used to show the logic gate function. All the logic gates have two inputs except the NOT gate, which has only one input. When drawing a truth table, the binary values 0 and 1 are used. Every possible combination depends on the number of inputs. If you don't know about the logic gates and their truth tables and need guidance on them, please go through the following infographic that gives an overview of logic gates with their symbols and truth tables. The basic logic gates are categorized into seven: AND, OR, XOR, NAND, NOR, XNOR, and NOT.

AND Gate

The AND gate is a digital logic gate with 'n' inputs one outputs, which performs logical conjunction based on the combinations of its inputs. The output of this gate is true only when all the inputs are true. When one or more inputs of the AND gates inputs are false, then only the output of the AND gate is false. The symbol and truth table of an AND gate with two inputs is shown below.

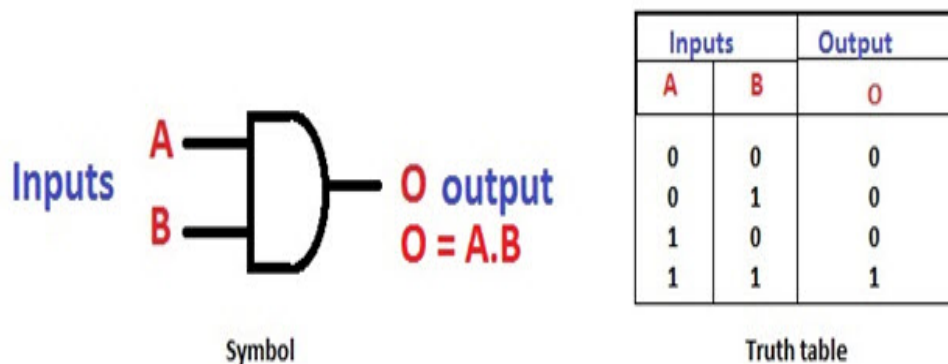


Fig 1.7 And Gate

OR Gate

The OR gate is a digital logic gate with 'n' inputs and one outputs, that performs logical conjunction based on the combinations of its inputs. The output of the OR gate is true only when one or more inputs are true. If all the inputs of the gate are false, then only the output of the OR gate is false. The symbol and truth table of an OR gate with two inputs is shown below.

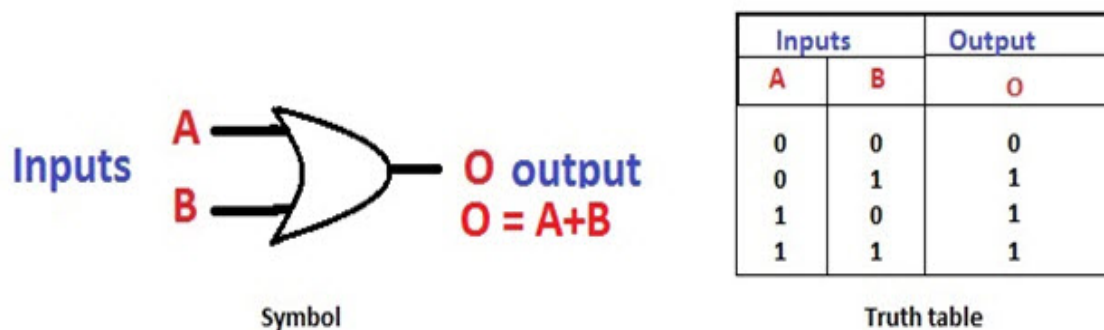


Fig 1.8 Or Gate

Exclusive-OR Gate (XOR GATE)

The Exclusive-OR (XOR) gate is a digital logic gate with two inputs and one output. The short form of this gate is Ex-OR. It performs based on the operation of the OR gate. . If any one of the inputs of this gate is high, then the output of the EX-OR gate will be high. The symbol and truth table of the EX-OR are shown below.

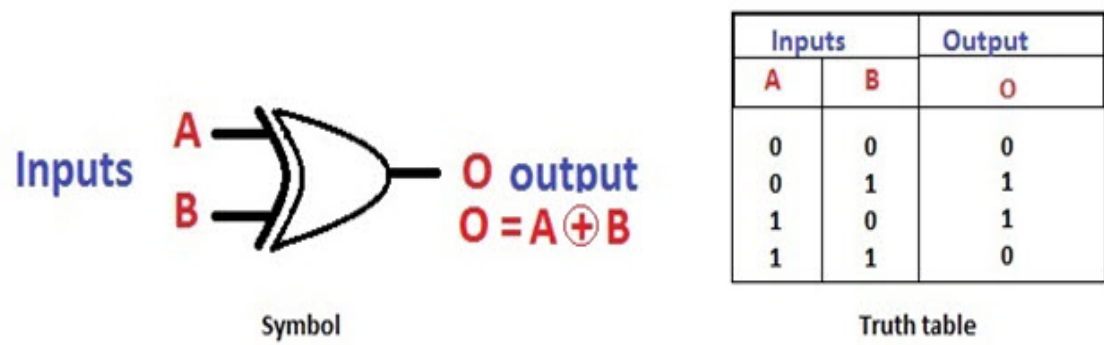


Fig 1.9 Xor Gate

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

This chapter discusses about the literature survey and summary, it also gives detailed ideas on the existing.

2.1 LITERATURE SURVEY

A.MOMENI, J.HAN, F.LOMBARDI (2015):

Designed and analysed the Dadda multiplier using two new approximate 4:2 compressors and to achieve low area and low power consumption. Two novel approximate 4:2 compressors have better delay and power consumption than the optimized 4:2 compressors. The multiplier is designed using these proposed compressors. The second module plays a pivotal role in terms of delay, power consumption and circuit complexity. Compressors have been widely used to speed up the CSA tree and decrease its power dissipation, so to achieve fast and low power operation. The use of approximate compressor in the CSA tree of a multiplier results in an approximate multiplier. This paper has initially focussed on compression as used in a multiplier. The approximate compressor reduce the transistor, power consumption and delay compared with an exact design. Therefore, it shows that an approximate design of an approximate compressor, multipliers can be designed for inexact computing; these multipliers offer significant advantages in terms of both circuit-level and error figures of merit.

M. Ha, S. Lee (2018):

Designed approximate multipliers with significantly decreased power, area, delay characteristics and a novel error recovery unit design. An improved multiplier design has been derived by manipulating the truth table entries the result in erroneous outputs in a 4:2 compressors. Carry propagation, shown with dashed and solid arrows in the diagram, only occurs in few places and in a non-cascading manner. Finally, error analysis show that the proposed multiplier design improves

mean error distance (MED) of multiplication results by 11.7% and more over previous approximate multiplier designs.

Using truncation and approximate compressors in the less significant bits of the partial end accumulator products results in decreased power consumption and circuit area. This design uses a small modification of an existing 4:2 compressor design that changes the error profile such that all errors results in slightly decreased values (over the exact values). The resulting error profile is such that all such error points can be easily located with a simple 2-input. The proposed 4:2 compressor can be used in the most significant bit position of the approximate region.

D. Esposito, E. Napoli, N. Petra (2018):

The present novel approximate compressor that overcome previously proposed circuits in terms of error performance and circuit complexity. The proposed approximate compressor is implemented by using AND-OR gates (no XOR gates are required) to minimize the error probability and the average error. By using the proposed approach, we have synthesized approximate multipliers for several operand lengths using a 40nm library. This provides approximate computing and it can be applied in several error-resilient applications like multimedia processing, data mining and recognition and machine learning. Applications to image filtering and to adaptive least mean squares filtering are also presented. The paper shows that the tolerable approximation level strongly depend on the application, motivating the need of energy-efficient design-time (or run-time) quality-configurable systems. In both image filtering and LMS system, proposed approximate multipliers show remarkable good results, compared with the state of art.

Y.-J. Chang, Y.-C. Cheng, Y.-F. Lin, S.-C. Liao, C.-H. Lai (2019):

In this case, novel 4:2 imprecise compressor is used which helps in improving energy-quality efficiency of image processing applications and error rate. The multiplier which uses the proposed imprecise design can save power consumption and improve in delay. The truth table of precise 4:2 compressor in image processing to implement the proposed imprecise 4:2 compressor. According to the pattern distribution and value difference of image outputs, resynthesize the 4:2 compressor in imprecise style.

For further simulation, the multiplier with the proposed design is used in image processing applications. It provides at the gate level, such as gate count, power consumption, latency, error rate and good image quality with high energy efficiency. It shows that the multiplier with the proposed imprecise 4:2 compressor can improve PSNR about 50% on average. Compared to precise 4:2 compressor, the proposed 4:2 compressor can reduce power consumption-56% and delay-39%. Therefore, multiplier M3 which adopts the proposed imprecise 4:2 compressor can achieve PSNR and MSSIM above 33 and 0.99 in average, respectively. The image of quality of their design is good for human perception because peak signal to noise ratio (PSNR) values are more than 33.

K. Manikantta Reddy, M. H. Vasantha, Y. B. N. Kumar (2019):

Assessed the effectiveness of multiplier by some of the image processing applications. For the effective utilization of the proposed compressor and to reduce the error of the output and modified architecture of Dadda multiplier is proposed. The input C_{in} and output C_{out} in the conventional 4:2compressor are completely ignored in the design of approximate 4:2 compressor. The full adder takes the input X_3, X_2, X_1 and produces the outputs S, C . The outputs signal of approximate compressors are denoted by 'SUM' and 'CARRY' to differentiate from exact compressors outputs. The proposed approximate 4:2 compressor design shows least error rate (12.4%) and ED (± 1) compared to the other approximate compressors. The multiplier can be designed for approximate computing by an approximate design of compressor; this multiplier offers advantages in terms of design parameters compared to exact multipliers, and in terms of accuracy metrics compared to the other approximate multipliers present in the literature.

PRANOSE J. EDAVOOR, SITHARA RAVEENDRAN (2020):

Increased the performance efficiency for dual stage 4:2 compressor for high speed multimedia applications. Maintained the balance between delay, area and power by approximate computing. Optimised the hardware utilisation of the proposed design, this paper proposed an alternate architecture for multipliers with more than 3 stages of cascaded compressors.

The modified dual stage 4:2 compressors reduces area, delay and power dissipation compared to proposed high speed area-efficient 4:2 compressor and other compressors in the literature due to the reduction in transistor count. The propose modified dual stage 4:2 compressor has the same output in cascaded architectures with 18.23% and 14.84% reduction in area and power respectively when compared to proposed high speed area efficient 4:2 compressor. The accuracy remains unaffected with the modifications introduced. The paper propose the modified dual stage compressor, which further optimized the area, delay and power without altering the accuracy metrics. The architecture was designed and implemented at the transistor level 45nm technology with the supply voltage of 1V. The design was validated using 8*8, 16*16 Dadda multiplier in image processing applications, like image multiplication and smoothing.

2.2 LITERATURE SUMMARY

Several designs have been proposed for faster analysis and performance of the architectures of dual stage 4:2 compressor using different types of techniques. These designs made several trade-offs between area, delay and power. The main idea of this project is to compare the parameters of high speed multimedia applications using dual stage 4:2 compressor.

CHAPTER 3

EXISTING SYSTEM

The existing area-efficient 4:2 approximate compressor has inputs A1, A2, A3 and A4, outputs are CARRY and SUM. In proposed modified Dual-stage 4:2 compressor architecture MUX, one XOR, one AND and two OR gates are required. Since OR and AND gates each need 6 transistors to avoid this transistor count an architecture is proposed with NAND and NOR gates.

A multiplexer (MUX) based design approach is used to generate SUM. Output of XOR gate acts as the select line for the MUX. When the select line is high (A3A4) is selected and when the select line is low (A3+A4) is selected. The proposed 4:2 compressor is able to reduce carry generation logic to an OR gate by introducing an error distance 1 in the truth table of the exact compressor.

Logical expressions for realization of SUM and CARRY:

$$SUM = (A_1 \oplus A_2)A_3A_4 + (A_1 \oplus A_2)(A_3 + A_4)$$

$$CARRY = A_1 + A_2$$

To optimise the hardware utilisation of the design, an alternate architecture for multipliers with more than three stages of cascaded compressors is proposed. Even though the SUM and CARRY generated by the modified architecture is not as same as that of the proposed 4 : 2 compressor architecture, with cascading of the compressor in multiples of 2, the error is nullified.

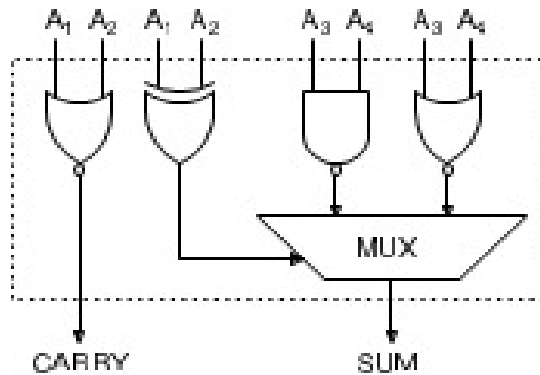


Fig 3.1 Basic block of Dual-stage 4:2 compressor

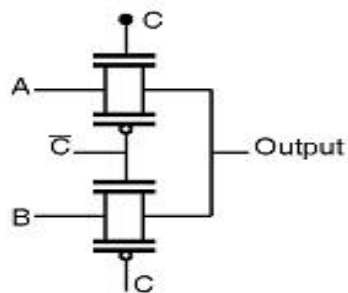
The outputs at the Stage 1 differ for both the architectures, but the occurrence of negation in the order of an integral multiple of two in the modified dual-stage 4:2 compressor will ensure that the outputs at Stage 2 are same. The modified dual-stage 4:2 compressor reduces area, delay and power dissipation compared to the proposed high speed area-efficient 4:2 compressor and other compressors in the literature due to the reduction in transistor count.

3.1 2:1 MUX

A 2:1 multiplexer selects either input A or B on the basis of the value of the control signal 'C'. When control signal C is logic low the output is equal to the input A and when control signal C is logic high the output is equal to the input B. A 2:1 multiplexer can be implemented using transmission gates. The 2:1 MUX selects either A or B depending upon the control signal C. This is equivalent to implementing the Boolean function,

$$F = (A \times C + B \times \neg C)$$

When the control signal C is high then the upper transmission gate is ON and it passes A through it so that output = A. When the control signal C is low then the upper transmission gate turns OFF and it will not allow A to pass through it, at the same time the lower transmission gate is 'ON' and it allows B to pass through it so the output = B.



2 : 1 MUX using transmission gate

Fig 3.2 2:1 Mux Using Transmission Gate

3.2 OR GATE

The implementation of OR function using NMOS transistors only. In this gate if the B input is high the right NMOS is turned ON and copies logic 1 to F and this operation does not affected by 'A' input. When B is low the left NMOS is turned ON the logic of 'A' is copied to the output F.

The input variables are controlling the pMOS and transmission gate. The upper branch passes data when $A = 1$, and transmission gate passes B when $A = 0$.

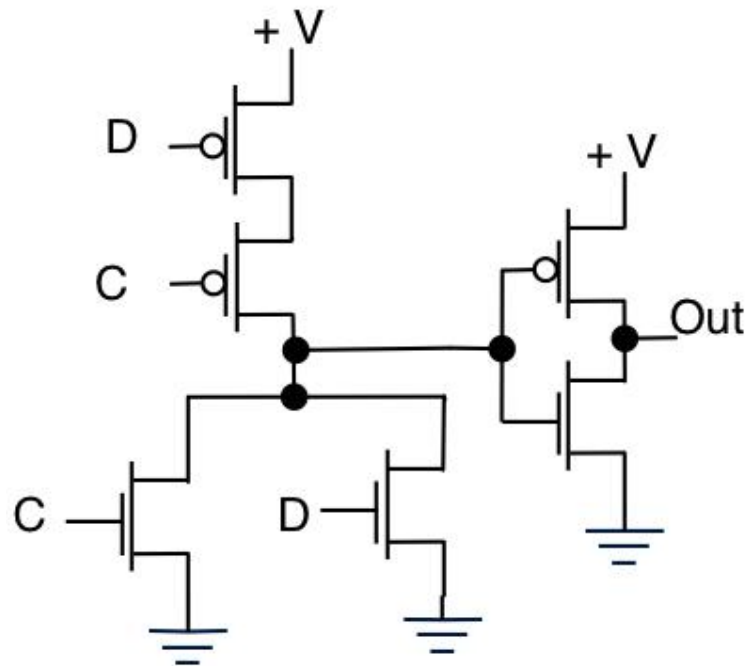


Fig 3.3 Or Gate Using Transmission Gate

3.3 XOR GATE

In this gate if the B input is low then left NMOS transistor is ON and the logic value of A is copied to the output F.

When B input is high right NMOS transistor is ON and the inverted logic value of A is copied to the output F, which satisfies the truth table of the XOR gate.

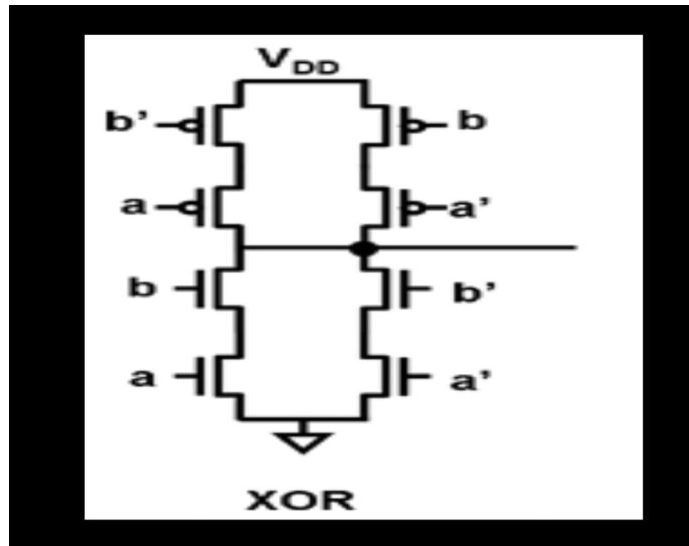


Fig 3.4 Xor Using Transmission Gate

3.4 NAND GATE

Whenever at least one of the inputs is low, the corresponding PMOS transistor will be conducting while the NMOS transistor will be closed. Consequently, the output voltage will be high. Conversely, if both inputs are high, then both PMOS transistors at the top will be open circuits and both NMOS transistors will be conducting. Hence, the output voltage is low. The function of this gate can be summarized by the table. If logical 1's are associated with high voltages then the function of this gate is called NAND for negated AND. Again, there is never a conducting path from the supply voltage to ground.

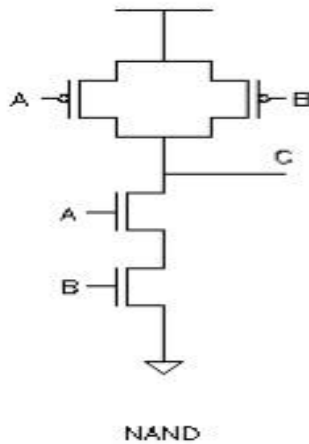


Fig 3.5 Nand Using Transmission Gate

3.5 NOR GATE

Whenever at least one of the inputs is high, the corresponding N-type transistor will be closed while the P-type transistor will be open. Consequently, the output voltage will be low. Conversely, if both inputs are low, then both P-type transistors at the top will be closed circuits and the N-type transistors will be open. Hence, the output voltage is high. The function of this gate can be summarized by the table. If logical 1's are associated with high voltages then the function of this gate is called NOR for negated OR. Again, there is never a conducting path from the supply voltage to ground.

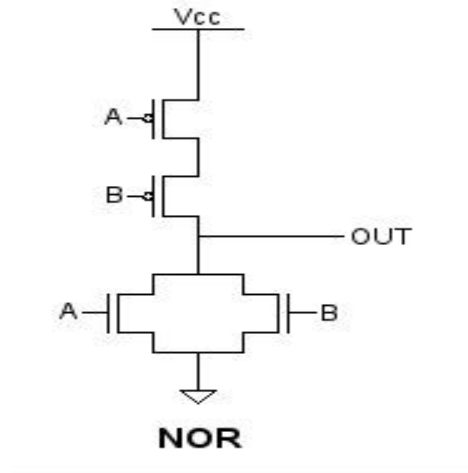


Fig 3.6 Nor Using Transmisson Gate

3.6 AND GATE

The AND gate is a digital logic gate with 'n' inputs one outputs, which performs logical conjunction based on the combinations of its inputs. The output of this gate is true only when all the inputs are true. When one or more inputs of the AND gates inputs are false, then only the output of the AND gate is false.

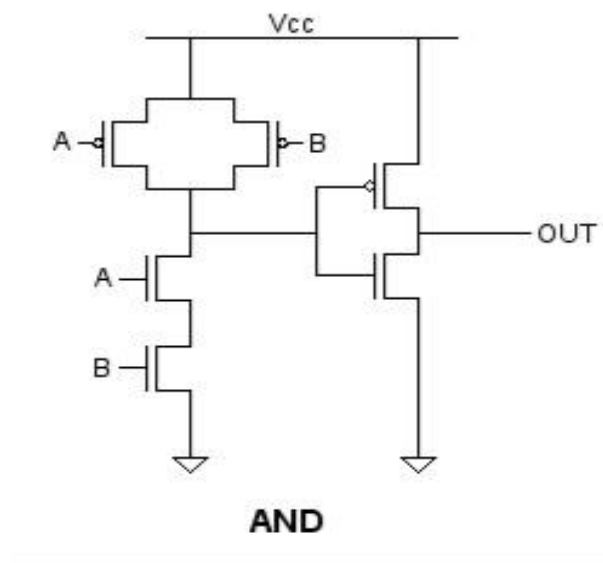


Fig 3.7 And Using Transmission Gate

CHAPTER 4

MODIFIED DUAL STAGE 4:2 COMPRESSOR USING STACK TECHNIQUE

In existing work it is designed using 4:2 compressors architecture. In the proposed system the 4:2 compressor is designed by implementing forced stack technique which give low power and area compared to existing system. By using stack method, it trade-offs to reduce to low power and it reduces the leakage of current when flows from one transistor to other transistor.

4.1 STACK TECHNIQUE

In forced stack technique, which forces a stack affect by breaking down an existing transistor into two half size transistors. Subthreshold leakage is exponentially related to the threshold voltage of the device, and the threshold voltage changes due to body effect. From these tow facts, one can reduce the subthreshold leakage in the device by stacking two or more serially.

Forced stack is also known as Back Biasing to Reduce Sub Threshold Leakage. Leakage is well known to be a major issue in nanometre VLSI circuits, as it has become a major portion of the overall power budget. The problem is particularly critical in circuits and cells that intrinsically have a considerably high leakage under a given transistor size (e.g., inverters, since they cannot benefit from stack effect). Leakage is exacerbated in circuits driving heavily loaded nodes, as it occurs for buffers, which are usually oversized to achieve a targeted delay. This work is focused on circuits where stack forcing is employed to reduce leakage, as in inverters and heavily loaded tapered buffers. In low-standby current applications, forced stacks are widely adopted to reduce the leakage of each inverter (and hence of the overall buffer). In this approach, a single transistor is replaced by two stacked transistors with halved aspect ratio.

Stack forcing tends to be less effective in downscaled technologies, hence low-standby power applications typically require the adoption of additional techniques to further reduce leakage. This happens due to the reduction of gate to source voltage and reduction of DIBL coefficient due to lower drain to source potential thereby further reducing leakage.

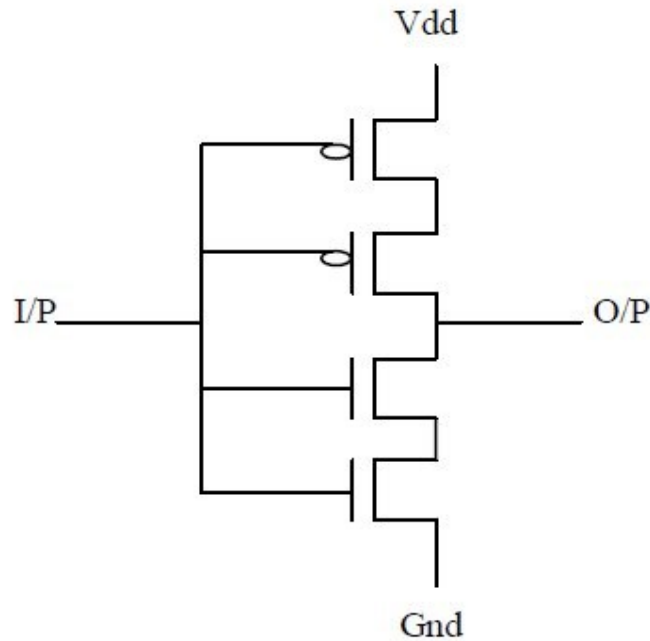


Fig 4.1 Stack Diagram

Leakage power consumption is an important issue in CMOS VLSI circuits. The main contribution of Power Dissipation in CMOS circuit increases with the reduction of channel length, Threshold voltage and gate oxide thickness.

Subthreshold leakage current (I_{sub}) in MOS transistors, which occurs the gate voltage is below the threshold voltage and mainly, consists of diffusion current.

4.2 MODIFIED DUAL STAGE 4:2 COMPRESSOR USING STACK TECHNIQUE

In proposed system the forced stack is applied to the dual stage 4:2 compressors which consume less power. By adding forced stack novel technique it reduce it by half. Its transistors are dived by half its ratio, and consume less power when compare to exiting system.

Therefore, in proposed system to compare the results better, have changed the length of each gate level into 130nm and 32nm and observed the parameters such as area, power and power delay product.

The dependence of subthreshold current is exploited by the transistor stacking effect and an increase in the source voltage V_s of the transistor reduces the sub-threshold leakage current exponentially. More leakage power savings can be obtained by increasing the number of transistors connected in stack structure. For circuits without stacking structure, forced stacking can be implemented. In forced stacking, a single transistor of width " W " can be replaced by two transistors of width " $W/2$ " each. This results in two transistors switching off at the same time reducing leakage current.

4.3 2*1 MUX USING STACK TECHNIQUE

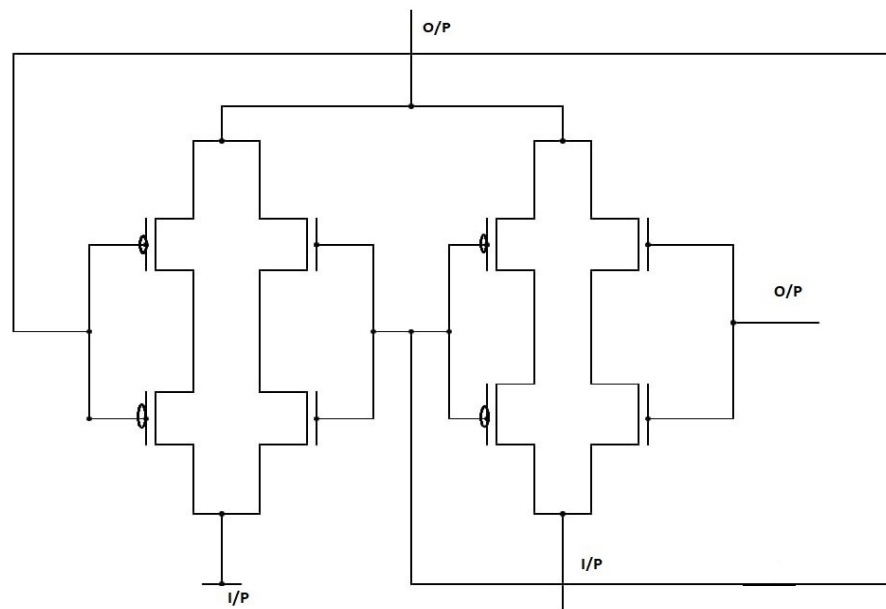


Fig 4.2 2*1 Mux Using Stack Technique

4.4 OR GATE USING STACK TECHNIQUE

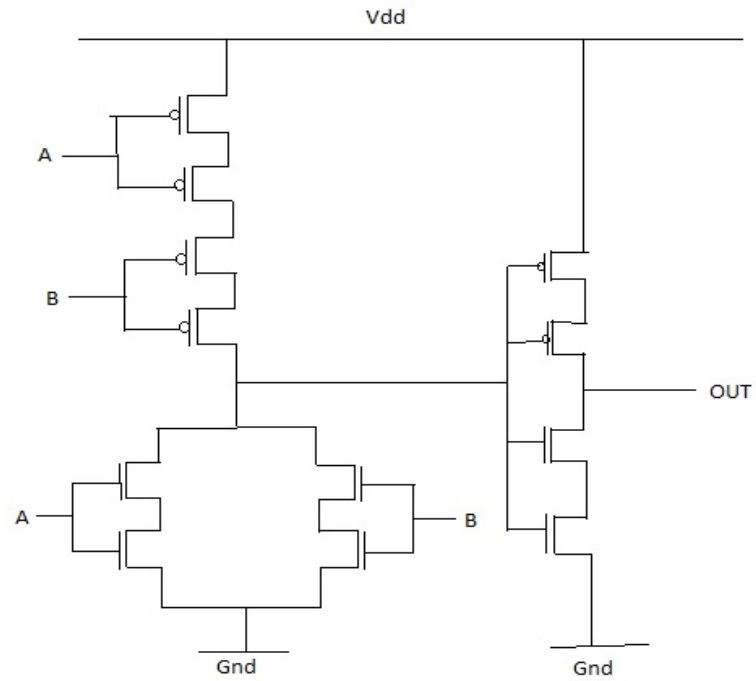


Fig 4.3 Or Gate Using Stack Technique

4.5 AND GATE USING STACK TECHNIQUE

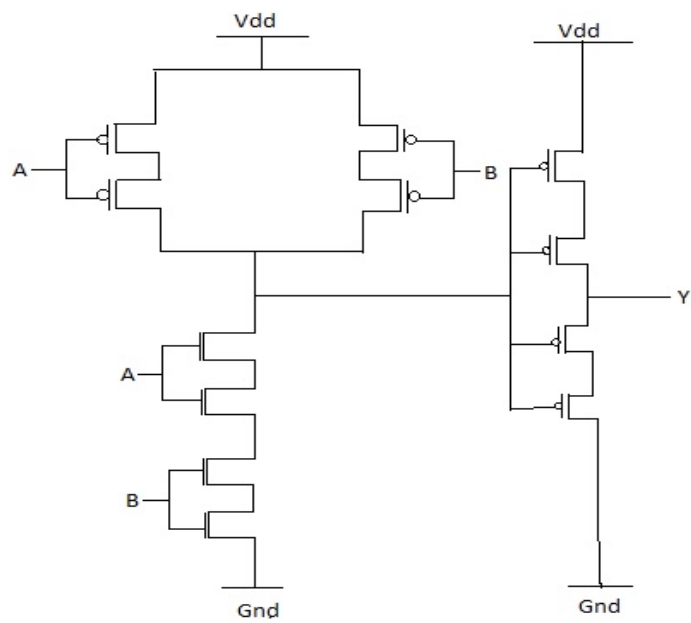


Fig 4.4 And Gate Using Stack Technique

4.6 XOR GATE USING STACK TECHNIQUE

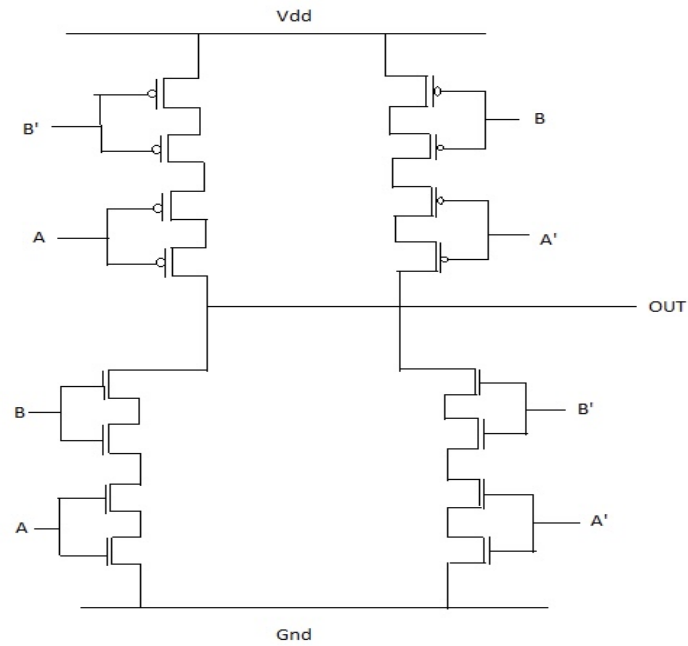


Fig 4.5 Xor Gate Using Stack Technique

CHAPTER 5

RESULTS AND DISCUSSION

The existing and proposed architecture are simulated by using MODELSIM simulator output of the existing High area-efficient 4:2 compressor and proposed High area-efficient 4:2 compressor are analysed from the result and it is concluded that the proposed architecture reduces the power compared with existing system. The synthesis is done using HSPICE

5.1 SIMULATION RESULTS

5.1.1 4-2 COMPRESSORS SIMULATION OUTPUT

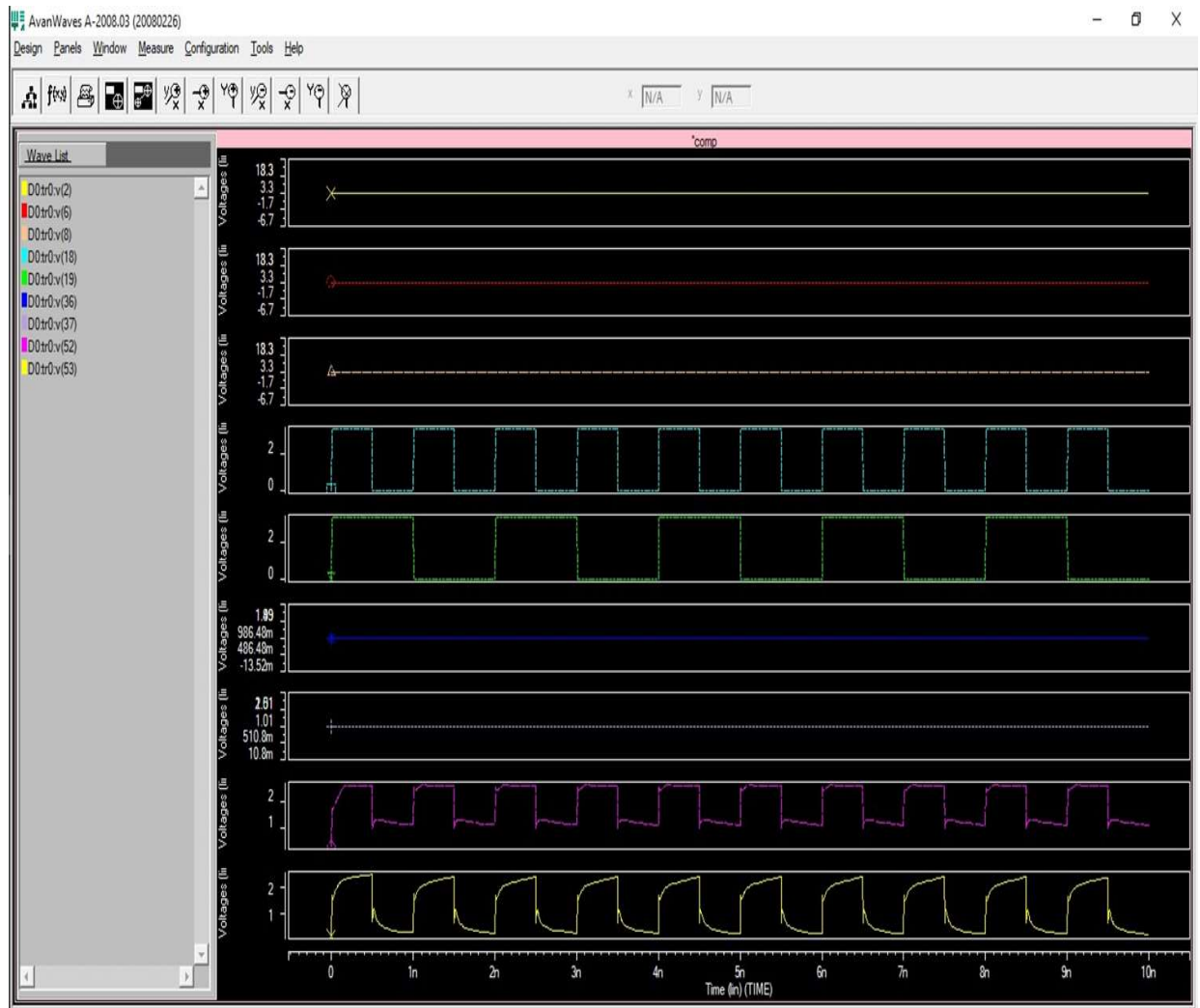


Fig 5.1 4-2 Compressors Simulation Output

5.1.2 2*1 MUX SIMULATION OUTPUT

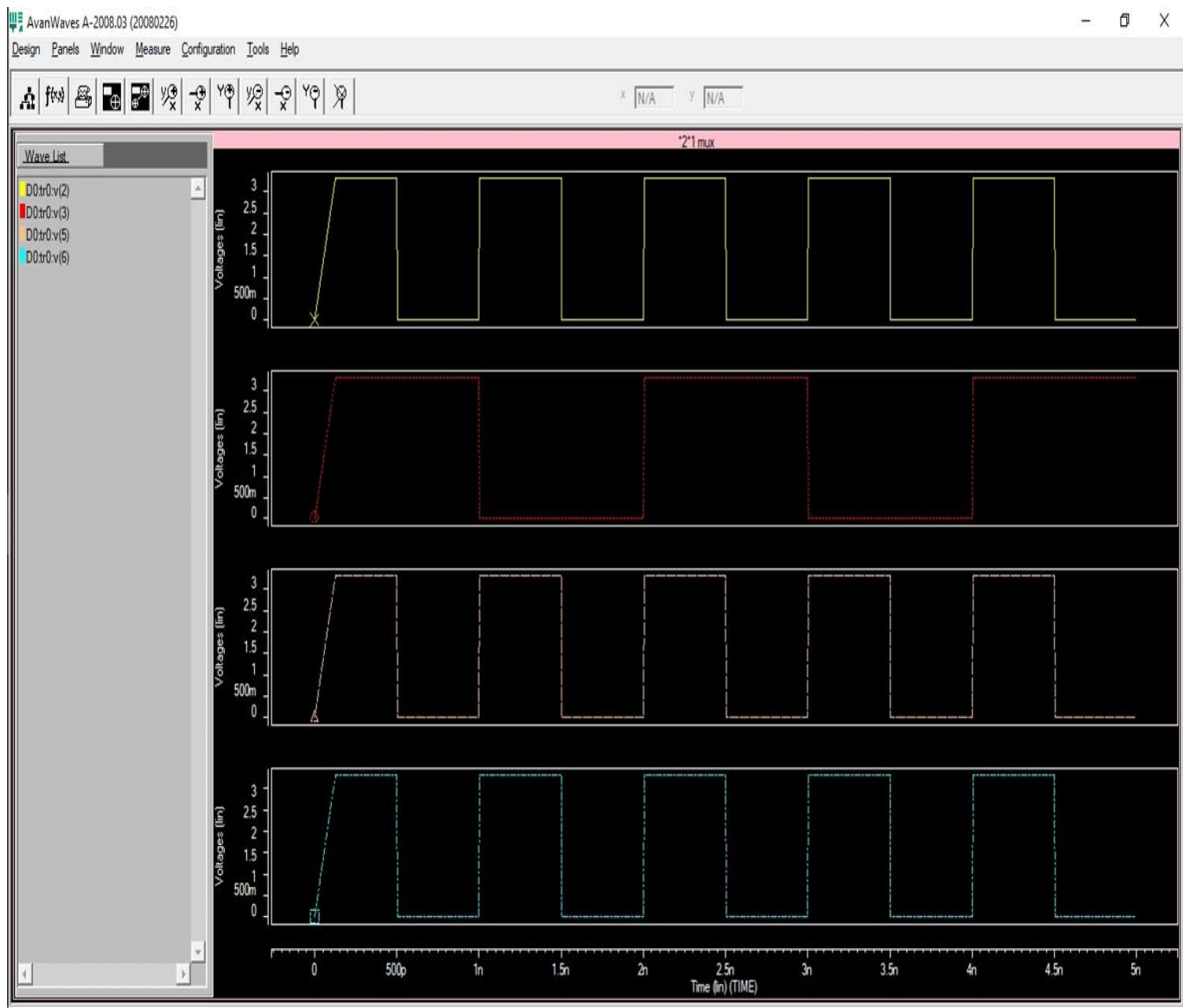


Fig 5.22*1 Mux Simulation Output

5.1.3 OR GATE SIMULATION OUTPUT

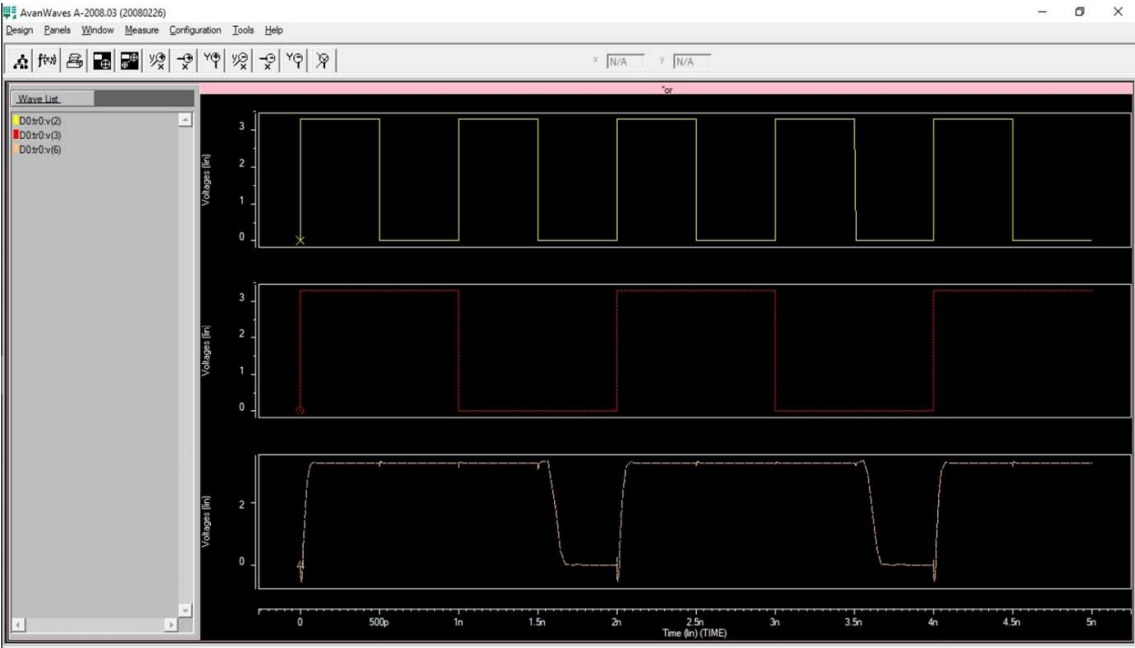


Fig 5.3 Or Gate Simulation Output

5.1.4 AND GATE SIMULATION OUTPUT

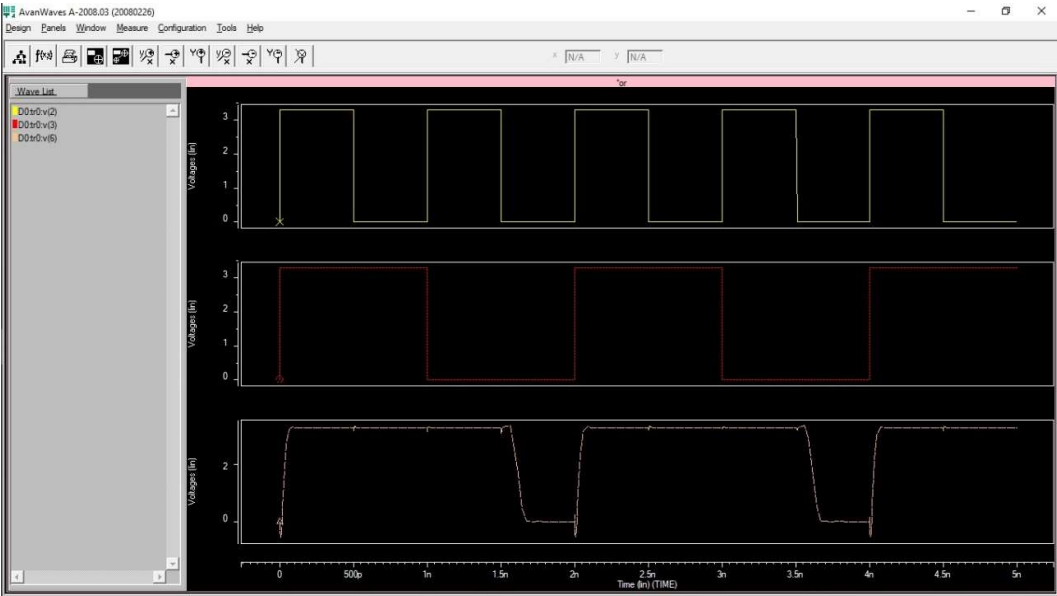


Fig 5.4 And Gate Simulation Output

5.1.5XOR GATE SIMULATION OUTPUT

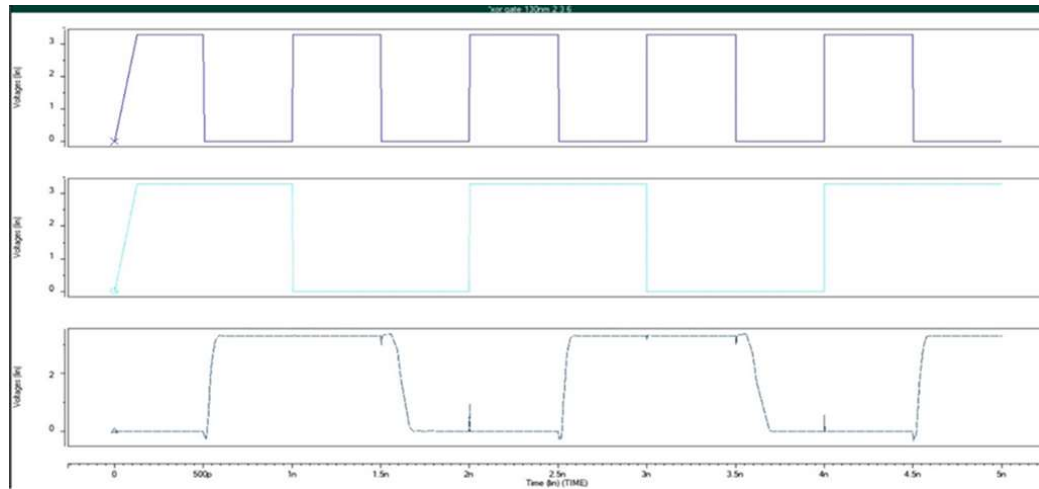


Fig 5.5 Xor Gate Simulation Output

5.1.6SIMULATION RESULTS OF 2:1 MULTIPLEXER

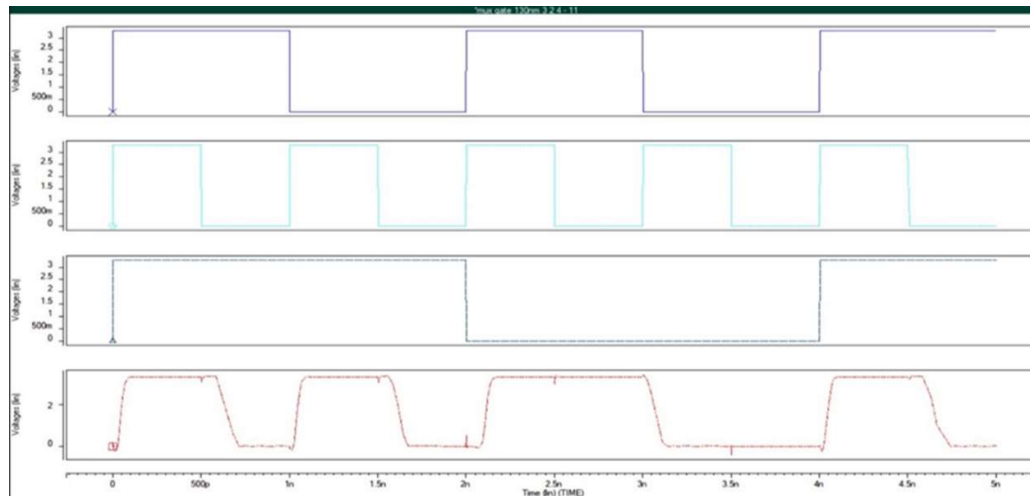


Fig 5.6 Simulation Results Of 2:1 Multiplexer

5.1.7 SIMULATION RESULTS OF MODIFIED 4:2 COMPRESSOR

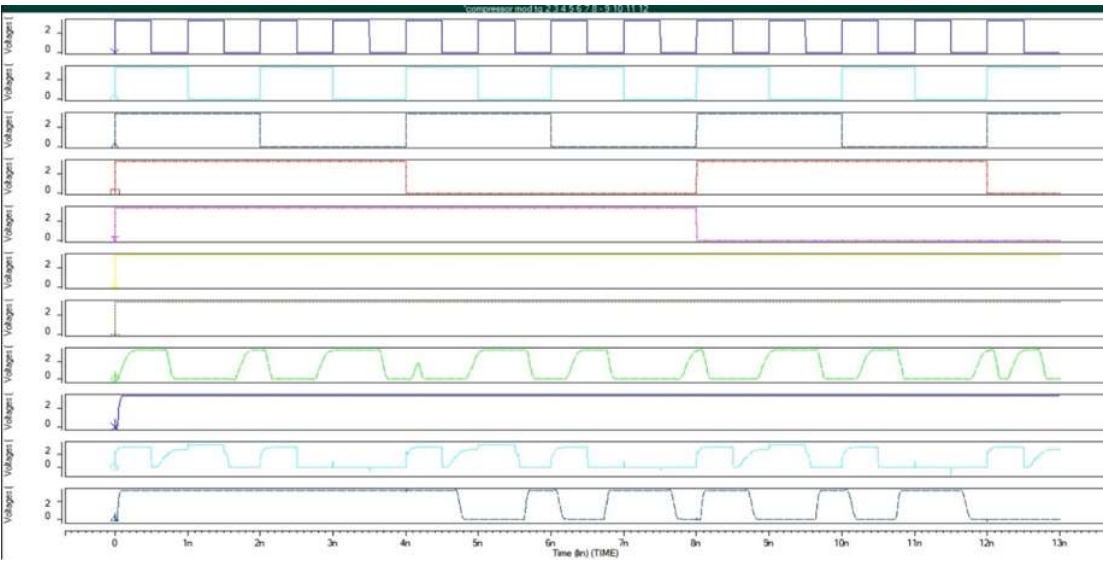


Fig 5.7 Simulation Results Of Modified 4:2 Compressor

5.1.8 SIMULATION RESULTS OF MULTIPLIER USING 4:2 COMPRESSOR

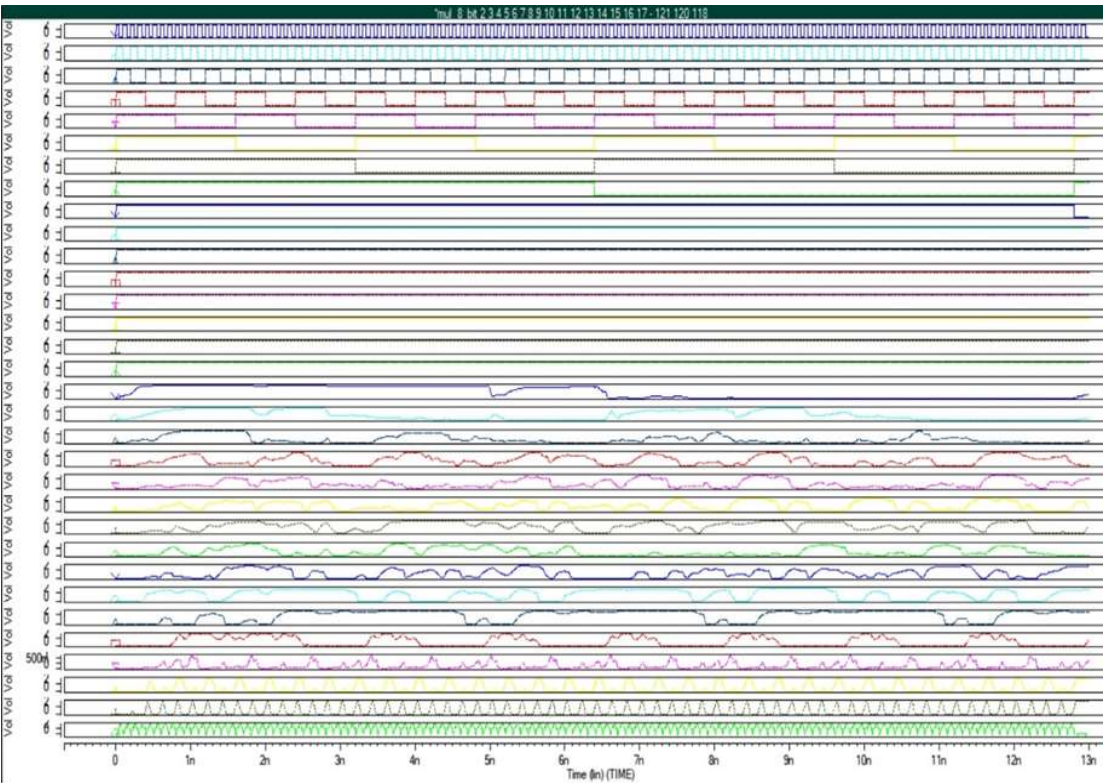


Fig 5.8 Simulation Results Of Multiplier Using 4:2 Compressor

5.2 PERFORMANCE ANALYSIS

5.2.1 PERFORMANCE ANALYSIS OF 130nm COMPRESSOR

TABLE 5.1 PERFORMANCE ANALYSIS OF 130nm COMPRESSOR

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	17.90u	54.25p	971.075a
XOR	17.15u	55.21p	946.8515a
AND	16.34u	25.69p	419.7746a
MUX	41.047u	54.21p	2225.157a
COMPRESSOR	93.80u	65.21p	6116.698a

5.2.2 PERFORMANCE ANALYSIS OF 130nm MODIFIED COMPRESSOR using P-STACK

TABLE 5.2 PERFORMANCE ANALYSIS OF 130nm MODIFIED COMPRESSOR
using P-STACK

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	14.21u	51.25p	728.2625a
XOR	16.25u	52.12p	846.95a
AND	11.25u	23.56p	265.05a
MUX	38.26u	51.24p	1960.4424a
COMPRESSOR	89.56u	60.12p	5384.347a

5.2.3 PERFORMANCE ANALYSIS OF 130nm MODIFIED COMPRESSOR using N-STACK

TABLE 5.3 PERFORMANCE ANALYSIS OF 130nm MODIFIED COMPRESSOR using N-STACK

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	11.01u	50.23p	553.0323a
XOR	14.25u	51.22p	729.885a
AND	10.12u	21.89p	221.5268a
MUX	35.26u	50.21p	1770.4046a
COMPRESSOR	85.26u	58.65p	5000.499a

5.2.4 PERFORMANCE ANALYSIS OF 130nm MODIFIED COMPRESSOR using FULL-STACK

TABLE 5.4 PERFORMANCE ANALYSIS OF 130nm MODIFIED COMPRESSOR using FULL-STACK

DEVICE	POWER(W)	DELYA(S)	PDP (J)
OR	9.59u	48.36p	463.772a
XOR	11.25u	49.58p	557.775a
AND	9.56u	19.56p	186.993a
MUX	32.59u	48.59p	1583.548a
COMPRESSOR	80.25u	56.26p	4514.865a

5.2.5 PERFORMANCE ANALYSIS OF 32nm COMPRESSOR

TABLE 5.5 PERFORMANCE ANALYSIS OF 32nm COMPRESSOR

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	7.58u	46.25p	350.575a
XOR	9.56u	48.52p	463.851a
AND	8.45u	18.25p	154.212a
MUX	30.25u	47.25p	1429.312a
COMPRESSOR	78.25u	54.25p	4245.062a

5.2.6 PERFORMANCE ANALYSIS OF 32nm MODIFIED COMPRESSOR using P-STACK

TABLE 5.6 PERFORMANCE ANALYSIS OF 32nm COMPRESSOR using N-STACK

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	6.23u	38.25p	238.297a
XOR	7.85u	46.52p	365.182a
AND	7.12u	16.33p	116.269a
MUX	24.23u	45.13p	1093.4999a
COMPRESSOR	69.25u	52.12p	3609.31a

5.2.7 PERFORMANCE ANALYSIS OF 32nm MODIFIED COMPRESSOR using N-STACK

TABLE 5.7 PERFORMANCE ANALYSIS OF 32nm MODIFIED COMPRESSOR
using N-STACK

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	5.12u	36.58p	187.289a
XOR	6.58u	44.15p	290.507a
AND	6.33u	15.23p	96.4059a
MUX	21.56u	43.12p	929.667a
COMPRESSOR	62.15u	50.12p	3114.958a

5.2.8 PERFORMANCE ANALYSIS OF 32nm MODIFIED COMPRESSOR using FULL-STACK

TABLE 5.8 PERFORMANCE ANALYSIS OF 32nm MODIFIED COMPRESSOR
using FULL-STACK

DEVICE	POWER(W)	DELAY(S)	PDP (J)
OR	4.85u	34.12p	165.482a
XOR	6.01u	42.15p	253.321a
AND	5.56u	13.25p	73.67a
MUX	18.54u	41.55p	770.337a
COMPRESSOR	59.12u	48.25p	2852.54a

CHAPTER 6

CONCLUSION AND SUMMARY

A new technique is proposed to design stack technique using unique replacement of stack transistors, which gives better response in terms of average power and delay in comparison to the conventional stack technique. We have achieved a design of a stack technique using a 4:2 area-efficient dual stage compressor which has reduced the power to 3.125×10^{-4} watt and reduced the delay of the multiplier considerably. Since our objective was to reduce the power of the multiplier and it has been reduced by 3.125×10^{-4} watt, hence we achieved our objective. We propose a novel technique called STACK for designing High area-efficient 4:2 dual stage compressor which significantly cuts down the leakage current without increasing the dynamic power dissipation. This increases the resistance of the path from V_{DD} to ground, leading to significant decrease in leakage currents. The gate-level netlist of the given circuit is first converted into a static CMOS complex gate implementation and then STACK techniques are introduced to obtain a leakage-controlled circuit. Further, the proposed technique overcomes the limitations posed by other existing methods for leakage reduction. From the results obtained it can be verified that there is a significant amount of reduction in power dissipation of the circuits when STACK technique was used. Low power consumption in turn increases the efficiency of the overall system when compared to the existing systems. The significant feature of stack is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction compared to other techniques.

Further, the proposed technique overcomes the limitations posed by other existing methods for leakage reduction. An analysis of a High area-efficient 4:2 dual stage compressor has been designed using stack 130nm and 32nm MOSFET technology.

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