

PERFORMANCE ANALYSIS OF AN EFFICIENT SRAM ARRAY ARCHITECTURE USING FINFET TECHNOLOGY

Submitted in partial fulfilment of requirements for the award of
Bachelor of Engineering in
Electronics and Communication Engineering

by

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SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of MUKKA SUSHITHA REDDY (Reg.No.37130258) and LOKAM SAI SUPRIYA (Reg.No.37130221) who carried out the project entitled "**PERFORMANCE ANALYSIS OF AN EFFICIENT SRAM ARRAY ARCHITECTURE USING FINFET TECHNOLOGY**" under our supervision from December 2020 to March 2021.

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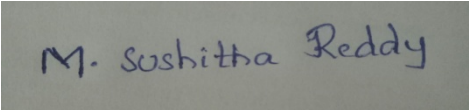
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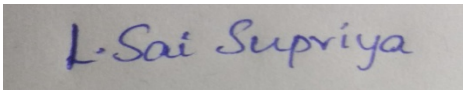
DECLARATION

We, MUKKA SUSHITHA REDDY (Reg.No. 37130258) and LOKAM SAI SUPRIYA (Reg.No.37130221) hereby declare that the Project Report entitled “**PERFORMANCE ANALYSIS OF AN EFFICIENT SRAM ARRAY ARCHITECTURE USING FINFET TECHNOLOGY**” done by us under the guidance of Mr.MATHAN N.,M.Tech.,(Ph.D), Assistance Professor is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

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ABSTRACT

Nanotechnology developments contribute to transistor shrinkage to area of the nanotechnology. However, due to the scaling of transistors such as short channel effects (SCEs) and threshold voltage (V_{th}) problems, there are several problems. FINFET (Fine Field Effect Transistor) is an alternative technology for solving traditional MOSFET flat problems and improving the efficiency and metallic properties of the Static Random-Access-Memory (SRAM) circuit design, thanks to its neutrally thin material. SRAMs that are primarily used as a memory cache are more reliable and fast for high-speed operations. The conflict in the size of the access transistor affects the classical 6T SRAM, which results in read and write stability. This project explores the stability performance of 7nm FINFET based 8T SRAM cell in retention, read and write mode. The 7 nm FINFET-based 6T and 8T SRAMs were compared to the MOSFET performances. The SRAM model is designed and simulated using 7nm technology in the tool Synopsys HSpice. To obtain and analyze the noise level on the basis of reading, writing, and retention, the butterfly curve is extracted by means of the voltage transfer curve (VTC) of two cross-connected FINFET inverters. Two more n-finfets are added to the 8T SRAM cell in order to separate read and write operating path for improved readability. The traditional 6T SRAM cell will be operated by the Read Word line (RWL). The results show that both FINFET and MOSFET 8T cell SRAM deliver better power consumption and efficiency in Static Noise Margin (SNM) than 6T cells.

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LIST OF SYMBOLS AND ABBREVIATIONS

SCES	SHORT CHANNEL EFFECTS
VTH	THRESHOLD VOLTAGE
VTC	VOLTAGE TRANSFER CHARACTERISTICS
SNM	THE STATIC NOISE MARGIN
RNM	READ NOISE MARGIN
WNM	WRITE NOISE MARGIN
RM AND WM	READ AND WRITE MARGINS
DGFET	DOUBLE-GATE MOSFET

RDF	RANDOM DOPANT FLUCTUATION
PDP	POWER-DELAY-PRODUCT
DIBL	DRAIN INDUCED BARRIER LOWERING
QG	QUADRUPLE GATE
WSNM	WRITE STATIC NOISE MARGIN
RSNM	READ STATIC NOISE MARGIN
GNERFET	GRAPHENE NANORIBBON FIELD-EFFECT TRANSISTOR
RAM	RANDOM ACCESS MEMORY
SRAM	STATIC RAM
SA	SENSE AMPLIFIERS
SOI	SILICON ON INSULATOR
SG	SHORT GATE
IG	INDEPENDENT GATE
WWL	WORD LINE
RWL	READ WORD LINE

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

With the introduction of portable devices, there is a growing demand for statical random access memory in high-performance VLSI and microprocessor systems with extensive SRAM. The focus for research work has been on optimization of SRAM, as memory structures occupy a large portion of the microprocessor chip region. As the leakage current in a single cache cell is high, reducing it helps to reduce a significant fraction of the total power in the microprocessor. The optimisation of performance parameters would lead to overall chip performance optimisation. The scaling of CMOS has brought digital circuits to develop performance. However, the size of the transistors such as short channel effects (SCEs) and the threshold voltage (V_{th}) roll-off problems presents major problems for this form of technology. In order to solve these problems, the FINFET-based SRAM design was proposed as an alternative to large devices for low-performance DMC technology.

A robustness measurement of an SRAM cell during reading is known as reading stability. When the word line of the cell should be disabled, the stability to maintain is determined by fitting the largest square into the voltage transfer characterstica (VTC) of the coupling inverters in the SRAM array. SRAM cells are important for read- and hold-stability in the SRAM FINFET architecture. As a result, in order to improve SRAM efficiency and achieve good cache system performance, an accurate and well-organized estimate of FINFET based SRAM cell stability is needed early in the design process. The Static Noise Margin is a measure of the stability of SRAM cells (SNM). Another significant scaling problem for SRAM technology is maintaining a broad reading margin (RNM). Variation in the Writing Noise Margin (WNM) has also been shown to have a significant effect on the stability of the SRAM cell during writing for partially depleted insulator (SOI) silicone.

Based on the gate width of the MOSFETs, read and write margins (RM and WM) have been established so far. This approach is however not sufficient for the scaled CMOS technology in the near future, where a random change in system output is important as result of the processes. The trade-off between Read Margin and Write Margin would then be so difficult to handle to ensure that both Read Margin and Written Margin are managed only through the gate-wide agreement. In these circumstances, such groundbreaking circuits will boost RM and WM as well as help overcome the challenge.

The performance of the SRAM architecture is primarily determined by the efficiency and time required to operate the massive loads of bitline and wordline. A leakage current is a significant contributor to the total power dissipation of SRAMs due to its wide size, as it is used in digital circuits at nanometer nodes. The massive increase in leakage current results in a high standby capability. Increased transistor leakage, short channel effect, and parameter variance pose challenges for SRAM cell scaling. The insulation leakage well, the leaking of the sub-threshold device, and the tunneling current for gate-oxides are all contributions to SRAM's standby leakage. The key problem in future SRAM cells is leakage energy consumption. Because of the lower threshold stress in subsequent technologies, ductuation potential is rising. Several designs of SRAM cells were suggested for leakage control. System Architecture optimization in sub-15 nm Fin-FET technology is critical for low power and solid SRAM cell design in order to overcome these challenges.

A Fin-FET makes use of an intrinsic body. The machine performance variability is greatly reduced due to dope-ion fluctuation, which necessitates a heavily doped channel as a planar-bulk MOSFET, resulting in extreme process variability. As a result, we must increase the 6-T SRAM cell capacity by making proper use of FINFET-based technology and the latest design technique. Short channel transistor process variance improvement decreases the solidity of bulk-based SRAM. The FINFET-based SRAM circuit is proposed as a good alternative solution for bulk FET devices due to its higher channel mobility, superior scalability for a given gate insulating thickness, and lack of random fluctuating dopant impact. The effects and leakage current of fin-short-channel FETs are well suited for future nano-scale memory designs. This project investigates the retention, reading, and

writing stability efficiency of a 15nm FINFET-based 8T SRAM mode. MOSFETs were compared to 15nm FINFET-based SRAMs of 6T and 8T.

The simulation and design of the SRAM model are accomplished in the Synopsys HSpice tool based on 15nm technology. A butterfly curve is extracted from the voltage transfer curve (VTC) of two cross-coupled FINFET-based inverters to obtain and analyze the noise margin based on the read, write, and retention operations.

1.2 PROBLEMS FACED IN MOSFET BASED SRAM CELL DESIGN

Scaling of the MOSFET structure to the sub130 nm regime requires heavy canal doping for short-channel effects and heavy super halo-implants are required in order to regulate sub-surface leakage currents. Heavy doping decreases mobility due to the presence of impurity scatter and a strong transverse electrical field in the state worsens the swing of the lower threshold. Therefore, the current of an on-state drive is decreased for a given off-state leakage current.

On the other side, due to a band-by-band tunnelling between the drain and the body, the off-state leakage current is enhanced. A additional major problem for MOSFET bulk nanoscale devices is the threshold voltage (V_{th}) variability produced by spontaneous doping fluctuations. With rising variations, it will be very difficult for large arrays in low power embedded applications to provide nearly limited SRAM architecture stability. Conversely, the primary reason for scaling is firstly to reduce transistor density by increasing the scale. Time of access depends mainly on SRAM system delays and columns. Segmentation is widely used to accelerate the SRAM cells. The overhead area of sense amplifiers becomes important with further reductions in the height of the bit-line.

A tremendous increase in leakage current leads to high standby outputs in a bulk of traditional MOSFET-based SRAM. In addition, process variations lead to contradictions in the intensity of various devices inside the SRAM cell. Such a contradiction may lead to parametric defects which degrade the output of the design. Due to the high leakage current and increased parametric changes, the design of low-performance and robust SRAMs in nanoscale technologies is an important challenge. Thanks to the enhanced short channel (SCE) effect, it is getting too hard to scale single gate bulk CMOS systems beyond sub-50nm nodes.

Due to its high immunity, improved scalability and increased current compared to the single gate MOSFET devices ultra-double- gate body MOSFET (DGFET) devices are being used in the sub-50nm technology. Moreover, negligible junction capacitance present in DGFET helps in reducing the circuit delay. whereas, the channel in DGFET devices is very lightly doped and the threshold voltage is predominantly controlled using metal gate work function and this lightly doped channel helps in eliminating the threshold voltage variations with the help of random dopant fluctuation (RDF).

1.3 FINFET BASED SRAM CELL DESIGN

FINFET devices are emerged as the best alternative devices for DGFET structure as given in the below figure 1.1. Proper optimization of the FINFET devices is vital for decreasing leakage and also improving the stability in Fin-FET based SRAM cells. The supply voltage, Fin height (H_{fin}), and threshold voltage (V_{th}) optimization will be helpful for reducing leakage in Fin-FET SRAM designs by increasing Fin height which allows a reduction in supply voltage. However, reduction in supply voltage has a very strong negative impact on the stability of the cell under parametric variations. In order to lower standby leakage and increase the stability of an SRAM cell, it is very important to have an optimization method of FINFETs. FINFET-based SRAM cells are used to conduct memories requiring less time, low power dissipation and environmental tolerance. The lowest static dissipation between multiple circuit configurations and compatibility of current logical processes makes FINFET dependent SRAM cells most attractive. In addition, the FINFET system also provides superior margins for noise and switching speed.

As mentioned, it is essential for the correct operation to have the size FINFET M5 and M6 when sizes are selected for M1-M2 and M3-M4 inverters. To allow the flip-flop to switch from Q5 '0' state to Q5 '1' state, the switching limit for inverter ratio $(M5-M6)-M2$ is below the switching threshold on the M3-M4 inverter. The sizes of the FINFET system can be selected by simulation, when transistors M5 and M6 are combined into one transistor twice the length of each transistor. Size of the devices affects noise, efficiency and control. It is well known. The sizes

should therefore be carefully selected to improve the compromise between efficiency, reliability and power for pFINFET and nFINFET devices. Thus, here we have studied FINFET-based SRAM design issues, such as: the static margin of noise (SNM), cell read and write margins, power evaluation, efficiency, and how process-induced changes affect these issues.

1.4 PERFORMANCE METRICS OF THE SRAM CELL DESIGN

1.4.1 Static Noise Margin (SNM)

One of the most important parameters is the Static Noise Margin(SNM), which is defined to be the minimum noise voltages that occur at each cell node needed to reverse cell state. The SNM is measured at the side of the largest square within the SRAM cross-coupled inverter centered on FINFET. This feature was calculated when it was read ($BL = BL' = VD$ and $WL = VD$). The standard calculation of the stability in SRAM architecture cells is Static Noise Margin. For the FINFETs used in the SRAM cells, the SNM depended on the V_{th} alternative. A high threshold voltage means that the driving current of these devices is weak, making it very difficult to write, thereby raising the number of devices. One best way to achieve a low power cell with high stability is by using high- v_{th} equipment. FINFET equipment also delivers a high current and a bigger V_{th} , achieving high noise margins with reasonable stability in write.

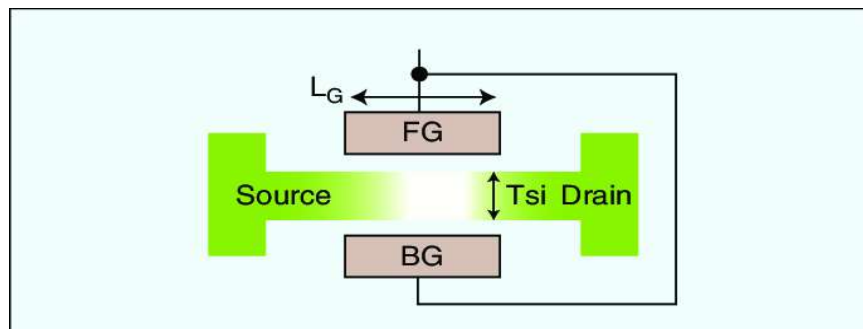


Fig 1.1 : Double gate FINFET

The SNM appears to be the most sensitive to access threshold voltage fluctuations and less reactive to pull-up pFINFET fluctuations. The effect of L_g

variance on threshold voltage is proven to be small for FINFET devices, so it is also a small impact on the SNM.

1.4.2 Power and Delay

Cell utility estimate on mobile devices for power dissipation of the FINFET SRAM architecture. The main benefit of FINFET-based SRAM is its low access time and dissipation of power due to low SCE and FINFET leakage. During strong driving current access time is reduced and the power dissipation in the SRAM cell is increased. In SRAM, the time spent propagating depends primarily on the column height and the wire delay.

As a result, segmentation reduces the delay. Since the power retardation product for one unit remains constant, increasing the one results in a decrease and vice versa. The SRAM Cell FINFET system extension reduces delay at the cost of moderate power dissipation. However, leakage currents should be minimized to minimize dissipation by allowing the length of a channel to increase or leading to higher transistor thrust voltages. More delay results from longer channel duration, resulting in a compromise between these two performance indices.

1.4.3 Power-delay-product (PDP)

The power-delay-product (PDP) is defined as the product of the propagation delay and the power consumed of the circuit. It should be minimum for good performance and robustness. Hence we turn to the use of FINFETs for enhancement of metrics that will make SRAM to perform better.

1.5 NOT GATE

The NOT gate is an electronic digital circuit that generates an inverted version of the input. Often referred to as an inverter. The inverted output is regarded as NOT A if the input variable is A.

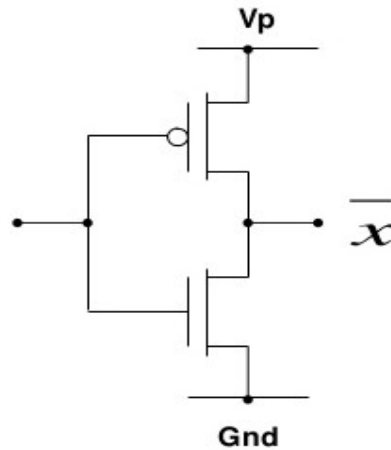


Fig 1.2: CMOS Not gate

The standard NOT gate is represented with the shape of a triangle pointing to the right with a circle at its output end as shown in fig 1.3. This circle is known as an “inversion bubble” and it is used in NOT, NAND and NOR gates at their output to indicate the logical operation of the NOT function. This bubble denotes a signal inversion of the signal.

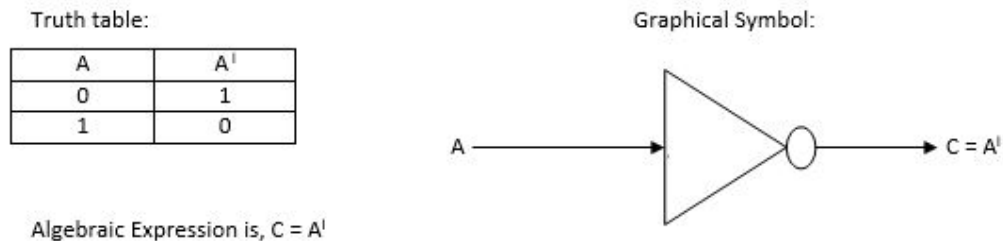


Fig 1.3: Symbol and truth table of not gate

1.6 AND GATE

The **AND gate** is a basic digital electronic circuit that implements logical conjunction i.e it works according to its truth table as shown in fig 1.4. The output of the AND gate is High(1) only if all the inputs to the AND gate are HIGH (1). The output of AND gate is LOW(0) even if one of the output is low. The function can be extended to any number of inputs.

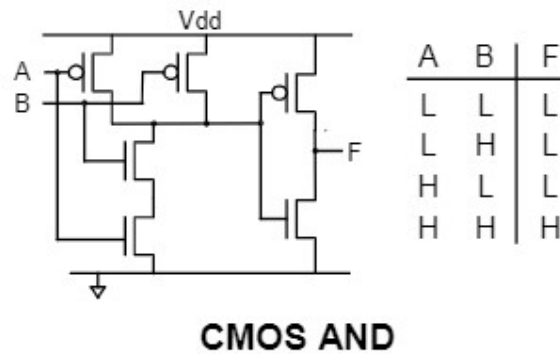


Fig 1.4: CMOS and gate symbol and truth table

1.7 2*4 DECODER

Decoder is an electronic combination circuit, with input lines 'n' and with up to 2^n output lines. One of these outputs is activated (High) depending on the combination of present inputs if the decoder is activated. The term "Decoder" means translating or decoding information coded from one format into another.

INPUTS		OUTPUTS			
A	B	D0	D1	D2	D3
0	0	1	0	0	0
0	1	0	1	0	0
0	1	0	0	1	0
1	1	0	0	0	1

Fig 1.5: 2*4 decoder circuit truth table

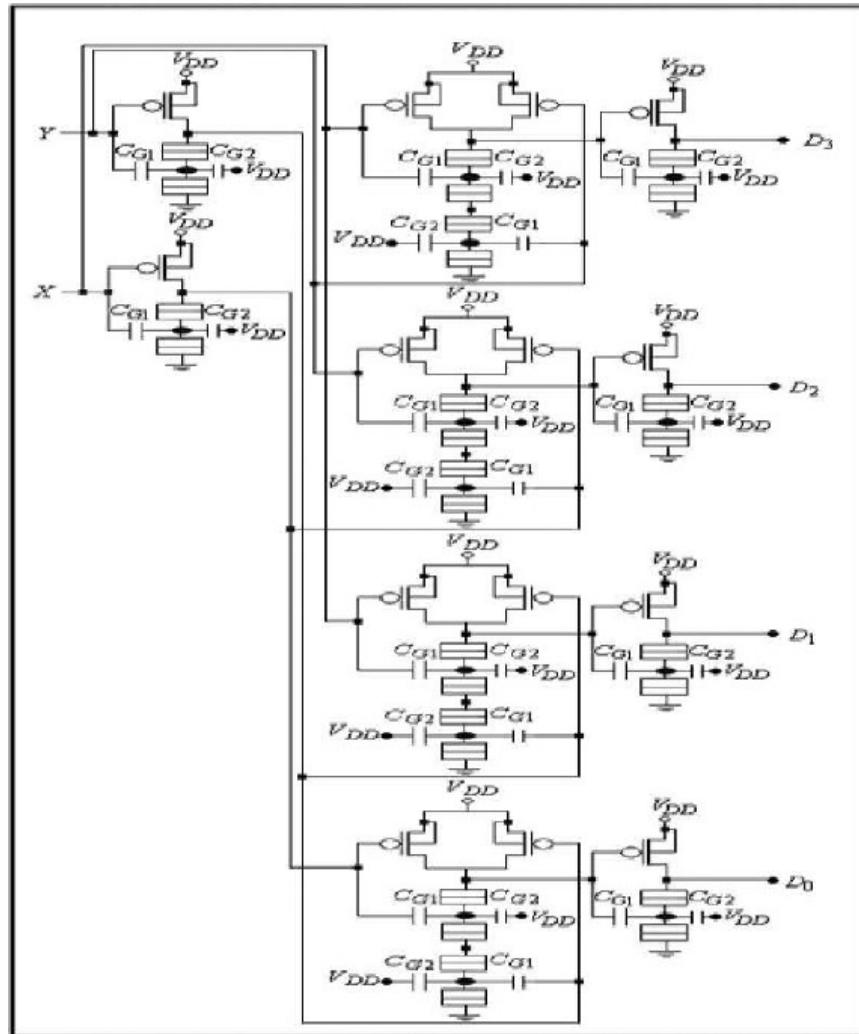


Fig 1.6: 2*4 CMOS Decoder circuit

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

This chapter discusses about the literature survey and summary. It is also gives a detailed idea on the existing SRAM array, CMOS technology, FINFET technology and how their structures are synthesized.

2.1 LITERATURE SURVEY

Ho Le Minh Toan, SrutiSuvadarsini Singh,(VLSI DCS 2020)In the absence of a corner metal gate, Sentaurus TCAD tool is used for an investigation into Quadruple gate (QG) FINFET. The DC output symbol, such as Drive Current (I_{on}), Leakage Current (I_{on}/I_{off}), Drain-induced barrier decrease (DIBL) with the Sentaurus TCAD method. Moreover, the short-channel effects are presented by varying channel duration, such as transconductivity (g_m), output conductance, and intrinsic gain. The simulation was carried out by Synopsis' Sentaurus TCAD instrument, and the results are simulated by integrating different models, such as drift diffusion (DD), for carrier transportation.

Ajay Kumar, ShankulSaini,Abhisht Gupta, Neha Gupta, Madan Mohan Tripathi, RishuChaujar, (ICSC 2020) We examine high-performance analog applications with a very low power supply in this paper. Compared to ordinary FINFET, the performance analysis for 9 nm SOI-FINFET gate lengths was high. It has been assessed that the system proposed offers better solutions for improved sub-threshold pitch, reduced threshold voltage, equipment reliability, and a higher I_{on}/I_{off} ratio. This facilitates high performance switching applications with high-end SOI-FINFET dielectric. FINFET is not much different from planar FET, because it essentially is a FET form and a trigate transistor, usually recognized.

Prashant U.Jain, V.K.Tomar ,(ESCI 2020)The traditional MOSFET technology is able to replace FINFET technology in order to reduce the power discharge and to increase the overall efficiency of digital logic circuits. For MOSFETs, FINFETs are the best option under 32nm, because short channel effects below 32nm can present more problems. FINFET technology is prominent and commonly used in

nearly all digital circuits with low leakage and low power function. rather than traditional MOS. Innovative ways to efficiently build using FINFET technology are explored in the semiconductor industry. The ultimate connections are energy conservation and scalability. FINFET architecture and processes for lithography are still not precise.

Vivek Kumar, V.K.Tomar,(PARC 2020) Compare the standard 6T-, 7T- and 8T SRAM cells with the Cadence FINFET process design kit of 18nm cdsfmp (Cadence FINFET Model). These considered cells have been investigated with SRAM parameters such as stability, power dissipation and delay. We may compare the output of SRAM cells from all of the above simulations. The overall output of the 7T is good with the exception of writing delays, but the single end is not considered as consistent as the difference between these cells in the single end operation. At the speed benchmark of 6T cells, their read capacity is not as strong as other topologies, but their reading power is too high.

Deepak mittal, V.K.Tomal, (ICCCNT 2020) Implement different SRAM cell topologies with the Cadence virtuoso tool on 90nm node technology. To determine power read-and-write dissipation, read delay, write the WSNM (static noise margin) and read all considered topologies, read and write actions for each cell of the SRAM. Read and write actions. The 7T,8T and 9T SRAM cells were correlated in this research paper with traditional 6T SRAM cells for power reading and write dissipation, read delay and process delay, WSNM, and RSNM.

MathanNatarajamoorthy, Jayashri Subbiah, Nurul Ezaila Alias and Michael Loong Peng Tan, (ESCI) The development of semiconductor nano electronic devices leads to the shrinking of the transistor channel to a nanometer dimension. GNRFET is a developing technology that will undoubtedly solve the problem imposed by quantum mechanical effects on conventional planar MOSFETs (QM). The graph nano ribbon field-effect transistor is a new technology. Because of their exceptional electronic properties, GNRFETs can also be used in static Access Random Memory (SRAM) circuit designs. SRAM cells are more well-known and can be used as a memory cache for high-speed operations more quickly. GNRFET with concatenated parallel ribbons to increase driving strength from source, gate, and drain. The gate can be used to control the channel..

2.2 LITERATURE SUMMARY

The Sentaurus TCAD tool is used for a four-piece gate (QG) FINFET in the absence of the corner metal gate. Compared to ordinary FINFET, the performance analysis for 9 nm SOI-FINFET gate lengths was high. The traditional MOSFET technology is able to replace FINFET technology in order to reduce the power discharge and to increase the overall efficiency of digital logic circuits. For MOSFETs, FINFETs are the best option under 32nm, because short channel effects below 32nm can present more problems. Comparative study of standard 6T, 7T and 8T SRAM cells using Cadence Virtuoso (Cadence FINFET model) 18nm cdsffmpt process design package. In terms of read capacity and power diminution, reading delay and writing delay, WSNM and RSNM, the 6T SRAM cell was compared with the 7T,8 and 9T SRAM cells. SRAM cells are more well known and quicker to be used as the memory cache for high-speed operations.

2.3 PROBLEM DEFINITION

The scaling of CMOS has led to the development of the performance of digital circuits. However, this technology faces significant challenges due to the size scaling of the transistors such as short channel effects (SCEs) and threshold voltage (V_{th}) roll-off issues. FINFET based SRAM design has been proposed as an alternative solution to the bulk devices for low-power digital CMOS technologies to overcome these issues. conventional 6T SRAM cell suffers with stability degradation issue because of access disturbance at low power mode. The major problem in 6T SRAM is that, when the output voltage declined below the threshold voltage of the transistor, it will destroy the read operation of the 6T SRAM cell. The noises are very easy to devastate the stored-data present in the nodes of the 6T SRAM cell because of the direct path between storage nodes and bit lines. To overcome this issue, an 8T SRAM cell has been proposed where the read stability is improved compared to 6T SRAM.

2.4 OBJECTIVE OF THE PROJECT

- To increase the efficiency of the SRAM Array by modifying the SRAM Cell for Low Power applications

- In order to improve Efficiency Low Power Techniques will be applied in all Circuits
- To compare the characteristics of both MOSFET and FINFET Technology in terms of Power, Delay and Power Delay Product
- To identify the Feasibility of FINFET for Memory Devices

CHAPTER 3

PROCEDURE FOR EXISTING METHODOLOGY

3.1 SRAM CELL

SRAM is one of the most commonly accepted embedded storage systems used on contemporary digital circuits due to its better compatibility with logic circuits and fast, random access compared with DRAM, ROM, etc. The main components of an SRAM cell are memory cells. Just one bit of data can be stored on an SRAM cell. An SRAM cell comprises a latch and two access transistors with two cross-sections. Transistors for access to cell material are used to read and write.

The two common types of Random Access Memory (RAM) are SRAM (Static RAM) and DRAM (Dynamic RAM). The data stored in DRAM should be refreshed regularly due to present of capacitor and a transistor in its structure. On the other hand, the data in sram cannot be refreshed because cross-connected transistors in SRAM carry the data and the power supply is not disconnected. Due to this, during write and read operations, SRAM works much faster. Despite this advantage, SRAM Array requires more chip area, because more transistors are needed to store a bit of data. However, a certain region for good results is worth sacrificing. The current list of traditional SRAM cells in 4T, 6T, 7T, 8T and 9T SRAM cells is shown in Figure 3.1.

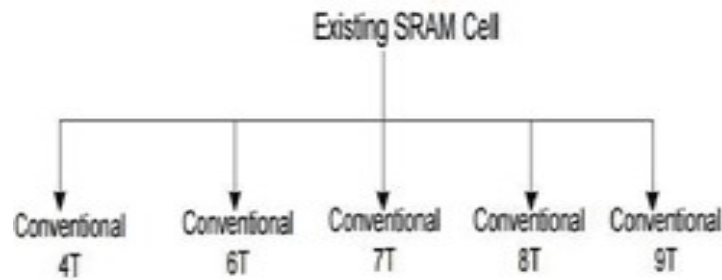


Fig 3.1 : Different types of SRAM cells

Two cross-coupling inverters forming a positive feedback are the fundamental structure of the SRAM cell. The 4T, 6T, 7T, 8T or 9T cell difference depends on the number of transistor accesses associated with the two inverters. The key emphasis of this paper is on 6T and 8T SRAM.

3.2 ARCHITECTURE OF ANMOSFET BASEDSRAM UNIT

The periphery blocks in an SRAM array architecture make easier access to the cells for the read or write operation. In application, multiple bits are accessed for the read or write operation during the same time. Based on application, the word size, M, usually ranges from a dozen bits to 64 bits. In regular SRAM cells only one word is accessed at a time. The number of words that are accommodated in the unit defines the length of address field, N. Yet, The total number of cells in an array could be calculated as $M \times N$.

There are several peripheral blocks in an SRAM unit. An array adapts to the cell diversity. The binary encoded input address is decoded by a decoder. Sense amplifiers(SA) and writing drivers are used to communicate with the cell bitlines during reading and writing operations. The Sense Amplifier and write driver is a time-control device for generating the correct time signal for the wordline activation during the reading and writing process.

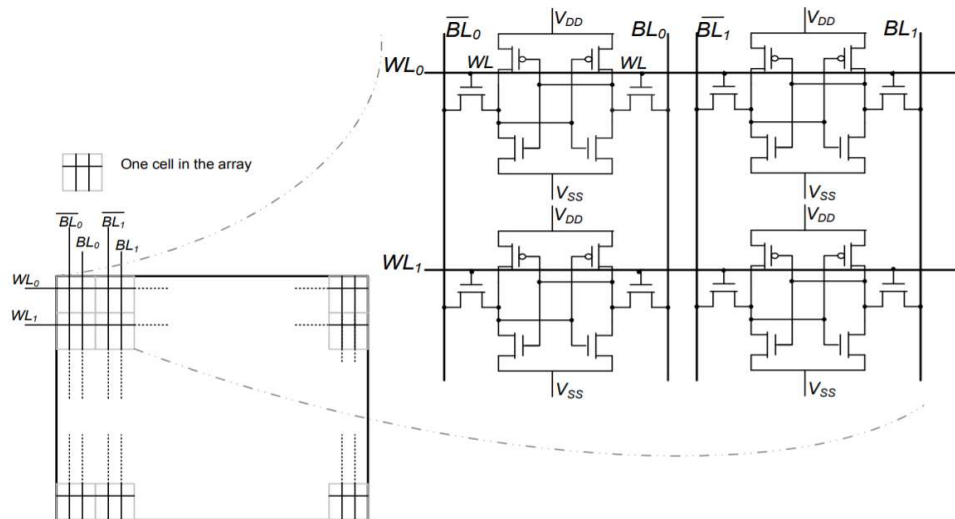


Fig 3.2: Construction of an array based on a plurality of SRAM cells

A group of cells arranged beside each other form an array. The cells which are sitting on the same row share the same wordline and those which are on the same column share the same pair of bitlines. Figure 3.2 explains the construction of an array and the connected bitlines and wordlines. Clearly, many cells which

are on the same bitline and also the short distance between the neighboring columns foist a significant capacitive load on the bitlines. For each and every access, only one wordline is active in an array architecture. All SRAM cells on the row will discharge their corresponding bitlines when wordline is activated. Therefore, all the bitlines are discharged as a result of wordline activation.

3.2.1 Row Decoder and Column Multiplexer

Multiple words are commonly placed in single row in applications with normal word size i.e ($M < 128$). Different bits of the words on a row of the cell are interleaved to share fringe circuits such as Sense Amplifier, write driver and row decoder. Figure 3.3 shows an array architecture in which each row accommodates 2^n and each word contains M bits. The first bit(b_0) of all the 2^n words on the same row are placed beside each other and the next bit of all words are placed at the neighboring set of cells. Hence, only one Sense Amplifier and write driver serves the first bit(b_0) of all the 2^n words. in the block.

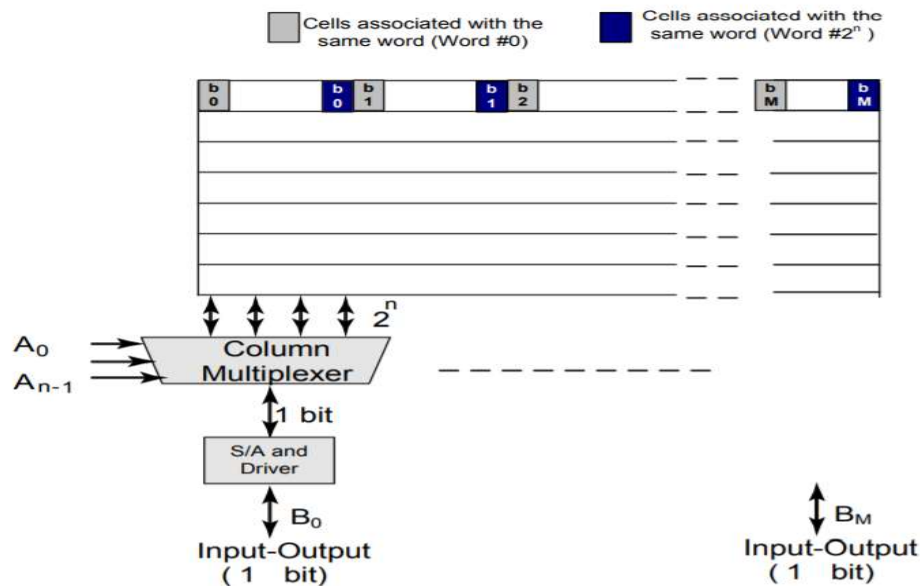


Fig 3.3: The concept of interleaving in an SRAM array

A column multiplexer used to select the bitline which is connected to the Sense Amplifier or write driver. It is evident that for a word size which is equal to M there are $M \times 2^n$ cells on the same row and $M \times 2^n$ columns.

The accessed word location is indicated by the address inputs of the SRAM architecture. Specified by $A_0 - A_{K-1}$, the address input is a binary encoded number with the bit width of $K = \log_2 (N)$ bits. The address input is decoded to locate the word that is desired for an access.

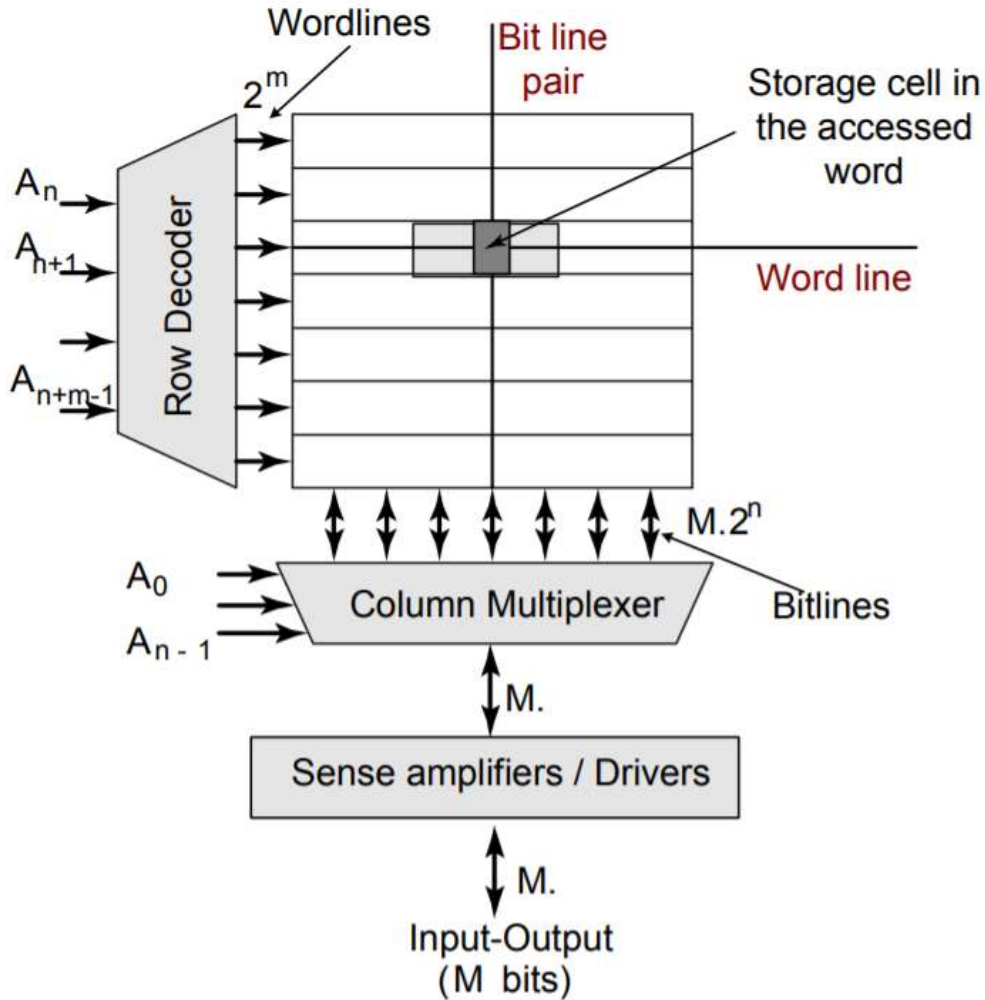


Fig 3.4: Array architecture

The words are often located by specifying the row on which the specified word is placed and therefore the columns on which different cells like different bits of an equivalent word are placed. Therefore, the K address bits are divided into column address bits $A_0 - A_{n-1}$ and row address bits $A_n - A_{n+m-1}$ where $K = n + m$. Figure 3.4 clarifies this system. The column address bits drive the column multiplexer and specify which word within the row is accessed. Driven by the row

address bits, the row decoder specifies the row during which the accessed word is found by activating the wordline of that word.

A row decoder is typically supported two pre-decoders and a post-decoder as shown in Figure 3.5. it's been reported that equal division of the row address field between two equal pre-decoders exhibits shortest delay time.

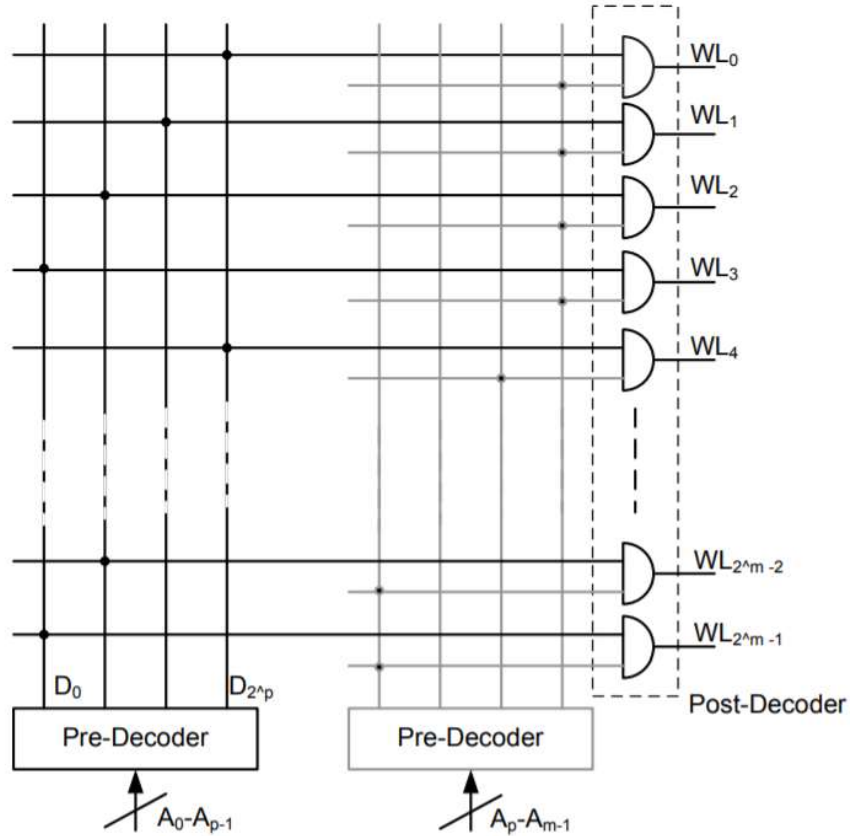


Fig 3.5: Implementation of the row decoder based on post decoders and a pre decoder

For a given address, only one of the outputs of every pre-decoder is active. The post-decoder consists of a plurality of AND gates. The output of the AND gates drive the wordlines of every row. The AND gates are driven by the 2 pre-decoders such as the output of the AND gates produce all combinations of the pre-decoders' output. Basically, one input of each AND circuit is driven by one among the pre-decoders whereas the opposite input of the AND circuit is driven by the other pre-decoder. Therefore, for any address input, just one of the post-decoder's outputs will be active. it's noteworthy that, the length of an AND circuit within the post-decoder that drive the wordline should match the length of the

SRAM cells within the array. This limitation should be considered within the layout of such AND gates.

3.2.2 Sense Amplifier and Write Driver

The communication between an SRAM cell within the array and the outside world is happened with the help of a pair of bitlines. Bitlines have two important characteristics. First of all, bitlines conduct the information in a differential fashion. Second, bitlines are highly capacitive interconnects because of their being a long low metal layer and the numerous access transistors that loads them. Because of these characteristics, the voltage levels appear on the bitlines are limited to save power and delay time. A sensor amplifier and a writing driver interface between the bit lines and thus CMOS gates on the I/O info route to ensure correct translation on both sides of the voltage level

The sense amplifier is a semiconductor device used to amplify a small analog differential voltage developed on the bitlines that are associated with cell. Usage of Sense Amplifier helps to reduces the size of the SRAM cell because the drive transistors does not require the fully discharged bitlines. A Sense Amplifier needs to satisfy some electrical requirements to achieve best operation in the SRAM cell. First, at input of Sense Amplifier, the necessary minimum difference tension swing must be smaller than the minimum differentiation tension produced with the help of the SRAM cell through the bitlines. Secondly, when the sense amplifier exercises minimum input differential voltage, the output should be able to provide the amplifying time (T_{sa}) sensor.

SRAM sense amplifiers is divided into two categories: (i) Linear amplifiers and (ii) latch type amplifiers as shown in Figure 3.6. Linear amplifiers are classical differential pair along with current mirror active load that is used to amplify the small differential voltage present on the bitlines. These amplifiers has the advantage of eleminating the common mode voltage variation. Even though, it demands an ample amount of gate source voltage over drive $V_{gs} - V_{th}$ at its input transistor gates for better Performance.

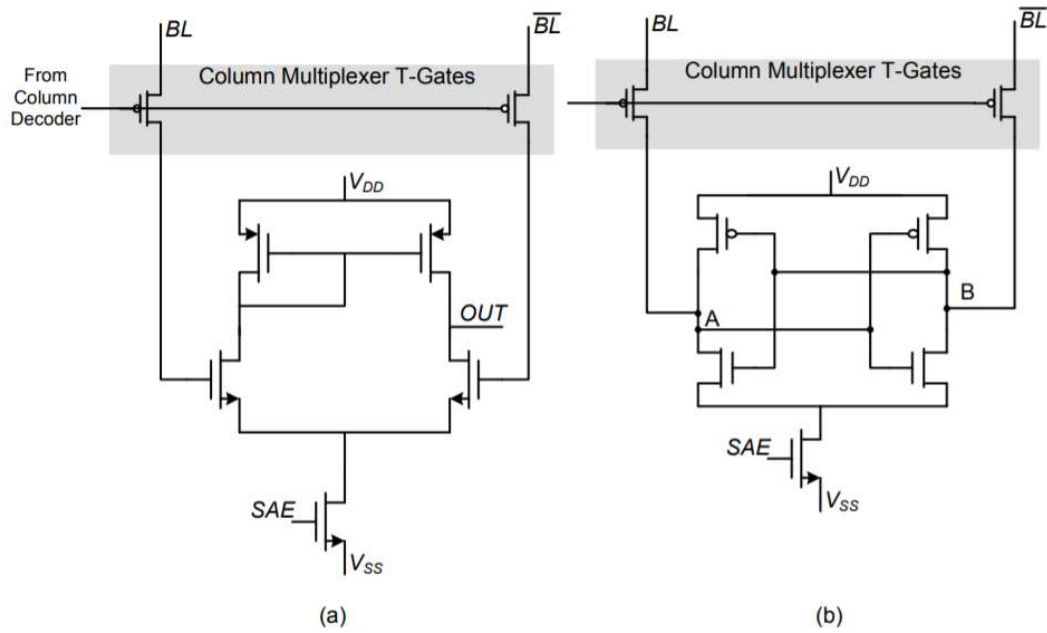


Fig 3.6: (a) A linear sense amplifier and (b) a latch type sense amplifier

Conversly, a latch type sense amplifier is mainly depended on a cross coupled inverter. Unlike a linear Sense Amplifier, a latch type Sense Amplifier needs an accurate timing for better performance. This timing is shown in Figure 3.7. At the beginning both the internal nodes of the Sense Amplifier are floating and they are precharged to V_{DD} because of sense amplifier enable (SAE) Inactive signal. Inactive signal. When the bitline is unloaded it is connected through the multiplexer pass doors to the internal nodes of the Sense Amplifier. Once a large voltage is produced over the bitlines, the multiplexer gates are shut down to separate the Sense Amplifier from the bitlines.

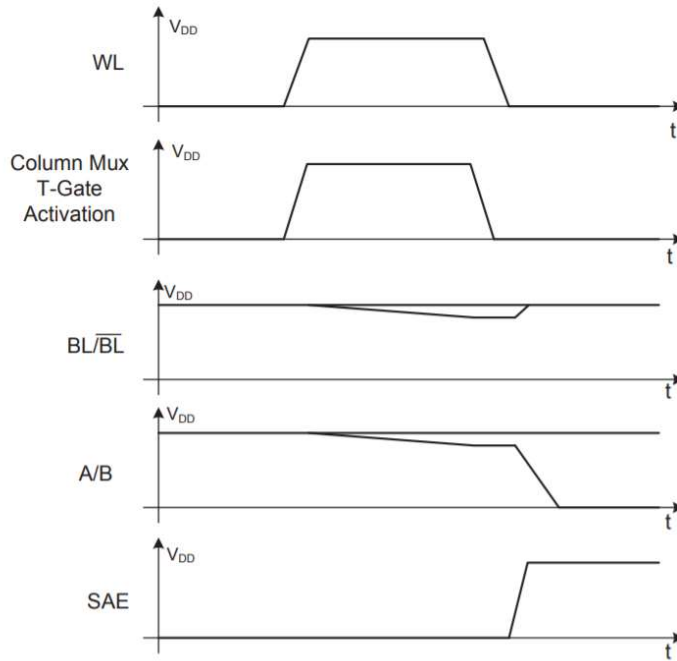


Fig 3.7: Timing in Read operation

During the discharge of bitline, they are connected to the internal nodes of the Sense Amplifier through the multiplexer's pass gates. Once an ample amount of differential voltage is developed over the bitlines, the multiplexer's pass gates turns off to isolate the Sense Amplifier from the bitlines. The activation of the Sense Amplifier Enable signal concurs with the isolation of the Sense Amplifier from the bitline. Such type of timing eliminates an unwanted full swing discharging of the bitlines.

Write drivers are used to unload the bitlines quickly before or during the wordlines of the selected cell to a level below the written cell margin. Figure 3.9 displays two standard write drivers. The input of the data selects the downloaded bitline. Only when the written operation is intended is the W E signal active. Alternatively, the W E separates the write drivers bit. Figure 3.9(b) is faster, as there are very less transistor stacked in the discharge direction, while the two writer drivers have the same feature.

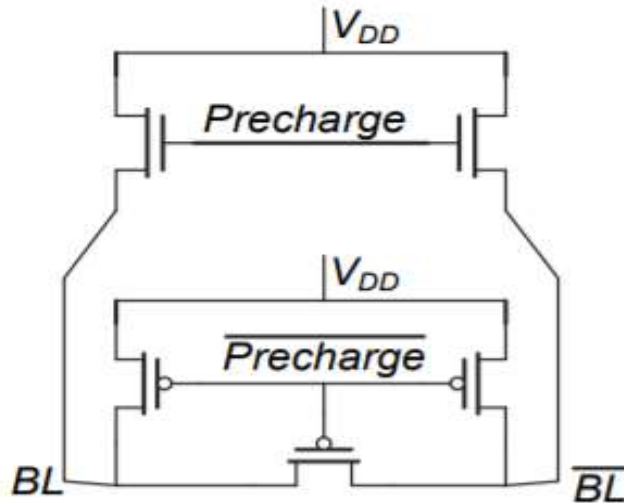


Fig 3.8: Precharge Circuitry

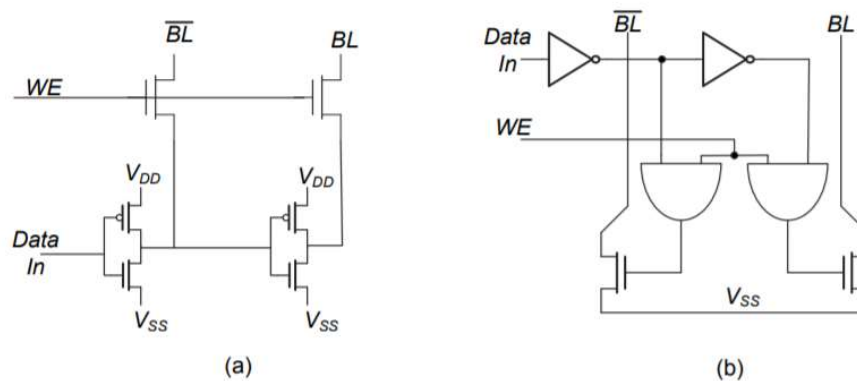


Fig 3.9: Two types of write drivers that offer write voltage of V_{ss}

3.3 MOSFET BASED 6T SRAM CELL

Figure 3.10 shows the diagram of conventional Bitlines (BLs) and Wordlines (WL) are aligned in vertical and horizontal directions respectively. During standby mode, WL is in off state and bitlines are pre-charged to V_{DD} . Wordline which is used to control the state of access transistors (AC1 and AC2) will only activated during the read and write operation.

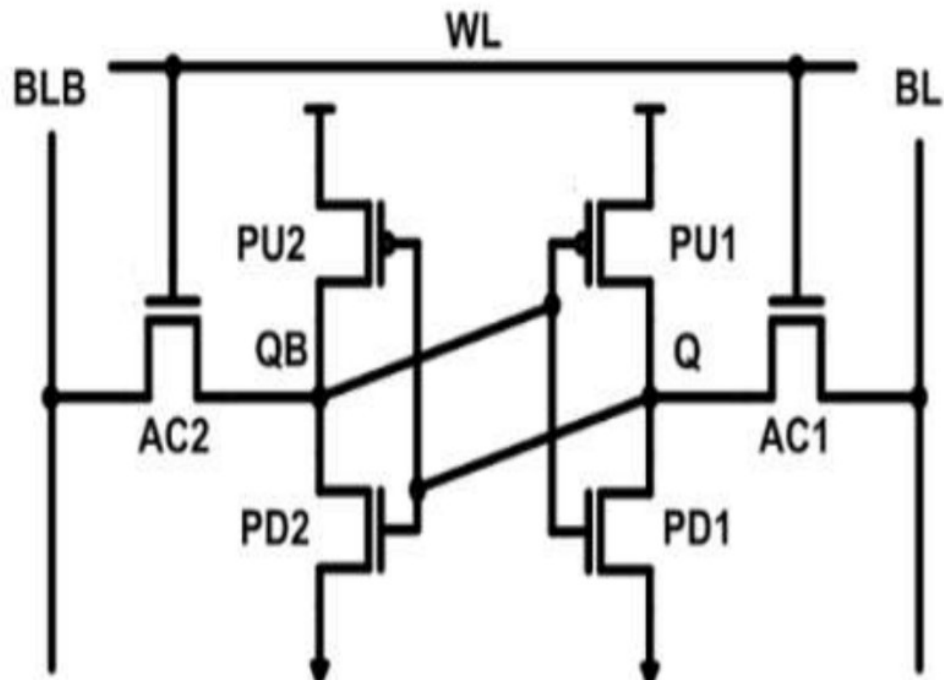


Fig 3.10: Schematic diagram for 6T SRAM cell

3.3.1 Operation of 6T SRAM cell

SRAM cell operates in three modes i.e retention mode, read mode and write mode.

Retention mode

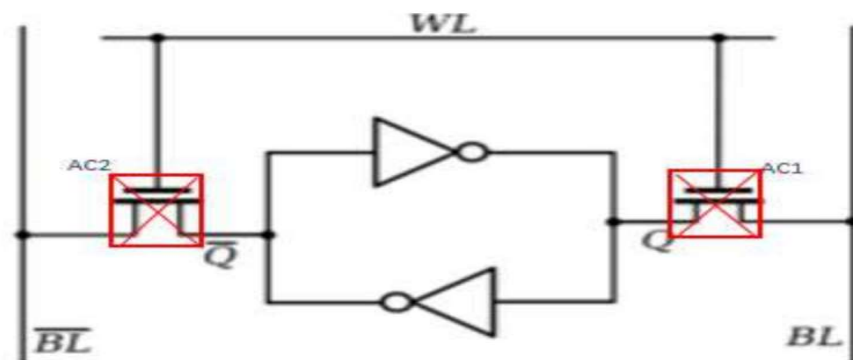


Fig 3.11: 6T SRAM cell during retention mode

Word Line is disabled when retaining, causing both access transistors to be switched off (as shown in Figure 3.11). The two cross-connection inverters form a positive feedback loop and are held in the cell as long as the power is ON.

Read mode

Theoretically, learning requires only the Wordline to be allowed, and SRAM cell state read operations can be performed with only one access transistor and a bit line (BA and AC1 or BL and AC2). However, this is not the case since the bits are relatively long and have large parasitic capacities, causing the read process to be more slow. When both Bitlines are pre-charged to HIGH in order to speed up the reading process, a more complicated technique is used. The word line is then triggered, allowing the Access transistors (AC1 and AC2) to turn on, resulting in a minor drop in the voltage in BL (PD is enabled and PU is disabled) or a slight increase in the voltage in BL (PU is on and PD is off).

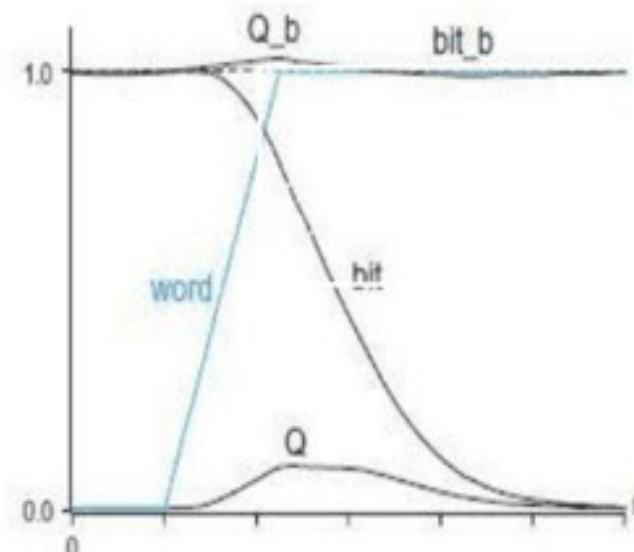


Fig : 3.12 : 6T SRAM cell during read

Write Mode

Whatever the original information is in the SRAM cell, the data present can be set to any binary value. We'd add a "0" to the bit row, i.e. setting BL to 1 and BLB to 0, if we want to write a "0". This applies to the use of a reset pulse in an SR-lock, which changes the status of the flip flop. A binary value of "1" is also written by inverting bitline values. This will then reaffirm wordline and

lock the value to be stored in. It works because the inputs on the bit lines are engineered so that they are stronger than the comparatively weak transistors inside the cell itself.

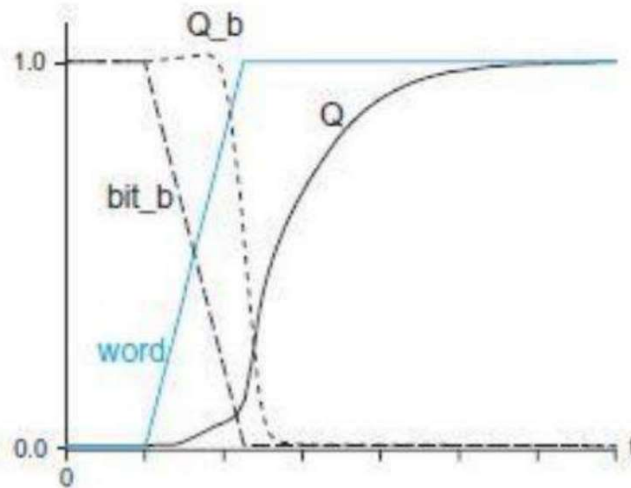


Fig 3.13: 6T SRAM cell during write

3.4 MOSFET BASED 8T SRAMCELL

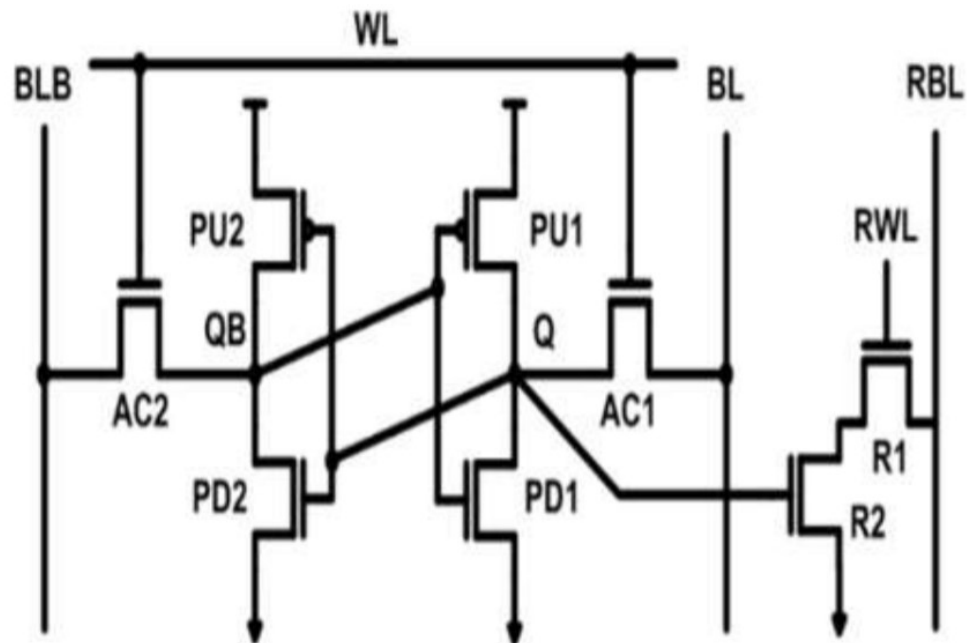


Fig 3.14: 8T SRAM cell schematic

The 8T SRAM cell in Figure 3.14 is composed of a standard 6T SRAM cell with two additional access transistors (RWL and RBL) that make a dedicated port

for reading operation. The dedicated read ports provide trouble-free reading and thus help to optimize read and write operations.

3.4.1 Operation of 8T SRAM cell

Retention mode

8T SRAM cell operates in a retention mode similar to 6T SRAM cell in a way that is OFF switched on the access transistors(AC1 and AC2) and the read port(R1 and R2) also OFF. The data are stored in the cell by the two-cross pair inverters, as the power is ON.

Read Mode

8T SRAM cell read operation is completely decoupled by the data sensing through a specific read port operated by an independent reading worldwide line from the write operation (RWL). The WordLine is set to LOW, which will switch the access transistors OFF during reading operation (AC1 and AC2). In the ON state, however, R1 and R2 would be. Data from the two-cross inverters are then read.

Write Mode

Just like retention, 8T SRAM write operation is the same as the 6T SRAM write operation. As R1, R2, R2 are OFF and thus write operation, these two other transistors are independent of the dedicated reading port.

CHAPTER 4

PROCEDURE FOR PROPOSED SYSTEM

4.1 FINFET TECHNOLOGY

A multigate tool otherwise multiple gate field-effect transistor (MuGFET) point out a MOSFET (metal-oxide-semiconductor field effect transistor) Including a single device over and above a gate. Controlled by a special gate electrode that acts as a single port electrically by the multiple gate externals or by free gate electrodes, the various gates are numerous. A gadget with many gates that often involves free gate electrodes called a Multiple Independent Gate Field Effect Transistor(MIGFET).

At submicron level universal MOSFET suffer from many submicron problems, such as small channel effects, difference in threshold voltage, etc. The short channel effects are supposed to be regulated by FINFET. FINFET structure is shown below,

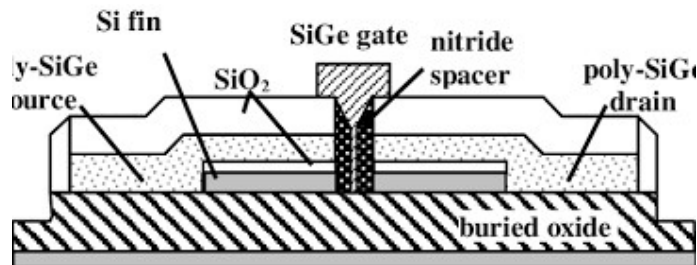


Fig 4.1:Structure of FINFET

With the FINFET process in conjunction with the tense silicone process, the flexibility of the carriers is improved. Design of FINFET appliance The processes for building FINFET are based on silicone on insulator (SOI). The fin is placed with a single poly-silicon sheet. Poly silicone beside the finish structure forms gates which are completely aligned. Here a fin behaves like a canal and stops from the source and drain. On both sides. The poly silicon gate in a typical MOSFET system is formed over the silicon substratum. The channel is controlled by poly silicone gate. Structured gate-controlled gate characteristics contrast to MOSFET enable poly silicon gate sanding across the Silicon fin. The dimension of the

channel is equal to the thickness of the fin given that the gate covers the end. As there are prolific double doors on either side of the end that we can write, the channel's thickness is twice the height of the fin, which is $w=2 \cdot h$. The tenure of fin pitch is used to mark the world with two fins flanked. The FINFET altitude is compatible with the MOSFET thickness. If w is formerly the fine pitch of the same area performance, the compulsory fine is $w/2$. However, realistic tests have shown that fine height for w fine pitches can be prominent than $w/2$. FINFET thus achieves an increased efficiency of area compared to MOSFET.

FINFET technology has recently seen a significant increase in acceptance for use on integrated circuits. FINFET transistor technology provides few major advantages in IC design compared with the usual planar technology. The FINFET technology convinces to ensure that the current progress towards increased integration within integrated circuits can be sustained at the highest levels of expandability required. In IC processing, the FINFET provides numerous additional advantages which make it a major way forward for integration into the IC technology.

4.2 FINFET STRUCTURE

The continuous down mounting of bulk CMOS generates foremost affair owing to its ignoble material. The primary impediment to the scaling of bulk CMOS to 32nm gate lengths incorporate short channel effects, Sub-threshold leakage, gate-dielectric leakage and device to device variations. But FINFET based enterprises proposals the healthier controller over short channel effects, little leakage and finer yield underneath 45nm supports to overwhelmed the hindrances in scaling. Double Gate devices have been worn in a assortment of ground-breaking ways in digital and analog circuit designs. A parallel transistor pair comprise of two transistors with their source and drain terminals tied together. In Double-Gate (DG) FINFETs, the second gate is supplementary opponent to the traditional gate, which has stayed predictable for their possible to healthier control short channel effects, over and above to switch leakage current.

4.3 DESIGN OF FINFET BASED INVERTER

The inverters were developed using a 22nm n-channel and p-channel FINFET enhanced unit. The FINFET founded inverter performance characteristics are simulated. The inverter voltage transfer features (VTC) have been acquired. Then, in the 6t SRAM cell circuit design, the improved, grounded FINFET inverter was united. Two inverter circuits and two additional n-FINFET are part of the 6T SRAM cell. In addition to performing a 6T SRAM cell in retention, read mode and write mode, the butterfly curve of the 6T SRAM cell has also been repeated. The 8T SRAM cell is composed of a 6T SRAM cell, with two more n-FINFETs, in order to determine the read process.

4.4 FINFET DESIGN FOR 6T AND 8T SRAM

Memories are expected to be the most important element in future design. This fact makes scal much more difficult and significant. This is due to. The gate electrostatic force on the countless sides of the fine is amplified in FINFET. MOSFETs, for example, boost shorter canal effects such as subthreshold loss, V_{th} roll of width lengths, and DIBL. Memory is required for quick access, low power dissipation, and low flow rate; thus, FINFET-built SRAM cells are preferred over CMOS-based SRAM cells. FINFET-built SRAM cells are more common due to their low power dissipation. FINFET's 6T SRAM cell structure varies from conventional SRAM 6T.

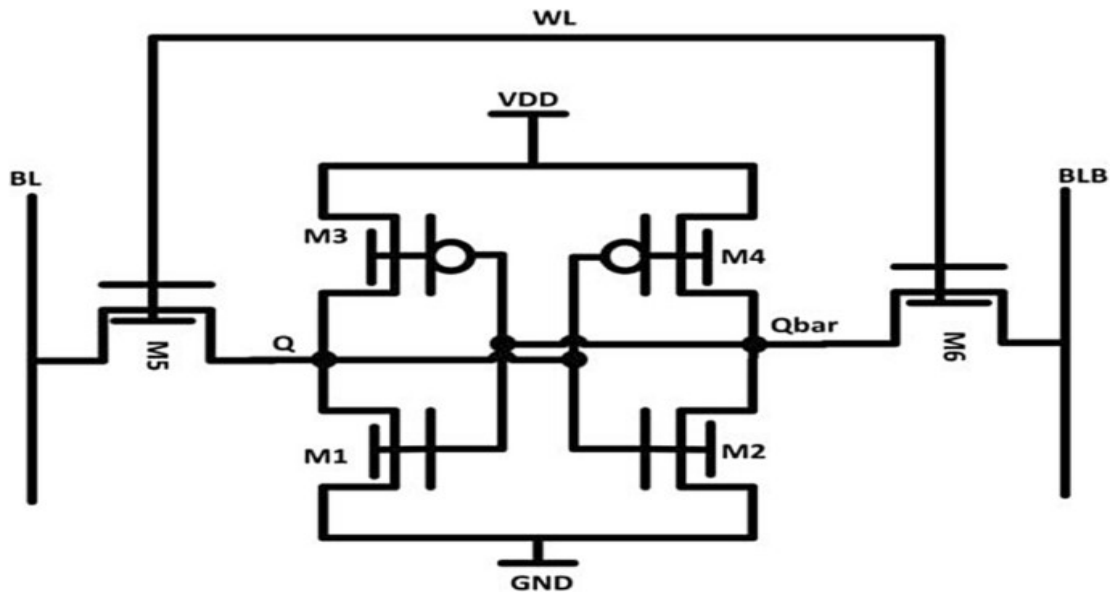


Fig 4.2: FINFET based 6T SRAM cell

The 6T SRAM cell is built by connecting two FINFET inverters back to back and two n-channel access FINFETs, as shown. The data portion reserved in the Bit Line (BL) and Bit Line Bar (BLB) during the internal storage nodes of the SRAM cell formed by the output port of the two opposing inverter pairs, Q and Q bar. The FINFET arrangement mode employs the Low-Power (LP) FINFET mode in the conformist 6T SRAM structure strategy. Word Line (WL) is a control signal that is used to control the on/off operation of the two pass transistors. When the turn-on WL evolution is allowed, the 6T SRAM cell performs either a read or a write operation.

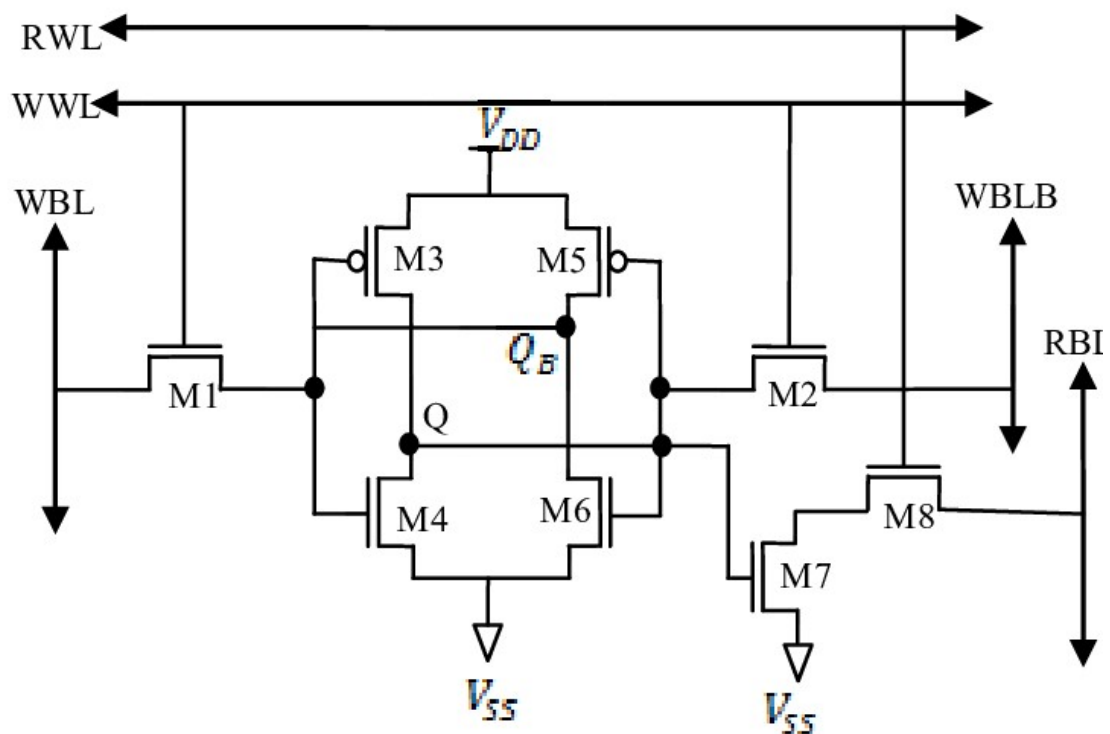


Fig 4.3: FINFET based 8T SRAM cell

The FINFET has better control over the channel and lower overall capacitance, which will expand the presentation of the 6T SRAM circuit design. It will aid in lowering bit line loading and thus improving SRAM efficiency. At low strength, the traditional 6T SRAM cell can tolerate significant stability degeneracy due to admittance disruption.

CHAPTER 5

RESULTS AND DISCUSSION

The existing and proposed architecture are simulated by using AvanWaves simulator. Output of the existing MOSFET and proposed FINFET are analysed from the results and it is concluded that the proposed architecture reduces the power consumption compared with the existing system. The Synthesis is done using Hspice UI.

5.1 SIMULATION OF WAVEFORMS USING 130NM MOSFET TECHNOLOGY

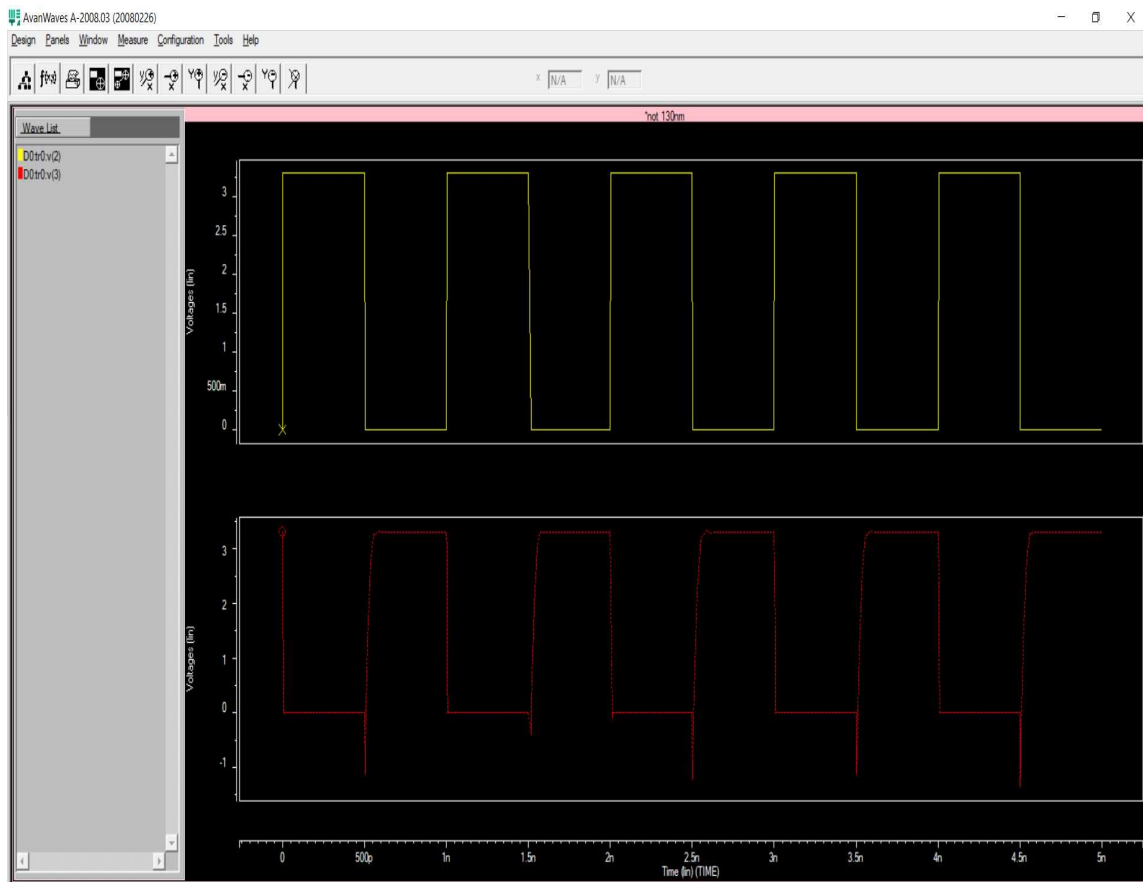


Fig 5.1: Simulation results for NOT gate 130nm MOSFET technology

Figure 5.1 shows the simulation output of NOT Gate 130nm MOSFET technology. The inputs given were v(2) and the output is taken by v(3).

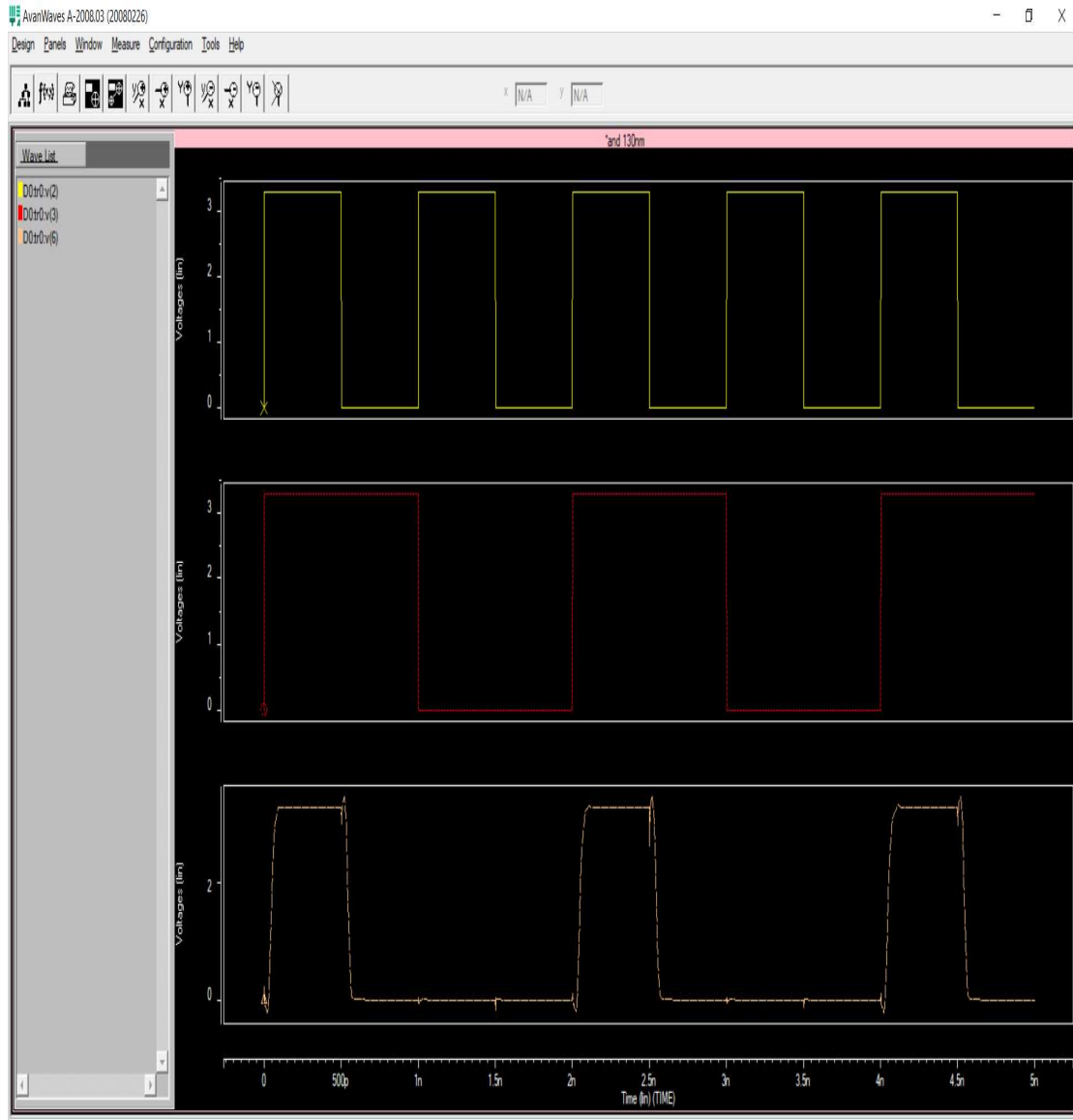


Fig 5.2: Simulation results for AND gate 130nm MOSFET technology

Figure 5.2 shows the simulation output of AND Gate 130nm MOSFET technology.

The inputs given were v(2), v(3) and the output is taken by v(6).

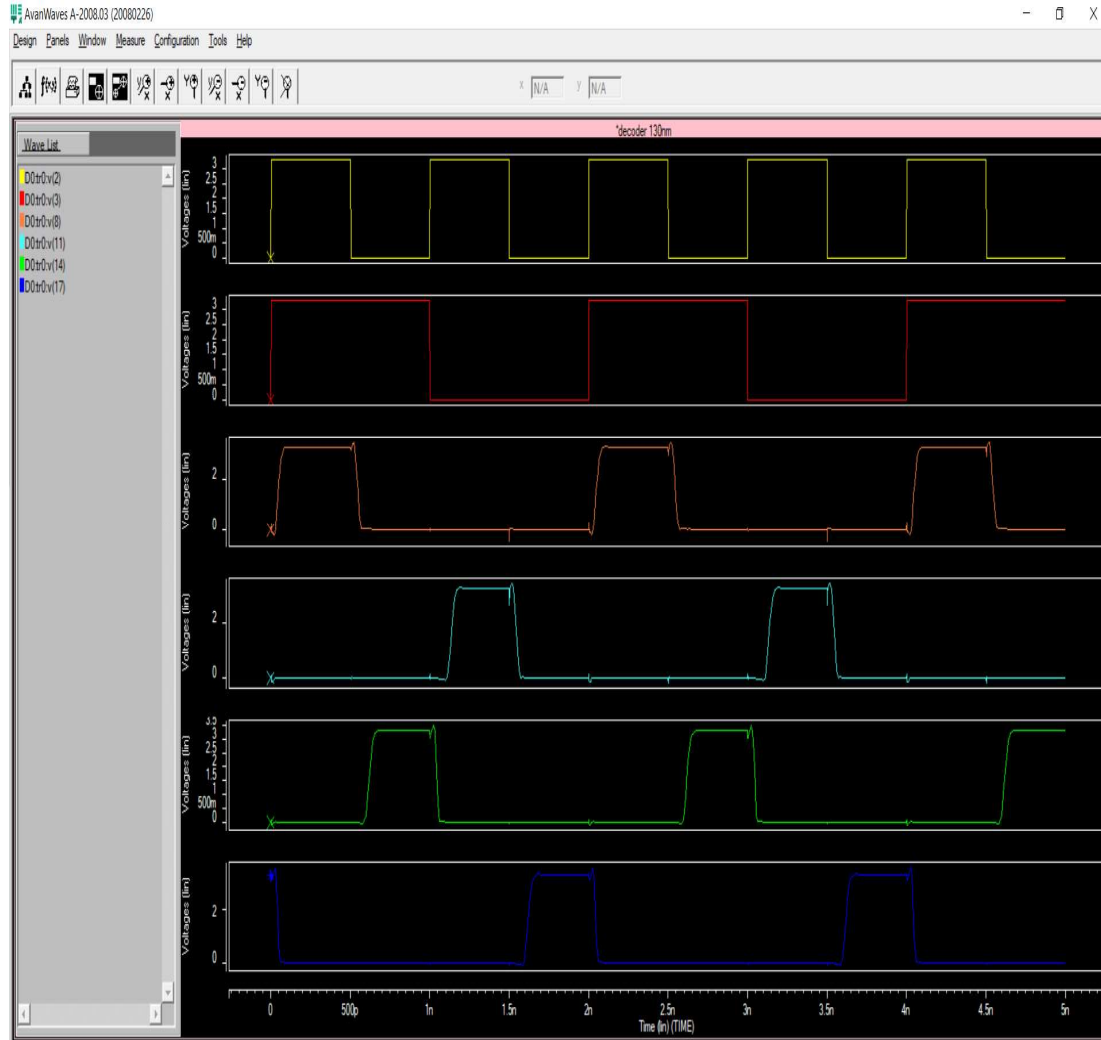


Fig 5.3: Simulation results for DECODER 130nm MOSFET technology

Figure 5.3 shows the simulation output of Decoder 130nm MOSFET technology.

The inputs given were v(2), v(3) and the output is taken by v(8), v(11), v(14), v(17).

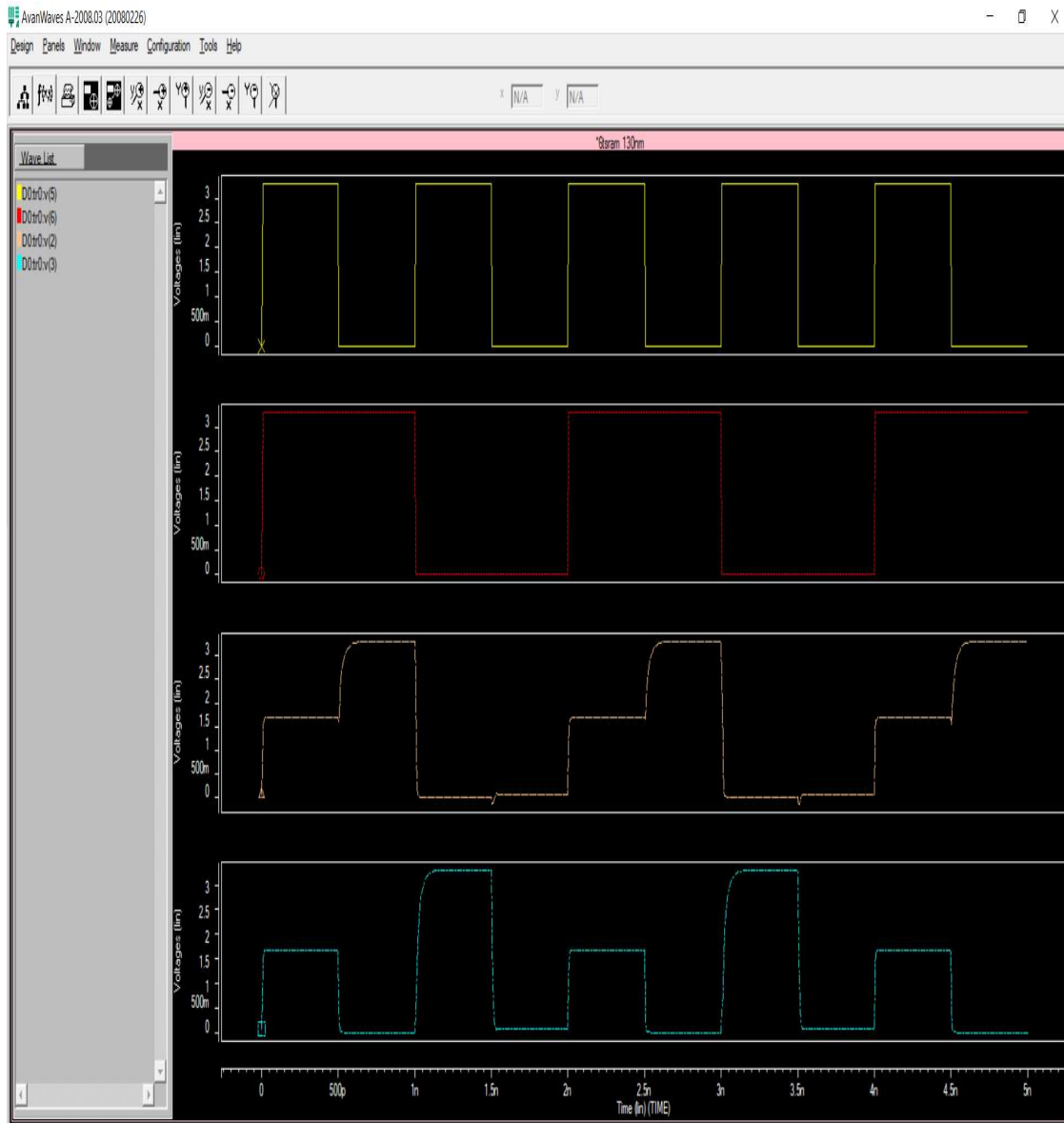


Fig 5.4: Simulation results for 6T SRAM 130nm MOSFET technology

Figure 5.4 shows the simulation output of 6T SRAM Gate 130nm MOSFET technology. The inputs given were v(5), v(6) and the output is taken by v(2), v(3).

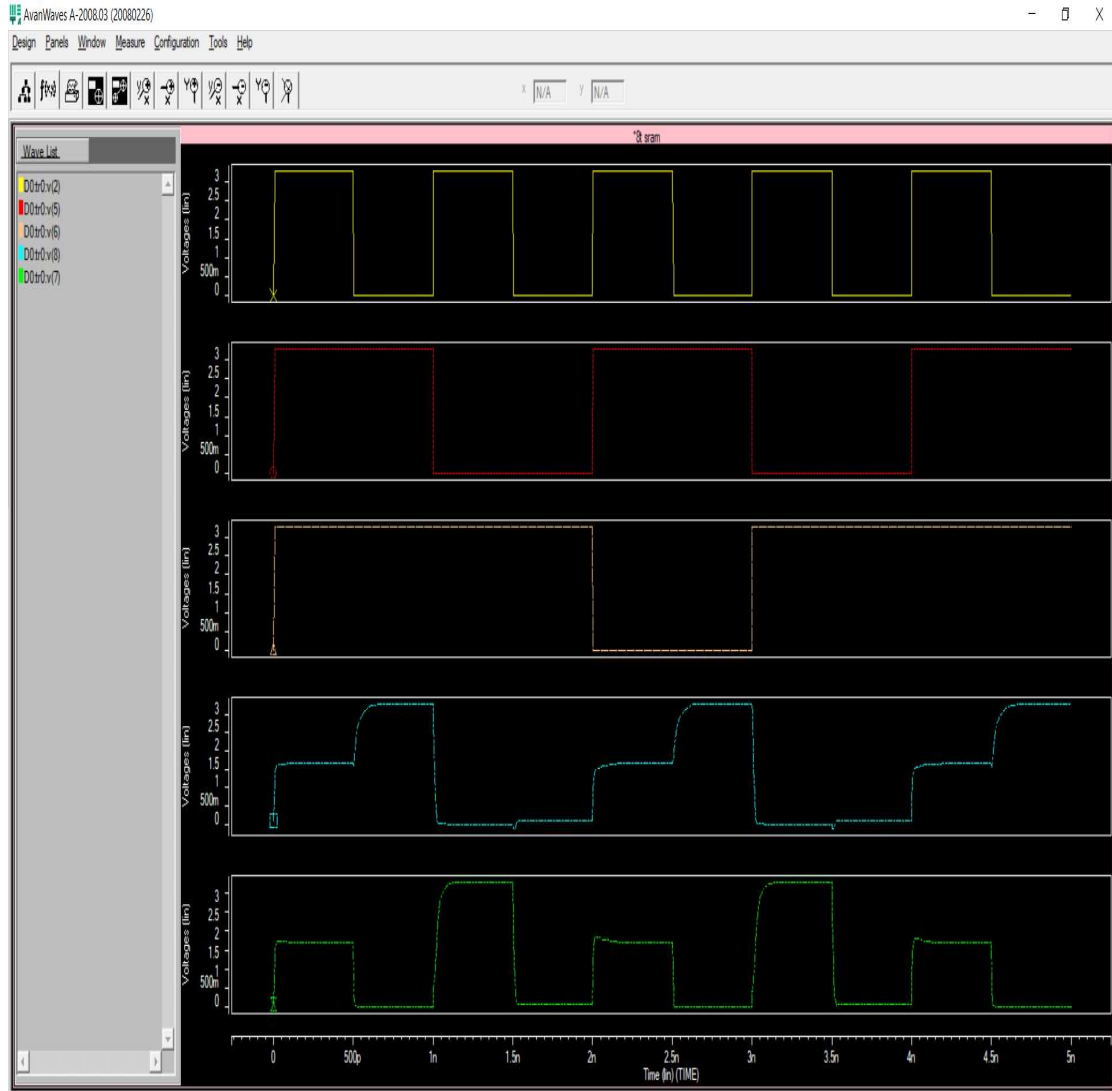


Fig 5.5:Simulation results for 8T SRAM 130nm MOSFET technology

Figure 5.5 shows the simulation output of 8T SRAM 130nm MOSFET technology. The inputs given were v(2), v(5) and the output is taken by v(6), v(8), v(7).

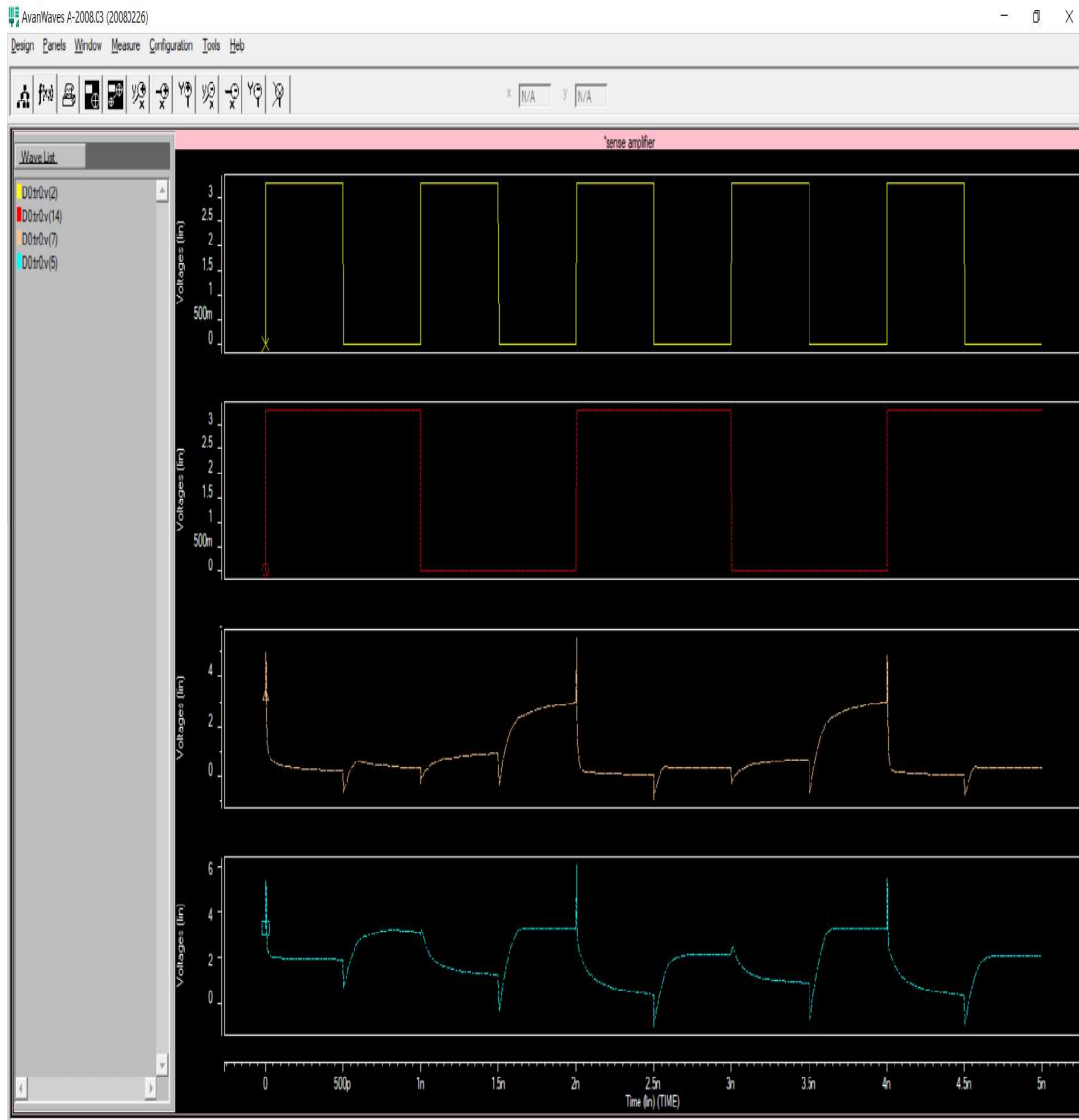


Fig 5.6: Simulation results for Sense Amplifier 130nm MOSFET technology

Figure 5.6 shows the simulation output of Sense Amplifier 130nm MOSFET technology. The inputs given were v(2), v(14) and the output is taken by v(7), v(5).

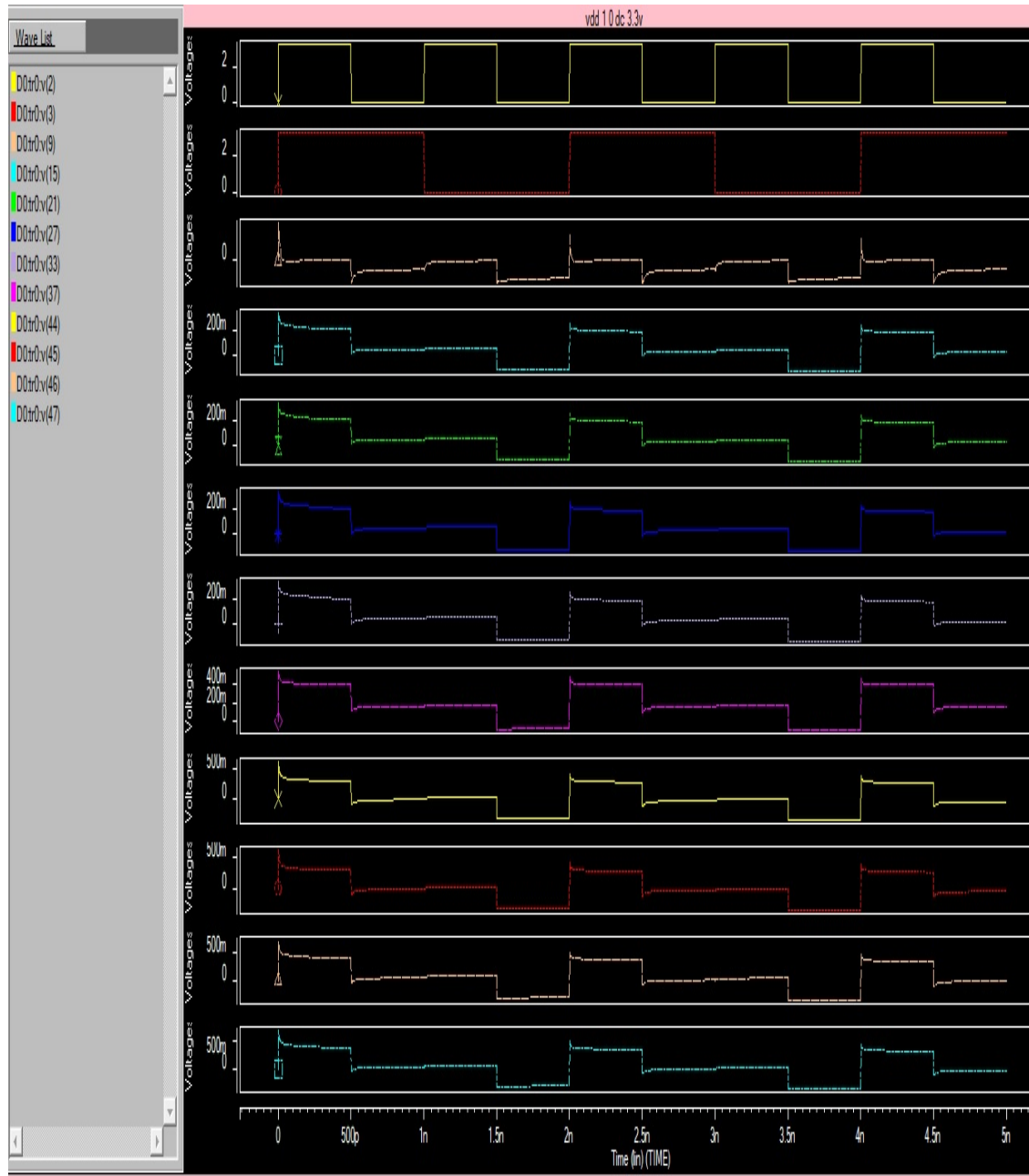


Fig 5.7:Simulation results for SRAM Array architecture 130nm MOSFET technology

Figure 5.7 shows the simulation output of SRAM Array architecture 130nm MOSFET technology. The inputs given were v(2), v(3) and the output is taken by v(9), v(15) , v(21), v(27), v(33), v(37), v(44), v(45), v(46), v(47).

5.2 PERFORMANCE ANALYSIS BY USING 130NM MOSFET TECHNOLOGY

Table 5.1 Performance analysis by using 130nm MOSFET technology

DEVICES	POWER(W)	DELAY(s)	POWERDELAY PRODUCT(J)
Not Gate	7.878 u	2.6076p	20.5426 a
And Gate	17.9 u	46.594p	834.0326a
2:4 Decoder	111.0 u	43.688p	4849.368a
6T SRAM	7.760 u	2.6239p	20.3614a
8T SRAM	9.242 u	4.5847p	42.3717a
Sense Amplifier	316.3 u	6.0539p	1914.84857a
SRAM Array Architecture	484.6 u	498.52p	241582.792a

5.3 SIMULATION OF WAVEFORMS USING 32NM MOSFET TECHNOLOGY

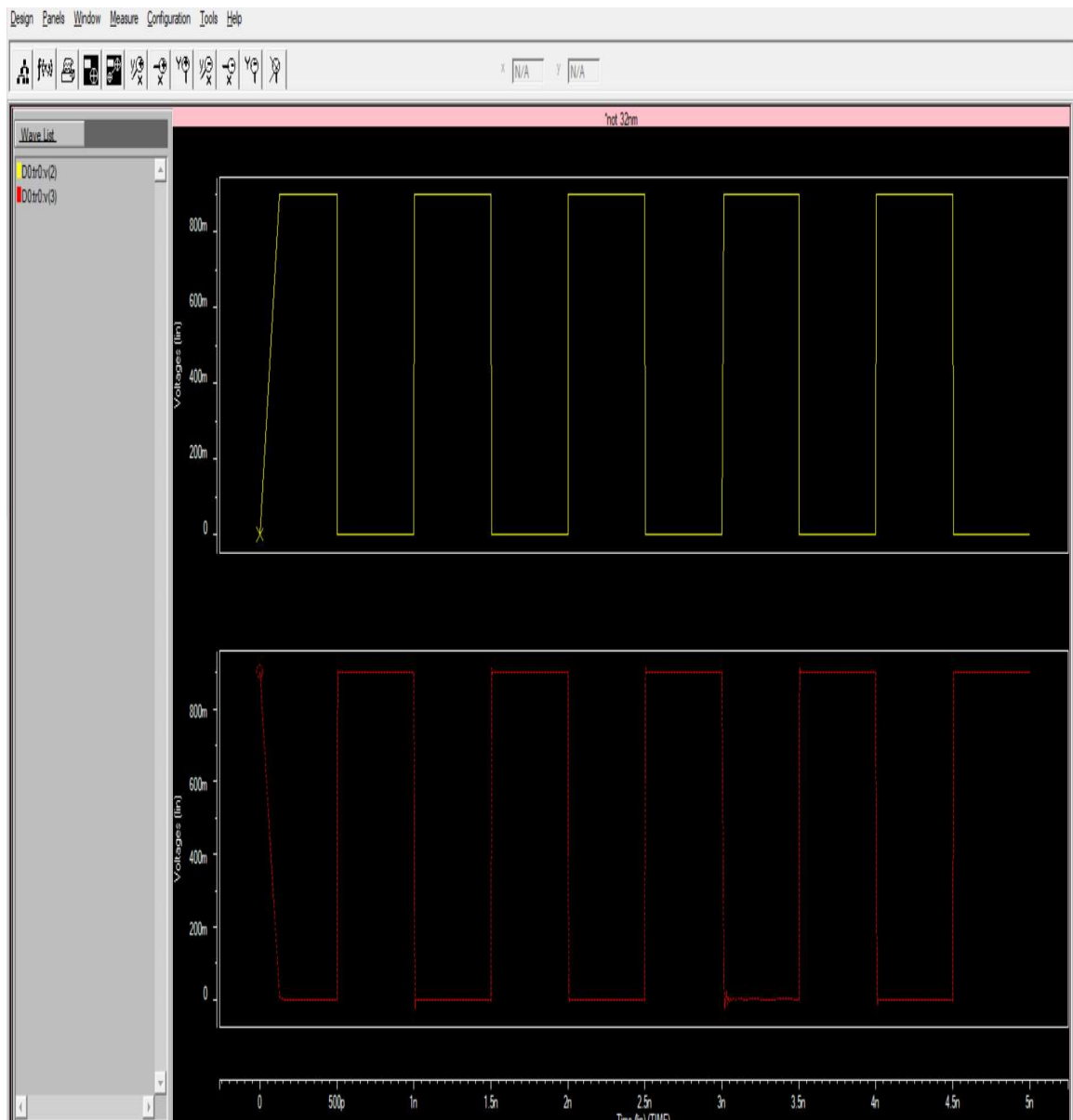


Fig5.8: Simulation results for NOT gate using 32nm MOSFET Technology

Figure 5.8 shows the simulation output of NOT Gate 32nm MOSFET technology.

The inputs given were v(2) and the output is taken by v(3).

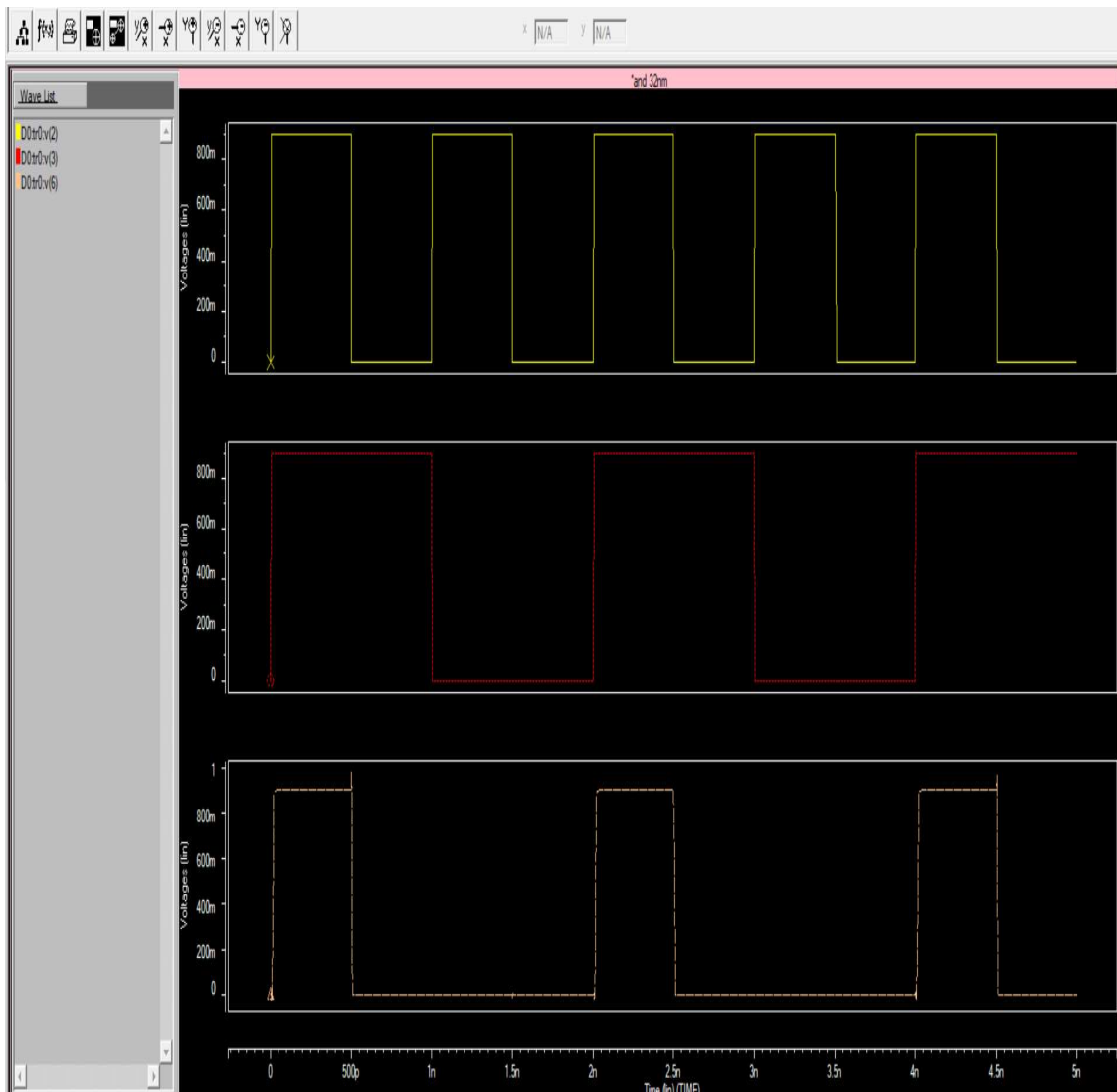


Fig5.9: Simulation results for AND gate using 32nm MOSFET Technology

Figure 5.9 shows the simulation output of AND Gate 32nm MOSFET technology. The inputs given were v(2), v(3) and the output is taken by v(6).

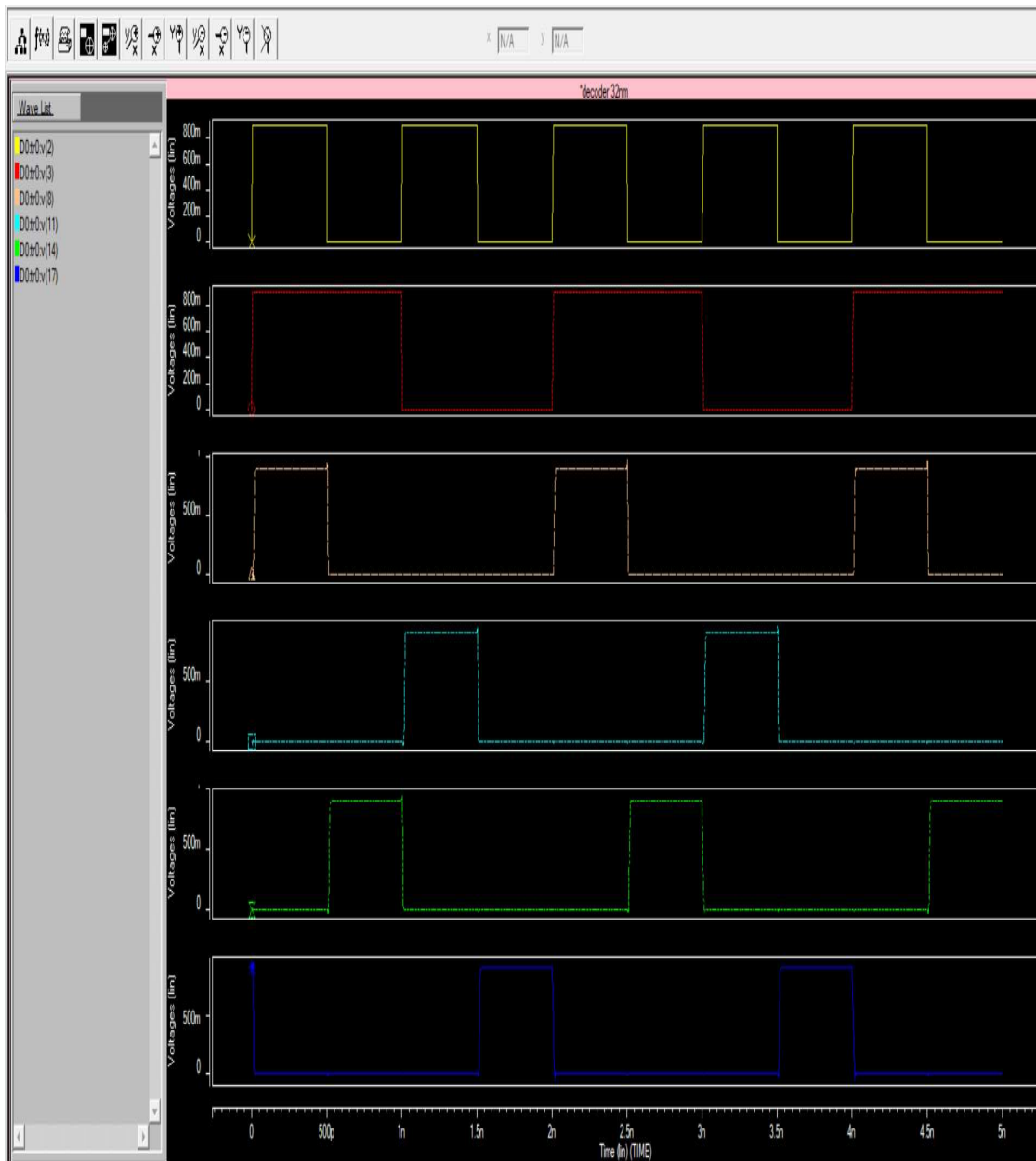


Fig 5.10:Simulation results for DECODER using 32nm MOSFET Technology

Figure 5.10 shows the simulation output of Decoder 32nm MOSFET technology. The inputs given were v(2), v(3) and the output is taken by v(8), v(11), v(14), v(17).

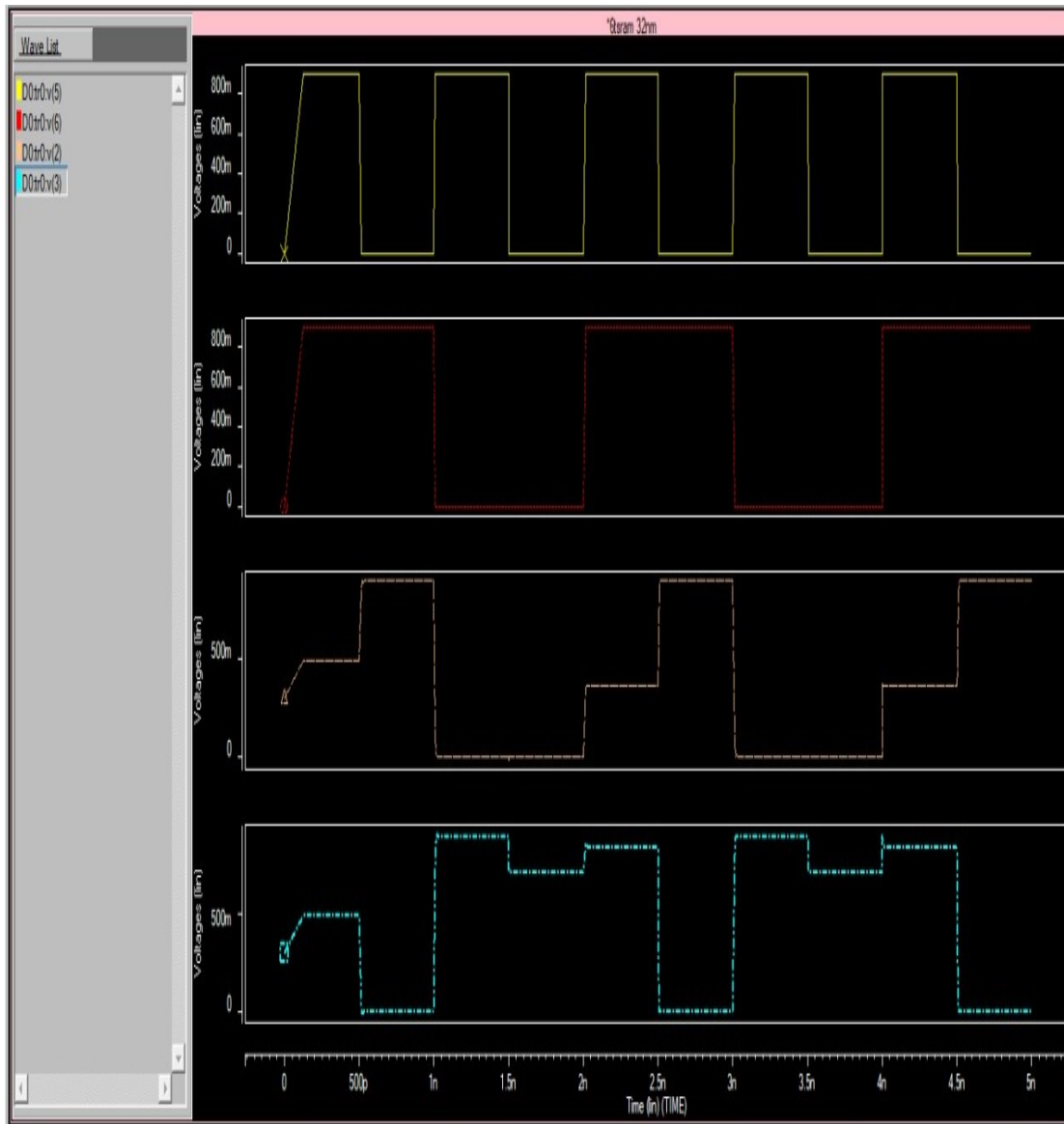


Fig 5.11: Simulation results for 6T SRAM using 32nm MOSFET Technology

Figure 5.11 shows the simulation output of 6T SRAM 32nm MOSFET technology. The inputs given were v(5), v(6) and the output is taken by v(2), v(3).

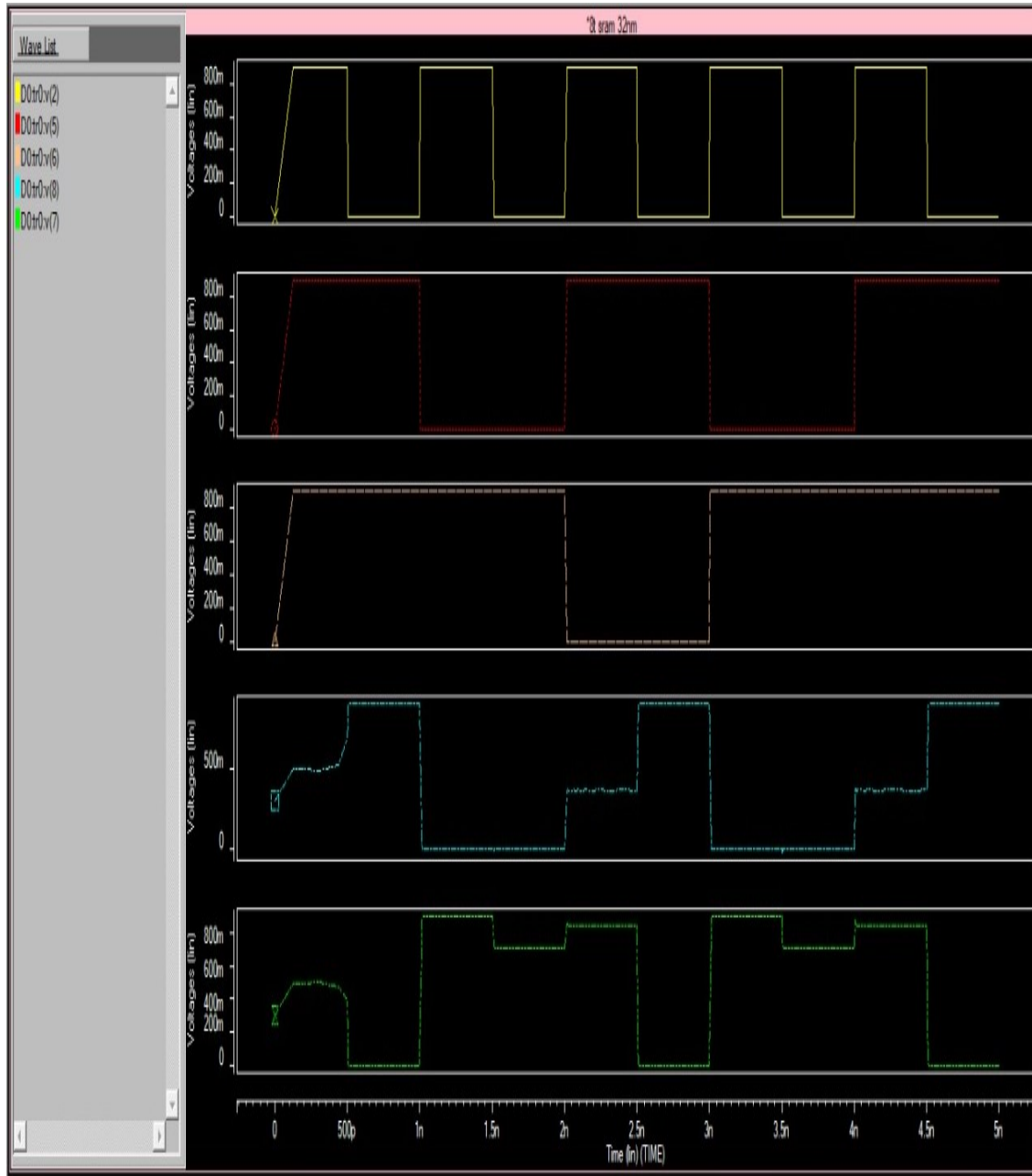


Fig 5.12: Simulation results for 8T SRAM using 32nm MOSFET Technology

Figure 5.12 shows the simulation output of 8T SRAM 32nm MOSFET technology. The inputs given were v(2), v(5) and the output is taken by v(6), v(8), v(7).

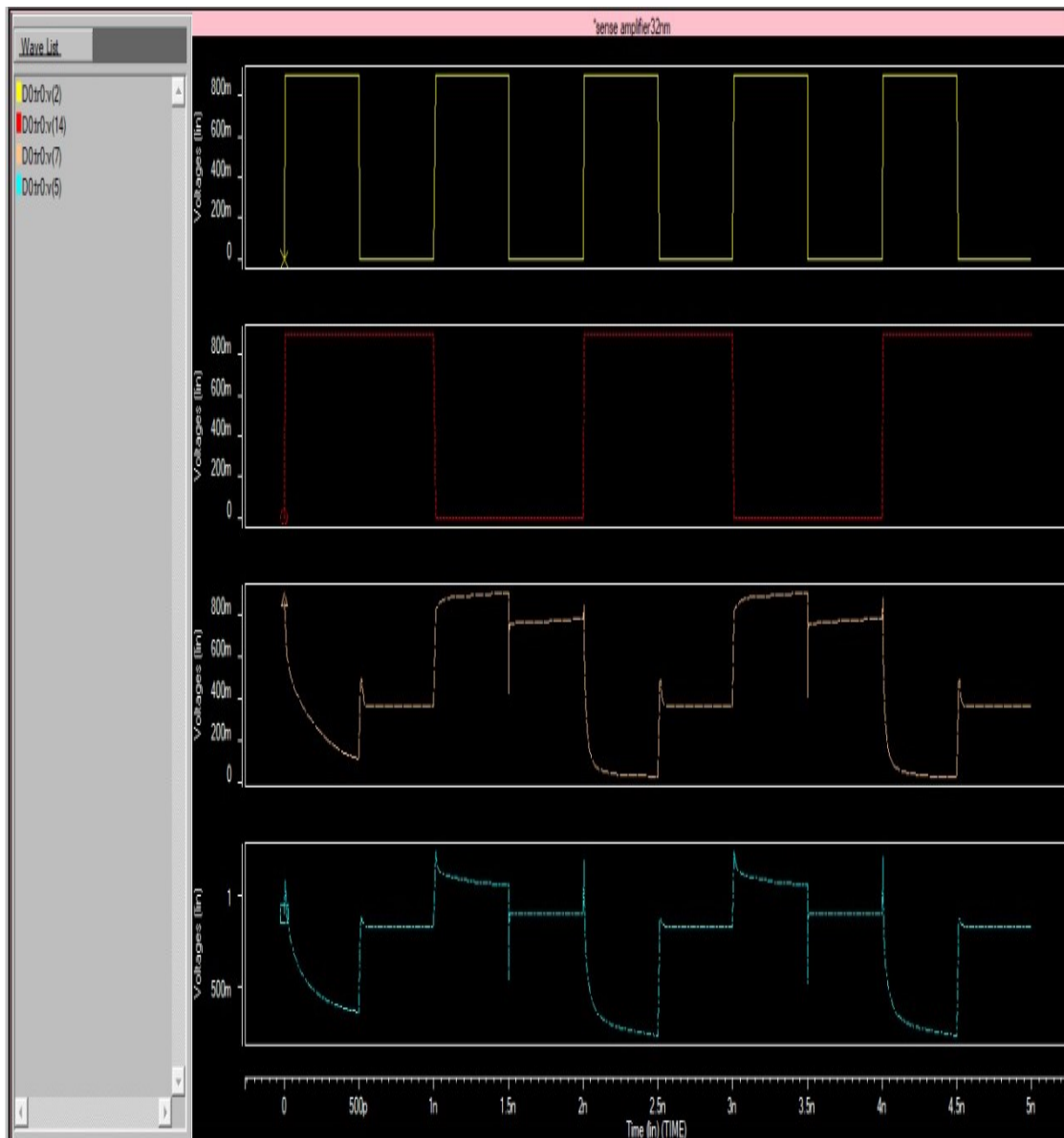


Fig 5.13: Simulation results for SENSE AMPLIFIER using 32nm MOSFET Technology

Figure 5.13 shows the simulation output of Sense Amplifier 32nm MOSFET technology. The inputs given were v(2), v(14) and the output is taken by v(7), v(5).

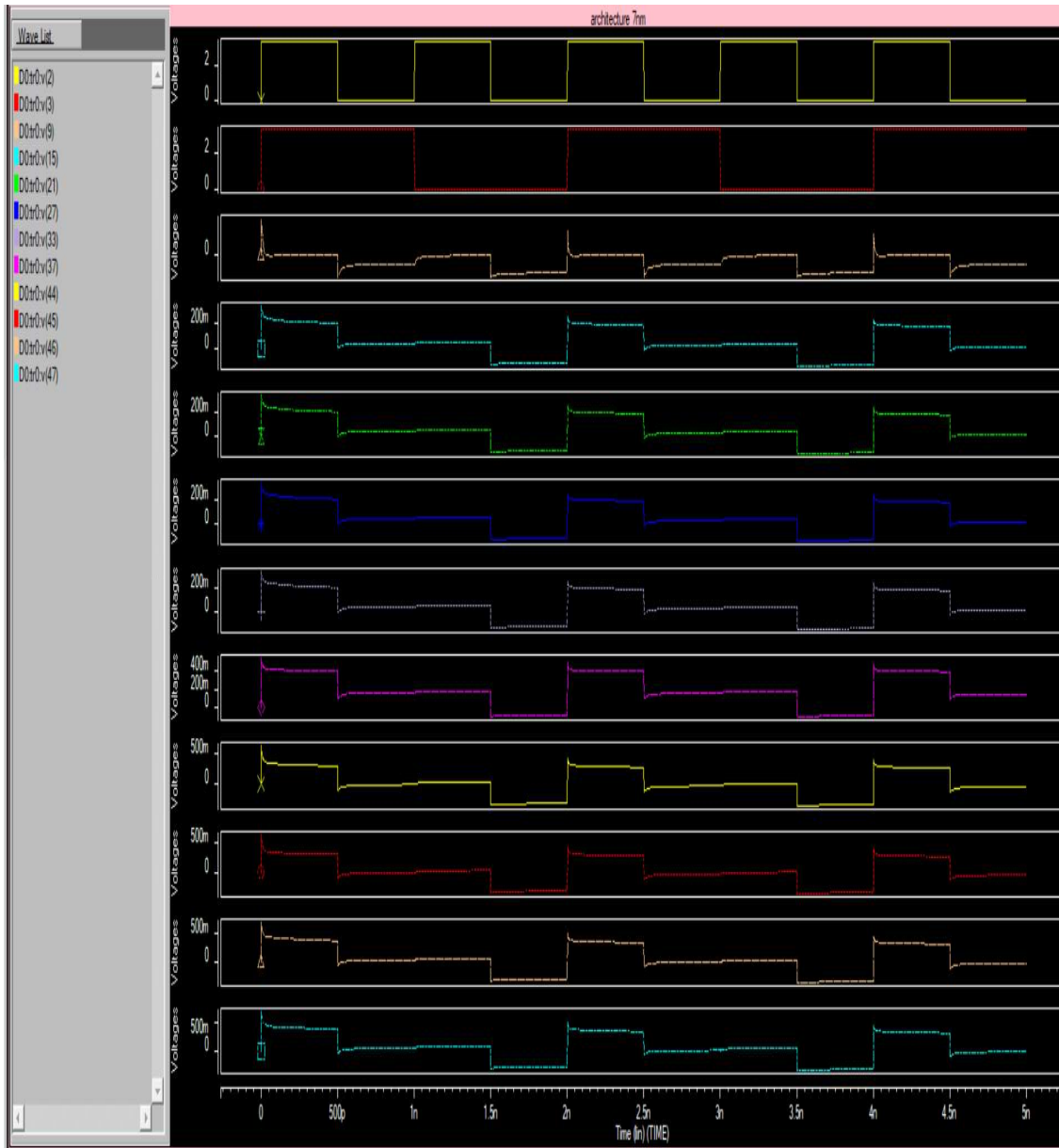


Fig 5.14: Simulation results for SRAM ARRAY ARCHITECTURE using 32nm MOSFET Technology

Figure 5.14 shows the simulation output of SRAM Array architecture 32nm MOSFET technology. The inputs given were v(2), v(3) and the output is taken by v(9), v(15) , v(21), v(27), v(33), v(37), v(44), v(45), v(46), v(47).

5.4 PERFORMANCE ANALYSIS BY USING 32NM MOSFET TECHNOLOGY

Table 5.2 Performance analysis by using 32nm MOSFET Technology

DEVICES	POWER	DELAY(s)	POWER DELAY PRODUCT(J)
Not Gate	0.04849u	0.41401p	0.0200753 a
And Gate	0.1961u	4.6525p	0.9123 a
2*4 Decoder	0.9495u	4.8707p	4.6247 a
6T SRAM	13.25u	2.2323p	29.5779 a
8T SRAM	16.45u	3.3387p	54.9216 a
Sense Amplifier	1.553u	9.1829p	14.2610 a
SRAM Array Architecture	14.32u	62.792p	899.1814 a

5.5 SIMULATION OF WAVEFORMS USING 7NM FINFET TECHNOLOGY

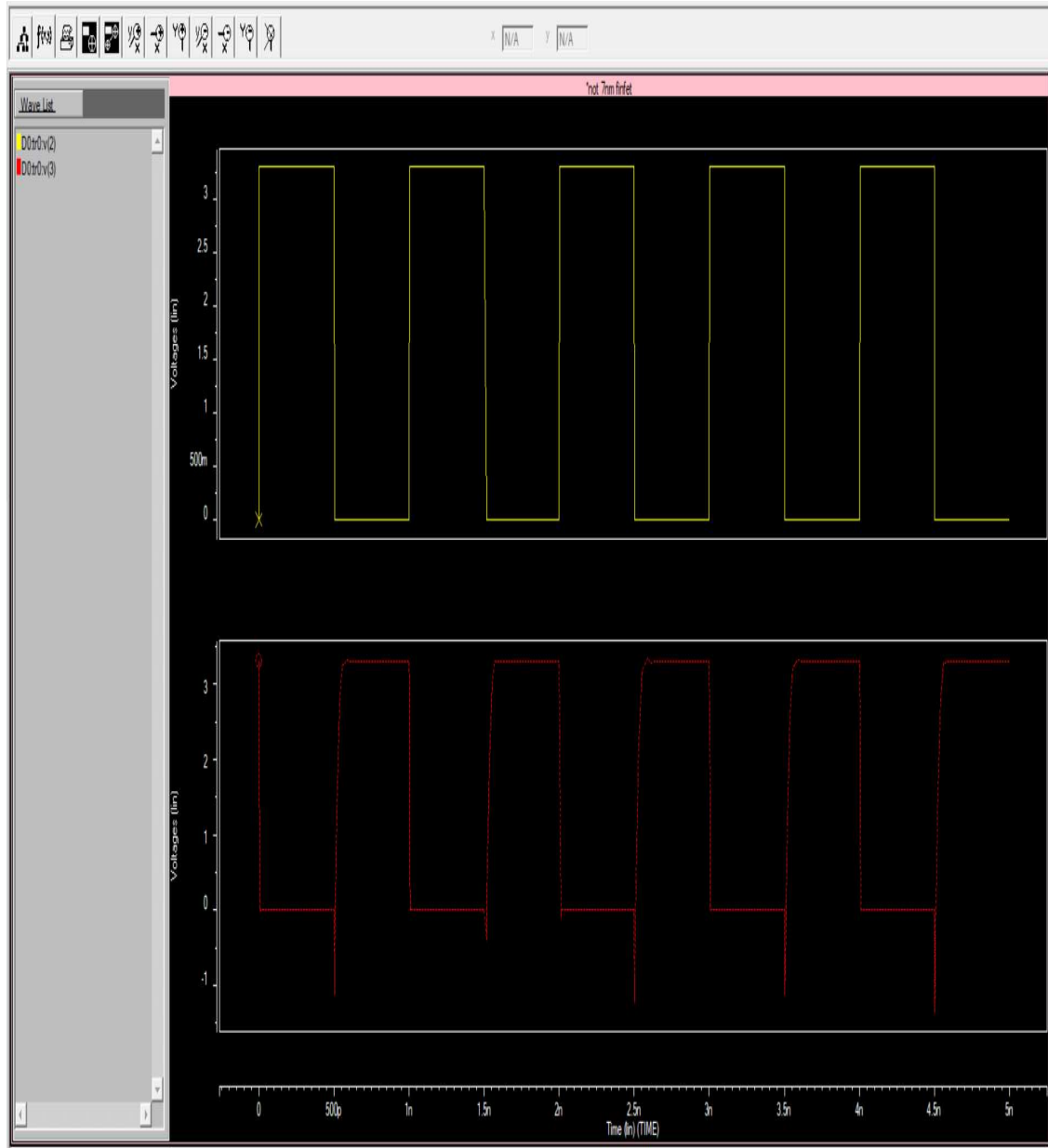


Fig 5.15: Simulation results for NOT gate using 7nm FINFET technology.

Figure 5.15 shows the simulation output of NOT Gate 7nm FINFET technology. The inputs given were v(2) and the output is taken by v(3).

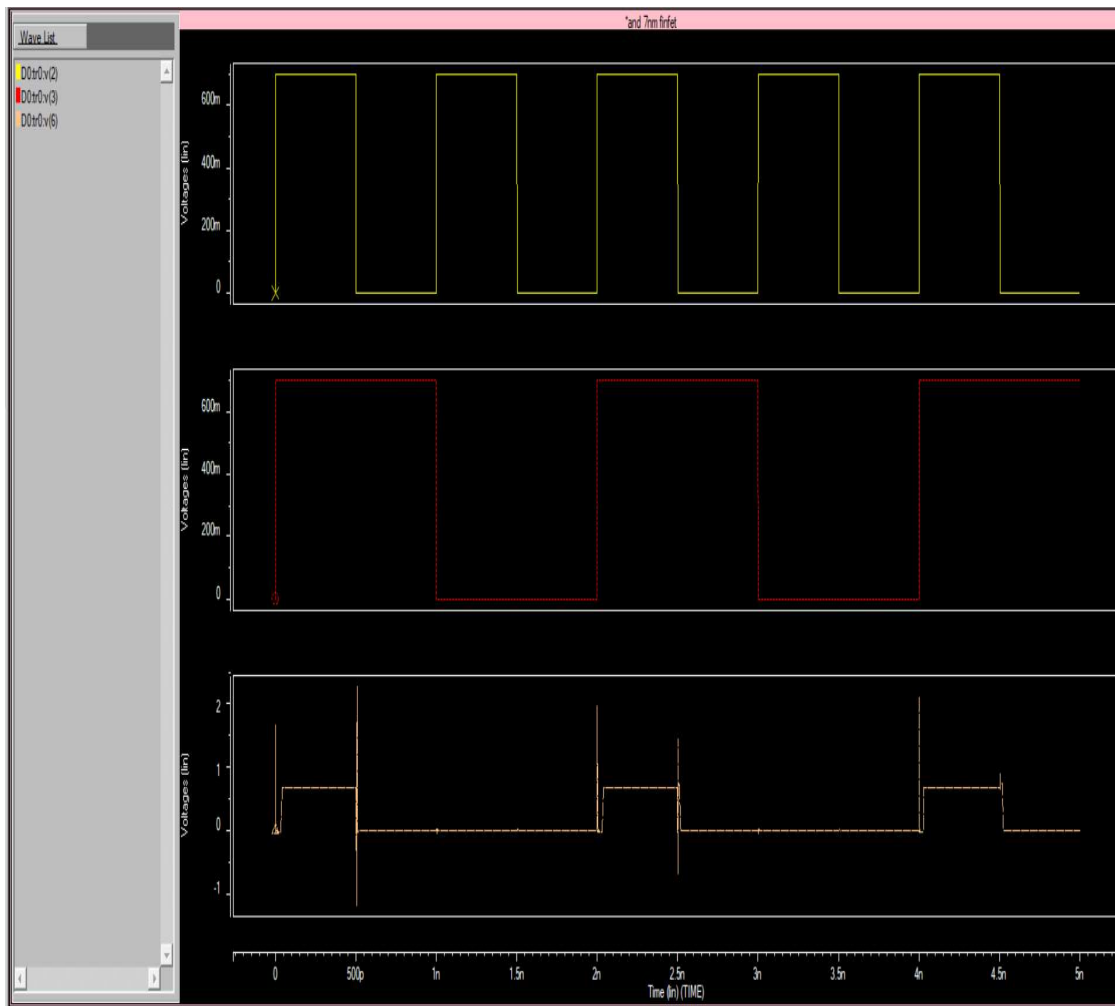


Fig 5.16: Simulation results for AND gate using 7nm FINFET technology.

Figure 5.16 shows the simulation output of AND Gate 7nm FINFET technology. The inputs given were v(2), v(3) and the output is taken by v(6).

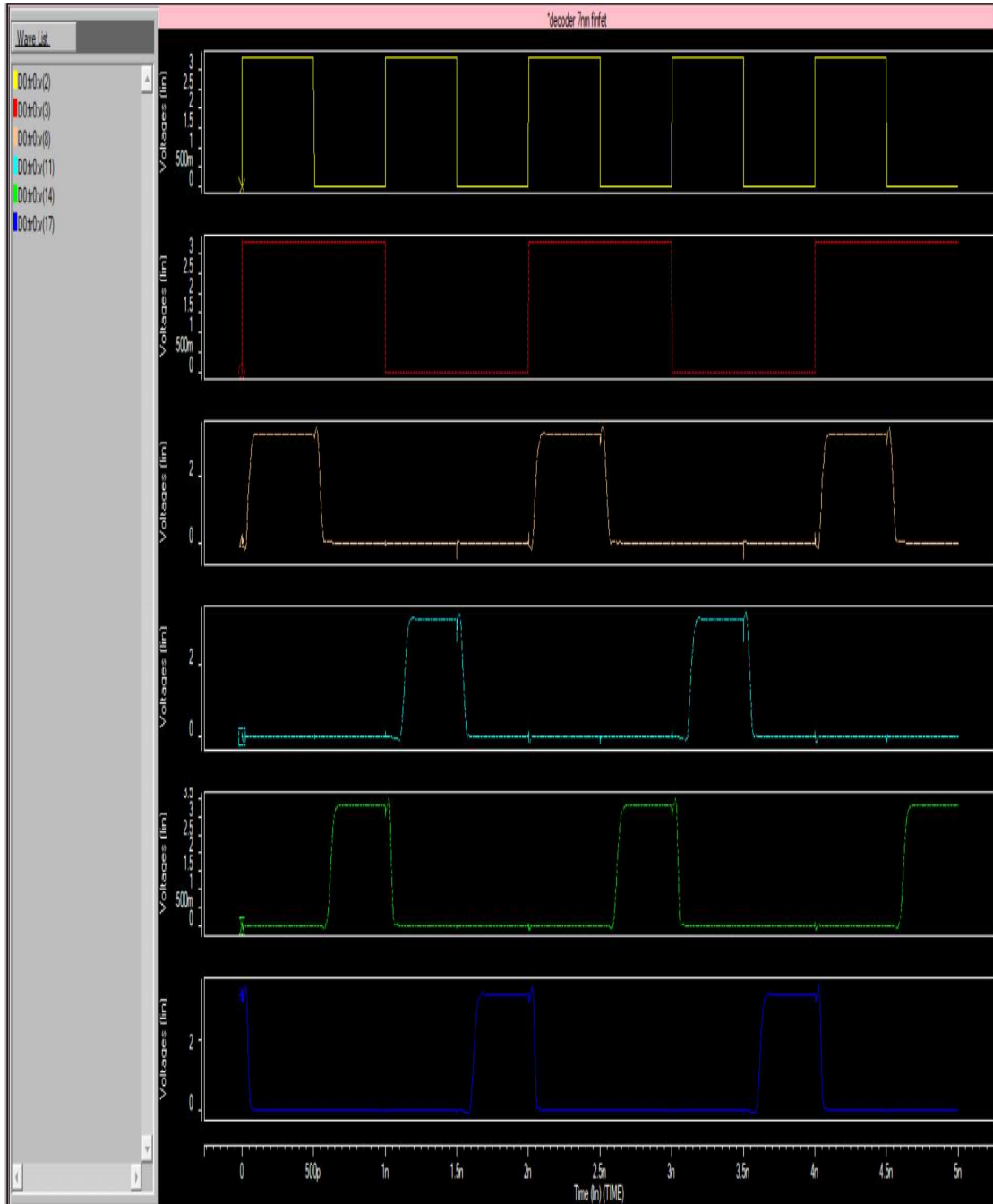


Fig 5.17: Simulation results for DECODER using 7nm FINFET technology.

Figure 5.17 shows the simulation output of Decoder 7nm FINFET technology. The inputs given were v(2), v(3) and the output is taken by v(8), v(11), v(14), v(17).

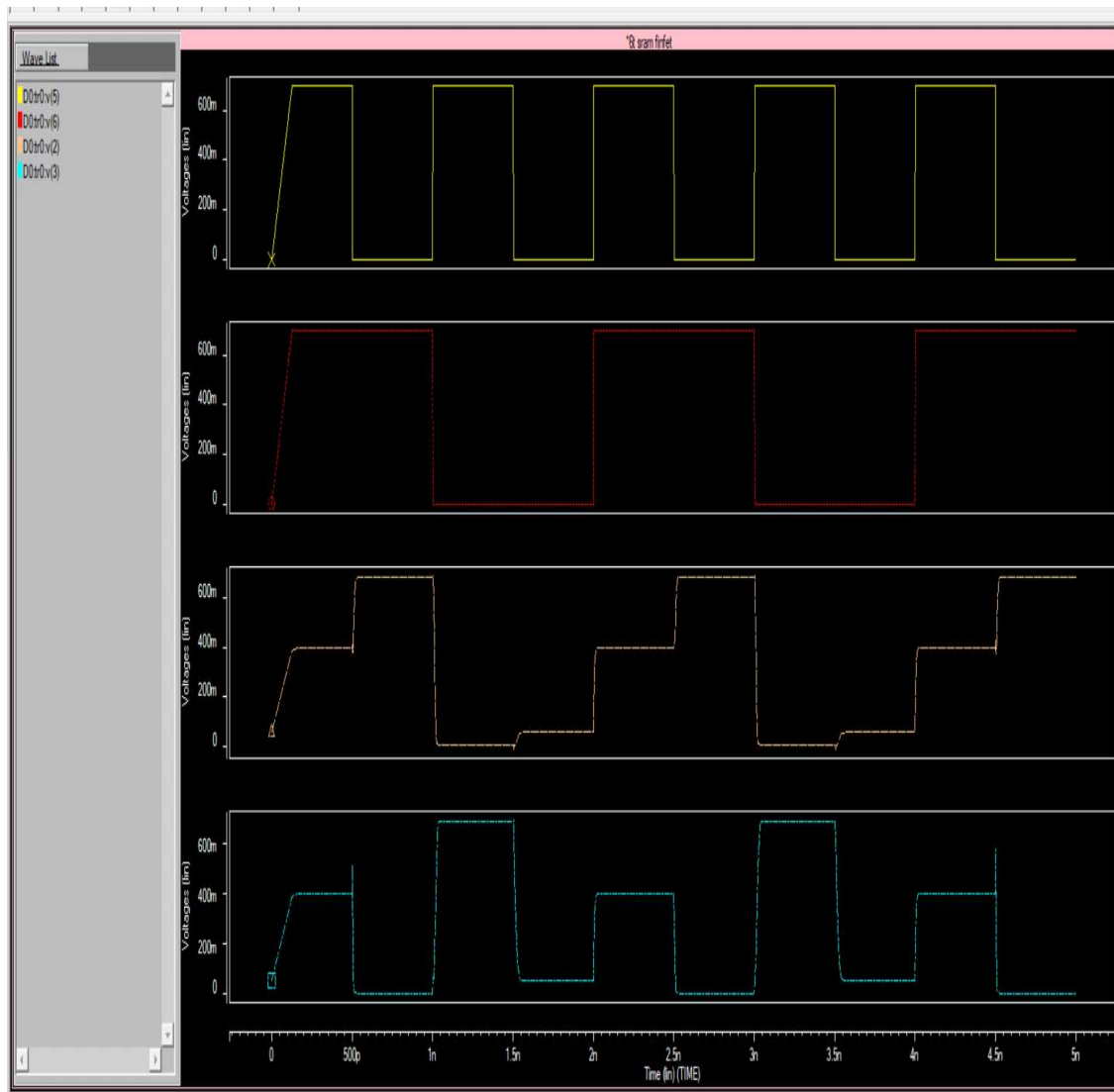


Fig 5.18: Simulation results for 6T SRAM using 7nm FINFET technology.

Figure 5.18 shows the simulation output of 6T SRAM 7nm FINFET technology. The inputs given were v(5), v(6) and the output is taken by v(2), v(3).

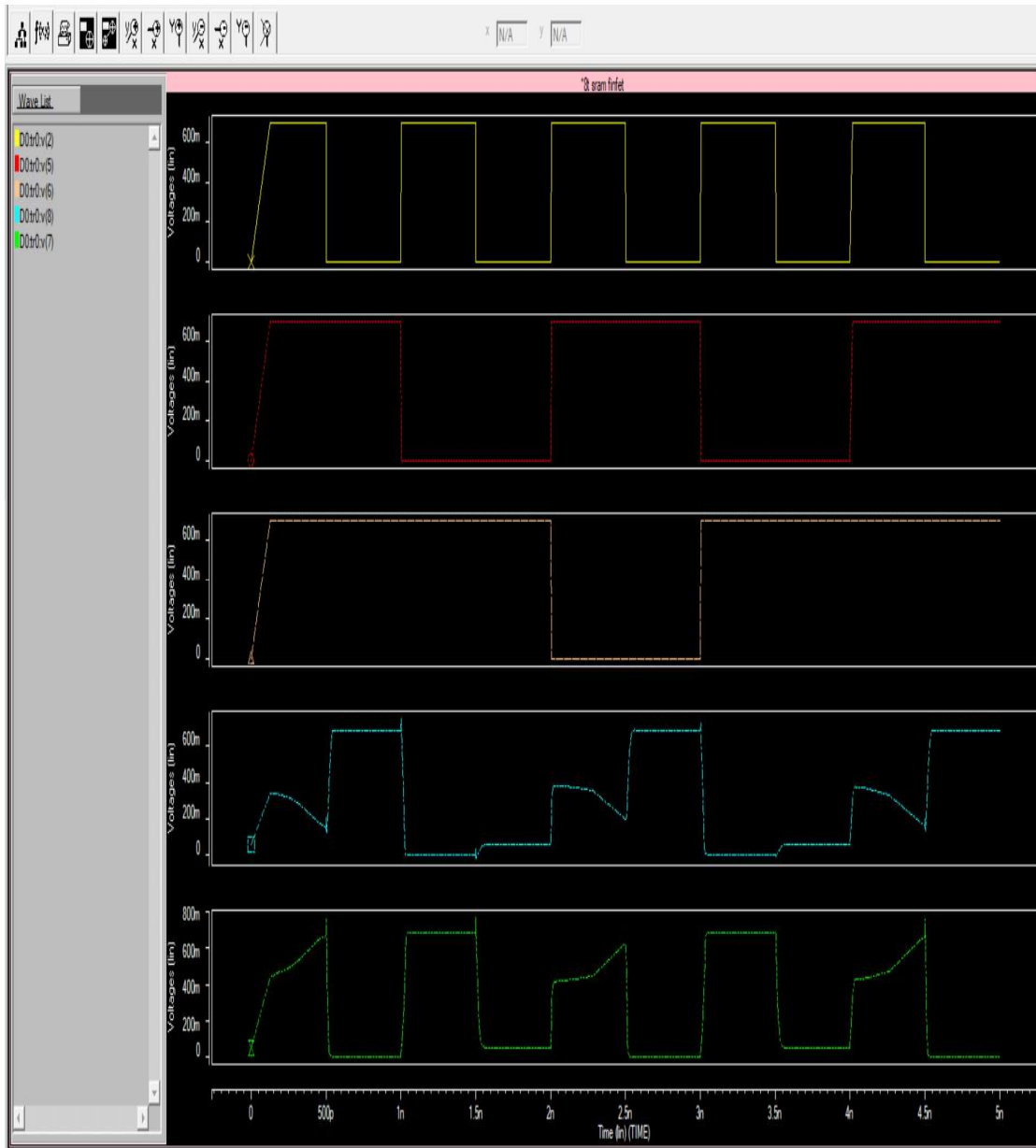


Fig 5.19: Simulation results for 8T SRAM using 7nm FINFET technology.

Figure 5.19 shows the simulation output of 8T SRAM using 7nm FINFET technology. The inputs given were v(2), v(5) and the output is taken by v(6), v(8), v(7).

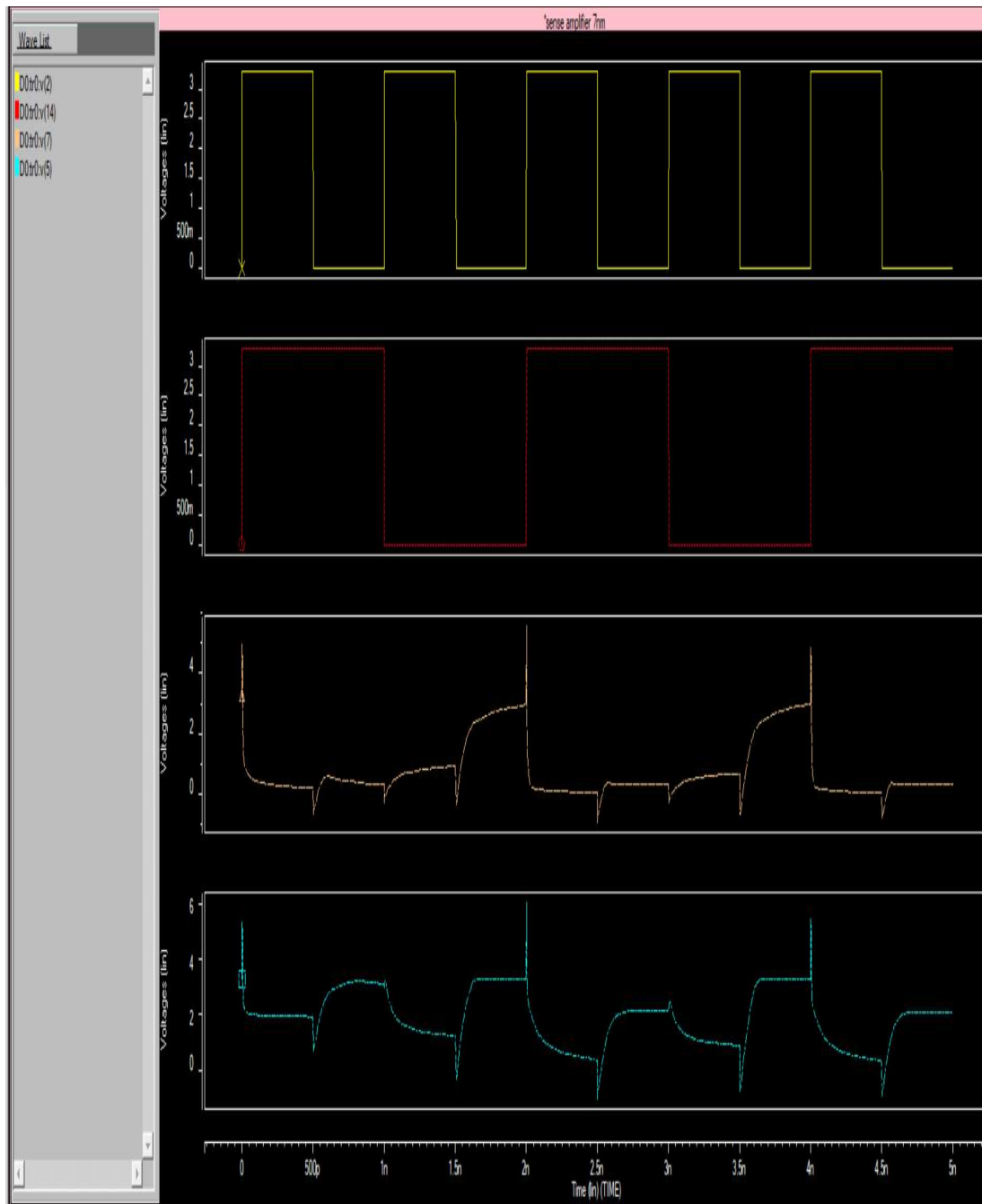


Fig 5.20: Simulation results for SENSE AMPLIFIER using 7nm FINFET technology.

Figure 5.20 shows the simulation output of SENSE AMPLIFIER using 7nm FINFET technology. The inputs given were v(2), v(14) and the output is taken by v(7), v(5).

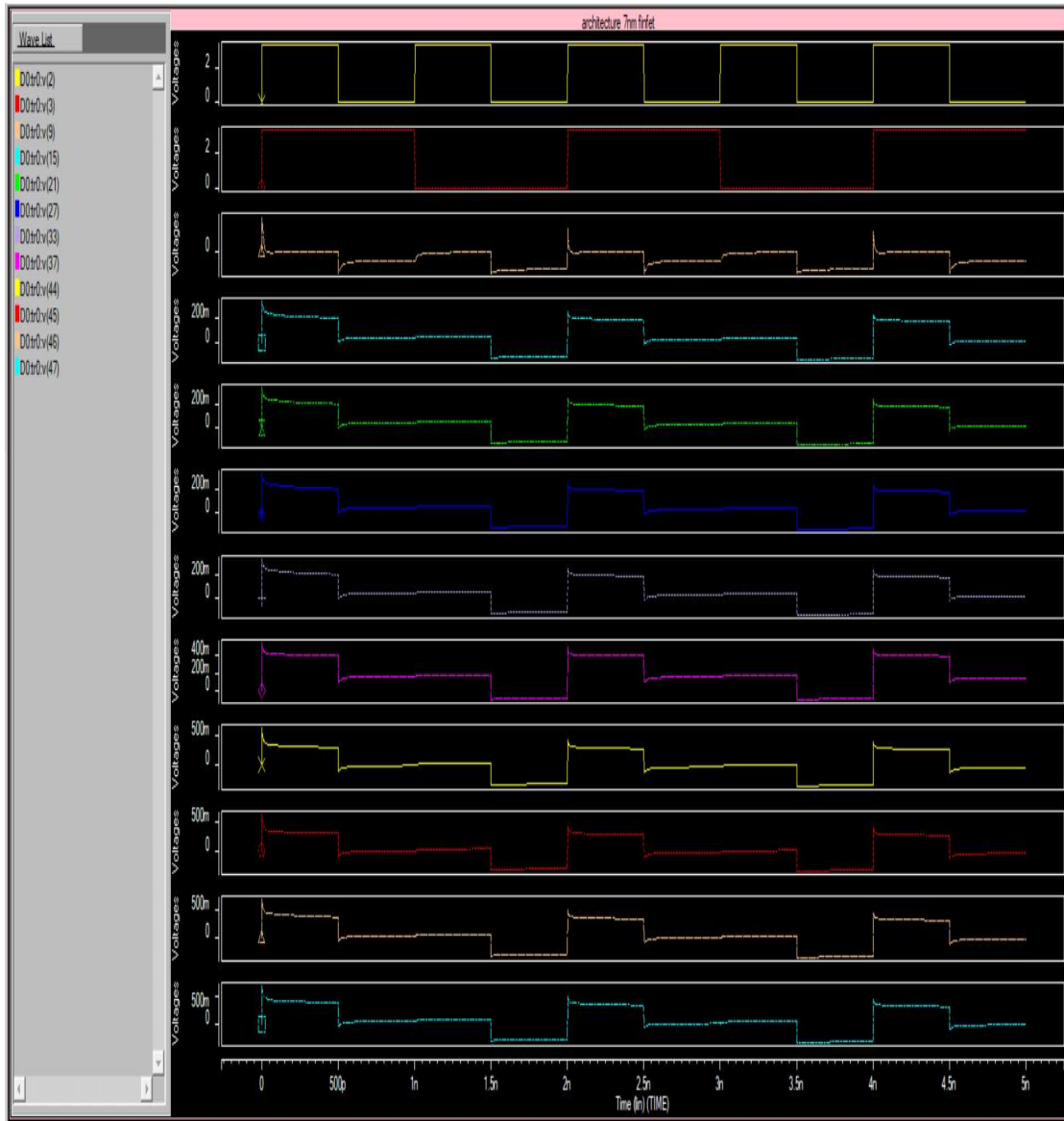


Fig 5.21: Simulation results for SRAM ARRAY ARCHITECTURE using 7nm FINFET technology.

Figure 5.21 shows the simulation output of SRAM Array architecture using 7nm FINFET technology. The inputs given were v(2), v(3) and the output is taken by v(9), v(15), v(21), v(27), v(33), v(37), v(44), v(45), v(46), v(47).

5.6 PERFORMANCE ANALYSIS BY USING 7NM FINFET TECHNOLOGY

Table 5.3 Performance analysis by using 7nm FINFET technology

DEVICES	POWER(W)	DELAY(s)	POWER DELAY PRODUCT(J)
Not Gate	0.04332 u	4.13f	0.0001789116a
And Gate	0.07520 u	6.85f	0.00051512 a
2:4 Decoder	0.3431 u	24.99f	0.008574069a
6T SRAM	0.1776 u	7.4625f	0.00132534 a
8T SRAM	0.2330 u	13.319f	0.003103327 a
Sense Amplifier	0.006273 u	56.98f	0.0003574355 a
SRAM Array Architecture	0.5815 u	87.22f	0.05071843 a

5.7 DC ANALYSIS OF SRAM ARCHITECTURE USING FINFET TECHNOLOGY

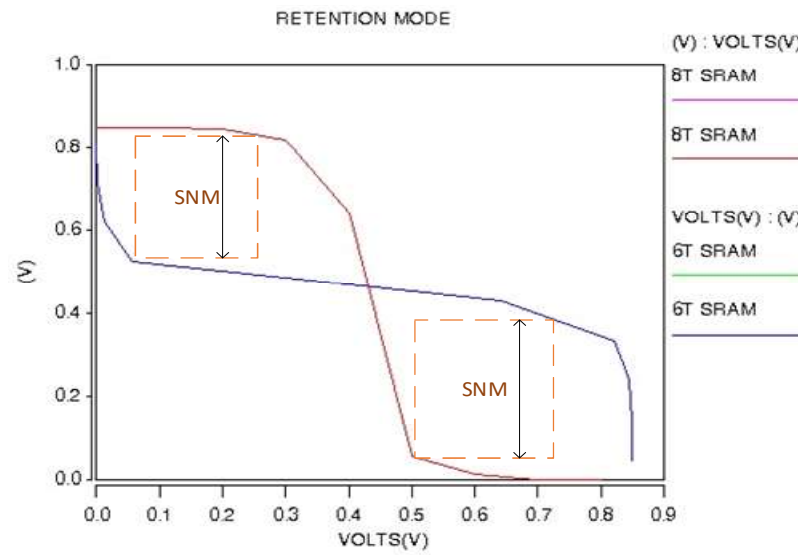


Fig 5.22: Butterfly curve of FINFET-based SRAM architecture in retention mode

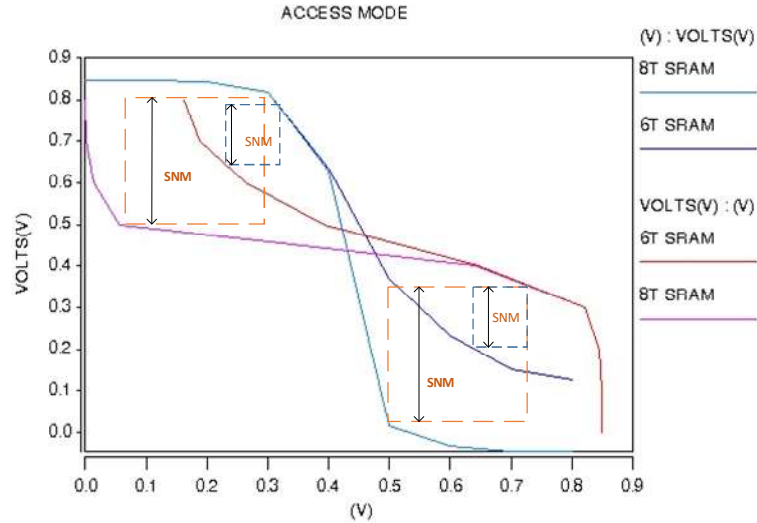


Fig 5.23: Butterfly curve of FINFET-based SRAM architecture in access mode

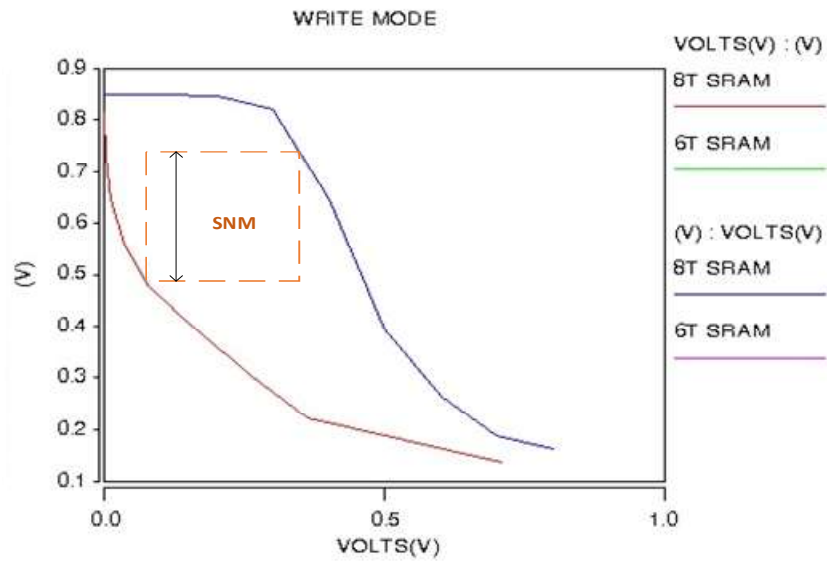


Fig 5.24: Butterfly curve of FINFET-based SRAM architecture in write mode

Table 5.4: Analysis of noise margin using MOSFET and FINFET

SRAM CHARACTERISTICS	SRAM ARCHITECTURE	
	MOSFET	FINFET
SNM (mV)	245	300
RSNM (mV)	170	215
WSNM (mV)	359	390

5.8 COMPARISON OF POWER IN EXISTING SYSTEM USING CMOS130NM AND CMOS 32NM, FINFET 7NM

TABLE 5.5 COMPARISION OF POWER

COMPONENTS	Power at CMOS 130NM	Power at CMOS 32NM	Power at FINFET 7NM
NOT	7.878 u	0.04849u	0.04332 u
AND	17.9 u	0.1961u	0.07520 u
2:4 DECODER	111.0 u	0.9495u	0.3431 u
6T SRAM	7.760 u	13.25u	0.1776 u
8T SRAM	9.242 u	16.45u	0.2330 u
SENSE AMPLIFIER	316.3 u	1.553u	0.006273 u
SRAM ARRAY ARCHITECTURE	484.6 u	14.32u	0.5815 u

5.9 COMPARISON OF DELAY IN EXISTING SYSTEM USING CMOS 130NM AND CMOS 32NM, FINFET 7NM

TABLE 5.6 COMPARISION OF DELAY

COMPONENTS	Delay at CMOS 130NM	Delay at CMOS32NM	Delay atFINFET 7NM
NOT	2.6076p	0.41401p	4.13f
AND	46.594p	4.6525p	6.85f
2:4 DECODER	43.688p	4.8707p	24.99f
6T SRAM	2.6239p	2.2323p	7.4625f
8T SRAM	4.5847p	3.3387p	13.319f
SENSE AMPLIFIER	6.0539p	9.1829p	56.98f
SRAM ARRAY ARCHITECTURE	498.52p	62.792p	87.22f

5.10 COMPARISON OF POWERDELAYPRODUCT IN EXISTING SYSTEM USING CMOS 130NM AND CMOS 32NM, FINFET 7NM

TABLE 5.7 COMPARISION OF POWER DELAY PRODUCT

COMPONENTS	Power delay product at CMOS 130NM	Power delay product at CMOS 32NM	Power delay product atFINFET7NM
NOT	20.5426a	0.0200753a	0.0001789116a
AND	834.0326a	0.9123a	0.00051512a
2:4 DECODER	4849.368a	4.6247a	0.008574069a
6T SRAM	20.3614a	29.5779a	0.00132534a
8T SRAM	42.3717a	54.9216a	0.003103327a
SENSE AMPLIFIER	1914.84857a	14.2610a	0.0003574355a
SRAM ARRAY ARCHITECTURE	241582.792a	899.1814a	0.05071843a

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

FINFET is a another promising substitute to remove the challenges and obstacles that are faced by conventional planar MOSFET in sub-100 nm technology. The usage of FINFET has made further scaling of SRAM due to reduced random dopant fluctuation, steeper subthreshold slope, and relief of high-K material as gate oxide. We have performed simulation and analysis of 6T SRAM, 8T SRAM and SRAM array architecture by using 130 nm, 32 nm MOSFET technology and 7nm FINFET technology. And compared the characteristics of both MOSFET and FINFET Technology in terms of Power, Delay and Power Delay Product. The design and simulation of the SRAM model are accomplished in Synopsys HSpice tool based on 15nm technology. The simulation results reveal that the FINFET-based 6T SRAM, 8T SRAM, SRAM Array Architecture cells show significant improvement in their performance with better stability and low-power consumption than MOSFET based 6T SRAM cell, 8T SRAM cell and SRAM array architecture respectively.

This project also investigates on the stability performance in retention, read and write mode of 7nm FINFET based 8T SRAM cell. A butterfly curve is extracted from the voltage transfer curve (VTC) of two cross-coupled FINFET-based inverters to obtain and analyse the noise margin based on the read, write and retention operations. SNM acquired from the maximum square of the VTC of the inverter. There are two types of the SNM that affect the stability of the SRAM cell, namely, the write static noise margin (WSNM) and access static noise margin(ASNM). FINFET, and MOSFET-based 8T SRAM cells improved access static noise margin considerably by 28%, and 20.5%, respectively, as well as average power consumption significantly by 99.05%, and 83.3%, respectively, to the FINFET, and MOSFET-based 6T SRAM design. From the findings, It can be concluded that both FINFET and MOSFET 8T SRAM cell gives better performance in Static Noise Margin (SNM) and power consumption than 6T SRAM cells.

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