

PERFORMANCE METRICS OF AN EFFICIENT PWM ARCHITECTURE USING GNRFET TECHNOLOGY

Submitted in partial fulfillment of the requirements for the award of Bachelor of
Engineering degree in Electronics and Communication Engineering

By

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of DAKAMURI MEGHANA (Register No:- 37130094) and EPPEPALLE SIREESHA (Register No:- 3713012) who carried out the project entitled Performance Metrics of an Efficient PWM Architecture Using GNR FET Technology under my supervision from November 2020 to April 2021.

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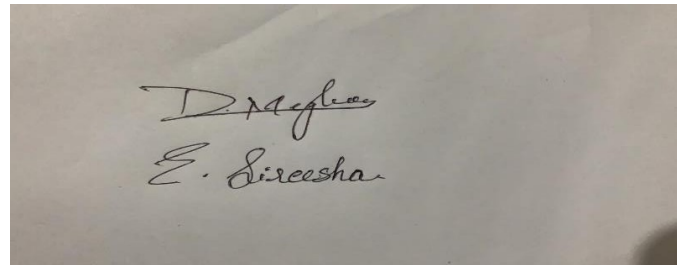
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DECLARATION

We, D.Meghana and E.Sireesha hereby declare that the Project Report entitled “Performance metrics of an efficient PWM architecture using GNR FET” done by us under the guidance of Mr.N.Mathan.,M.Tech., (Ph.D) is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering / Technology degree in Electronics and Communication Engineering.

DATE:

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A photograph of a piece of paper with two handwritten signatures in black ink. The first signature is 'D. Meghana' and the second is 'E. Sireesha'.

SIGNATURE OF CANDIDATES

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ABSTRACT

Pulse-Width Modulation (PWM) is a technique for reducing the average power provided by an electrical signal by efficiently dividing it into discrete components. The average voltage (and current) value supplied to the load is regulated by rapidly switching the load's power supply on and off. The longer the switch is engaged, the more total power is supplied to the load. It is one of the primary ways, along with maximum power point tracking (MPPT), of reducing the output of solar panels to what a battery can use. PWM is particularly suited to inertial loads such as motors, which react slowly due to their inertia and are thus less easily influenced by this discrete switch. The PWM switching frequency must be high enough so that it does not impact the load, i.e. the resulting waveform of the load must be as smooth as possible. Since it can operate at low voltage, the digital buck converter has recently been studied for low voltage applications in a number of ways. The digital PWM controller adjusts the PWM duty ratio using a fast shift record and a slow bidirectional shift register. The automated buck converter, on the other hand, is ineffective since the shift register employs quantized delays. This optical buck converter's PWM resolution must be increased in order to reliably track the output current and reduce the output voltage rib. A PWM buck converter is proposed that uses only D flip-flops (DFFs) to generate a PWM signal in a PWM duty-ratio shift register, thereby reducing clock power.

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CHAPTER 1

INTRODUCTION

Graphene, a monolayer of carbon atoms wrapped in a two-dimensional wave grid, has emerged as a promising candidate material for nanoelectronics applications outside of the CMOS system. Graphene-based devices have high mobility for ballistic transport, rapid switching and high carrier speeds, thin body monolayers for optimal electrostatic scaling, and excellent thermal conductivity. Wafer-scale graphene films with full planar processing have a high integration potential with conventional CMOS manufacturing procedures (CNTs). Although two-dimensional graphene is a zero-band-gap half-metal, when a FET channel is made of nanometer-wide nano-bands, a band-gap opens (GNR). A recent experiment revealed that all sub-10nm GNRs are semiconductants due to the edge effect, making them more suitable for electronic device applications than CNTs, which are metal-and-semiconductor mixtures.

A important difference between GNRFETs and scaled CMOS nodes is that the optimum EDP of GNRFETs at operating point B is 40–168X higher in scaled CMOS. GNRFETs have a lower noise margin and are more susceptible to variability and defects than scaled CMOS.

Quantum effects and atomic scale features are unavoidable in nano-electronic devices and circuits. From the ground up, we designed a multi-scale simulation architecture that addresses atomic characteristics in circuit simulations. The simulation framework is used to investigate GNRFET circuits, with a particular emphasis on variability and load impurity effects. The GNR material allows for ultra- small, fast, and low-energy FETs, but it has two significant side effects due to variability and defects: leakage and low noise levels. A couple of A difference in channel width, for example, changes the leakage current by an order of magnitude, and a single coulomb charge impurity reduces the FET current by around 30%. Dense memories, which are the most promising opportunities for graphic devices, are particularly vulnerable to changes and failures, with almost no noise and increasing leakage capability.

This analysis of the effect of variability, defects, and parasites on circuit performance demonstrates the importance of these factors.

1.1 MOTIVATIONS

To improve the performance of PWM Architecture, the digital design will be updated for low-power applications to improve low-power efficiency technologies. Power, loss, power delay, rise time, and fall time characteristics of MOSFET and GNRFET technology for GNRFET DSP applications.

1.2 NOT GATE

An inverter circuit generates a voltage that is diametrically opposed to the frequency of its input logic. Its primary function is to invert the applied input signal. The output is high if the input is low, and vice versa. Inverters may be constructed with a single NMOS transistor or a single PMOS transistor and a resistor. This 'resistive-drain' solution can be produced at a low cost since it only uses a single transistor shape. Even so, since current flows through a resistor in either of the two states, the resistive drain configuration is inefficient in terms of power consumption and processing speed. Inverters in a CMOS configuration can also be constructed using two complementary transistors. Since one of the transistors is always turned off in both logical states, this design significantly reduces power consumption.

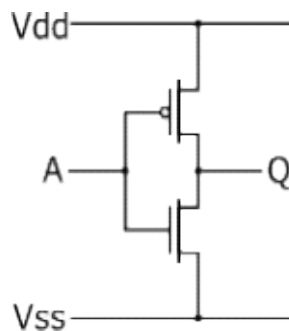


Fig 1.1 NOT Gate

1.3 BUFFER

A wireless buffer is a kind of electronic circuit element that separates the input from the output by providing either no voltage or no voltage. The same as the input voltage. It draws very little current and does not interfere with the original circuit. It is known as a unit buffer

because it has a gain of one, ensuring that it has no distortion at most the same voltage as the input voltage.

The feedback impedances of a stress buffer are very high (the opposition to current flow viewed from the load). Because of the high input impedance, a stress buffer is used. Because of the high input buffer impedance, a circuit containing a voltage buffer often draws a small amount of power. The power source is also unaffected..

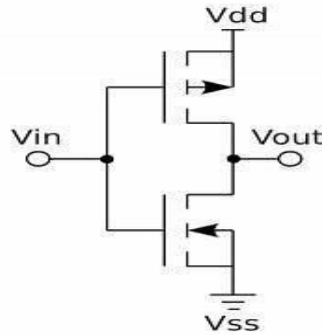


Fig 1.2 Buffer

1.4OR GATE

The OR gate is a digital logic gate that acts in conjunction with the truth table on the right to execute logical disjunction. The result is HIGH performance if one or both of the gate's inputs are HIGH (1). 1. formal introductory phrase If none of the inputs is high, the result is a LOW performance (0). OR gates are basic logic gates that can be used in TTL and CMOS logic families. They find the limit of two binary digits in the same way as the complementary AND function considers the lowest. The 4071 is a 4000 series CMOS IC with four separate two-input OR gates. The 7432 is a transistor-transistor-logic (TTL) computer. There are several variants of the original 7432 OR doors, each with the same pinout but a different internal architecture that enables them to operate over a broader range of voltages and/or at higher speeds. In addition to the standard 2-input OR gate, 3- and 4-input OR gates are open. The CMOS series is made up of

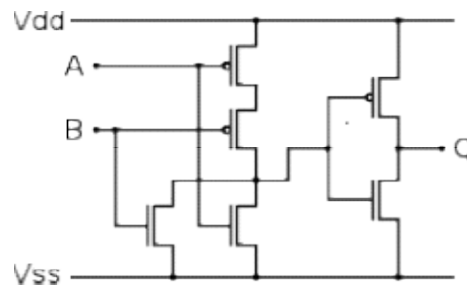


Fig 1.3: OR Gate

1.5XOR GATE

When the number of true inputs is odd, the XOR gate (also known as EOR or EXOR and pronounced Exclusive OR) generates a true (1 or HIGH) output. An XOR gate implements an exclusive or, which means that a valid output is generated if any one of the gate's inputs is true. If all of the inputs are false (0/LOW) and both outputs are true, the result is a false output. The inequality function is defined by XOR, with the result true if the inputs are not equivalent and false otherwise. "Should have one or the other but not both" is a good way to describe XOR. XOR is also defined as inclusion modulo two. As a practice, XOR gates are used in computers to execute binary addition. A half adder is composed of an XOR gate and an AND gate. Subtractors, comparators, and controlled inverters are some of the other implementations.

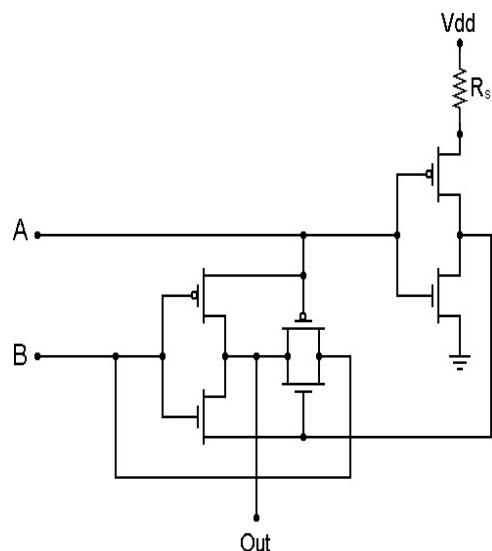


Fig 1.4 XOR Gate

1.6 NOR GATE

The NOR gate is a programme logic gate that performs logical NOR; it operates in conjunction with the truth table seen on the right. If all of the gate's inputs are LOW (0), a HIGH output (1) is generated; if one or all of the gate's inputs are HIGH (1), a LOW output (0) is produced. NOR is the product of negating the OR operator. In many ways, it can be thought of as the inverse of an AND gate. NOR is a functionally complete operation that can be used to construct any logical function by combining NOR gates. This is a property shared by the NAND gate. The OR operator, on the other hand, is monotonic since it can only move from LOW to HIGH and not vice versa. Another very, but not all, circuit implementations, including CMOS and TTL, provide the negation for free. In such logic families, OR is the more complicated operation; it can use a NOR followed by a NOT. Exceptions include any forms of the domino logic family.

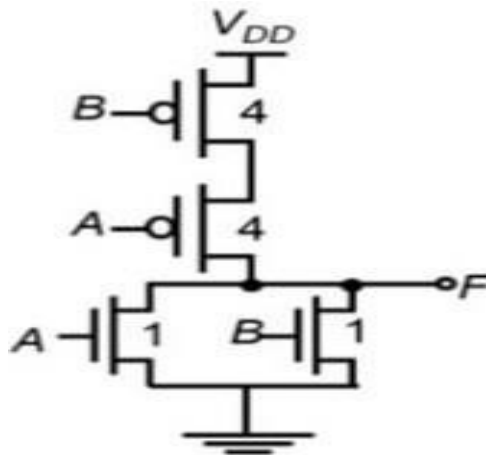


Fig: 1.5 NOR Gate

1.7 AND GATE

According to the table of facts, the AND gate is an effective digital gate for logical conjunction – it behaves to the right. Only when all of the AND gate inputs are HIGH does the output (1) become HIGH (1). The LOW output is enabled if none of the AND gate inputs are HIGH. The function is generalizable to other inputs. An AND gate can only be built with N-channel (shown) or P-channel MOSFETs, usually both (CMOS). The digital inputs a and b result in the same output F as the AND function.

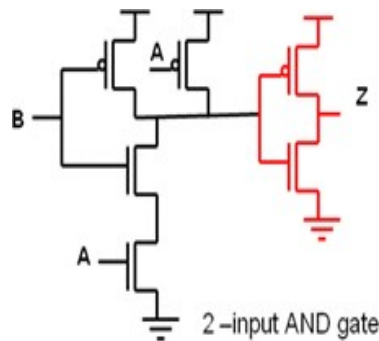


Fig 1.6: AND Gate

1.8 D FLIP FLOP

The D flip-flop is widely used. It is also known as a "wait" or "information" flip-flop. The D-flop stores the D-input value for a certain portion of the clock cycle (such as the rising edge of the clock). The Q output is the caught profit. At all moments, the performance Q does not change. The D flip flop can act as a memory cell, a zero-order hold, or a delay thread.

Like an SR flip-flop, most D flip-flops on ICs can be forced to set or re-set (while the D and clock inputs are ignored). In d-type flip-flops, an illegal $S = R = 1$ condition is normally solved. Setting $S = R = 0$ causes the flip-flop to occur as described above. Here is the truth table for the other possible S and R combinations. These flops are extremely useful because they serve as the foundation for modifying registers and are an essential part of many electronic devices. The benefit of using a D flip flop over a "transparent latch" is that the signal on the D input pin is caught when the flip-flop is clocked, and subsequent corrections on the D input are ignored before the next clock event. Some flip-flops, though, have a "reset" signal input that restores Q (to zero) and can be either asynchronous or clock-based.

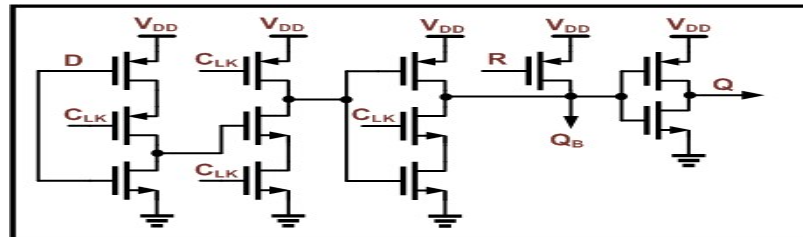


Fig 1.7 D Flip-Flop

1.9 MULTIPLEXER

The electronics system is also known as a data selector or a multiplexer (or mux), as it selects between multiple analogue or digital input signals and forwards the selected input to a single output line. The set is handled by a separate community of individuals. Pick lines are analogue inputs. Select lines have been used in a multiplexer of inputs to select which input line to send to the output.

A multiplexer, rather than having one unit for each input signal, requires multiple input signals to share a single system or resource, such as an analog-to-digital converter or a communications transmission medium. Multiplexers can also be used to enforce Boolean functions for multiple variables.

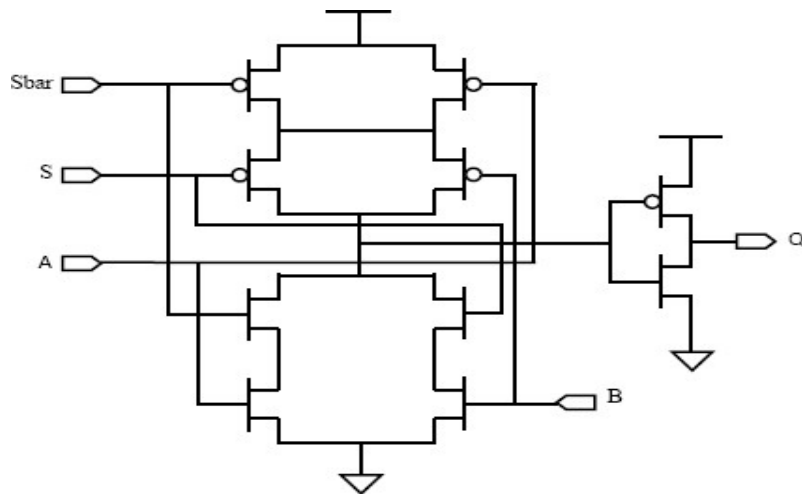


Fig 1.8 Multiplexer

1.10 SHIFT REGISTER

A shift register is a type of digital circuit that employs a cascade of flip flops, with the output of one flip flop connected to the input of the next. They share a common clock signal, allowing the system's storage data to transfer from one location to another. By inserting the last flip-flop back to the first, the data would repeat for a long time through the shifters, which function like digital memories. Delay line memory systems are somewhat similar in this role and were widely used to replace the form of memory in the late 1960s and early 1970s. In most cases, parallel shift registers are used to provide a larger memory pool known as a "bit array." Data was stored in an array and read in parallel, often as a computer word, with each bit stored serially. Registers should be moved. Shift registers are a type of register. The bit array architecture has an

inherent compromise; inserting more flip-flops in the line allows a single shifter to store more bits but requires more clock cycles to transfer the data through both shifters before data is read again. Shift registers may provide both parallel and serial inputs and outputs. This is usually configured as "Serial In, Parallel In" (SIPO) or "Parallel In, Serial Out" (PISO).

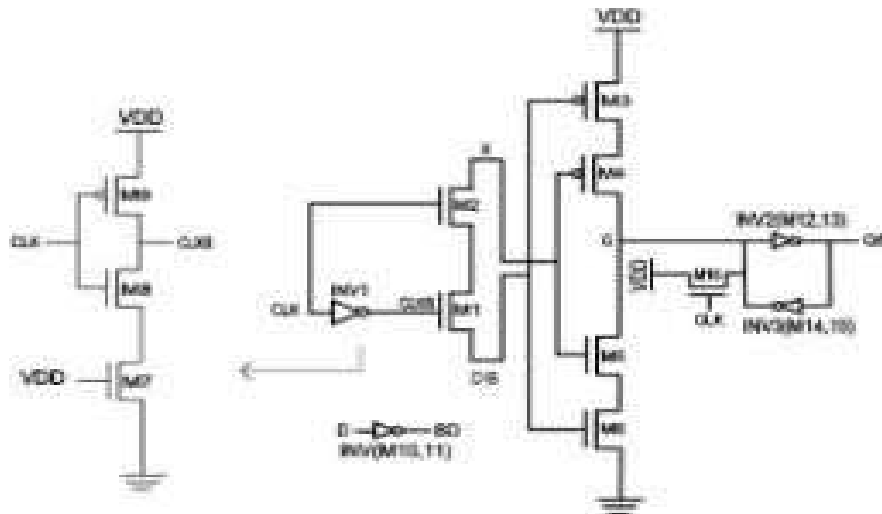


Fig 1.9 Shift Register

1.11 BIDIRECTIONAL SHIFT REGISTER

Data may be moved to the right or left using the bidirectional Transfer Register. It can be implemented using logical gate circuitry, which allows data to be transferred from one point to the next based on the control line level.

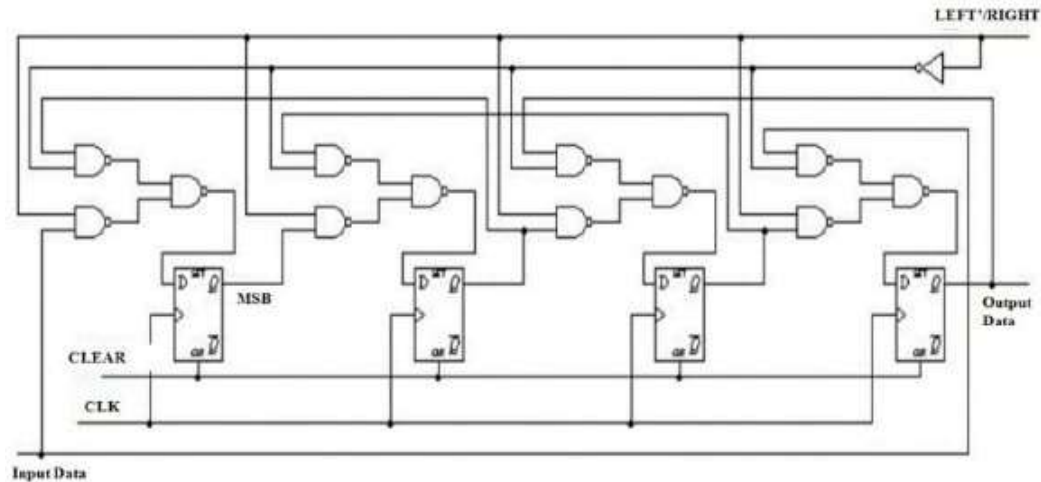


Fig: 1.10 BIDIRECTIONAL SHIFT REGISTER

1.12 PWM ARCHITECTURE

PWM (pulse width modulation) is a method for reducing the average strength of an electric signal by effectively splitting it into discerning bits. The average voltage (and current) supplied to the load is controlled by rapidly switching the supply and load on and off. The longer the switch is engaged, the more total power is supplied to the load. This, along with maximum power point control (MPPT), is one of the most effective strategies for reducing the output of solar panels to that of a battery. PWM is particularly suited to inertial loads such as engines, which react slowly due to their inertia and are thus less readily affected by this discrete transition. The PWM switching frequency must be high enough so that the load is not disturbed, i.e. the resulting waveform of the load must be as smooth as possible.

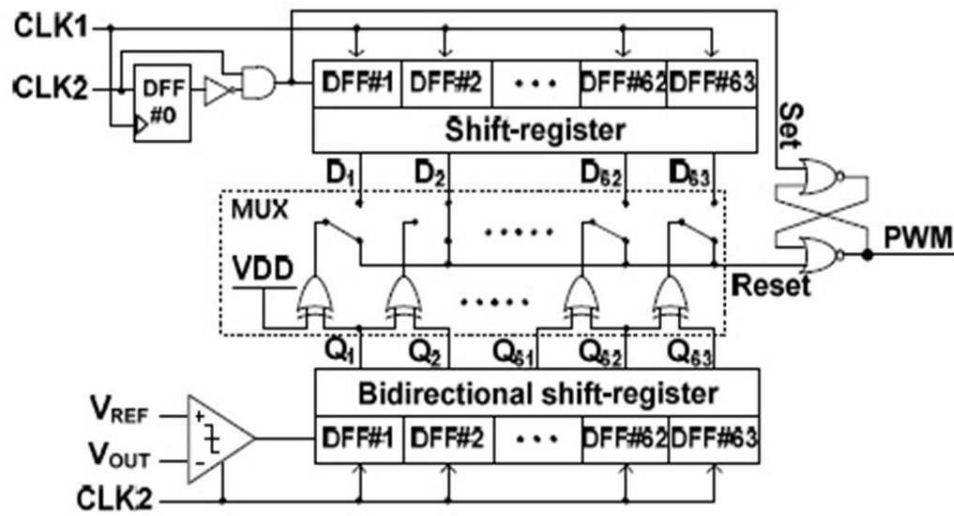


Fig: 1.11 PWM ARCHITECTURE

CHAPTER 2

LITERATURE SURVEY

2.1 LITERATURE SURVEY

X. Zhang et al. 2014: A new PV-aided energy-efficient LSI CCM/DCM controller with a low-voltage buck converter is launched. Various techniques are being considered, including digital PWM monitoring, Dual-Mode - Body-Biased (DMBB), and Ultra-Low-Power Hysteresis Voltage detector. Non-overlap generation is also included in the planned automatic CCM/DCM controller. An ultra-low-power voltage detector is used to transform the zero-crossing detector body adaptively.

P. Chen et al. (2015). Low power digital circuits operating in the near/sub-threshold range are often used in these applications to create energy-efficient devices, A comparison of performance between the proposed circuit and cutting-edge buck converters. With a sufficient inductor size, this tri-mode converter achieves low output power and a wide output range.

Sarat kumar Sahoo, A. Ramulu, Saachi Batta, Shweta Duggal 2012: Multiple pulse width modulation, trapezoidal pulse width modulation, staircase pulsing width modulation, and sinusoidal pulse width modulation (SPWM) are all PWM methods that are used (THPWM). The SPWM and THPWM methods have been shown to increase performance. It was also checked whether higher order harmonics were eliminated after the filter was inserted, and whether THD was reduced.

K.Deepa, P.Ajay Kumar, V.Sai Krishna, P.N. Koteswara Rao, Mounika.A, D.Medhini 2017: To compare and test various PWM strategies, a seven-level multi-level inverter with fewer switches will be used. Carrier-Overlap PWM (CO-PWM), Variable Frequency PWM (VF-PWM), PS-PWM (PS-PWM), Alternate Opposition Phase Disposition PWM (APOD-PWM), PWM(PD-PWM), PWM(PD-PWM), Opposition Phase Disposition PWM (PWM) are among the techniques considered (POD-PWM). To decide the PWM technique to use, the given topology is modelled and simulated in MATLAB/SIMULINK. Leads to a low THD value.

H,V. Ravish Aradhya, Madan H R, Suraj M S, Megaraj T Mahadikar, Muniraj R, Mohammed Moiz, Abhijith Bharadwaj 2016: The parameters of the digital device performance are discovered, including total power dissipation, critical propagation delay, and power delay product. The results were tabled and graphically interpreted below. The results of the tests show that the performance parameters of GNR-FET- based architectures are significantly higher than those of CMOS-based designs, both in terms of energy consumption and propagation delay.

Mounica Patnala, Trond Ytterdal, and Maher Rizkalla: There are several different design methodologies for DACs, but the most recent design method is W-2W Current Mirror Topology. This architecture technique can be used to create DACs with less FET devices in a smaller interface setting capable of developing ULSI applications.

Tae-Hyeong Kim, Dae-Jin Kim, Hyeon-Sam Shin, Sang-Ho Lee, Jae-Won Suh, and Byung-Do Yang : A 63-bit tree-structured clock-gating circuit and a 63-bit DFF shift-register are used in the proposed shift-register (D flip-flops). The number of transistors in the proposed clock gate shift register grows from 1,260 to 1,638. By including the clock signal, the proposed clock gating shift registry restricts clock power only to the DFFs used to generate the PWM service ratio in the shift register (CLK1). The optical PWM buck converter was used in a 65nm CMOS procedure. The operation rate of the proposed reform register is 0.12W-1.22W. It operates at CCM with a fixed PWM duty ratio of 50% and at DCM with a PWM duty ratio of 10%-50%. This saves 22% to 93% of the change register power, while the PWM duty ratio at DCM and CCM is 10% to 50%.

2.2 LITERATURE SUMMARY

For a 0.35 V and 0.5 V output voltage, the potency of the 100 A output current increases by 20% and 9%, respectively. Because of the low power controller, the proposed buck converter achieves a peak output of 94 percent with a current range of 50 A to 10 mA. For powering high energy efficiency digital CMOS circuits near/sub-threshold, the output voltage (VOUT) ranges from 0.35 to 0.5V. It has also been shown that higher order harmonics have been eliminated and THD has been reduced since the filter was mounted. As a result, this article focuses on harmonic reduction in inverter output voltage waveforms. Six PWM techniques were used for seven layers of MLI, and the resulting data was used in comparative studies. CO PWM, VF PWM, PS PWM, APOD PWM, PD PWM, and POD PWM are the six approaches used in PWM. The simulation results show that for the 7 stage inverter (MLI) considered for RL loads, the multi-carrier PWM phase change produces less THD. THD voltage and THD current are 7.96 and 7.77 volts, respectively. MLI uses only seven switches, which reduces switch failure as compared to standard Cascaded H- Bridge MLI. In comparison to CMOS-based designs, the results show a significant improvement in the performance parameters of GNRFET-based designs, both in terms of power consumption and propagation time.

1.3 OBJECTIVE OF THE PROJECT

Both circuits can be used to improve the efficiency of the PWM Architecture by digital interface modifications for low-energy applications in order to increase the competitiveness of low-energy technology. To assess the capacity, latency, Power Loss, Rise Time, Fall Time, and viability of GNRFET for DSP applications with MOSFET and GNRFET technology features.

CHAPTER 3 EXISTING METHODOLOGY

3.1 PWM ARCHITECTURE USING MOSFET (130 nm)

The 130 nm process refers to the semiconductor MOSFET (CMOS) stage marketed by leading semiconductor companies such as Fujitsu, IBM, Intel, Texas Instruments, and TSMC in 2001- 2002. The 130 nm value has a historical root because it follows a 70 percent scaling trend that occurs every 2-3 years. The International Semiconductor Technology Roadmap formally decides on the name (ITRS). The Pentium III Intel Tualatin processor family was among the first to use this method to manufacture CPUs. The PWM architecture used for this project is depicted in the figure below. Hspice was used to write a code in 130 nm format, and the results were collected. Average capacity, delay, electricity, rising time, and fall were among the parameters investigated.

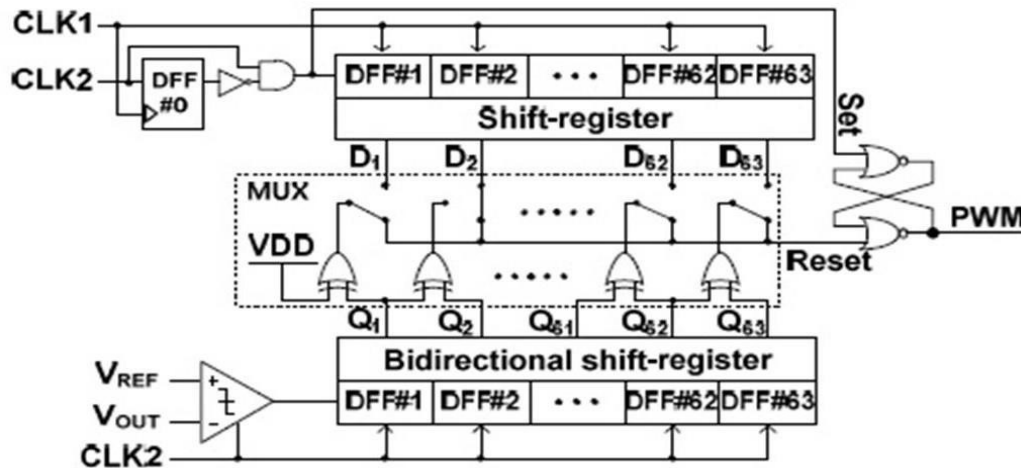


Fig. 3.1: PWM ARCHITECTURE

3.2 PWM ARCHITECTURE USING MOSFET (32 nm)

At this technical point, "32-nanometer" corresponds to a normal half-pitch of a memory cell (meaning half the difference between similar characteristics). Toshiba produced 32 GiB NAND commercial flash memory chips in 2009 using a 32 nm process. In the early 2010s, Intel and AMD produced industrial microchips using the 32-nanometer technique. Furthermore, IBM and the Famous Platform developed a metal gate system with a height

of 32 nm. On January 7, 2010, Intel began shipping the first 32 nm processors based on the Westmere architecture. The 28-nanometer node was a half-node that was shrinking in accordance with the 32-nanometer process. In 2012, the 32 nm technology was phased out in favour of commercial 22 nm manufacturing. The code for the simulation was written in 32 nm format for the PWM architecture using Hspice and the 32 nm library. Average power, delay, power delay (energy), rising and dropping times have all been measured.

3.3 PWM ARCHITECTURE USING GNRFET (15 nm)

3.3.1 GNRFET

Field-effect transistors based on carbon-based nanomaterials have emerged as promising next-generation products due to their outstanding electrical properties and integration capabilities from modern manufacturing methods. Carbon nanotube FETs (CNFETs) and Nano graph FETs are the most commonly studied (GNRFETs). GNRs, unlike cylindrical CNTs, can be grown using silicon-compatible, non-transfer, and in situ methods, with nonalignment and CNT-based circuits as applied to transmission problems. A Nano Graphene Belt Field-Effect Transistor is a field-effect transistor in which the channel material is a single graph sheet or a sequence of graph sheets rather than bulk silicon. Important developments in GNRFETs were first seen in 2004, promising an alternative substrate for silicon substitution in future electronics. The GNRFET is a cutting-edge device that has received a lot of recognition in recent years. Recent work on GNRFET circuit simulations has demonstrated that GNRFETs can be useful in low-power applications.

Graphene is an crystalline carbon allotropic. Carbon atoms are closely embedded in graphene in an atomic chicken wire (hexagonal) pattern of regular sp^2 bonded dimension. A single atomic dense graphite sheet can be used to portray graphene. High-quality graphene is a solid, thin, nearly transparent material that is also an excellent heat and electricity conductor. Its interactions with other materials and light, as well as its inherent bidimensionality, produce unique properties such as the bipolar transistor effect, ballistic charging, and large quantity oscillations. Graphene research evolved quickly due to its familiarity, extraordinary properties, and unexplained isolation. It has an unusual composition, consisting of a single layer of carbon dioxide (only a dense atom) arranged in a grid resembling standard chicken wires. This structure gives graphs their exciting

electronic properties: electrons fly almost effortlessly at very high speeds over this two-dimensional Nano carbon universe, behaving like massless particles. This means that the electronics industry will be able to build more powerful instruments that are much smaller than silicon allows.

3.3.2 Advantages of GNRFET:

It generates very little heat and can operate at an astounding 400GHz. They have a high current capacity as well as thermal conductivity. It is 100 times faster than a MOSFET. The mobility of a GNRFET is 200,000 cm²/ft, while that of a CNTFET and a MOSFET is 1400cm²/ft and 100,000cm²/ft, respectively. The temperature range is 13°C to 55°C for silicon. It is possible that very expensive operations will be carried out. MOSFETs are also smaller and more durable. GNRFETs can be used to create circuits that almost superconduct electronic components, potentially accelerating their performance by up to 1000 times.

3.3.3 PWM using GNRFET:

Our works included a code for the PWM architecture written in Hspice in 15 nm format, as well as a simulation library written in Hspice in 15 nm format. The applications Hspice and Cosmoscope have been used to detect parameters such as average power, latency, power delay product (energetics), increased time, and fell time.

CHAPTER 4

PROPOSED METHODOLOGY

4.1 Low Power Flip–Flop:

Low-power flip-flops are flip-flops designed for low-power electronics such as smartphones and laptop computers. A flip flop, also known as a latch, is a two-stable circuit that can be used to store state information.

Most VLSI devices' maximum power dissipation is due to the clock network and clocked sequential modules. The total power may range between 25% and 40% depending on a number of parameters such as clock frequency, deeper pipelining, and so on. As the internal capacitance of sequential modules, latches, and flip flops is switched, power is dissipated. This can happen in any clock transition/pulse in the sequential element. Sequential elements are often required to change their state, but their state and output are frequently the same before and after the clock pulse. As a result of the clock shift, unnecessary power is dissipated. If flip flops are built in such a way that they can link the clock to their own internal data paths, power dissipation can only be minimised when the clock is required.

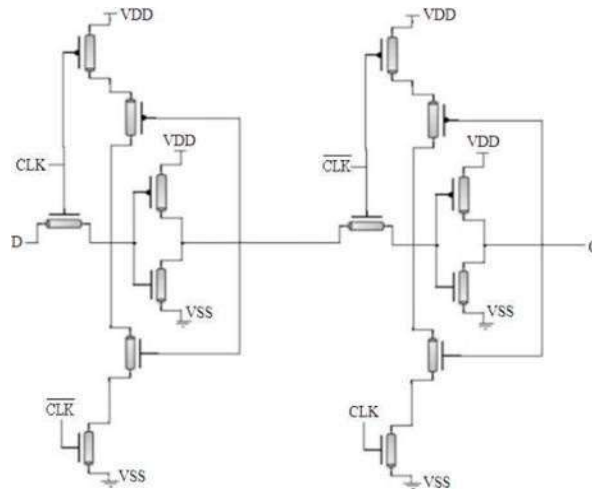


Fig 4.1 Modified D Flip Flop

4.2 MODIFICATION OF PWM ARCHITECTURE:

The PWM architecture had been modified by changing the D-flip flop into low power flip flop to meet our objectives. Following the modification, a Hspice code in 130 nm format was written and the results were obtained. Average capacity, delay, electricity, rising time, and fall were among the parameters investigated.

A 32 nm code was written to PWM architecture using Hspice after the upgrade and a 32 nm library was used to simulate. Measured were average capacity, pause, power delay (energy), increase time and autumn time.

Following the update, a code of 15 nm Hspice was applied to the PWM architecture, and the simulation consisted of a 15 nm library. The Hspice- and Cosmospice applications were used to monitor parameters such as Average Power, latency, power delay products (energy), increasing time, and falling time.

PWM (pulse width modulation) is a method for reducing the average strength of an electric signal by effectively splitting it into discerning bits. The average voltage (and current) supplied to the load is controlled by rapidly switching the supply and load on and off. The longer the switch is engaged, the more total power is supplied to the load. This, along with maximum power point control (MPPT), is one of the most effective strategies for reducing the output of solar panels to that of a battery. PWM is particularly suited to inertial loads such as engines, which react slowly due to their inertia and are thus less readily affected by this discrete transition. The PWM switching frequency must be high enough so that the load is not disturbed, i.e. the resulting waveform of the load must be as smooth as possible.

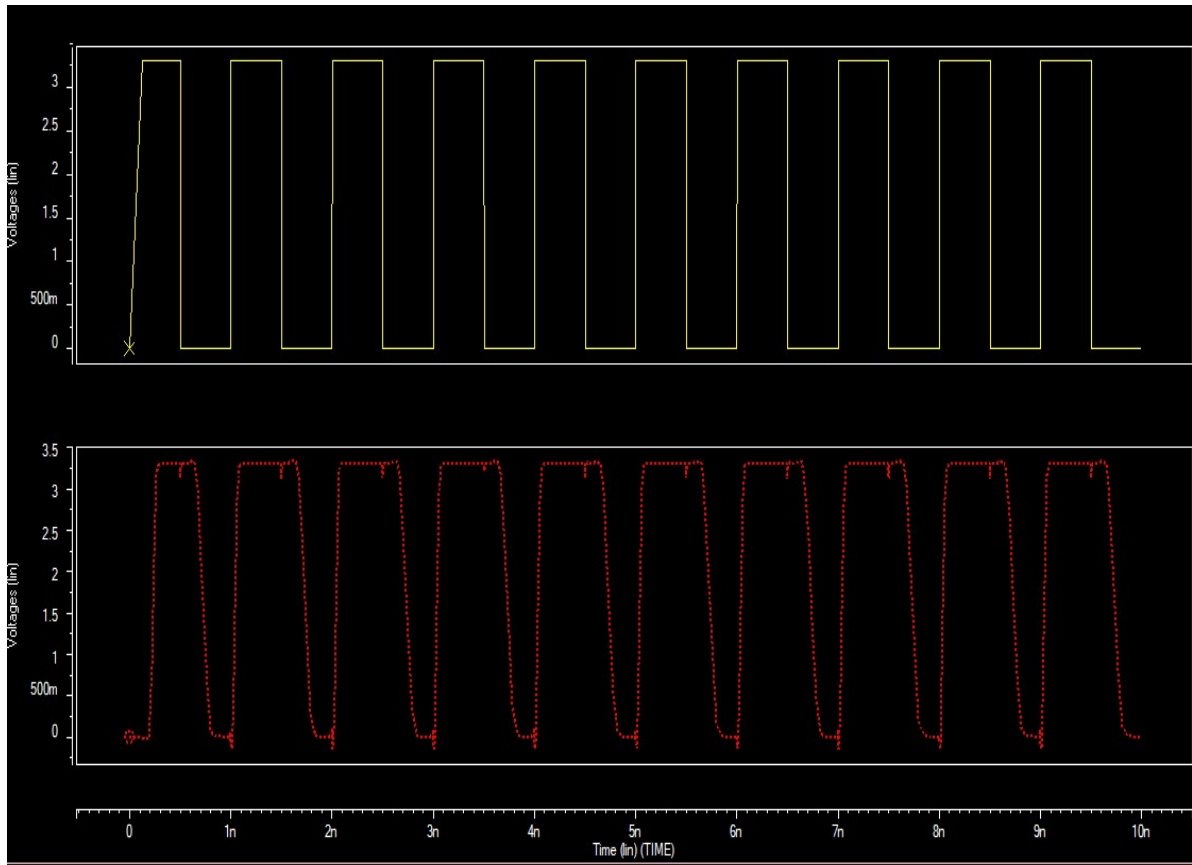
CHAPTER 5

RESULTS AND DISCUSSION

The architecture is designed using VLSI and simulated using HSPICE. The simulation results for the existing and proposed architecture are obtained.

5.1 SIMULATION RESULTS FOR D-FLIPFLOP MOSFET

TOOL USED: HSPICE

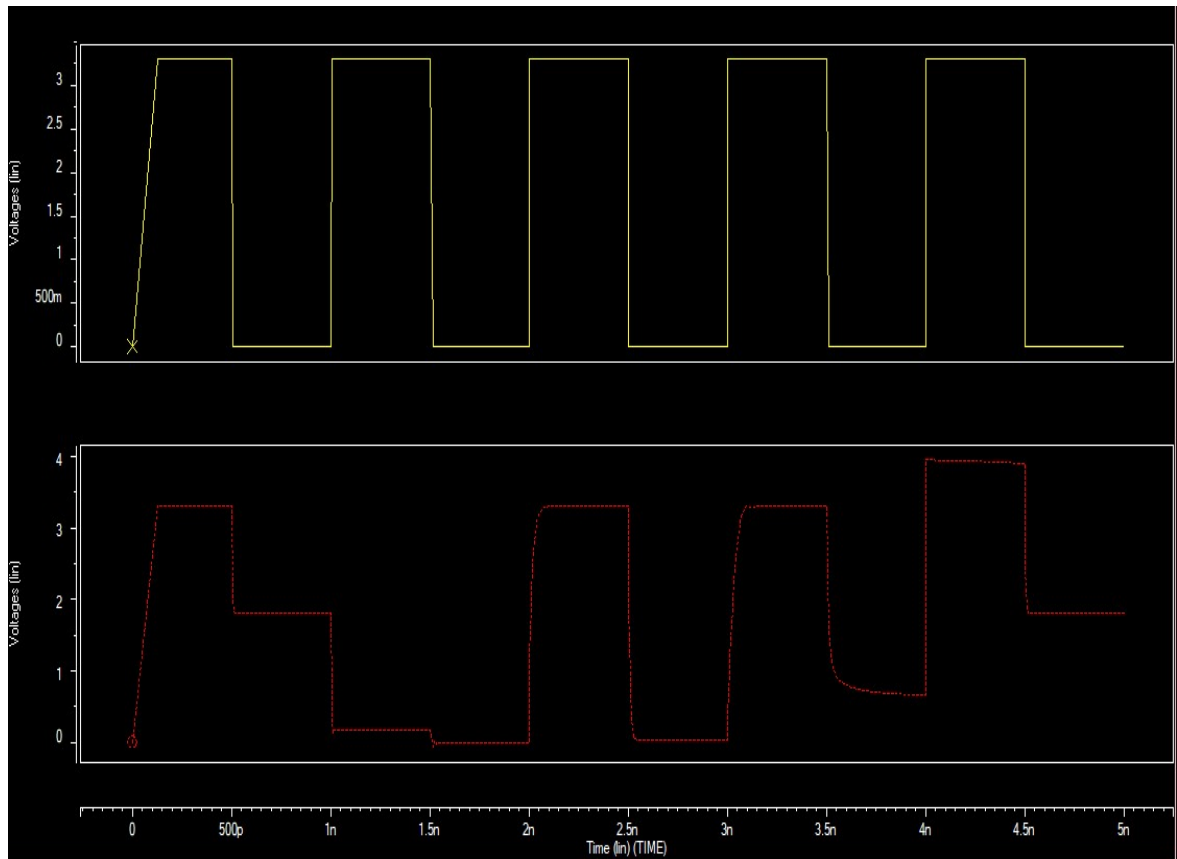


DFF : yellow : input DFF : Red : output

Fig 5.1 Simulation results for D-Flipflop MOSFET

5.2 SIMULATION RESULTS FOR MUX(2*1) MOSFET

TOOL USED: HSPICE



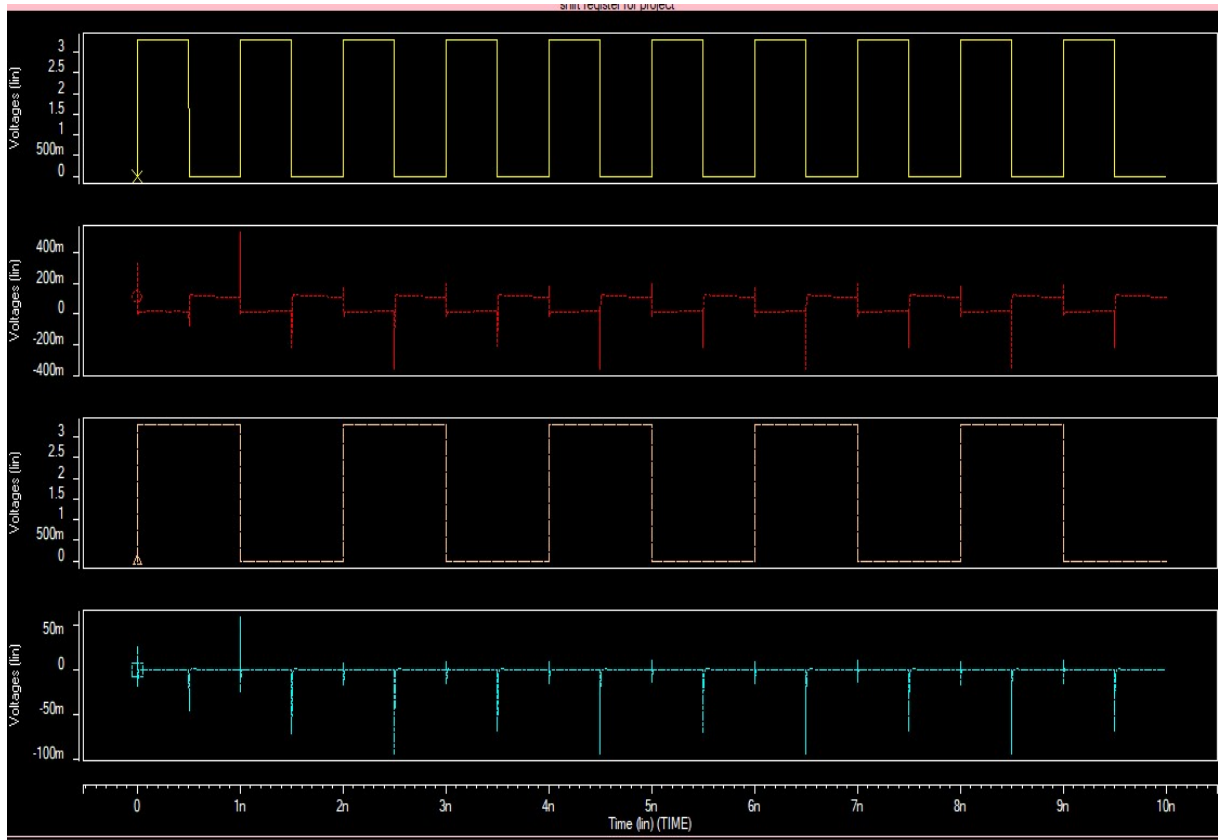
Mux : yellow : input

Mux: red : output

*Fig 5.2: Simulation results for Mux(2*1) MOSFET*

5.3 SIMULATION RESULTS FOR SHIFT REGISTER MOSFET

TOOL USED: HSPICE



Dff : yellow : input

Shift reg: light brown : input

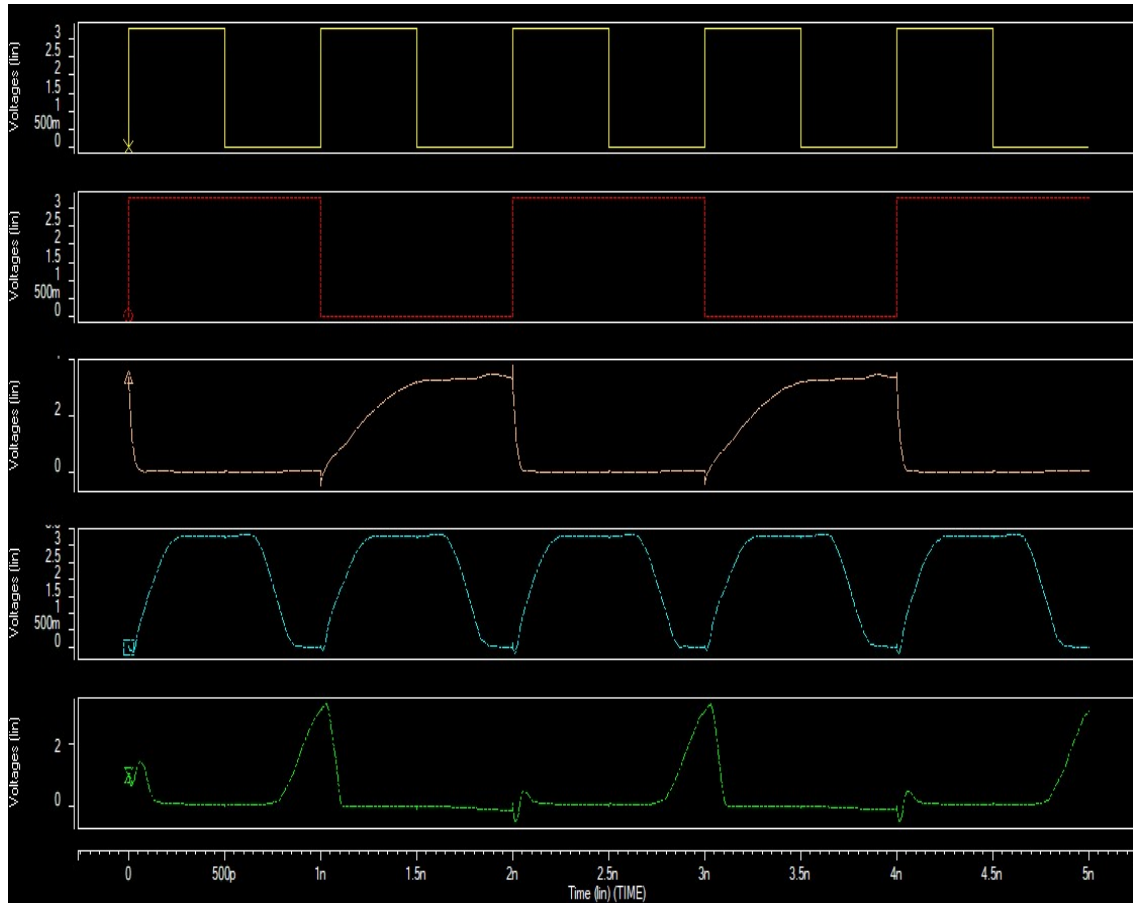
Dff : red : output

Shift reg : blue : output

Fig 5.3: Simulation results for Shift Register MOSFET

5.4 SIMULATION RESULTS FOR BIDIRECTIONAL SHIFT REGISTER MOSFET

TOOL USED: HSPICE



Bidirectional shift reg: red : input

Bidirectional shift reg : blue : output

And : yellow : input

And : Brown : output

Or : yellow : input

Or : brown : output

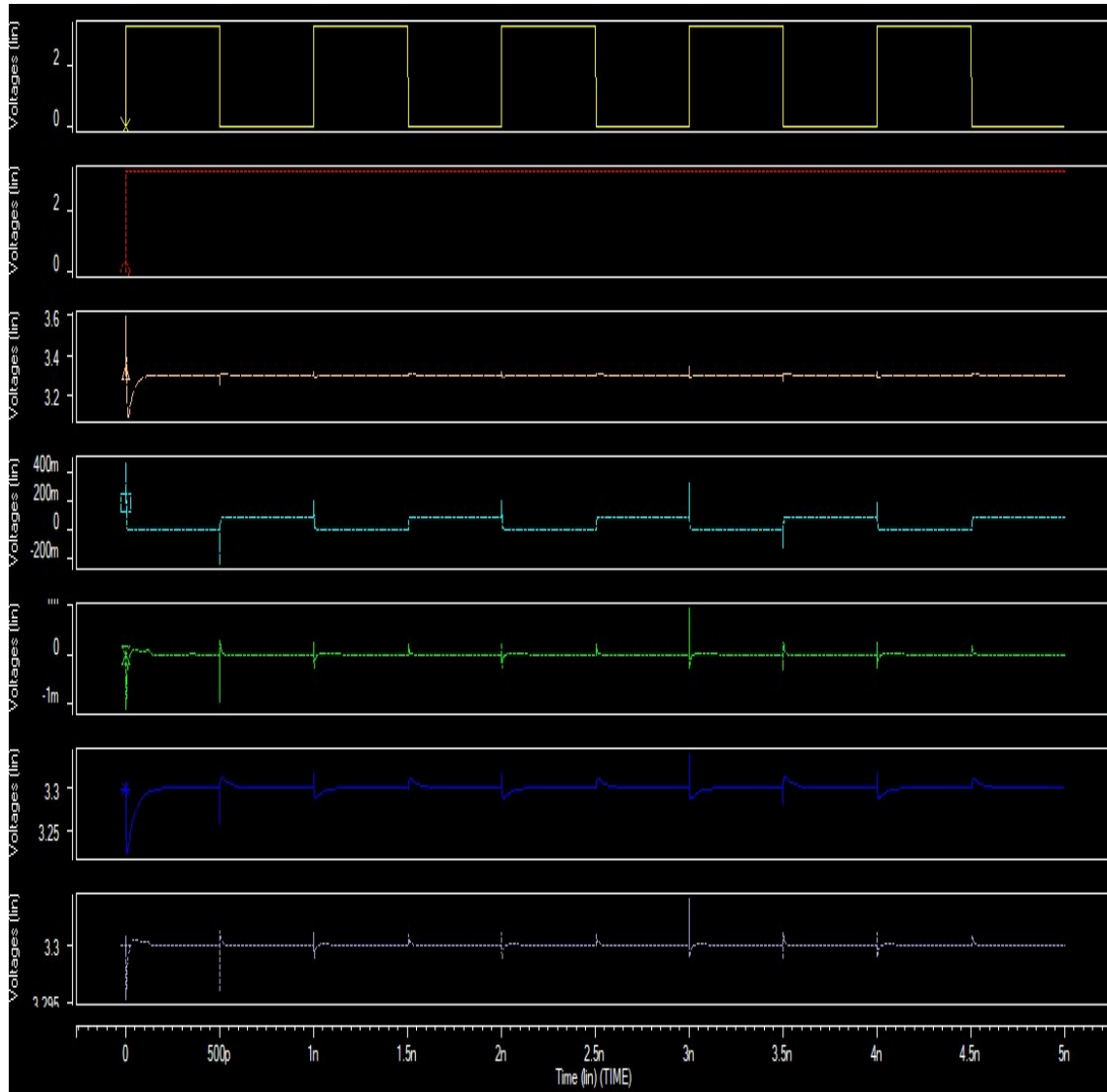
Not : yellow : input

Not : red : output

Fig 5.4: Simulation results for Bidirectional Shift Register MOSFET

5.5 SIMULATION RESULTS FOR PWM MOSFET

TOOL USED: HSPICE



Pwm : yellow : input

shiftreg : red : input

Pwm : dark blue: output

shiftreg : purple : output

dff : yellow : input

buffer : yellow : input

dff : dark blue : output

buffer : brown : output

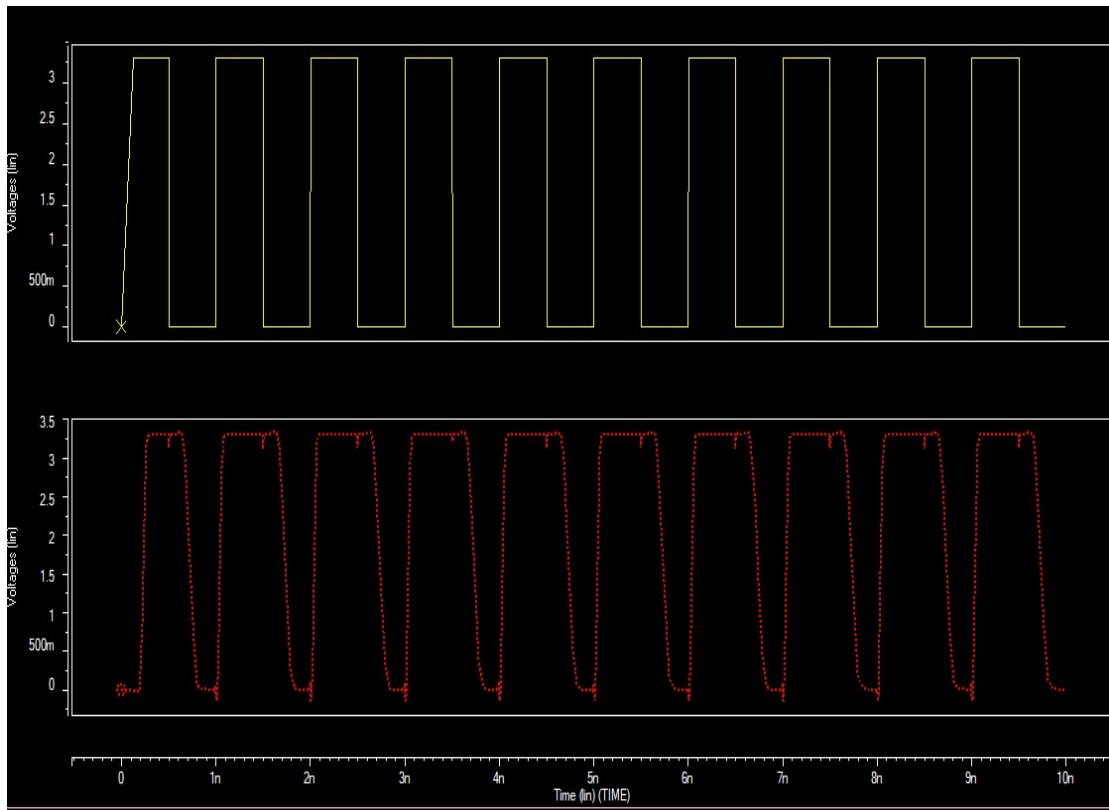
xor:yellow:input

xor : blue:output

Fig 5.5: Simulation results for PWM MOSFET

5.6 SIMULATION RESULTS FOR D-FLIPFLOP (15nm) GNRFET

TOOL USED: HSPICE



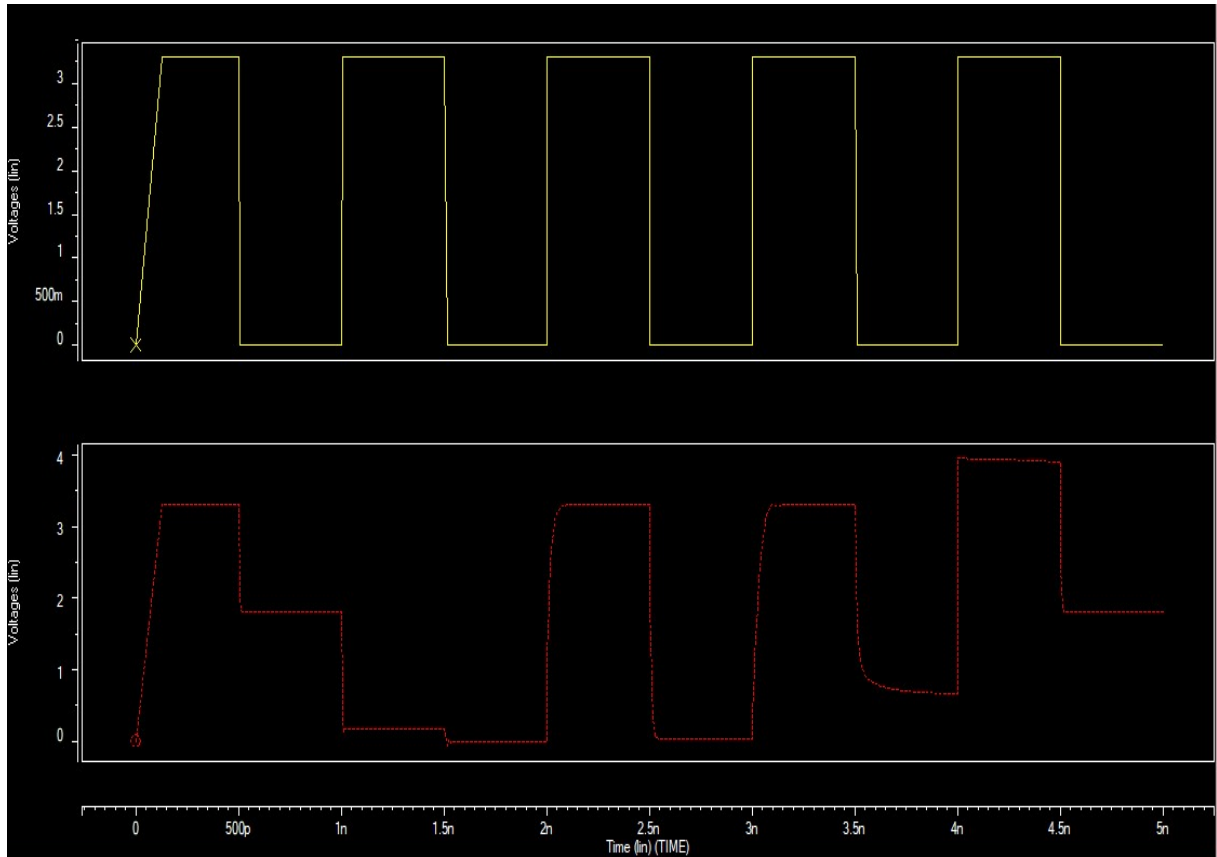
DFF : yellow : input

DFF : Red : output

Fig 5.6: Simulation results for D-Flipflop 15nm - GNRFET

5.7 SIMULATION RESULTS FOR MUX(2*1) (15nm)GNRFET

TOOL USED: HSPICE



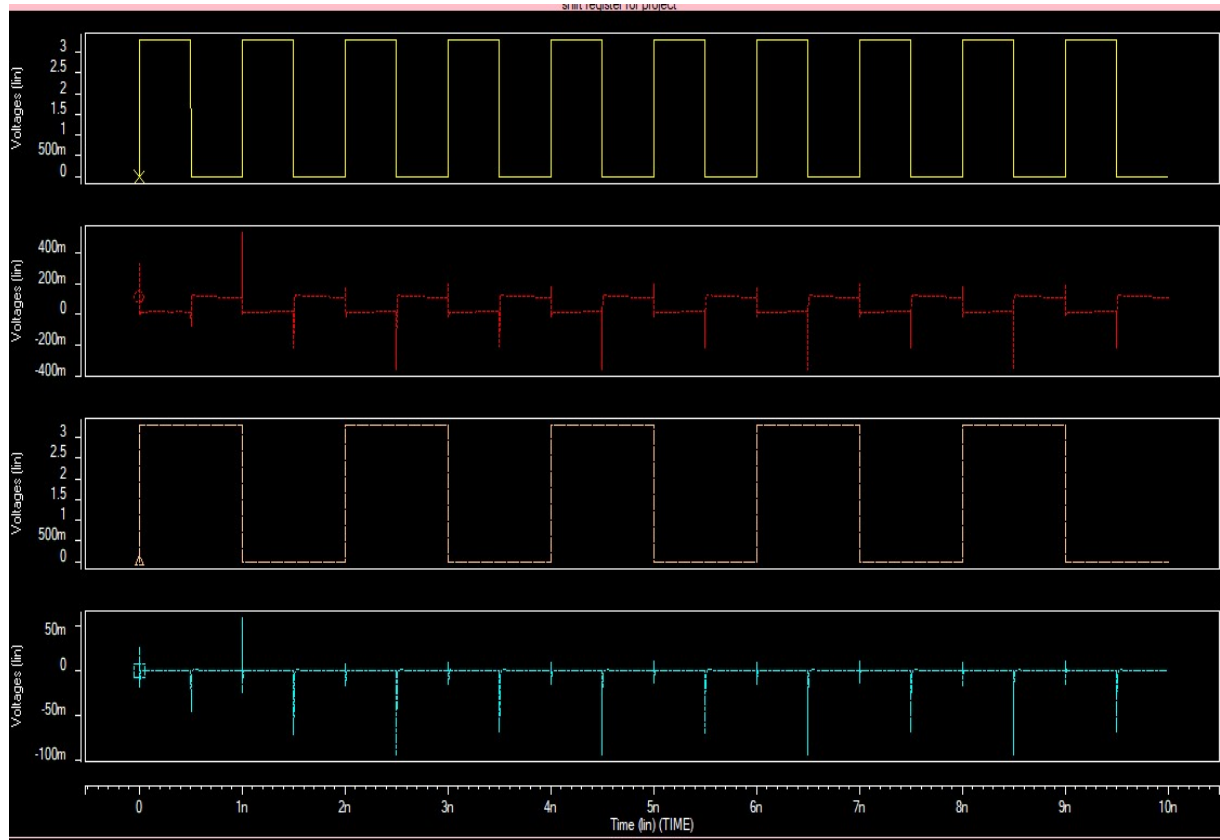
Mux : yellow : input

Mux: red : output

*Fig 5.7: Simulation results for Mux(2*1) 15nm-GNRFET*

5.8 SIMULATION RESULTS FOR SHIFT REGISTER (15nm)GNRFET

TOOL USED: HSPICE



Dff : yellow : input

Shift reg: light brown : input

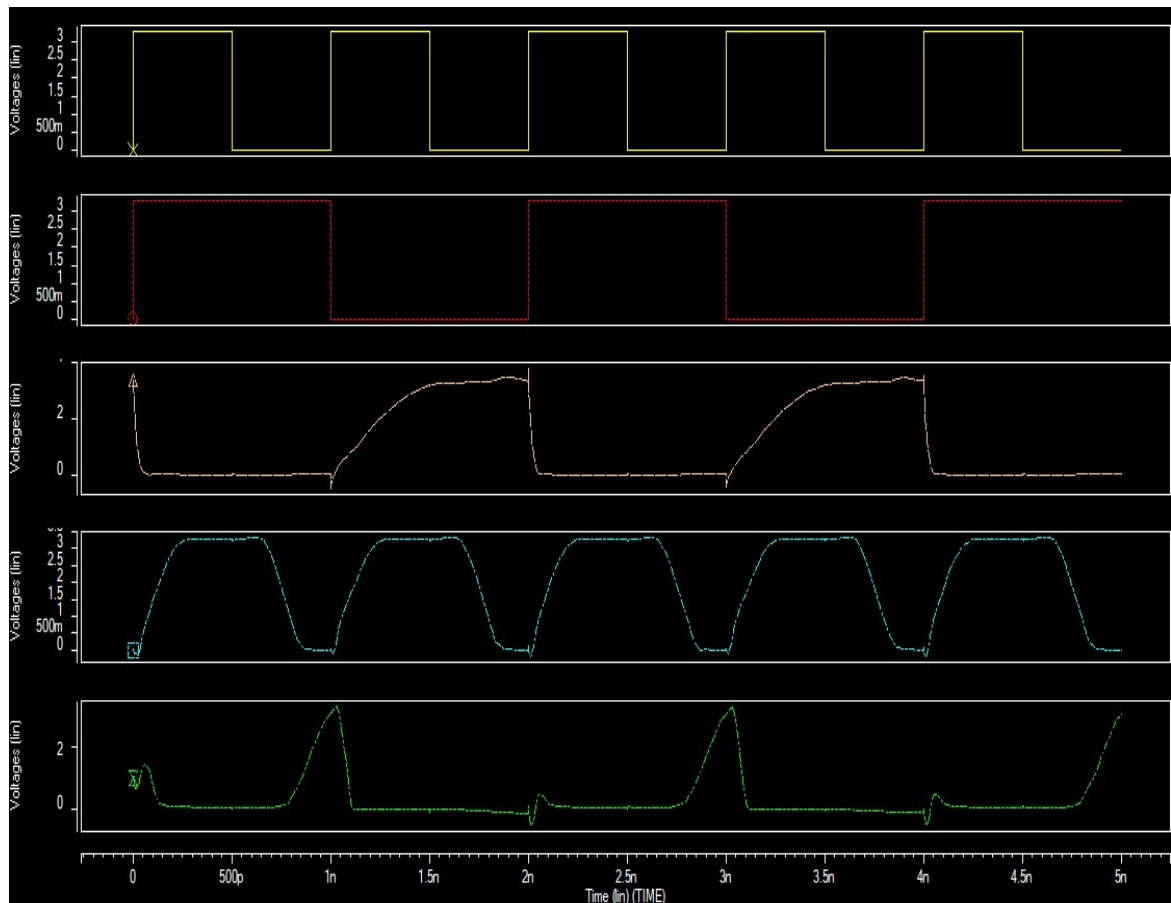
Dff : red : output

Shift reg : blue : output

Fig 5.8: Simulation results for Shift Register 15nm-GNRFET

5.9 SIMULATION RESULTS FOR BIDIRECTIONAL SHIFT REGISTER (15nm) GNRFET

TOOL USED: HSPICE



Bidirectional shift reg: red : input

Bidirectional shift reg : blue : output

And : yellow : input

And : Brown : output

Or : yellow : input

Or : brown : output

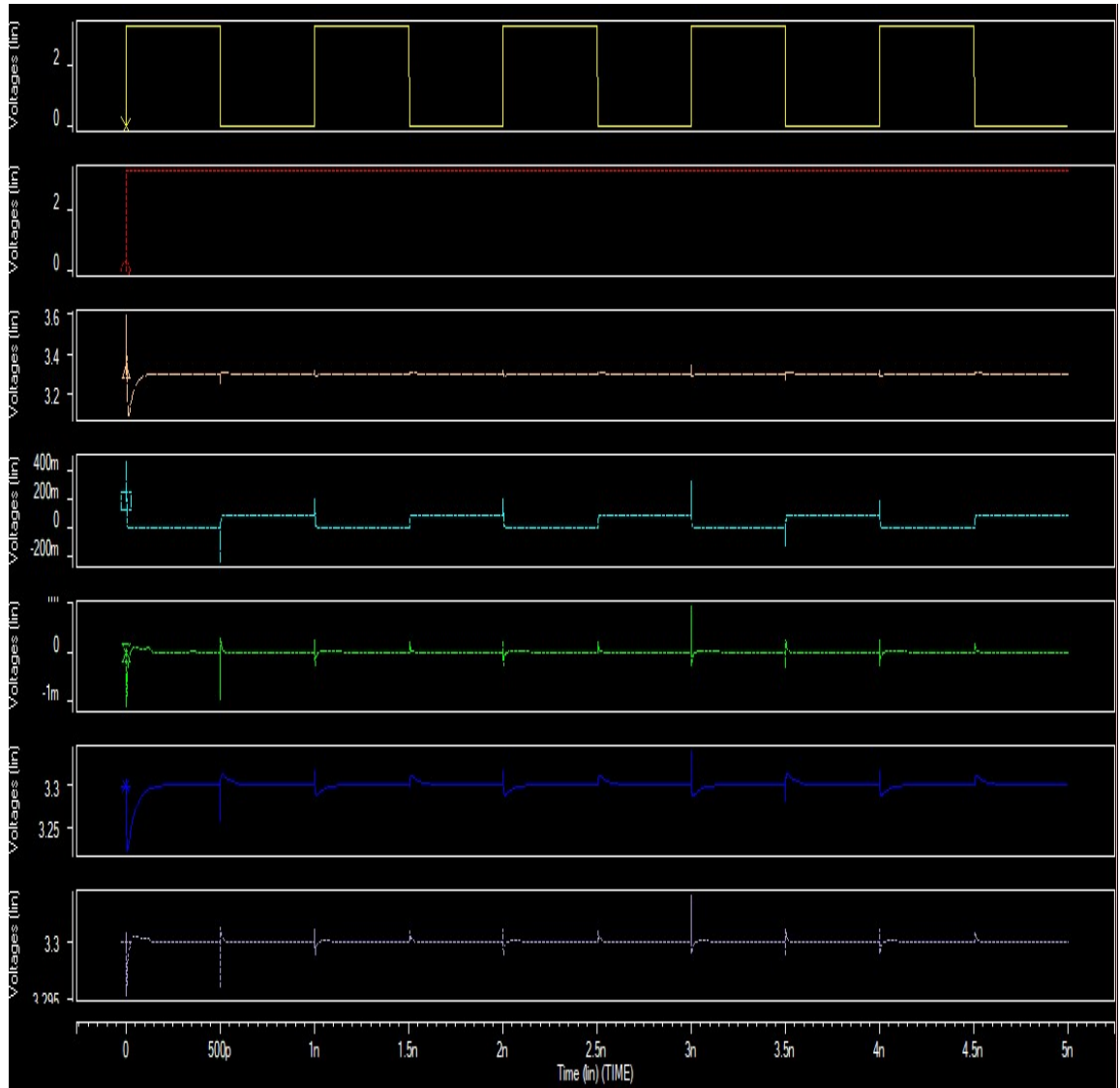
Not : yellow : input

Not : red : output

Fig 5.9: Simulation results for Bidirectional Shift Register 15nm-GNRFET

5.10 SIMULATION RESULTS FOR PWM (15nm) GNRFET

TOOL USED: HSPICE



Pwm : yellow : input

shiftreg : red : input

Pwm : dark blue: output

shiftreg : purple : output

dff : yellow : input

buffer : yellow : input

dff : dark blue : output

buffer : brown : output

xor:yellow:input

xor : blue:output

Fig 5.10: Simulation results for PWM 15nm-GNRFET

Table 5.1: Performance Analysis of 130nm MOSFET

DEVICE	AVG POWER	DELAY	ENERGY	RISE TIME	FALL TIME
D flip flop	10.5uW	34.623ps	363.541aJ	38.28ps	109.95p
Mux	53.04uW	54.26ps	2877.9aJ	54.58ps	114.39ps
Shift register	89.08uW	75.55ps	6729.9aJ	89.65ps	125.36ps
Bidirectional shift register	127.7uW	90.716p	11584.4aJ	153.3ps	142.81p
PWM	381.5uW	106.58ps	40660.27aJ	205.6ps	269.69ps
Modified PWM	227.1UW	102.59ps	23298.18aJ	100ps	142.7ps

Table 5.2: Performance Analysis of 32nm MOSFET

DEVICE	AVG POWER	DELAY	ENERGY	RISE TIME	FALL TIME
D flip flop	10.5uW	34.623ps	363.541aJ	38.28ps	109.95p
Mux	53.04uW	54.26ps	2877.9aJ	54.58ps	114.39ps
Shift register	89.08uW	75.55ps	6729.9aJ	89.65ps	125.36ps
Bidirectional shift register	127.7uW	90.716p	11584.4aJ	153.3ps	142.81p
PWM	381.5uW	106.58ps	40660.27aJ	205.6ps	269.69ps
Modified PWM	227.1UW	102.59ps	23298.18aJ	100ps	142.7ps

Table 5.3: Performance Analysis of 15nm GNRFET

DEVICE	AVG POWER	DELAY	ENERGY	RISE TIME	FALL TIME
D FLIP FLOP	4.1uW	16.98ps	69.618aJ	24.56ps	82.25ps
MUX	28.69uW	34.28ps	983.49aJ	40.78ps	88.25ps
SHIFT REGISTER	32.58uW	57.89ps	1886.05aJ	78.45ps	98.54ps
BIDIRECTIONAL SHIFT REGISTER	65.21uW	68.22ps	4448.62aJ	126.3ps	114.58ps
PWM	197.65uW	81.02ps	16013.6aJ	154.23ps	201.56ps
MODIFIED PWM	114.21uW	61.25PS	6995.36aJ	89.65ps	164.22ps

CHAPTER 6

CONCLUSION

In this project, the circuits were initially designed using 130nm CMOS and 32nm CMOS technology. The circuits were then designed with 15nm GNR-FET Technology and the performance parameters power, delay, power delay product, Rise time and fall time were compared. Next the GNR-FET model was used to design the circuits. Later, the circuits designed with the model were modified using the low power techniques and the circuit parameters were compared with the base models. The simulation for 130nm MOSFET was carried out at 3.3 V, while 32nm MOSFET and GNR-FETs were simulated at 1 V. The transient, power, delay and power delay product analyses have been carried out. These observations are compared. It is noted that, on an average, the GNR-FET Model consumes 98% less power than the 130nm MOSFET and 85% less power than the 32nm MOSFET. The PWM architecture is designed using 130nm CMOS, 32nm CMOS and 15nm GNR-FET technologies. Then the performance parameters like power, delay, power delay product, rise time and fall time are measured for PWM architecture in 130nm CMOS, 32nm CMOS and 15 nm GNR-FET technology, which ensure that GNR-FET designs are consuming low power and providing high speed than CMOS designs.

In recent years, graphene has shown huge promise as material that can swap silicon-based materials in the future due to its outstanding electrical properties and other characteristics. MOSFETs have disadvantages with shorter channels causing short channel effects but Graphene has many uncommon properties. It is the strongest material ever tested, conducts heat and electricity efficiently, high mobility at room temperature, low atomic thickness, large current density, and is nearly transparent, Graphene shows a large and nonlinear diamagnetism. Graphene is an allotrope form of carbon consisting of a single layer of carbon atoms arranged in a hexagonal lattice. It is a semimetal with small overlap between the valence and the conduction bands and overall, with reduced short channel effects. In our project also, using GNR-FET we have increased the efficiency of the architecture.

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