

EVALUATION OF UNIVERSAL SHIFT REGISTER IN NANOSCALE TRANSISTOR TECHNOLOGY

Submitted in partial fulfilment of the requirements for the award of Bachelor of
Engineering Degree in Electronics and Communication Engineering

by

SANGHAMITRA CHOUDHURI (37130356)

SHWETA YADAV (37130378)



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION
ENGINEERING
SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING**

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119

MARCH - 2021



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

Accredited with “A” grade by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI 600 119

www.sathyabama.ac.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **Sanghamitra Choudhuri (37130356)** and **Shweta Yadav (37130378)**, who carried out the project entitled **“EVALUATION OF UNIVERSAL SHIFT REGISTER IN NANOSCALE TRANSISTOR TECHNOLOGY”** under my supervision from November 2020 to March 2021.

Internal Guide & Head of the Department

Dr. T.RAVI, M.E., Ph.D.,

Submitted for Viva voce Examination held on _____

Internal Examiner

External Examiner

DECLARATION

We **Sanghamitra Choudhuri (37130356)** and **Shweta Yadav (37130378)**, hereby declare that the Project Report entitled “**EVALUATION OF UNIVERSAL SHIFT REGISTER IN NANOSCALE TRANSISTOR TECHNOLOGY**” done by us under the guidance of **Dr. T.RAVI, M.E., Ph.D.**, is submitted in partial fulfilment of the requirements for the award of the Bachelor of Engineering degree in Electronics and Communication Engineering.

1) *Sanghamitra Choudhuri*

2) *Shweta Yadav*

DATE:

PLACE:

SIGNATURE OF THE CANDIDATES

ACKNOWLEDGEMENT

We are pleased to acknowledge our sincere thanks to Board of Management of **SATHYABAMA** for their kind encouragement in doing this project and for completing it successfully. We are grateful to them.

We convey our thanks to **Dr. N.M. NANDHITHA, M.E., Ph.D., Dean, School of Electrical and Electronics** and **Dr. T. RAVI, M.E., Ph.D., Head of the Department, Department of Electronics and Communication Engineering** for providing us necessary support and details at the right time during the progressive reviews.

We would like to express our sincere and deep sense of gratitude to our Project Guide **Dr. T. RAVI, M.E., Ph.D., Head of the Department, Department of Communication and Engineering** for his valuable guidance, suggestions and constant encouragement paved way for the successful completion of the project work.

We wish to express our thanks to all Teaching and Non-teaching staff members of the **Department of Electronics and Communication Engineering** who were helpful in many ways for the completion of the project.

We express our gratitude to our parents for their constant encouragement and support for the completion of the project.

ABSTRACT

A shift register comprises of cascaded FF, with one FF yield associated with another. FF assume the significant part in rising the power of Universal shift register. A USR is kind of register that performs unidirectional, bidirectional, and equal stacking or parallel loading register. The activity mode switches with the select lines of the plan. The project focuses on the plan and testing of the Universal Shift Register in 130 nm CMOS technology that is assessed in Synopsis HSPICE tool. The proposed USR is planned utilizing low force D-FF and 4×1 Modified GDI based MUX. The proposed Universal Shift Register shows better execution as fare as force and postponement. The aim is to evaluate and analyse the performance parameters of universal shift register so that it can further be utilized in complex VLSI architectures to achieve better performances.

TABLE OF CONTENTS

CHAPTER No.	TITLE	PAGE No.
	ABSTRACT	5
	LIST OF FIGURES	8
	LIST OF TABLES	9
1	INTRODUCTION	
	1.1 MOTIVATIONS	11
	1.2 SHIFT REGISTER	12
	1.2.1 Serial In Serial Out Shift register	13
	1.2.2 Serial In Parallel Out Shift register	14
	1.2.3 Parallel In Serial Out Shift register	14
	1.2.4 Parallel In Parallel Out Shift register	15
	1.2.5 Bidirectional Shift register	16
	1.3 MUX	17
	1.3.1 2×1 MUX	18
	1.3.2 4×1 MUX	19
	1.4 ORAGANIZATION OF THE REPORT	20
2	LITERATURE SURVEY AND OBJECTIVES	
	2.1 LITERATURE SURVEY	21
	2.2 LITERATURE SUMMAREY	22
	2.3 PROBLEM DEFINITION	23
	2.4 OBJECTIVE OF THE PROJECT	23
3	AIM AND SCOPE OF PRESENT INVESTIGATION	
	3.1 PROPOSED METHODOLOGY	24

	3.2 AREA OF PROPOSED WORK AND APPLICATION	24
	3.3 D FLIP FLOP	24
	3.4 4×1 MULTIPLEXER	27
	3.5 EXISTING 4×1 UNIVERSAL SHIFT REGISTER	28
	3.6 PROPOSED UNIVERSAL SHIFT REGISTER	31
4	PROPOSED UNIVERSAL SHIFT REGISTER	
	4.1 2×1 MUTLIPLEXER USING MODIFIED GDI TECHNIQUE	34
5	RESULT AND DISSCUSION	
	5.1 EXISTING LOW POWER DFF SIMULATION OUTPUT	37
	5.2 EXISTING 4×1 MUX SIMULATION OUTPUT	38
	5.3 EXISTING UNIVERSAL SHIFT REGISTER SIMULATION OUTPUT	38
	5.4 PROPOSED 4×1 MUX SIMULATION OUTPUT	39
	5.5 PROPOSED USR SIMULATION OUTPUT	39
	5.6 PERFORMANCE ANALYSIS	40
	5.6.1 Power And Delay Analysis Of Existing System	40
	5.6.2 Power And Delay Analysis Of Proposed USR	41
		42
6.	CONCLUSION AND FUTURE SCOPE	
	REFERENCES	43

LIST OF FIGURES

FIGURE.NO.	DESCRIPTION	PAGE NO.
1.1	Serial in-Serial out Shift Register	13
1.2	Serial in-Parallel out Shift Register	14
1.3	Parallel in-Serial out Shift Register	15
1.4	Parallel in-Parallel out Shift Register	15
1.5	Symbolic Diagram of MUX	17
1.6	Block Diagram of 2×1 MUX	18
1.7	Logic Diagram of 4×1 MUX	19
3.1	Block Diagram of D-FF	26
3.2	Block Diagram of 4×1 MUX	27
3.3	n-bit Universal Shift Register	29
3.4	Block Diagram of 4×1 USR	30
4.1	low power D-FF	33
4.2	2×1 MUX using MGDI Technique	35
4.3	Modified 4×1 MUX	36
5.1	Output Waveform for existing low power D-FF	37
5.2	Output Waveform for existing 4×1 GDI MUX	38
5.3	Output Waveform for existing USR	38
5.4	Output Waveform for proposed 4×1 MUX	39
5.5	Output Waveform for proposed USR using low power D-FF and 4×1 MUX using MGDI Technique	39

LIST OF TABLES

TABLE NO.	DESCRIPTION	PAGE NO.
1.1	Truth table of 4×1 MUX	19
3.1	Truth table of D-FF	26
3.2	Truth table of 4×1 MUX	28
3.3	Truth table of 4×1 USR	31
5.1	Design analysis of existing circuit	40
5.2	Design analysis of proposed USR	41

CHAPTER 1

INTRODUCTION

VLSI is that the means towards coordinating sizable amount of transistors into one chip. VLSI configuration is basically wont to limit the interconnecting textures region. The principle factors that limit the advancement of less significant and additional uncleared IC chip are the IC manufacture innovation, planner profitableness and also the expense. Contingent upon the applying, numerous execution viewpoints become vital. Shift register are thumping storage region incorporated into a Central process Unit. most modern day electronic equipment styles in the main use the 2 styles of register's. The steering register brings pointers from program counter holding each steering because it is being dead by our processor. The memory register's are used to pass info to processor. The capability season of within register's are terribly fugacious, since frequently hold info for not even specifically one msec. consumer open register's are larger than interior register's and often were holding info just a additional drawn out time. for example, AN info register could store singular qualities said being by a right away running project.

A location register contains memory addresses, that reference numerous squares of memory within the framework RAM. varied CPUs presently have universally helpful register's (GPRs), which can contain each info and memory addresses. Register's amendment in each variety and size, contingent upon the electronic equipment style. many processors have eight register's whereas others have sixteen, 32, or more. For an extended time, register's were 32-digit, but currently several are 64-cycle in size. A 64-digit register is significant for a 64-bit processor, since it empowers the electronic equipment to induce to 64-cycle memory addresses. A 64-digit register will likewise store 64-bit pointers, that cannot be stacked into a 32-cycle register. during this means, most comes composed for 32-digit processors will run on 64-bit PCs, whereas 64-cycle programs don't seem to be in reverse viable with 32-bit machines. Shift register's are primareilly sort of register which may ("shift") info. Register's are conventionally stockpiling devices that are created by cross connecting FF in totally different arerangement, as every FF is appropriate golf stroke away simply the

slightest bit at a time. A FF is one of electronic device with 2 moored expresses that's used to store double info. FF and hooks are fundamental structure squares of advanced hardware frameworks. The place away info is modified by applying unsteady information sources. At the purpose once the FF in an exceedingly register are associated in order that yield of single FF, turns into the contribution of the opposite, register creation takes place.

FF is a circuit that job sort of a lock. It all right could also be all over as a bistable vibrator which may shift between 2 states (0 or 1) There are some kinds of FF, however the foremost unremarkably used technique for recreating shift register's are the D (Delay)- FF. For the activity of the D FF that makes them thus enticing for shift register's, Whenever there's a amendment on the clock of delay FF (rising or falling, contingent upon the main points of the FF). At the yield "Q" turns into the same information because the one at the data "D". The Yield "Q" of the FF can stay at that esteem till the subsequent clock cycle, wherever it'll at that time amendment once more to the value(High or low, one or 0) at the data. A one-way register is provided for moving simply one means. A two-way register is provided for acquiring each the ways in which. Presently let we've got a register that may suited sporadically shift info in each the shift right and shift left, aboared the important info and yield terminals for equal exchange, at that time known as a register with parallel load or "universal shift register".

1.1 MOTIVATIONS

The need to differentiate ideal shift register for a sophisticated semiconductor started this examination. Register square measure basically a lot of storage for units of memory that we have a tendency to use to shift data. additionally referred to as memory register's, they very form a part of the laptop processor as some processor register. The register is satisfactorily immense to carry any type of data, like dates, steerage sets, warehousing addresses, pieces, arrangements, and characters. Some steerage sets square measure a part of the manner framed by register's. types of register's incorporate memory address register, memory support register, load yield address register, load yield cradle register, and register. during this exercise we are

going to zero in on shift register's. Shift Register is quite successor logic circuits, mapped for capability and shifting data. created from FF that are interconnected so the yield of 1 FF becomes load for the second FF, contingent upon the sort of shift register's created. Shift register's essentially square measure computerised memory hardware found in gadgets like mini-computers, PCs, and data making ready frameworks. With register, data or items square measure gone into framework in AN equal manner. the 2 finishes square measure combined to because the left and right closures.

Development of data is from left to right, from choice to left, or within the 2 headings to create a bidirectional register. Shift register's is dead to such AN extent that every piece may well be command in an exceedingly lock. The yield of hook is related to be contribution of another lock. place confidence in variety of connectors used to expand the electrical string. thanks to register's, data is taken care of at the same time (in equal). Shift register's will fill in as data additional rooms or data development gadgets. they're during this manner commonly dead in gadgets like adding machines or PCs. They fill in as impermanent warehousing units for paired data anticipating a numerical activity like growth or duplication. the overall register is referred to as as "The register which may be used to shift the data in each the ways that like left, right and might stack equal data too". This register is ready to try to to 3 types of activities, expressed: Parallel stacking ,Left shift and Right shift.

1.2 SHIFT REGISTER

Shift Register may be a gathering of FF accustomed store varied items of knowledge. A n-digit register are often framed by interfacing n FF wherever every FF stores one piece of knowledge. A register are often characterised as once a bunch of FFs are often associated within the arrangements , the that means of the register is that the purpose at that the place away data are often shifted within the register's. it's a ordered circuit, essentially accustomed storing.

A. Types of Shift Registers

Shift register square wave measure organized into varieties considerably by their technique of activity, either chronic or equal. There square wave measure six (6) essential types of shift register's that square wave measure recorded beneath albeit a number of them are often to boot separated keen about bearing data stream with move left or move right.

- SISO
- SIPO
- PISO
- PIPO
- Bidirectional SR

1.2.1 Serial In-Serial Out Shift Register (SISO)

SISO shift register's area unit shift register's that moves in info consecutive and streams out info too equally, systematically. This register permits serial information and creates a serial yield, thus this can be named as SISO register. Only one yield is present, and whenever info goes away from register the slightest bit in an exceedingly chronic manner. an easy serial in – serial Out 4-digit register is show, the register includes of four FF. The Serial in Serial out (SISO) logic circuit is shown below in figure 1.1[12].

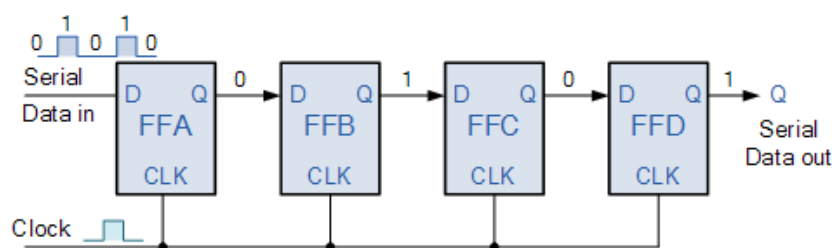


Fig:1.1 : Serial in – Serial out Shift register (SISO) (Source [12])

This circuit is worked with 4 delay FF's in consecutive. When the FF's interconnected then the equivalent CLK signal was passed down.

1.2.2 Serial In-Parallel Out Shift Register (SIPO)

The second variety of register we'll think about is that the SIPO. This register permits sequent data and production of an equal yield, thus this is often called sequent in equal SIPO. The sequent in equal out SIPO circuit is appeared beneath in figure one.2[12]. Four FF's were utilized to be worked upon on this rationale.

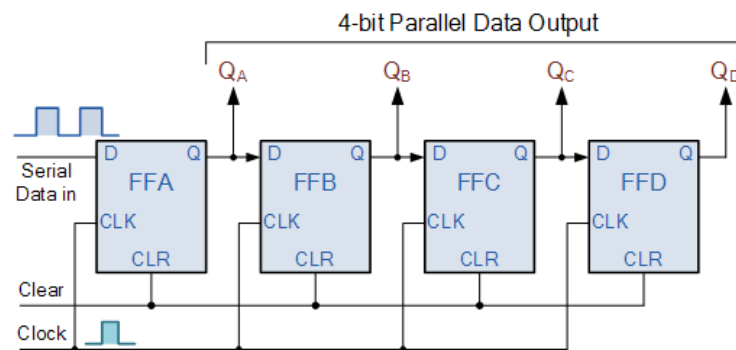


Fig:1.2 : Serial in-Parallel out (SIPO) Shift register
(Source [12])

The quite stockpiler, successive info are often taken from the left half the FF and produces a consistent yield. Stockpiling utilization add in some lines in lightweight of the original sense of basic capability of the SIPO register is to very successive information to equal information.

1.2.3 Parallel In-Serial Out Shift register (PISO)

This reasonably PISO device, given data is even. This register permits equal data and creates a successive yield, thus this is often referred to as PISO. PISO register circuit is appeared beneath in figure 1.3[12]. For this sort of register, the knowledge is provided in equal. This circuit is acquainted with 4 FF's, wherever CLK is merged foursquare to any or all the FFs. Be that because it could, information is associated severally FF utilizing a electronic device at each FF's info. The previous FF yield, even as even load, is associated towards the MUX's data and MUX's yield is related to the second FF. once the same CLK signal provided to FF, at that time all of the FF are going to be coinciding alongwith. The uses of those register's incorporate

dynamical equal data over to the successive data. This register is utilised to store and shift a 4-bit word.

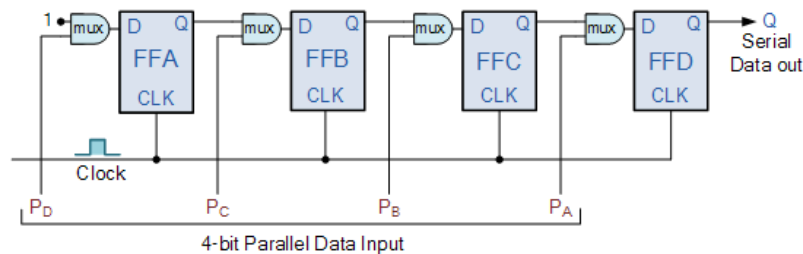


Fig:1.3 : Parallel in-Serial out (PISO) Shift register
(Source [12])

1.2.4 Parallel In-Parallel Out Shift register (PIPO)

PIPO register, the yield info across the equal yields show up all the whereas because the info is taken care of in. The register, which allows equal (information is obtainable severally to every FF associate degreed during a simultaneous way) and what is more delivers an equal yield is thought as Parallel-In equal out register. The logic circuit given at a lower place in figure one.4[12] shows associate degree equal in equal out register. The circuit contains of 4 D FF that are associated. CLR & CLK signals are related to all of the four FF. during this quite register, there contains no relation between FF as no info consecutive moving is crucial. A PIPO (Parallel in Parallel out) register are often used sort of a ephemeral warehousing contraption, like SISO register, and does kind of a defer element.

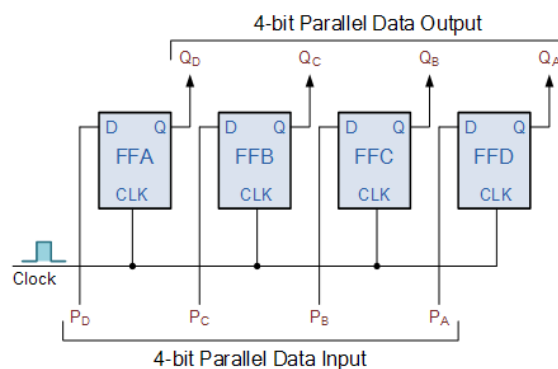


Fig:1.4 : Parallel in-Parallel out (PIPO) Shift Register
(Source [12])

1.2.5 Bidirectional Shift Register

Shift register's may either perform right or left info bit movement, or each relying upon the kind of register and their arrangement. In right move tasks, double info gets isolated with 2. On the off probability that this activity is switched, the 2fold info gets enhanced by two. With cheap utilization of combinational logic, a successive register will be organized to perform each activity.

B. Use cases of Shift Register:

Register's area unit use cases in electronic devices like computers as

- Temporary knowledge storage
- Data transfer
- Bit manipulation
- Electronic bit counting devices

Shift register's area unit utilised in PCs like memory parts. each one of the advanced frameworks ought to store immense live of knowledge, in a very productive way; there we have a tendency to use storage parts like RAM and alternative style of register's. a substantial ton of the computerised framework tasks like division, augmentation area unit performed by utilizing register's. the knowledge is moved through ordered shift register's and alternative type. Bit counting circuit area unit utilised as Digital tickers, Frequency bit counting circuit, Binary bit counting circuit then forth Sequential in ordered out register area unit utilised for delay. ordered in equal out register's area unit utilised for ever-changing knowledge from ordered structure over to jibe structure. thus these area unit in addition referred to as "Sequential to jibe converters".

Equal in ordered out register's area unit utilised for ever-changing the knowledge from equal structure over to ordered structure. thus these area unit likewise referred to as "Corresponding to chronic converters". resembling ordered modification, wherever they're utilised to diminish the amount of wires, or lines needed for correspondence between 2 gadgets, since ordered correspondence for the foremost

half need solely 2 wires contrasted with equal that depends upon the amount of items being sent. Shift register's area unit utilised in state register's that area unit utilised in consecutive gadgets. sort of a restricted memory machine, the subsequent condition of the gismo is consistently controlled by moving and embeddings another info into the previous position.

1.3 MULTIPLEXER

Multiplexing's that the generic term accustomed for explaining the operation of causing one or a lot of analogue or digital signals throughout typical cable at totally distinct time and velocity intrinsically, circuit we tend to use to try and do simply that's known as a electronic device. The electronic device, shortened to "MUX" or "MPX", may be a digital switch, conjointly known as as information selection circuit. Which is combinatory rationale with an load, one yield line and quite one choose line. It permits the binary data from many load lines or sources and counting on the set of choose lines , specific load line , is routed onto one yield line. the fundamental plan of multiplexing is shown below in figure one.5 that information from many sources are thrown towards yield line once the change switch is ON. The electronic device may be a combinatory logic circuit designed to transfer several load lines to a single-yield line. MUXs act like in no time multiple position rotary switches that link or management multiple load lines known as "channels" one at once to the yield. MUXs aren't restricted to easily changing a range of separate load lines or channels to at least one single customary yield. There also are forms which will transfer their loads to many yields and have 4-to-2,8-to-3 or perhaps 16-to-4 arrangements etc.

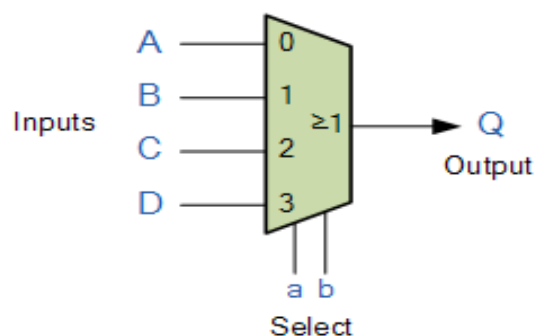


Fig:1.5 : Symbolic Diagram of MUX
(Source [13])

1.3.1 2×1 MULTIPLEXER

Use cases of MUXs are as follows, a electronic device is employed in varied use cases like, wherever multiple knowledge is transmitted employing an individual load. Communication System – electronic device is employed in communication machineries, storage – electronic device is employed in storage to stay up a huge quantity of memory within the computers, and additionally to decrease the quantity of copper lines necessary to attach the memory to different elements of the pc. Phone2phone Network – electronic device is employed in phone2phone networks to integrate the multiple audio signals on one line of transmission. Transmission from the pc System of a Satellite: electronic device is employed to send info signals from the pc to satellite machinery.

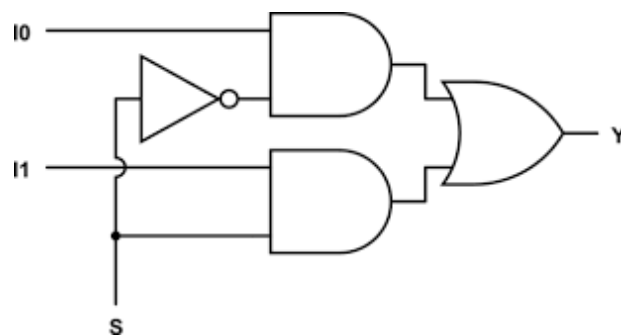


Fig:1.6 : Logic Diagram of 2x1 MUX

(Source [13])

A 2×1 electronic device consists of 2 I0 and I1 loads, one choose S load and one choose Y yield. The yield's attached to one of the loads, reckoning on the decide signal. Since there square measure 2 load signals, it's attainable to link the loads to the yields solely in 2 ways in which, therefore one choice is spare to try to operate. Whenever select load is minimal, the yield is swapped to load I0, or else the select load is maximal, the yield is swapped to load I1. Subsequent figure 1.6[13] explains the structure of 2×1 electronic device that connects 2 one bit loads to a standard route.

1.3.2 4×1 MULTIPLEXER

A 4×1 electronic device consists of 4 information load lines from D0 to D3, meaning the yield at Y is D0 once $S_1=0$ and $S_0=0$, equally Y is D1 once the choose loads $S_1=0$ and $S_0=1$ then on.

Table 1.1: Truth Table of 4×1 MUX

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

The below figure 1.7[13] visualizes a 4 x 1 MUX where the MUX reverse encodes the load by select statements.

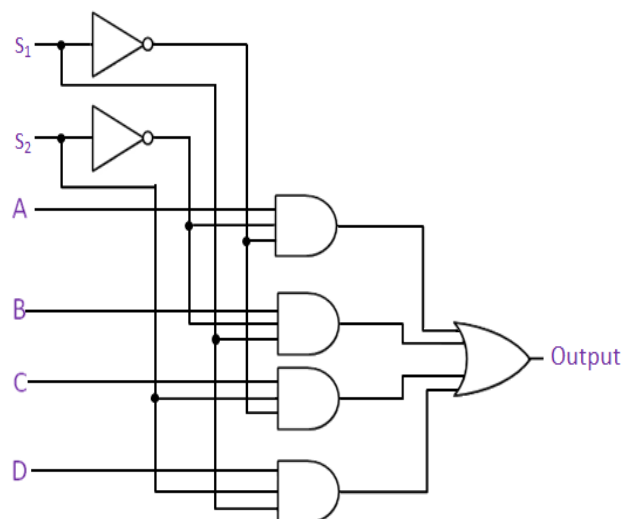


Fig:1.7 : Logic Diagram of 4x1 MUX
(Source [13])

1.4 ORGANIZATION OF THE REPORT

The project report is organized into six chapters

Chapter 1 discusses the background of VLSI, motivation, introduction of shift register's. It conjointly discusses concerning the varied MUXs and organization of the project work.

Chapter 2 delivers elaborated literature survey associated with the project, literature outline, problem definition, objectives of the project.

Chapter 3 describes the existing technical concepts of universal register.

Chapter 4 discusses the proposed low power universal register style victimization modified electronic device and low power d-FF to attenuate the delay.

Chapter 5 provides the simulation results and performance analysis of the prevailing and projected project work. It will a full compareative analysis on however the projected work is best off than the prevailing style.

Chapter 6 provides the conclusion project work. It conjointly provides the schema of the long run work that's however the project may be increased more. Finally, the references cited lead the project square measure given briefly

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

This chapter examines the concerning the writing summary and description. It likewise offers purpose by point thought on the present Universal register and the way their constructions square measure musical organisation.

2.1 LITERATURE SURVEY

Suchismita Senugupta et al. (2017) evaluated the performance metrices of a four Bit Universal register associated its Implementation in an Arithmetic and Logic Unit. during this paper, they need planned a quick low power four Bit Universal register and a complete examination of its presentation boundaries has been light-emitting diode. The four Bit Universal register planned utilizing Cadence Virtuoso in 45nm devours low power and has quick and shows the overall examination of the presentation boundaries, like Power, Speed, PDP and automatic data processing. Thus, the setup is energy effective and it's acceptable for low power quick frameworks. The components of the four Bit USR therefore planned were discovered to be energy productive as an example D FF and 4×1 electronic device.

Shazia Pervez et al. (2017) planned associate Implementation of four Bit Universal register utilizing Diode Free adiabatic Logic. adiabatic logic strategy once contrasted thereupon of a standard CMOS technique shows promising outcomes. a kind of adiabatic procedure, DFAL (Diode Free adiabatic Logic), has been focused during this paper. This paper presents an occasional power adiabatic Universal register, which might perform each serial and equal shift tasks. Contrasted with a traditional CMOS strategy the projected adiabatic logic technique shows viable outcomes. a sort of DFAL, was focused during this paper and this arrangements was used to develop NOR entry, NAND door, XOR door, D FF and Universal register. The investigation of DFAL circuits is targeted around semiconductor unit check, power scattering and deferral. each one of the circuits square measure recreated utilizing 180nm Pyxis innovation. D FF and Universal register were fictitious utilizing DFAL logic that devours less power than typical CMOS circuits. adiabatic exchanging may

be a typical low power strategy; anyway it is not administrated within the VLSI house that is of the quality. This technique is extraordinarily valuable for the low repeat very application. The essential logics could be used to fuse alternative.

Heranmoy Maity et al. (2017) designed a Quantum price economical four Bit Reversible Universal register. This paper have projected the setup of four cycle RUSR or reversible general register utilizing diminished no. of entryways and utilizing existing reversible logic doors. as a result of its low quantum price, less reversible logic entry variety and low trash yields, the projected configuration is exceptionally valuable in quantum reckoning. it's various use cases cheap for reversible ALU, cryptography and then on.

L. Subha et al. (2017) designed an occasional Power typical Universal register victimization 4:1 electronic device. This paper presents the general typical register utilizing edge set out D FF with low power and region adept use cases. The setup of a D FF primarily based Universal register with less territory, less power and diminished semiconductor unit tally. For this paper, micro wind demonstrate the setup of the widespread register and also the cmos innovation utilized is 6nm. The projected Universal register is assessed utilizing thorough recreation procedure, and also the consequences of the microwind re-enactment show that the set up projected is undeniably acceptable for low power, area.

2.2 LITERATURE SUMMAREY

Rather than having varied register's, Universal Shift Register's is used to try and do stack or recover data by performing arts either left or right shift even as equal stacking. on these lines presents Universal register and its executions in several use cases. The presentation examination of standard general register has been shown utilizing varied strategies.

2.3 PROBLEM DEFINITION

To design and analyse the performance parameters of low power Universal register in metric linear unit technology victimisation Modified GDI and MOSFET hybrid technology. Therefore, the performance of Universal Shift Register has become the bottle neck for the system performance.

2.4 OBJECTIVE OF THE PROJECT

- To analyse the existing Universal Shift Register.
- To design and analyse the proposed low power 4*1 MUX using MGDI Technology.
- To develop proposed low power Universal Shift Register and analyse its performance.

CHAPTER 3

AIM AND SCOPE OF PRESENT INVESTIGATION

3.1 PROPOSED METHODOLOGY

- The project aims to decrease the delay that exists in the current framework
- The number of transistors used in designing of the current framework can be reduced in the proposed work
- The proposed system is fare efficient in terms of power consumption

3.2 AREA OF THE PROPOSED WORK AND APPLICATION

Universal register has shown noticeable half within the incidental use cases, it needs order of FFs acquainted for ring counting circuitry shift some info for delivering a linear increase to $2 \times N$ states. A PISO register is employed for dynamic equalization of sequent info. The SISO & PIPO shift register's square measure utilised for making some delay towards computerised circuits. These register's square measure utilised for info shift, management and knowledge reposition. SIPO register was employed for dynamic chronic through tally info thus in communication stages.

3.3 D-FLIPFLOP

FF is AN semiconductor based circuitry with 2 stable expresses which will be used to store two fold data. The place away data are often modified through differing loads. FF's and locks area unit essential structure squares of processed gadgets frameworks used in PCs, interchanges, and various different types of frameworks. FF's and hooks area unit used as data repositing elements. it's the essential repositing part in consecutive logic. Their area unit considerably four varieties of FF, with the foremost well-known one being SR FF. This basic FF circuit incorporates a set data (S) and a reset load (R). In this circuit once you Set "S" as dynamic the yield "Q" would be high and "Q'" are going to be low. once the yields area unit originated, the wiring of the circuit is well-kept till "S" or "R" go high, or power is killed. As incontestable on top of, it's the foremost easy and simplest to grasp. the 2 yields, as

incontestable on top of, area unit the alternative of 1 another. One of the basic disservices of the essential SR gate Bistable circuit is that the unsure data state of $SET = "0"$ and $RESET = "0"$ is prohibited. This state can drive the 2 yields to be at logic "1", superseding the criticism golf shot activity and whichever data goes to logic level "1" 1st can let fully go, whereas the opposite information still at logic "0" controls the next condition of the lock. Yet, to stay this from happening AN electrical converter are often associated between the "SET" and therefore the "RESET" contributions to deliver another quite FF circuit referred to as an information Latch, Delay FF, D-type Bistable, D-type FF or basically a D FF because it is a lot of ordinarily known as. D flip – flops area unit to boot known as "Defer flip – flop" or "Information flip – flop". they're used to store one – bit double data. they're one amongst the widely used flip – flops in advanced gadgets.

The D FF is by a protracted shot the foremost vital of the regular FF because it guarantees that guarantees that loads S and R area unit ne'er love one at the same time. The D-type FF area unit designed from a gated SR FF with AN electrical converter accessorial between the S and therefore the R contributions to think about one D (Data) load. At that time this single data load, named "D" and is used rather than the "Set" signal, and therefore the electrical converter is used to form the reciprocal "Reset" load afterwards creating a level-touchy D-type FF from a level-delicate SR-hook as currently $S = D$ and $R = \text{not } D$ as appeared.

The D FF tracks the knowledge, allowing changes that suit load D. The D means that "information"; this FF stores the value on the knowledge line. It o.k. is also thought-about as a significant memory cell. immediately of a rising clock edge the Q yield takes the estimation of the D data. So it's referred to as the D FF, in light-weight of the actual fact that the yield takes the D data or knowledge load value, and Delays it by one clock tally. D flip – flop has 2 sources of information , a clock (CLK) load ANd an data (D) information and 2 yields; one is principle yield addressed by Q and therefore the different is supplement of Q addressed by Q'. "Expert Slave D-type FF" are often created through fall of 2 latches with opposite clock phases as shown in figure 3.1.

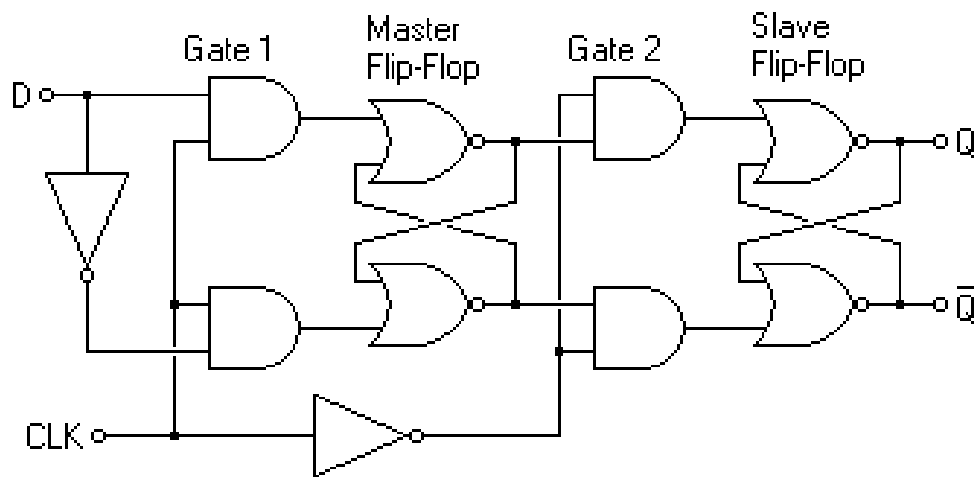


Fig:3.1 : Block Diagram of D-FF

(Source [14])

In a D FF, the yield will be simply modified at the clock edge, and if the data changes at completely different occasions, the yield are going to be unaffected. The distinction in condition of the yield is subject to the rising fringe of the check as incontestable truly table of d-FF given in table three.1[14]. The yield (Q) is same because the data and might simply modification at the rising fringe of the clock. Uses of FF: FF can discover their utilization in a very sizable heap of the fields in advanced gadgets. All amongst go beneath the classification of sequent circuits.

Table 3.1: Truth Table of D-FF

Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

3.4 4×1 MULTIPLEXER

MUX is a combinatory logic circuit which allows only 1 contribution at a particular chance to form the yield. The signs that management that data are going to be mirrored at the yield finish is controlled by the choose data lines. A electronic device is often composed as MUX within the truncated structure. it's likewise referred to as as Many-to-One circuit. this is often an on the spot results of its capability to settle on one sign out of various knowledge sources .Multiplexing is that the property of connection a minimum of one signals and causing on one channel .This is accomplished by the gizmo electronic device.

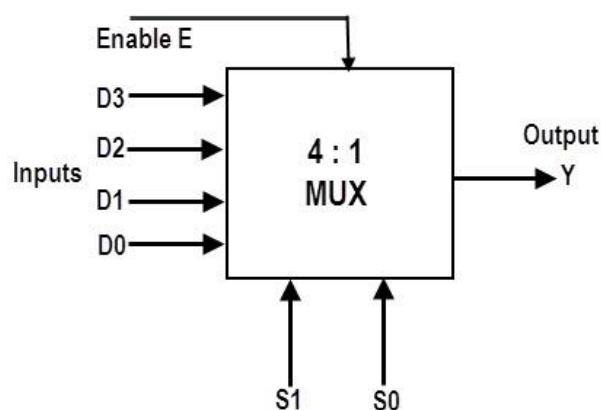


Fig:3.2 : Block Diagram of 4×1 MUX
(Source [13])

The truth table of a 4 x 1 sequential circuitry is demonstrated in table 3.2[13] that four load mixtures 00, 10, 01, 11. From the higher than face of the yield, some 4 x 1 electronic device may be enforced by victimisation fundamental rationale gate.

Table 3.2: Truth Table of 4×1 MUX

Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

3.5 EXISTING 4×1 UNIVERSAL SHIFT REGISTER

A Universal Shift Register may be a register with twin load containing each the proper shift and left shift. Widespread shift register's area unit used in PCs because the memory segments. A unifacial register permits moving away because it were. A bifacial register is appropriate occupancy each the ways that. Presently let we've got a register which may ready to shift info in each the shift right and shift left, aboard the vital info and yield terminals for equal exchange, at that time it's called a register with equal burden or 'general register.' The Universal register may be a bifacial register of 0.5 and 0.5 style and one direction register with equal burden arrangement. The widespread register may be a mix of MUXs and FF.

The FF may be a staple of consecutive logic circuits. it's a circuit that has 2 stable states and may mixture barely of information concerning the state. The yield changes state by applying signs to a minimum of one management loads. electronic device may be a combinatory circuit that have several information info and single yield contingent upon management or choose knowledge sources. A typical n-cycle widespread register is comprised of n FF and n 4×1 MUXs. to select the mode whereby the register works, all the n MUXs share similar choose lines (S_1 and S_0). The choose sources of information decide the proper contribution for the FF.

be an occasion of SISO, SIPO, PISO, PIPO) and two-way register is alluded to as a widespread register aboard equal burden arrangement. A Universal register could be a register that has each the right shift and left shift with equal burden talents. General shift register's area unit used as memory parts in PCs. An universal four-bit register comprises of 4 D-FF and 4 4×1 MUXs. to select the mode wherever the register works, each one of the four MUXs share an identical pick/select lines(S_1 and S_0). The decide sections decide the correct contribution for the FF. Figure 3.4 shows the sq. define of four $\times$ 1 Universal register.

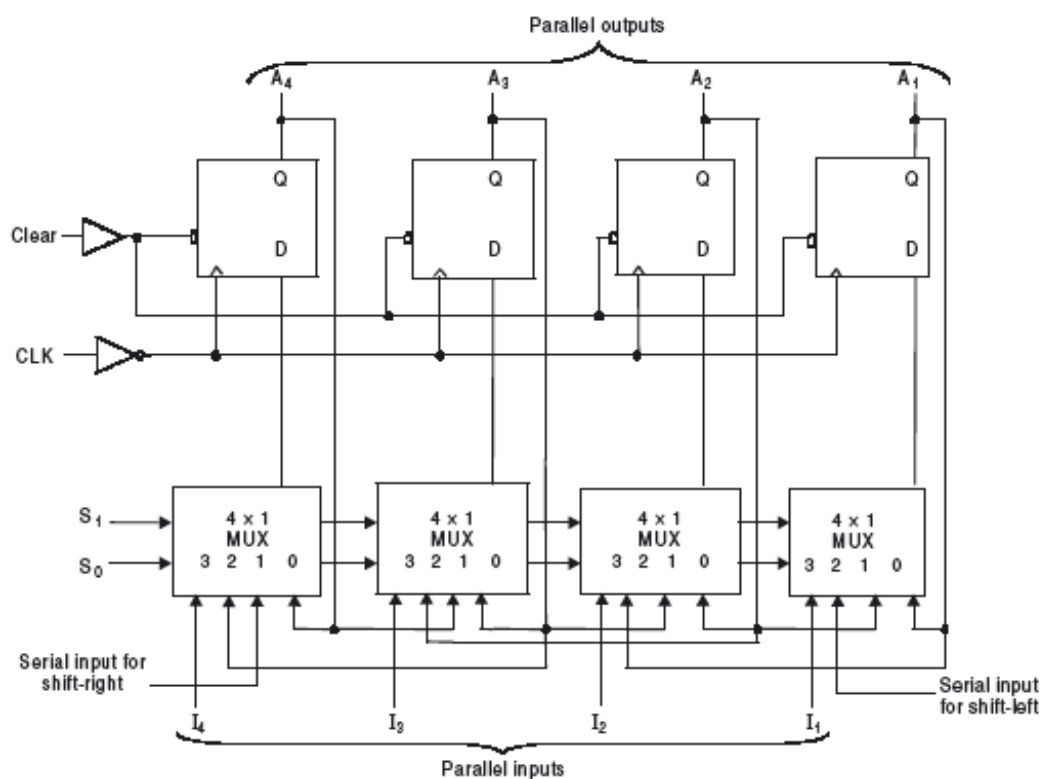


Fig:3.4 : Block Diagram of 4×1 USR

Basic associations - initial load (MUX 0th pin) is related to the yield pin of the examination FF. The next info (MUX 1st pin) is related to the yield of the previous FF that works with proper periodical shifts. 3rd data (MUX 2nd pin) is related to the yield of successive FF that works with the left shift. 4th data (MUX 3rd pin) is related to the distinct items of the data that works with equal stacking. The operating of Universal register is liable upon the sources of information lend to select lines. The register

activities taking place for various loads of select lines area unit visualized in tabular form in 3.3 as follows:

Table 3.3: Truth Table of 4×1 USR (Source [15])

S1	S0	REGISTER OPERATION
0	0	No changes
0	1	Shift right
1	0	Shift left
1	1	Parallel load

3.6 PROPOSED UNIVERSAL SHIFT REGISTER

USR could be one quite register that could be a mixture of unidirectional , biface, and equal stacking register. It utilizes FF for low power and territory effective use cases. Any n-bit USR includes of n number FF and n number 4×1 MUXs. Each n MUXs share similar select lines(S1 and S0) for choosing the modus operandi whenever the register starts working. Select sources of information choose the suitable contribution for the FF. The universal register by and huge uses edge go off D FF with least range of transistors consequently drop-off the region. So here we tend to are attending to examine existing widespread register in our planned work we are going to regulate the existing DFF for a low force DFF and moreover the ongoing electronic device is going to be altered with a planned MGDl primarily based 4×1 electronic device and later on arrange a planned low power universal register to such an extent that it decreases power and territory.

CHAPTER 4

PROPOSED UNIVERSAL SHIFT REGISTER

In the existing work the USR is intended employing a low power D-FF and 4*1 electronic device enforced exploitation GDI (Gate Diffusion Load) technique. within the projected work the USR styled employing a modified 4*1 electronic device exploitation MGDl (Modified Gate Diffusion Load) Technology and low power D-FF that has lesser delay compared to the prevailing design.

- **LOW POWER D-FF**

The repetitive advances and also the since a protracted time ago stacked semiconductor ways in which within the recently distributed FFs will basically expand the ability dissemination. To beat the antecedental mentioned difficulties, a SRFF is projected to adequately reduce the ability utilization while not dishonourable the speed execution. The schematic of the projected SRFF is made public in Figure four.1. The contingent charging hardware is employed within the new SRFF to require out the superfluous changes at node2. The restrictive charging hardware is formed out of 2 p-channel transistors (P7 and P9) associated in arrangements. The entrance terminals of P7 and P9 square measure determined by the integral sign of D (DB) and CLK, on an individual basis. The door terminal of P8 parallelized with P7 is affected by QB to forestall node2 from flying. With the restrictive charging hardware, node2 is restrictively charged relying upon this info contribution of the projected SRFF. Plus, there's no fault happening at the inner hubs of SRFF, that is ensured by the contingent charging circuitry and also the draw down transistors N8 and N9.

The low-to-high progress speed of yield letter of the alphabet is thus sped up with the projected SRFF. Besides, the sanely comparable semiconductors N9 and N12 in S2CFF square measure converged into one transistor N11 within the projected SRFF to diminish the circuit region. The projected SRFF square measure appeared in Figure four.1. At the purpose once CLK is low, P2, P9, and P11 square measure turned on. N4 and N10 square measure bring to a halt. Expecting that D shifts from

minima towards maxima, decibel advances from maxima towards minima. P7 gets turned on and N8 is bring to a halt. Node2 is charged to VDD through P7 and P9, during this method turning on N1. Node1 in ace lock is free, later killing N3. The slave hook holds QB at the recently tested high logic level by the positive load (N13, P11, and P12).

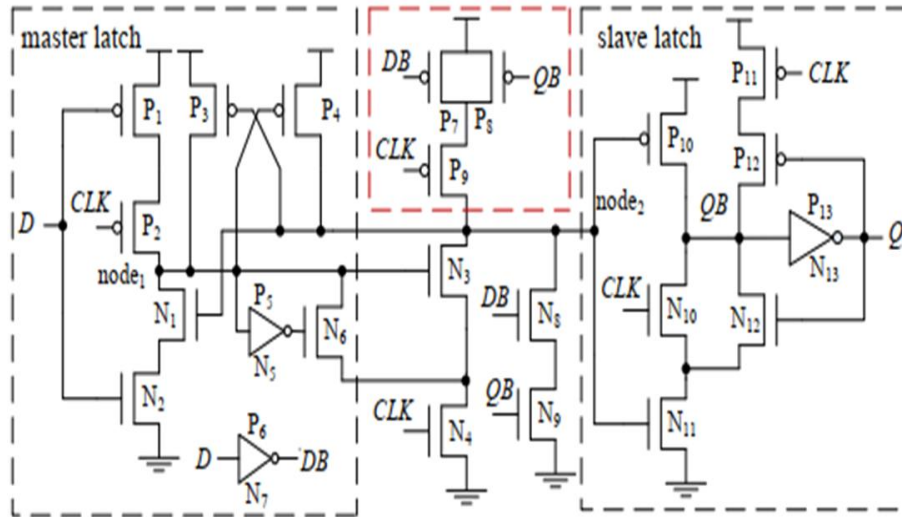


Fig:4.1 : Low Power D-FF

At the purpose once CLK advances to high, P2, P9, and P11 area unit stop. N4 and N10 buffers area unit turned on. Node1 is preserved at 0V by N4 and N6. Node2 within the distinctive stage is saved at VDD through P4. The slave hook is simple to shift the examined D to letter. The high-to - low amendment speed of QB is improved by shortening the emotional approach with the planned SRFF. The planned SRFF to boot shows faster amendment of yield that experiences spasmodic charging of inwards hubs and long charging ways that. on condition that D is command at VDD within the progressive varied clock cycles, node1 and node2 area unit statically preserved at 0V and VDD, separately. Accordingly, no repetitive amendment happens at the inside hubs of SRFF once D is preserved at VDD in back to back clock cycles. At the purpose once D changes from high to low, decibel is charged to VDD. P7 is killed. At the purpose once CLK is low, node1 within the professional lock is charged to VDD through P1 and P2, on these lines turning on N3. Node2 and QB

area unit preserved at the past logic levels wherever the powerful stage and slave hook area unit misty. At the purpose once CLK advances to high, node2 is discharged to 0V through N3 and N4. Node1 within the professional hook is protected at VDD through P3. QB is charged to VDD by the discharged node2. on condition that D is preserved at 0V within the progressive clock cycles, decibel is preserved at VDD. At the purpose once CLK is low, QB re-establishes the recently examined high logic level. P7 and P8 within the contingent charging circuitry area unit killed. Node2 is protected at 0V through N8 and N9.

At the purpose once CLK changes to high, node2 is heretofore preserved at 0V through N3 and N4. there's no excess progress within the planned SRFF once D is command at 0V for ordered clock cycles. the conventional power and shelve power utilization of the new SRFF has been determined as forty five.47 μ W and ninety one.88 pS . A single stage regular excess progress free FF is used for accomplishing higher power proficiency whereas maintaining comparable data to-yield delay. The inwards hubs of the planned SRFF area unit restrictively charged or discharged relying upon the data and yield. Excess changes happening at the inside hubs area unit distributed with within the planned SRFF by utilizing the contingent charging circuitry. Moreover, the since quite whereas ago stacked semiconductor ways that area unit stayed removed from within the planned SRFF.

4.1 2×1 MULTIPLEXER USING MODIFIED GDI TECHNIQUE

There are varied low power technique were gift today during which MGDI is additionally one amongst them. recently MGDI is that the most ordinarily utilised procedure for the reduction of power because it lessens the exchanging of yield. to boot a GDI strategy is used to reduce the amount of junction transistor for the decrease in house of chip. the foremost normally cell associate degree exceedingly. MGDI procedure is an electrical converter cell that is formed by the mix of one PMOS and NMOS. Here one data is given to the entree terminal of each and later on yield

is taken out. The at a lower place figure 4.2 shows the elemental a pair of 2×1 electronic device framed by the help of MGDl technique.

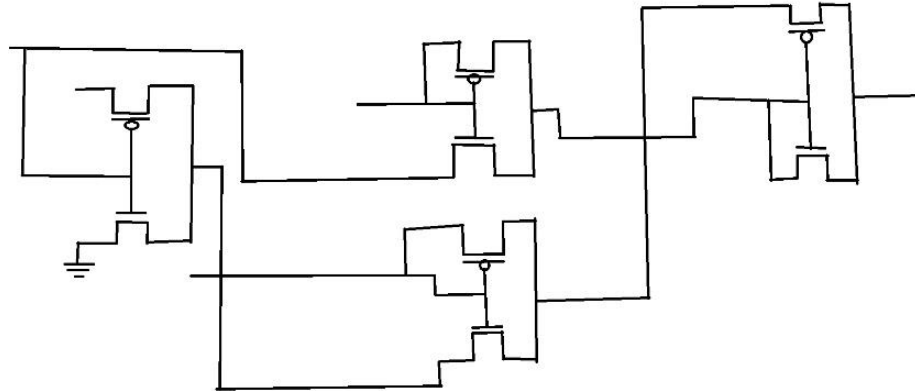


Fig:4.2: 2×1 MULTIPLEXER using MGDl technology

This technique permits major reduction in consumption of power and it's dissipation, timing lag and space binary encoded circuitry, whereas keeping lowkey quality of rationale circuit style. Performance comparison with typical CMOS techniques is conferred, with regard to the, delay and power dissipation, showing higher blessings of MGDl as compared to alternative existing ways. a spread of logic gates are enforced in a hundred thirty nm technology to check the MGDl technique with CMOS. This modified 2×1 electronic device victimisation MGDl technique is employed for the 4×1 electronic device. Now, the modified four $\times 1$ electronic device is shown in figure 4.3 as below.

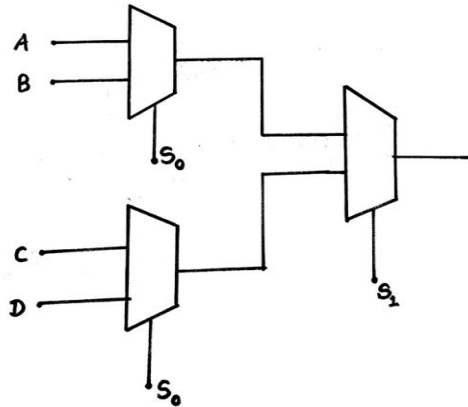


Fig:4.3 : Modified 4×1 MULTIPLEXER

The current electronic device are going to be adjusted, with the top goal that the planned style are going to be superior relating to average power, speed and energy utilization. planned 4×1 electronic device has been planned MGDI strategy. modified Gate Diffusion Load (GDI) another procedure of GDI or primarily a high level type for low power combinative computerised circuit configuration is outlined. The existing Universal register has been planned and poor down utilizing one low power D-FF and 4×1 electronic device execution utilizing regular GDI methodology. The planned low power 4×1 electronic device utilizing MGDI Technology aboared the traditional low power D-FF has been utilised within the planned Universal register to look at its presentation. during this planned style of 4×1 electronic device utilizing MGDI Technology and existing low power D-FF that has been utilised to diminish the facility and deferral of the Universal register.

CHAPTER 5

RESULTS AND DISCUSSION

The current and projected style square measure mimicked by utilizing HSPICE simulator. Yield of the present USR and projected USR square measure compound from the outcomes and it's inferred that the projected style lessens the deferral contrasted and therefore the current framework. the present and projected configuration square measure recreated in abstract HSPICE simulator.

The setup has been assessed in one hundred thirty metric linear unit innovation. The SPICE code of the schematic set up may be seen in alter NL in HSPICE device. it's reproduced. forwarded there's any mistake, it shows work reduce which may be even modified. The avanwaves in H-spice device shows the re-enacted output waveforms.

5.1 EXISTING LOW POWER D-FF SIMULATION OUTPUT

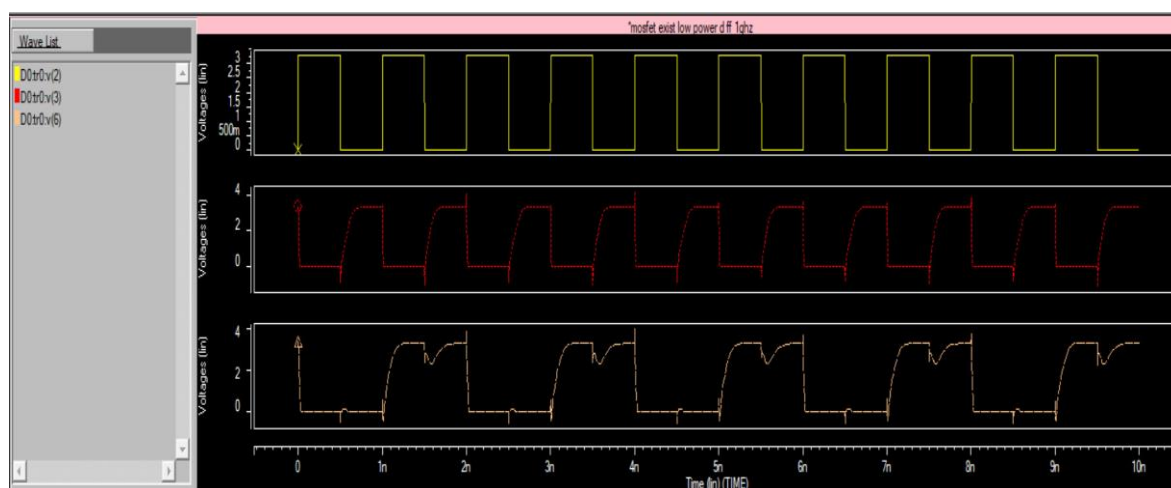


Fig:5.1 : Output Waveform for existing low power d-FF

Fig 5.1 demonstrates simulation of an existing D-FF. Input: v(3), Output : v(16) and CLK : v(2)

5.2 EXISTING 4×1 GDI MUX SIMULATION OUTPUT

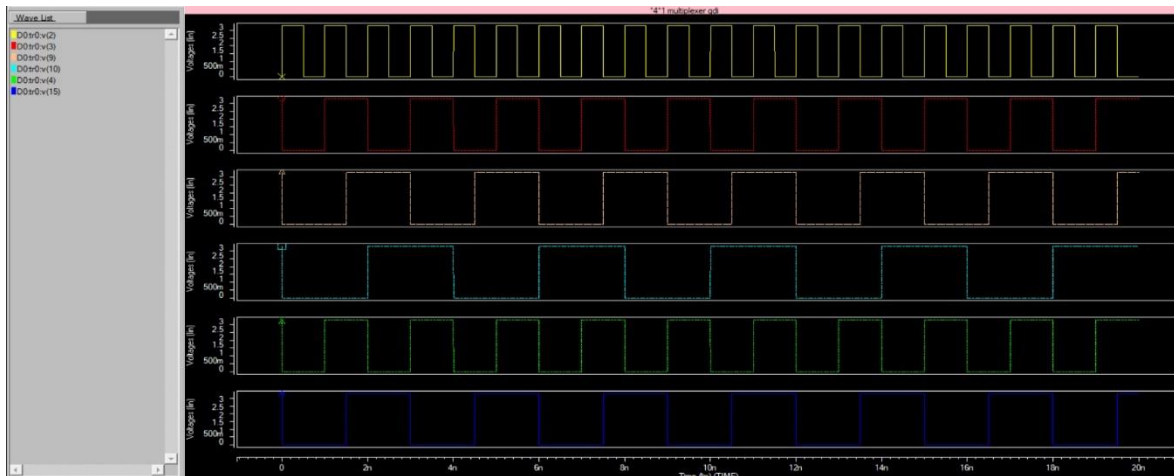


Fig:5.2 : Yield Waveform for existing 4×1 MUX using GDI technique

Fig 5.2 demonstrates simulation for existing 4 x 1 GDI MUX. Input : v(4), v(5), v(6), v(7), Output : v(14) and select line : v(3).

5.3 EXISTING UNIVERSAL SHIFT REGISTER SIMULATION OUTPUT

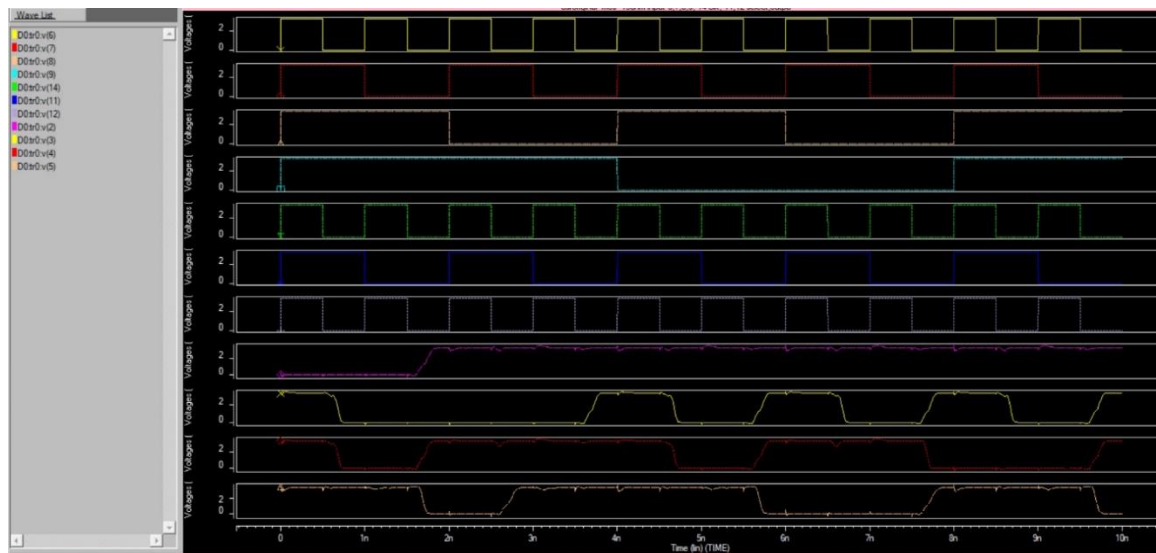


Fig:5.3 : Output Waveform for existing USR using low power DFF and GDI MUX

Fig 5.3 demonstrates simulation of an existing d-FF. Input : V(6), V(7), V(8), V(9) Output : V(2), V(3), V(4), V(5) and CLK : V(14), select line : V(12)

5.4 PROPOSED 4×1 MGDI MULTIPLEXER SIMULATION OUTPUT

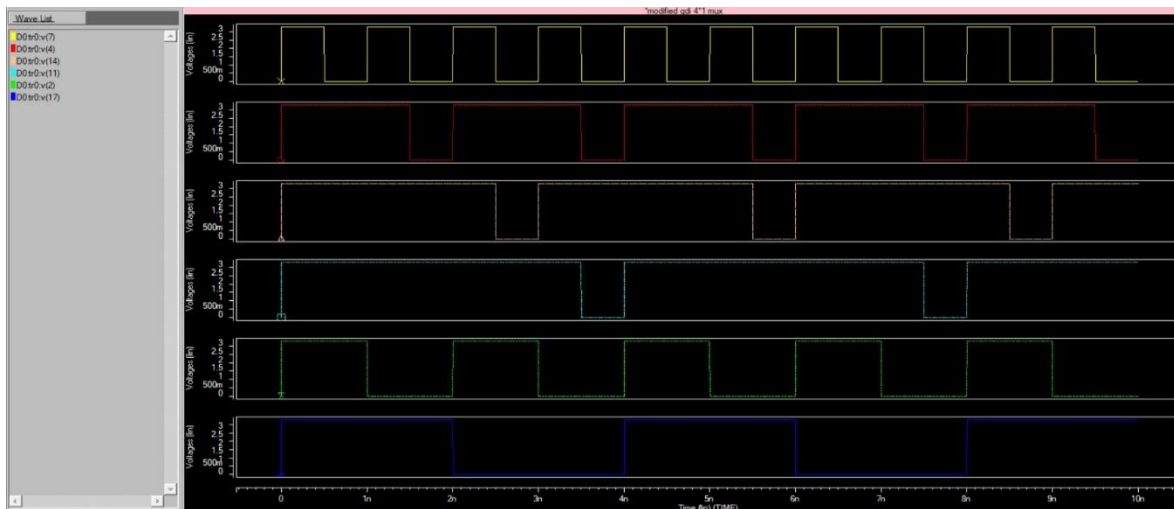


Fig:5.4 : Output Waveform for proposed 4×1 MUX using Modified GDI technique

Fig 5.4 demonstrates simulation of proposed MUX using MGDI methodology. Input :V(2), V(3), V(4), V(5), Output : V(10) and select lines : V(8), V(9).

5.5 PROPOSED USR SIMULATION OUTPUT USING MDGI MUX AND LOW POWER DFF

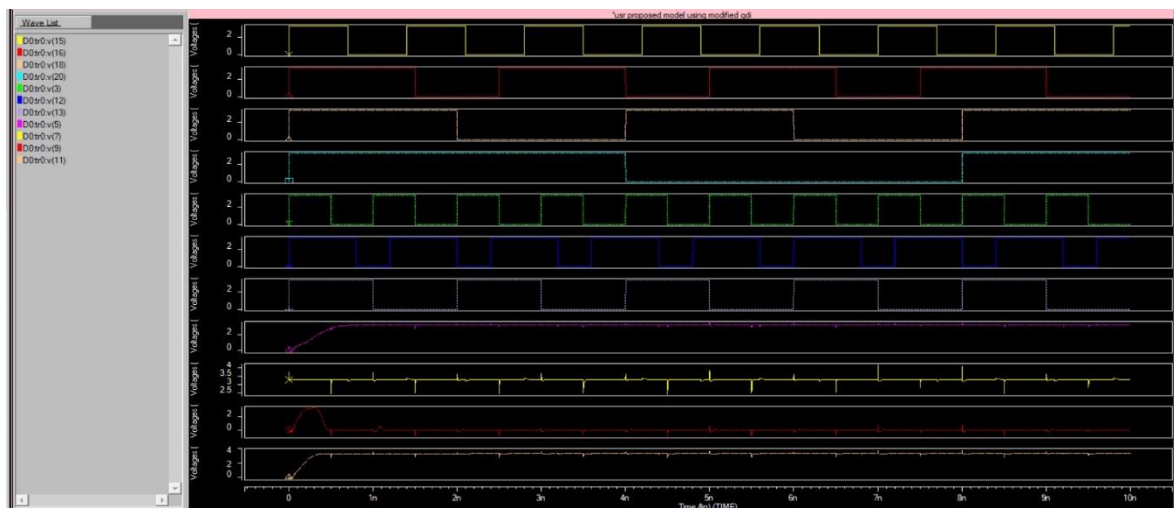


Fig:5.5 : Output waveform for proposed USR using low power d-FF and 4×1 MUX using MGDI technology

Fig 5.5 demonstrates simulation of proposed USR using existing low power DFF and proposed 4 x 1 MUX using MGDI. Input : V(15), V(16), V(18), V(20), Output : V(5), V(7), V(9), V(11), CLK : V(3), CLR : V(2), select lines : V(12) and V(13).

5.6 PERFORMANCE ANALYSIS

The performance analysis of d FF, MUX and USR in terms of power and delay has been given below.

5.6.1. Power And Delay Analysis Of Existing System

Table 5.1 shows the power, delay and PDP of existing design.

Table 5.1: Performance analysis of existing circuit

CIRCUIT (Existing)	AVERAGE POWER(μ W)	DELAY POWER(pS)	PDP(aJ)
LOW POWER D-FLIPFLOP	45.47 μ W	91.88 pS	4177.78 aJ
4*1 MUX USING GDI	72.28 μ W	98.61 pS	7127.54 aJ
UNIVERSAL SHIFT REGISTER	723.1 μ W	119.11 pS	86128.44 aJ

5.6.2 Performance Analysis of Proposed USR using Modified GDI technique

The table 5.2 shows the performance analysis of proposed work using low power D-FF and modified MUX.

Table 5.2: Performance analysis of proposed USR

CIRCUIT (Proposed)	AVERAGE POWER(μW)	DELAY POWER(pS)	PDP(aJ)
LOW POWER D-FLIPFLOP (CMOS)	45.47 μ W	91.88 pS	4177.78 aJ
PROPOSED 4*1 MUX (MGDI)	44.17 μ W	97.88 pS	4323.36 aJ
PROPOSED UNIVERSAL SHIFT REGISTER (CMOS & MGDI)	265.50 μ W	118.91 pS	31570.61 aJ

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

A. CONCLUSION

The aim of the project is to replacement economical Universal register exploitation low power D- FF and modified 4×1 electronic circuit, which provides higher response in terms of speed compared to the standard Universal register. we've achieved a style of a planned Universal register that is faster and has reduced the delay of the standard USR significantly. Since our objective was to reduce the delay of the USR and it's been reduced, thus the tendency to achieved our objective. So, the tendency to saw the planned USR with modified electronic circuit (using MGDI technology) is fare additional economical.

B. FUTURE SCOPE

Shift register may be used for the storage or the transfer of binary knowledge. So, rising its performance will improve the general potency of the system. Future work may be focused on space potency of the FF and electronic circuit and might acquire higher potency in terms of area. This planned universal register may be enforced and might acquire higher potency.

REFERENCES

- [1]. Heranmoy Maity, Anup Kr. Bhattarecherjee, Anita Pal "Design of Quantum Cost Efficient 4 Bit Reversible Universal Shift Register ", 2017 Devices for Integrated Circuit (DevIC)
- [2]. Mohammad Areif Sobhan Bhuiyan, Arevin Mahmoudbeik, Torikul Islam Badal, Mamun Bin Ibne Reaz, Labonnah F. Rahman, " Low power D FF serial in parallel out based shift register", 2016 International Conference on Advances in Electrical Electronics and Systems Engineering (ICAEEES), Pages: 180 – 184
- [3]. Rashid Anware, Jobin Abraham Ben, "A Novel Design of Reversible Universal Shift Register", International Journal of computer Science and Mobile Computing, 2014.
- [4]. Sareanya.M, V.Vijayakumare, T.Ravi, V.Kannan, "Design of Low Power Universal Shift Register", International Journal of Engineering & Technology (IERT), 2013.
- [5]. Subha, Surya "Low Power Conventional Universal Shift Register using 4:1 MUX", 2017 International Conference on Innovative Research In Electrical Sciences (IICIRES)
- [6]. Suchismita Sengupta, Ananya Dastidare "Evaluation of the Performance Metrics of a 4 Bit Universal Shift Register and its Implementation in an Arithmetic & Logic Unit", 2017 International Conference On Smart Technologies For Smart Nation (SmartTechCon)
- [7]. Tamoghna Purkayastha, Debashis De, Tanay Chattopadhyay, "Universal Shift Register Implementation using Quantum Dot Cellulare Automata", Ain Shams Engineering Journal, 2016.

- [8]. Yu Chien-Cheng, Chin Ping-Yuan "Design of Low-Power Double Edge Triggered FF Circuit" 2007 sixth IEEE Conference on ASIC, vol1, May 2005
- [9]. Raj Kumare Mistri, Rahul Ranjan, Pooja Prasad, Anupriya, "IC Layout Design of 4-bit Universal Shift Register using Electric VLSI Design System", International Journal of Engineering Research & Technology (IJERT), 2017
- [10]. M. Morris Mano, Michael D. Ciletti, Digital Design, 5th edition, Pearson 2013
- [11]. S.M. Sze, VLSI technology, 2nd edition, McGraw Hill Companies, 1988
- [12]. www.electronics-tutorials.ws/sequential
- [13]. www.electronicshub.org/MUXandmultiplexing
- [14]. [www.geeksforgeeks.org/FF-types-their-conversion-and-use cases](http://www.geeksforgeeks.org/FF-types-their-conversion-and-use-cases)
- [15]. www.geeksforgeeks.org/universal-shift-register-in-digital-logic

Turnitin Originality Report

Processed on: 15-Apr-2021 9:26 PM EDT

ID: 1560493209

Word Count: 8250

Submitted: 1

project report By Sanghamitra Choudhuri

Similarity Index		Similarity by Source	
9%		Internet Sources:	6%
		Publications:	5%
		Student Papers:	4%

1% match (Internet from 12-Nov-2020)

<https://circuitdigest.com/tutorial/what-is-shift-register-types-applications/>

1% match (publications)

[L Subha, A. Surya. "Low power conventional universal shift register using 4: 1 multiplexer", 2017 International Conference on Innovative Research In Electrical Sciences \(IICIRES\), 2017](#)

1% match (Internet from 15-Dec-2017)

<https://www.electronicshub.org/shift-registers/>

1% match (student papers from 06-May-2020)

[Submitted to Higher Education Commission Pakistan on 2020-05-06](#)

1% match (student papers from 04-Nov-2012)

[Submitted to Nanyang Technological University, Singapore on 2012-11-04](#)

1% match (Internet from 17-Nov-2019)

<http://www.iosrjournals.org/iosr-jvlsi/papers/vol9-issue1/E0901012833.pdf>

< 1% match (publications)

[Shazia Pervez, Manisha Sahoo, Arti Noor. "Implementation of 4-BIT universal shift register using diode free adiabatic logic", 2017 8th International Conference on Computing, Communication and Networking Technologies \(ICCCNT\), 2017](#)

< 1% match (Internet from 03-Dec-2020)

<https://www.elprocus.com/what-is-a-shift-register-different-types-counters-and-applications/>

< 1% match (Internet from 05-Dec-2020)

https://www.electronics-tutorials.ws/sequential/seq_5.html

< 1% match (Internet from 17-Nov-2019)

<http://iosrjen.org/pages/NWIOT-2018-Volume-1.html>

< 1% match (student papers from 31-May-2018)

[Submitted to Indian Institute of Information Technology, Allahabad on 2018-05-31](#)

< 1% match (student papers from 26-May-2018)

[Submitted to Indian Institute of Information Technology, Allahabad on 2018-05-26](#)

< 1% match (student papers from 02-Nov-2018)

[Submitted to Sri Sathya Sai Institute of Higher Learning on 2018-11-02](#)

< 1% match (student papers from 08-Feb-2020)

[Submitted to Management Development Institute Of Singapore on 2020-02-08](#)

< 1% match (student papers from 23-Oct-2013)

[Submitted to Bilkent University on 2013-10-23](#)

< 1% match (Internet from 04-Nov-2019)

<https://pdfs.semanticscholar.org/3c6c/2f3dbfb4050da829d833dd85a8bfb617c202.pdf>

< 1% match (publications)

[Digital Logic Design Using Verilog, 2016.](#)

< 1% match (student papers from 27-Sep-2019)

[Submitted to Melbourne Institute of Technology on 2019-09-27](#)

< 1% match (Internet from 10-Sep-2020)

https://ir.canterbury.ac.nz/bitstream/handle/10092/10494/scott_thesis.pdf?isAllowed=y&sequence=1

< 1% match (Internet from 23-Apr-2011)

<http://www.intelligence.tuc.gr/~petrakis/courses/datastructures/graphs.pdf>

< 1% match (student papers from 01-Apr-2021)

[Submitted to Al Musanna College of Technology on 2021-04-01](#)

< 1% match (Internet from 02-May-2016)

<http://bridgingthegaps.bris.ac.uk/Research/Algorithms/slides/icalp11.pdf>

< 1% match (publications)

[Shugin Lou, Chunling Yang. "Digital Electronic Circuits", Walter de Gruyter GmbH, 2019](#)

< 1% match (publications)

["Proceeding of the Second International Conference on Microelectronics, Computing & Communication Systems \(MCCS 2017\)", Springer Science and Business Media LLC, 2019](#)

< 1% match (Internet from 03-Jan-2021)

<https://ieeexplore.ieee.org/document/8078303/references#references>

< 1% match (Internet from 30-May-2019)

<https://www.scribd.com/document/389763243/10-07-2014-Thesis>

< 1% match ()

<http://epubs.surrey.ac.uk/843770/>

< 1% match (publications)

[Heranmoy Maity, Arindam Biswas, Anup Kr. Bhattacharjee, Anita Pal. "Design of quantum cost efficient 4-bit reversible universal shift register", 2017 Devices for Integrated Circuit \(DevIC\), 2017](#)

< 1% match (publications)

[Jun-Cheol Jeon. "Low-complexity QCA universal shift register design using multiplexer and D flip-flop based on electronic correlations", The Journal of Supercomputing, 2019](#)

< 1% match (publications)

[Maini. "Counters and Registers", Digital Electronics, 07/07/2007](#)

< 1% match (publications)

[Tamoghna Purkayastha, Debashis De, Tanay Chattopadhyay. "Universal shift register implementation using quantum dot cellular automata", Ain Shams Engineering Journal, 2018](#)

ABSTRACT A shift register comprises of cascaded FF, with one FF yield associated with another. FF assume the significant part in rising the power of  Begin Match to source 29 in source list: Jun-Cheol Jeon. [Universal shift register](#).  End Match A  Begin Match to source 29 in source list: Jun-Cheol Jeon. [USR is](#)  End Match kind of  Begin Match to source 29 in source list: Jun-Cheol Jeon. [register that](#)  End Match performs unidirectional,