

PERFORMANCE ANALYSIS OF AN EFFICIENT CONFIGURABLE LOGIC BLOCK FOR LOW POWER APPLICATIONS

Submitted in partial fulfilment of requirements for the award of
Bachelor of Engineering in
Electronics and Communication Engineering

By

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SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of MARTALA DHARMA TEJA (37130241) and MALLAMPALLI SURYA SAMEER (37130230) who carried out the project entitled "**Performance Analysis of an Efficient Configurable Logic Block for Low Power Applications**" under our supervision from December 2020 to April 2021.

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We, MARTALA DHARMA TEJA (37130241) and MALLAMPALLI SURYA SAMEER (37130230) hereby declare that the Project Report entitled **“Performance Analysis of an Efficient Configurable Logic Block for Low Power Applications”** done by us under the guidance of Dr. S. Poornapushpakala., Ph.D. is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

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ABSTRACT

VLSI is a Leading technology in developing various electronic gadgets. In VLSI the development of an electronic item is divided into two types. Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA). ASIC are full custom devices in which it is used only for specific application. These cannot be used for several applications. FPGAs are semi-custom devices; these can be programmed for different application. The functional element in a FPGA is configurable logic block (CLB). CLB is the main component in a FPGA which is used to store data, to transmit the data from one component to another component within the FPGA circuit and more. These are widely used in testing. In any electronic devices power consumption is a major factor that affects the performance of a FPGA circuit. A good FPGA circuit should consume less power, should have less delay, should have less error rate, and also less power dissipation. There are several techniques are available to develop a FPGA circuit with low power consumption, low delay with high efficiency. The most effective Technique is sleep technology. By sleepy technology, we obtained CLB with less power consumption. The power obtained for a CLB without applying sleep technology is 1.215 e-3W , where as the power consumed by a CLB when the sleep technology is applied when MOSFET transistors are used is 2.7 e-6W . 1.856 e-6W of power is utilized by a CLB when the sleep technology is applied when the circuit is built with CNTFET transistors. From the comparison of values of power consumptions in various circuits, it is concluded that by using sleep technology the power can be reduced.

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LIST OF SYMBOLS AND ABBREVIATIONS

VLSI	Very Large-Scale Integration
IC	Integrated Chip
CLB	Configurable Logic Block
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CNTFET	Carbon Nano-Tube Field Effect Transistor
FPGA	Field Programmable Gate Array
MUX	Multiplexer
DFF	Delay Flip Flop
SRFF	Set-Reset Flip Flop
TFF	Toggle Flip Flop
CMOS	Complementary Metal Oxide Semiconductor
PMOS	P-type Metal Oxide Semiconductor
NMOS	N-type Metal Oxide Semiconductor
NDRO	Non-Destructive Read Out
LUT	Look-Up Table
PDP	Power Dissipation
SPICE	Simulation Program with Integrated Circuit Emphasis

CHAPTER 1

INTRODUCTION

The people in the world changing day by day in other words we can say that the interests, likes and dislikes of human beings are continuously changing. The world is changing every day and the technology in the world is changing for every week. As the new technologies came, a lot of companies are established. These companies work for advanced technology which give better output with less cost. As a result of this, many inventions took place such as Smart phone, memory devices, etc. These inventions not only developed the technology but also decreased the size of the gadgets. Introduction of electronic components like transistor, diode, integrated circuits made the components to work in full efficiency. These components consume less electric current, occupy less space and it has more capability to do more work.

Electronic components work on DC supply of 5V or 7V or 12V or 24V it depends upon the board and inputs and outputs in the circuit. These components are controlled or monitored in binary language only. The binary language consists of two numbers. Those are 1's and 0's. The values 1's and 0's can be calculated by the supply voltage and the property of the material used in the components. By using two values the electronic components are designed and made them to work. Since, there are two values the chance of getting the errors is very less or it can be ignored also. The ICs are made by Silicon or Germanium. These two elements are one of the insulators in the periodic table.

The Silicon and Germanium are used as semiconductors because the orbits are far from the nucleus, have higher energy and are less tightly bound to the atom than those closer to the nucleus. This is due to the fact that the force of attraction between the positively charged nucleus and negatively charged electrons weakens as the space between them grows. The most energetic electrons are found in an atom's outermost shell, where they are closely bound to the atom. In addition to this,

the stability in the atom is more in Silicon and Germanium when compared to other atoms. Germanium valence electrons have high energy level than Silicon, therefore Germanium requires smaller amount of energy to escape during high temperature and results in excessive reverse current.

In VLSI integration is divided into Application Specific Integrated Circuits (ASIC) and Field Programmable Gate Arrays (FPGA). FPGAs are widely used in semi-custom and full-custom devices, but ASICs are used only in full custom devices. FPGAs are reprogrammable whereas ASICs are not reprogrammable.

The method of combining thousands of transistors onto a single chip is referred to as VLSI. VLSI architecture is mostly used to reduce the region of interconnecting fabrics. The IC fabrication technology, designer productivity, and cost are the key factors limiting the production of smaller and more complicated IC chips. Different output dimensions are relevant depending on the application. In field-programmable gate array (FPGA) technology, a CLB is a basic building block. Engineers will customize logic blocks to create reconfigurable logic gates. FPGA logic tools are the key computing components that execute and store the target circuit's functionality. Logic resource are composed of a two-dimensional matrix of a CLB that are simply referred as clusters. These clusters are connected to each other and share the data among them to get the output according to the user. These configurable logic blocks are connected to the memories and also input and output ports. Generally, CLB consists of flip-flop, multiplexer, gates, and etc. Each of them has their own purpose to do. Generally, multiplexers are used to select the data from the memories and the flip flops are used to send the data.

1.1. Multiplexers

Multiplexer is also called as mux; this is a digital circuit. This multiplexer is used for selection on data. In a multiplexer consists of selection signals, a greater number of inputs and only one output. So, a multiplexer is representing as "mux inputs x 1". For example, a multiplexer having sixteen (16) inputs then the multiplexer is

represented as “mux 16 x 1”. The selection of output from various inputs is done by selection signals.

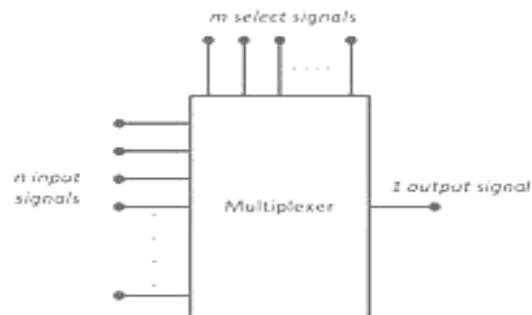


Fig 1.1 Block Diagram - multiplexer

Table 1.1 The truth table - a multiplexer

Selection lines	Inputs		Output
s	Input 1	Input 2	Y
0	0	0	0
0	0	1	1
1	1	0	1
1	1	1	1

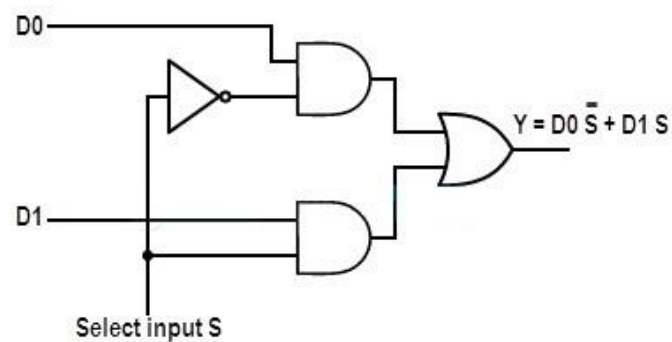


Fig 1.2 Circuit diagram - multiplexer 2:1

The output equation for a mux 2:1 is.

$$Y = D1 \cdot S + D2 \cdot S'$$

From the above equation, in a multiplexer circuit contains N number of AND gates (where n is number of inputs present in the multiplexer), only one OR gate and one NOT gate. At the time of fabrication, the AND gates and OR gate are realized with NAND gates or NOR gates. It is done to reduce the number of transistors that are needed to build a multiplexer.

1.2. Flip-Flop:

Flip-Flop is one of the digital circuits. It defined as one bit storage element. It is called as “Sequential circuit” that means the output of a flip flop depends not only on the present input but also previous output. Every flip flop output is dependent on clock signal. There are several types of flip flops, some of them are Set Reset flip flop, Toggle flip flop, Data flip flop and JK flip flop.

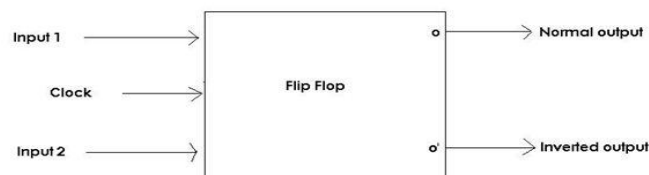


Fig 1.3 Block diagram - Flip Flop

1.3. Set Reset Flip Flop:

Set Reset flip flop is a SR flip flop, it is most simplified flip flop. It contains to four NAND gates. When the inputs of the flip flop S and R is logic 1 and logic 0 respectively, then the output of the flop is high state that is logic 1. When the inputs of the flip flop S and R is logic 0 and logic 1 respectively, then the output of the flop is high state that is logic 0. The main drawback of the SR flip flop is when both the

input states are high then the output of the flip is not determined.

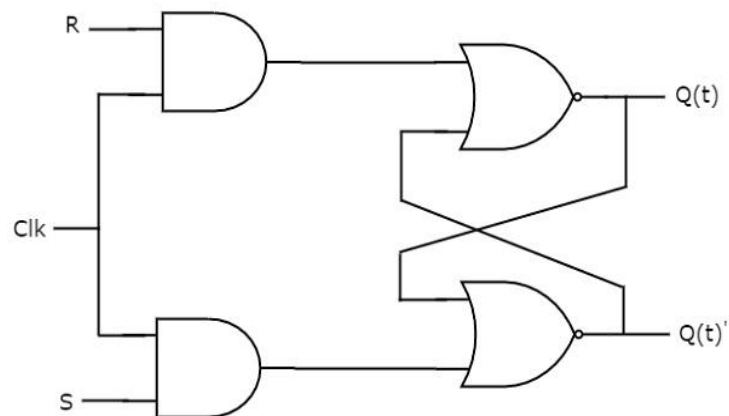


Fig 1.4 Circuit Diagram - SR flip flop

Table 1.2 Truth Table - SR flip flop

CLK	S	R	Q	QBAR
0	x	x	x	x
1	0	0	Q	QBAR
1	1	0	1	0
1	0	1	0	1
1	1	1	x	x

1.4. JK Flip Flop:

JK flip flop is a upgrade version of the SR flip flop. In this flip flop it contains four NAND gates with two input terminals, one clock signal and two outputs. In this flip flop the main drawback of the SR flip flop is rectified. When the two inputs are in logic 1 state then the output will be toggled by its previous state outputs.

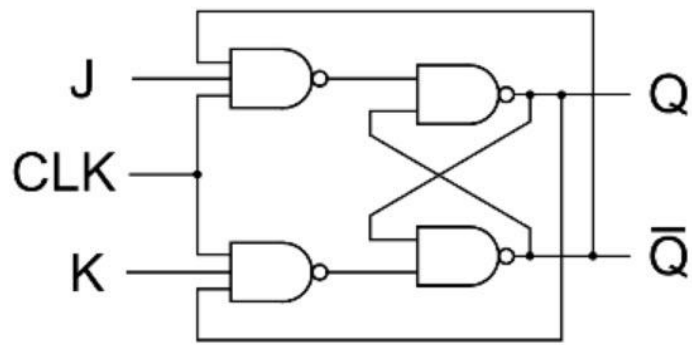


Fig 1.5 Circuit diagram - JK flip flop

Table 1.3 Truth Table - JK flip flop

CLK	J	K	Q	QBAR
0	X	x	x	
1	0	0	Q	QBAR
1	1	0	1	0
1	0	1	0	1
1	1	1	QBAR	Q

1.5. Toggle Flip Flop:

Toggle flip flop is called as T-flip flop. In T-flip flop the present output will be toggle of past output.

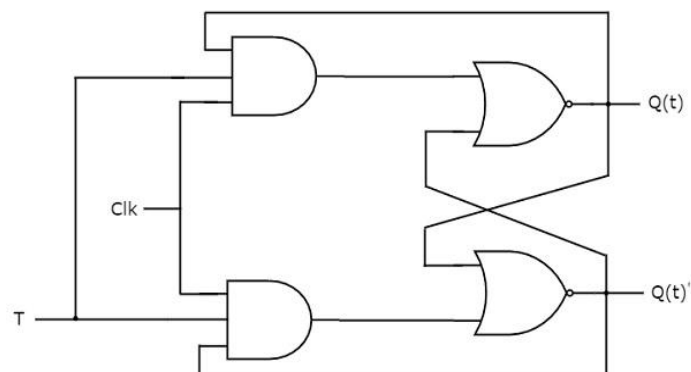


Fig 1.6 Circuit diagram - T flip flop

Table 1.4 Truth Table - T flip flop

CLK	T	Previous Output		Next State	
		Qpre	QBARpre	Qnext	QBARnext
0	x	x	x	x	x
1	0	0	1	0	1
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

1.6. Data Flip Flop:

Data flip flop is called as Delay flip flop or D flip flop. The output of the flip flop will be delayed by one clock signal and the output is same as input.

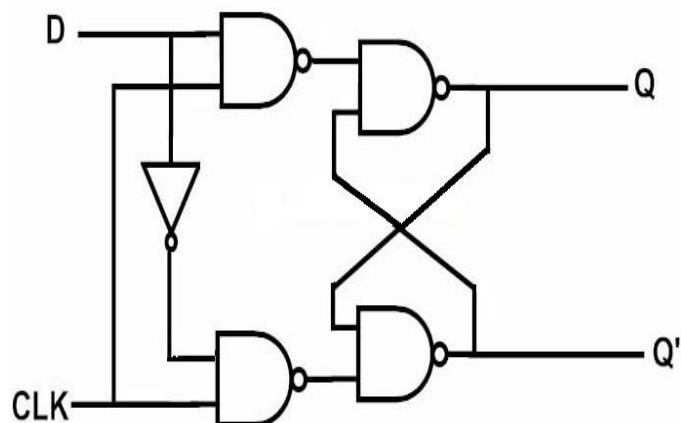


Fig 1.7 Circuit diagram - D flip flop

Table 1.5 Truth Table - D flip flop

CLK	D	Q	QBAR
0	x	x	x
1	0	0	1
1	1	1	0

1.7. Configurable Logic Block:

Configurable logic blocks are the functional element in a FPGA board. In a FPGA there will several millions of CLBs are present. Each CLB is interconnected either directly or through routing points or directional switches. These CLBs are used to collect the data from the input and output ports or memories. Every CLB has their own architecture, the architecture of a CLB is designed by an engineer. Generally a CLB consists of a multiplexer circuit and flip flop circuits. The multiplexer circuit in a CLB is used to select the data and the flip flop is used to transmit the data to the destination.

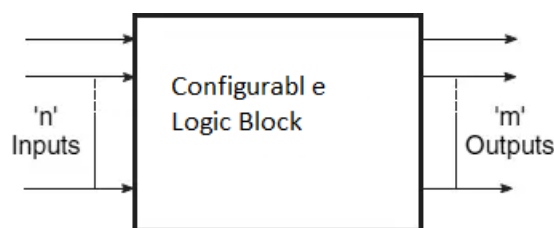


Fig 1.8 Block diagram - CLB

1.8. MOSFET Technology

Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a type of Complementary Metal Oxide Field Effect Transistor (CMOSFET). The CMOSFET technology consists of two types of transistors called P-type MOSFET transistor and N-type MOSFET transistor. The pair of transistors (P-type and N-type transistors) together is called a CMOS technology. The CMOS technology is used mainly in fabricating integrated circuits (ICs), microprocessors, micro controllers, memory chips and more. This type of technology is used in fabricating not only digital circuits but also analog circuits. The main application is developing transceivers.

The MOSFET technology was first developed by Bell laboratory in 1959 and the first microprocessor was developed by MOSFET technology in the year 1960. In late years, the CMOS technology was used in fabricating the ICs by very large-scale integrated circuits (VLSI).

The advantage of the MOSFET technology is high noise immunity, consumes less power and low power dissipation. In CMOS technology, in the pair of transistors one transistor is always in off state and other transistor is in on state, that means if the P-type transistor is in on state or logic high, the pair transistor which is N-type

transistor is in off state or logic low. Similarly, if the N-type transistor is in on state or logic high, the pair transistor which is P-type transistor will be in off state or logic 0.

1.9. CNTFET Technology

CNTFET is abbreviated as carbon nano tubes field effect transistor. The CNTFET is also a type of field effect transistor in which the silicon material in the MOSFET technology is replaced with carbon nano tube.

From the Moore's law, for every 18 months the count of the transistors used in the circuits are doubled. From the late 20th century, the Moore's law is deviated. Since the limitations offered by the MOSFET technology, the number of transistors are reduced due to the power and delay. To achieve more efficient CLB or circuits, the MOSFET technology is replaced by CNTFET technology transistors.

In the CNTFET technology the transistors are made up of carbon nano tubes. The carbon-to-carbon bond or structure in the carbon nano tubes is in hexagonal lattice structure. The diameter of the carbon nano tubes is calculated by the formula $(3d_0/\pi)\sqrt{(m^2 + mn + n^2)}$ and the chiral angle is $\phi = \tan^{-1}(\sqrt{3}n/(2m + n))$. Where d_0 is the distance between carbon and carbon bond and n, m is the point in the lattice. The properties of a transistor vary with the values given to the diameter and the chiral angle. If the values of n, m are equal the gap obtained for the semiconductor is small when the values of the n, m is different.

The advantages in choosing the CNTFET technology rather choosing MOSFET technology is better control over channel formation, the heat dissipation is very low, better threshold voltage, high electron mobility, high current density and high linearity.

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

This chapter discusses the about the literature survey and summary. It also gives a detailed idea on the existing DFF, MUX and CLB and how their structures are synthesized.

2.1. LITERATURE SURVEY

N. Katam, A. Shafaei, and M. Pedram et al. (2017) in this paper the usage of multiple input cell helps in reduction of area and power consumption. D flip flop in CLB circuit is used to balance the delay produced in the circuits. The cost of implementation of multiple input cells is very low when compared to the cost of implementation of single input cell. The advantages of multiple input cells and high-fanout splitters are used in synthesizing MUX, D flip flop, and CLB circuits.

C. Shawawreh, D. Amparo, J. Ren, M. Miller, M. Kamkar, A. Sahu, A. Inamdar, A. Kirichenko, O. Mukhanov, and I. Vernik, et al(2017) in this paper tells about a CLB circuit with superconducting materials. Josephson junctions acts as a resistor in the circuit. This bias resistance offered by Josephson junctions are used in path determined. By using this technology approximately 30% of the voltage is reduced. These circuits can be used at very high frequencies also. The efficiency of the circuit is very high at room temperatures when superconducting materials are used.

Vernik, A. Kirichenko, O. Mukhanov, and T. Ohki et al(2017) in this paper describes about the binary tree architecture. In this paper the decoder is designed using binary tree architecture. The decoder cells are based on single flux quantum technology switches controlled by dc currents via magnetic coupling. The dc bias voltage provided by a special Josephson transmission line acts as a dc voltage source. The voltage developed in the circuit by the Josephson transmission lines are approximately 25% of the DC voltage. The new decoder circuit using a scalable binary-tree architecture optimized for MRAM and register file applications.

Guang-Ming Tang, Kensuke Takata, Masamitsu Tanaka et al(2016) this paper The arithmetic and logic unit is defined. One of the two 32-bit operands is split into eight 4-bit slices. Starting from the least important operand slice, the eight pairs of operand slices are entered one by one. The ALU has eight input ports for a pair of operand slices, X0, X1, X2, X3, Y0, Y1, Y2, and Y3, as well as seven control signal ports, including Carry in, as mentioned below. It has four resulting slice output ports, Z0, Z1, Z2, and Z3, as well as a Carry out port for the product of unsigned SLT and EQ. The AIST ADP2 is used to enforce the physical architecture of the 4-bit bit-slice ALU, which has a minimum Josephson junction of 1.0 m square, a Nb nine-layer structure with dedicated layers for PTLs, and a critical current density of 10 kA/cm². PTLs are used for the wiring of adjacent pipeline stages to reduce the ALU's latency. We used a ladder-type built-in clock generator (CG) for on-chip testing and fabricated the ALU with shift-registers for high-speed input and output (SR IN and SR OUT). A micrograph of the ALU is seen in Fig. 2. SR IN, SR OUT, and CG are not present in the picture. The results for all the ALU operations at high-speed clock for several test vectors, such as (1111 1111 1111 1111 1111 1111 1111 1111, 0000 0000 0000 0000 0000 0000 0001) and pairs of random numbers. Output oscilloscope waveforms showing SUB operation

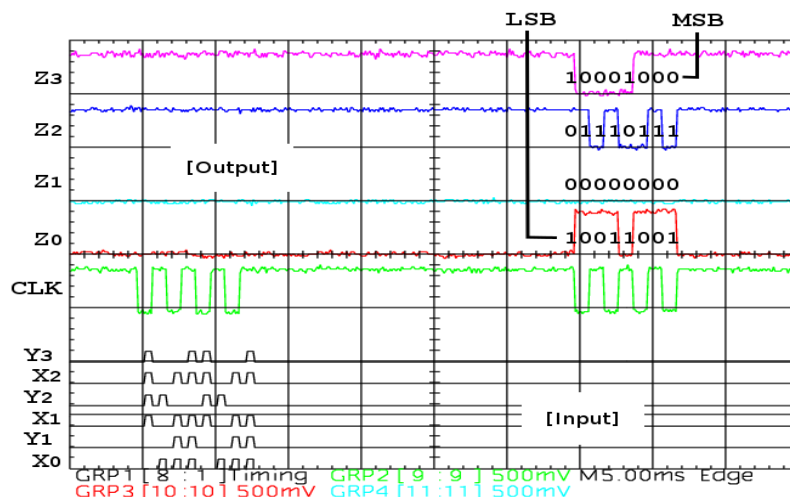


fig 2.1 output waveform - SUB operation

M. A. Manheimer et al (2015) this paper explains the complexities of cryogenic computing programming. Supercomputers and data centres, for example, necessitate massive amounts of electrical power, space, and infrastructure. The power-to-performance ratio for a superconducting machine is fine, but the difficulty is getting from where we are now to a working supercomputer. IARPA tested the validity of some of the latest cryogenic memory theories through a series of one-year seedling trials before deciding to fund C3. C3 is made up of the most effective seedlings.

The C3 program's mission is to create a small-scale prototype device that uses superconducting logic and cryogenic memory and is energy-efficient, scalable, and capable of solving interesting problems. Orthogonal spin transfer torque cells designed for 4 kelvin activity, cryogenic spin hall effect cells, and cells based on Josephson junctions with properties changed by magnetic layers are among the memories generated by the software.

Pankaj Kr. Pal, Rituraj S. Rathore, Ashwani K.Rana, Gaurav Saini et al(2010) this paper tells about the power consumption in full adder circuit with sleep technology and stack technology. In this paper several types of sleep technology, like full sleep technology, zig-zag sleep technology, half sleep technology and stack technology and also applied both the technologies, like sleepy-stack technology. The full adder circuit is implemented by adding transistors to the circuit. The power consumption is less when the sleep technology and stack technology when compared to normal full adder circuit. By applying the sleep technology, the power is reduced nearly 20% and in the stack technology the power is approximately reduced for 15%. When the two technologies are applied together the power consumption is decreased up to 25% of the power consumed by the traditional circuit. By applying the two technologies the efficiency is increased and the power utilization is decreased.

2.2. Literature Summary

The power consumption in a digital circuit is the major problem. This problem not only effects power utilization but also the efficiency of the configurable logic block. The efficiency of a digital circuit will depend on the operational frequency signal

given.

2.3 OBJECTIVES

- To analyse various Configurable Logic Block (CLB) architecture
- To analyse power efficiency of various CLB architecture by modifying the existing architecture
- To compare the results on both existing and proposed CLB using 130nm, 32nm MOSFET and CNTFET technologies in terms of power, delay and Power Dissipation.

CHAPTER 3

EXISTING METHODOLOGY

The existing architecture CLB consists of a program and store block, a 4 X 1 multiplexer for driving the output and Data flip flops for inputs. The CLB proposed is based on NDRO structure.

In the proposed methodology, the architecture of a configurable logic block is developed in island or hierarchical based configurable logic block. In island-style FPGA architecture the configurable logic blocks appear as islands in a sea of interconnects.

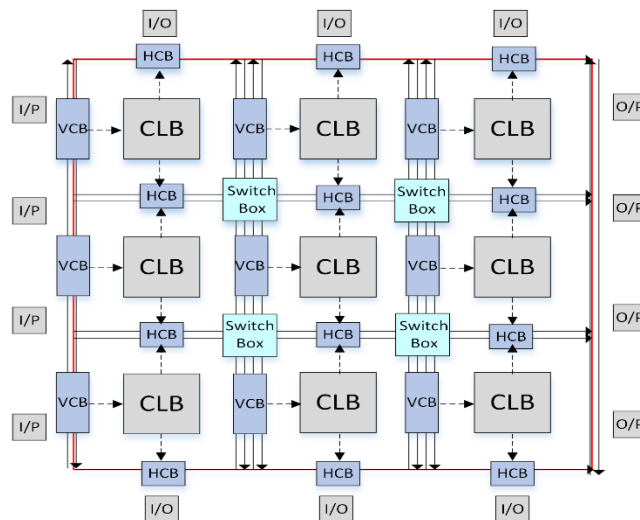


Fig 3.1 Block diagram - architecture (Existing)

In this style of configurable logic blocks are arranged in two-dimensional matrix. The two adjacent configurational logic blocks are connected each other through routing channels. In this architecture the interconnections are organized as horizontal routing channels and vertical routing channels. These routing channels are used to differentiate the direction of the data to be passed, whether the data is from input and output ports or to be passed to input and output ports. The routing channels are also used in transmitting the data from one configurable logic block to another configurable logic block. The direction of the data to be transmitted to its destination

is done by a programmable switch. These switches can be programmed, so that the data will be reached to its destination.

The interconnects that are called routing channels are unidirectional. To convert the unidirectional routing channels into bidirectional programmable switches are installed. The programmable switches can be programmed so that the routing channels are modified into bidirectional wires. Because of this problem the cost of routing network is increased. Since the addition of programmable switches in the circuit the delay produced in the circuit is increased.

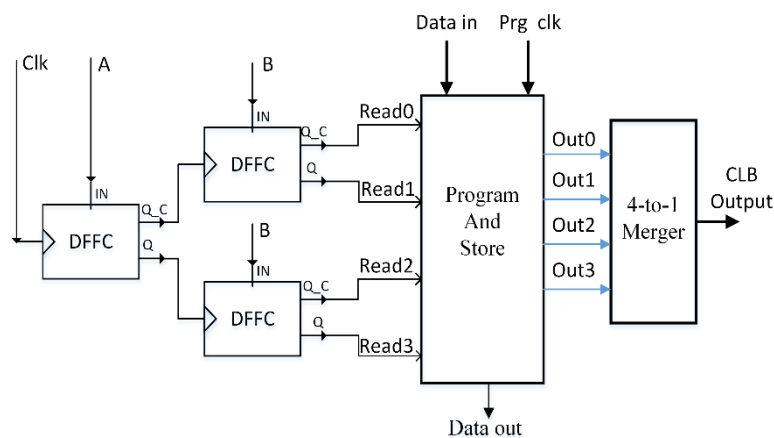


Fig 3.2 Block diagram of existing CLB

3.1. Program and Store Block

Commercially available CMOS FPGAs use static memory cells for programming and storing. The Non-Destructive Read Out (NDRO) is one of the methods for implementing a CLB. In the NDRO based CLB implementation program and store is one of the building blocks. The program and store block in the CLB is used to convert the CLB into desired gate.

The NDRO circuit consists of a four flip flops with parallel input and parallel output which the output is driven out with a separate clock signal called program clock. The program clock in the NDRO circuit in the program and store block has to be given very carefully. The clock signal must be given when the inputs of all the D flip flop must be arrived. If the program clock signal is given before the inputs are arrived

then the output of the CLB is not accurate and there will be more error bits are appeared which is not a condition for efficient CLB architecture. Before giving the program signal given to the program and store block the data in the NDRO cells are to be cleared. To clear the data a rest signal is given before diving the program clock signal. This makes the NDRO cells free from previous data, so that when the new data arrives to the NDRO cells, it drives exact data of the new data. By this process the error rate in the CLB gets reduced.

LUT based CLB the above figure 3.1 is implementation of a two-input gate. The program and store block in the configurable logic block has four input which stores all the different outputs of any of two input gates. The output values will be stored in the PS block only when the CLB is in programming mode only. The values will retain when the CLB gets another clock pulse for programming mode. Once the programming mode is completed the CLB is in reading mode. In this mode the inputs are mapped to the stored values and gets the required output. The output of the CLB is taken from the 4 to 1 multiplexer.

The switch box plays a major role in transmitting the data from one location to another location. The switch box is placed at each intersection of horizontal channels and vertical channels. Since the channels are unidirectional, the horizontal tracks contain two lines which runs from left to right. The vertical tracks contain four tracks. Each two tracks run from up to down directions.

The horizontal connection blocks and vertical connection blocks in the CLB are the routing channels and are a part of programmable routing. The inputs for the CLB are taken through vertical connection block and the outputs of the CLB are taken through vertical connection blocks. In the vertical connection blocks the signal will split and one signal is merged to input of the CLB.

CHAPTER 4

MODIFIED CLB USING SLEEP TECHNOLOGY

In the existing work the CLB is designed by NDRO cells. In this proposed methodology the CLB is designed using a modified network which has low power consumption when compared to existing model.

The main factor that effects the performance of a CLB is power, delay and power dissipation. There are several technologies available to reduce the effects of power, delay and power dissipation. Some of them are “Sleep Technology”. The CLB was designed in two technologies, one is using MOSFET technology, and another is CNTFET technology.

4.1. Logic analysis for NOT gate using MOSFET and CNTFET technologies

In MOSFET technology contains a pull-up network and pull-down network. Generally, the pull-up network contains only PMOS transistor, and the pull-up network is connected to source. Whereas the pulldown network contains all the NMOS transistors, and the pull-down network is connected to ground terminal.

In the NOT gate circuit, a pull-up network contains one PMOS transistor and in the pull-down network contains only one NMOS transistor. In the NOT gate circuit, the pull-up network and the pull-down network are connected in series. The nature of the PMOS transistor in any circuit is, When the input signal is logic 1 or high voltage, then the transistor will be in off state. Similarly, when the input signal given to PMOS transistor is logic 0 or low voltage, then the transistor will be in on state. The nature of NMOS transistor in the pull-down network is when the input signal is logic 0 or low voltage, then the NMOS transistor is in off state. Whereas, then the input signal is logic 1 or high voltage is given to the NMOS transistor, then the transistor is in on state.

In the NOT gate circuit, the PMOS transistor and NMOS transistor is connected in series and the output is taken from point of intersection of PMOS transistor and NMOS transistor. The input to the both the transistor is given from the same signal at same time. The same signal is given to both the transistor. When the input is

logic 1 or high voltage then PMOS transistor in the circuit is in off state and the NMOS transistor will be in on state. Since, the PMOS transistor is the off state which connects to the source, the voltage at the output port will have low voltage or logic 0. Similarly, when the input signal is logic 0 or low voltage, then the PMOS transistor is in on state and the NMOS transistor will be off state. Since the PMOS transistor is in on state the voltage from the source is moved to NMOS transistor. The NMOS transistor in the circuit is off state, the voltage in the circuit is will not be reached to ground terminal. So, the voltage at output port have logic 1 or high voltage. Hence the truth table of not gate is achieved. Since the NOT gate gets converts the logic 0 to logic 1 and logic 1 to logic 0. So, the not gate is also called as inverter.

The operation of the NOT gate is same in CNTFET technology also.

By combining the PMOS transistors and NMOS transistors we can achieve any type of digital circuit or analog circuit.

The project is done in H-spice simulator. In the H-spice simulator is used for calculating power, delay etc.

4.2. H-spice simulator

The acronym SPICE stands for "Simulation Program with Integrated Circuit Emphasis". It is a programming language used to check the design of an integrated circuit and board level circuit. Before fabricating an IC or other circuits. The cost of fabrication or photolithographic masks are very costly. In order to obtain the correct design and to check the circuit before fabrication. The board level circuits can be tested on the breadboard itself, but the values obtained from the circuit may not be accurate when compared to printed board. So, to measure the values accurately SPICE simulators are used. The SPICE simulator wants more information about the circuit. The SPICE simulator is a programming language which describes about the elements of the circuits like, transistor, capacitor, resistor, inductor and more. The programming in the SPICE model is the circuit connection. The elements in the circuit are converted into netlist by the simulator. By accruing all the information, the

simulator simulates the circuit and provides more accurate results of the circuit when compared to breadboard results. SPICE is one of the popular tools used in industries to analyze the circuit models or integrated circuits within less time and low error values. The simulator can analyze the AC characteristics, DC characteristics, noise level in the circuit and transfer functions. H-SPICE simulator simulates both linear circuits and non-linear circuits.

4.3. Operation of sleep technology

Sleep technology is one of the low power technologies that are used in industries. In sleep technology the word sleep means off state, that is whenever the sleep technology is on the circuit will be in off state. In sleep technology there will be additional signal is applied to the circuit. The additional signal in the sleep technology is sleep signal. There are several sleep technologies are used, they are “Full Sleep Technology”, “P-Half Technology”, “N-Half Technology”.

4.4. Full Sleep Technology

Full sleep technology is the most efficient and useful technology when compared to other types of sleep technologies. In this sleep technology additional two transistors are added one is PMOS transistor and another is NMOS transistors. The PMOS transistor is added between the pull up network and source terminal. The NMOS transistor is added between pull down network and ground terminal.

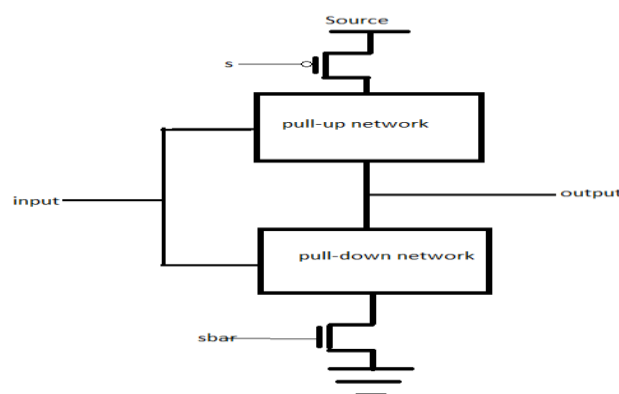


Fig 4.1 Block diagram of Full Sleep Technology

4.5. P-Half Sleep Technology

In P-Half technology only one transistor is added in to the full network. The additional PMOS transistor is placed between the source terminal and pull up network. In this technology only one sleep signal is present. Whenever the sleep signal is applied the output of the CLB is random and when the sleep signal is not applied the output will be driven out.

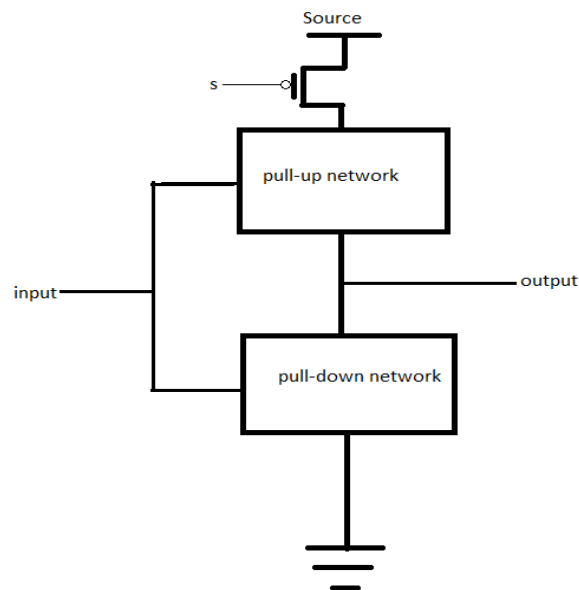


Fig 4.2 Block diagram of P-Half Sleep Technology

4.6. N-Half Sleep Technology

In N-Half technology one pull-down transistor is added to the circuit. The pull-down transistor, which is a NMOS transistor is placed between pull down network and ground terminal. In this technology sleep signal is given to the NMOS sleep transistor.

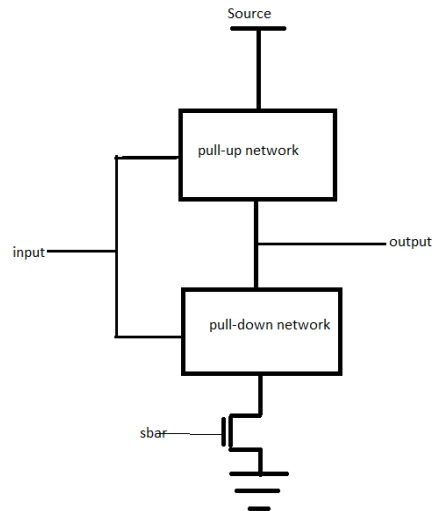


Fig 4.3 Block diagram of N-Half Sleep Technology

4.7. Modified CLB

In the existing architecture the inputs are given at Data flip-flops, and the output is taken from multiplexer. In the existing model the program and store block are replaced with four NDRO circuit that is Data flip flop. The output of the four D flip flops is given to inputs of multiplexer.

The performance of the CLB is done in N-Half Sleep technology, P-Half Sleep technology, Full Sleep Technology.

In P-Half sleep technology, the pull up network that is the PMOS transistor which are connected to source terminal (VDD) are connected to a sleep PMOS transistor (VSS) and the VDD terminal of the PMOS sleep transistor is connected to source terminal. The sleep signal given to the PMOS sleep transistor must be low to high signal. Since the property of a PMOS is output is inverted signal of input, that means when the input signal is logic 1 or high then the output is logic 0 or low. Similarly, when the input is logic 0 or low then the output is logic 1 or high. When sleep signal is applied to the circuit then the output is random signal and when the sleep signal is not applied the CLB gives the perfect output.

In N-Half sleep signal, the pull-down network that is NMOS transistors is added to the CLB circuit between the pull-down network and ground terminal. The statement defines that in NMOS transistors that are connected to ground terminal (VSS) are connected to VDD of NMOS sleep transistor and the VSS of the NMOS

sleep transistor is connected to ground terminal. The sleep signals must be low to high signal. Since the property of a NMOS is output is same signal as of input signal, that means when the input signal is logic 1 or high then the output is also logic 1 or high. Similarly, when the input is logic 0 or low then the output is logic 0 or low. When sleep signal is applied to the circuit then the output is random signal and when the sleep signal is not applied the CLB gives the perfect output.

In Full sleep signal, both pull-up network and pull-down network are added. The pull-up network and pull-down network is PMOS transistor and NMOS transistor respectively. For PMOS transistor the sleep signal must be high to low signal, whereas the sleep signal for NMOS sleep transistor but be low to high signal. When sleep signal is applied to the circuit then the output is random signal and when the sleep signal is not applied the CLB gives the exact output.

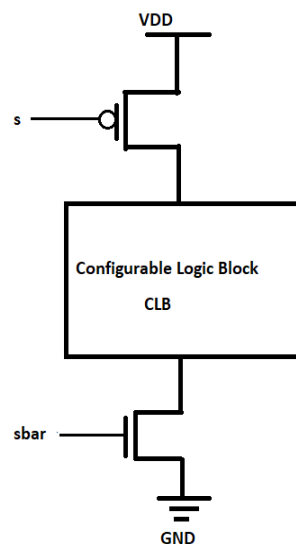


Fig 4.4 Block diagram of modified CLB

By adding the above circuit, the power consumed by a CLB block will be decreased. The designed CLB consists of a mux circuit and a D-flip flop circuit. The circuit of a mux or D-flip flop or any other digital circuit contains transistors which are made of PMOS transistors and NMOS transistors in MOSFET technology. These transistors are connected either in serially or parallelly according to the circuit behavior. The transistor level realization of any circuits are obtained only in either in NAND gates or NOR gates but not any other gates like AND gate, OR gate or any other gates. So, the NAND gate and NOR gates are called the universal gates.

The NAND gate is the combination of two gates. The two gates are AND gate and NOT gate. So, the output of the NAND gate is invert signal of AND gate.

Equation of NAND gate: $(A.B)'$

Where A and B are the input signals of NAND gate.

Therefore the truth table of the NAND gate is invert to the AND gate truth table

Table 4.1 NAND gate - Truth Table

A	B	OUTPUT
0	0	1
0	1	1
1	0	1
1	1	0

In CMOS technology, there are two types of network will be present. They are pull-up network and pull-down network. The pull-up network in the NAND gate contains two P-type MOS transistors (P1,P2). The two P-type MOS transistors are connected in parallel, whereas in the pull-down network contain two N-type MOS transistors (N1,N2), the two N-type MOS transistors are connected serially. The pull-up network and pull-down network are connected in series only. The output of the NAND gate is taken from the connection point of both pull-up network and pull-down network that is the junction point of P-type MOS transistor network and N-type MOS transistor. For a normal NAND gate have two input ports and one output port. Let us consider the two inputs as signal A and signal B. One input signal, consider A is given to a PMOS transistor P1 and the same signal is given to NMOS transistor N1, the second signal B is given to transistor P2 and the same signal is also connected to NMOS transistor N2. The operation of P-type MOS transistor and N-type Transistor is known. The pull-up network is connected to source or supply terminal and the pull-down network is connected to ground terminal. When the signals are given to circuit, let us consider the input A is given logic 1 and the input signal B is given logic 1, then the PMOS transistors P1 and P2 are off state and the NMOS transistors N1 and N2 are on state. Since the both the PMOS are in off state the voltage or current does not pass

through the transistors. So, that the voltage level at output port is zero which is called as logic 0. When the input signal A is logic 0 and input signal B is logic 1 then the transistor P1 is in on state and transistor P2 is in off state and NMOS transistors N1 is in off state and N2 is in on state. The current flows through N1 transistor via P1 transistor. Since, the N1 transistor is off the voltage at the output terminal is high which is called as logic 1. Similarly, When the input signal A is logic 1 and input signal B is logic 0 then the transistor P1 is in off state and transistor P2 is in on state and NMOS transistors N2 is in off state and N1 is in on state. The current flows through pull-down network transistor via P2 transistor. Since, the N2 transistor is off the voltage at the output terminal is high which is called as logic 1. When both the input signals are logic 0, the PMOS transistors will be in on state and the NMOS transistor will be in off state. So, the voltage level at output port is logic 1 or high. The NOR gate is the combination of two gates. The two gates are OR gate and NOT gate. So, the output of the NOR gate is invert signal of OR gate.

Equation of NOR gate: $(A+B)'$

Where A and B are the input signals of NOR gate.

Therefore, the truth table of the NOR gate is invert to the OR gate truth table

Table 4.2 NOR gate - Truth Table

A	B	OUTPUT
0	0	1
0	1	0
1	0	0
1	1	0

In CMOS technology, there are two types of network will be present. They are pull-up network and pull-down network. The pull-up network in the NAND gate contains two P-type MOS transistors (P1,P2). The two P-type MOS transistors are connected in series, whereas in the pull-down network contain two N-type MOS transistors (N1,N2), the two N-type MOS transistors are connected parallelly. The pull-up network and pull-down network are connected in series only. The output of the NOR gate is taken from the connection point of both pull-up network and pull-down

network that is the junction point of P-type MOS transistor network and N-type MOS transistor.

For a normal NOR gate have two input ports and one output port. Let us consider the two inputs as signal A and signal B. One input signal, consider A is given to a PMOS transistor P1 and the same signal is given to NMOS transistor N1, the second signal B is given to transistor P2 and the same signal is also connected to NMOS transistor N2. The operation of P-type MOS transistor and N-type Transistor is known. The pull-up network is connected to source or supply terminal and the pull-down network is connected to ground terminal. When the signals are given to circuit, let us consider the input A is given logic 1 and the input signal B is given logic 1, then the PMOS transistors P1 and P2 are off state and the NMOS transistors N1 and N2 are on state. Since the both the PMOS are in off state the voltage or current does not pass through the transistors. So, that the voltage level at output port is zero which is called as logic 0. When the input signal A is logic 0 and input signal B is logic 1 then the transistor P1 is in on state and transistor P2 is in off state and NMOS transistors N1 is in off state and N2 is in on state. Since, the P2 transistor is off the voltage at the output terminal is low which is called as logic 0. Similarly, When the input signal A is logic 1 and input signal B is logic0 then the transistor P1 is in off state and transistor P2 is in on state and NMOS transistors N2 is in off state and N1 is in on state. Since, the P2 transistor is off the voltage at the output terminal is high which is called as logic 1. When both the input signals are logic 0, the PMOS transistors will be in on state and the NMOS transistor will be in off state. So, the voltage level at output port is logic 1 or high. The circuit of the CLB is designed using MOSFET technology and CNTFET technology. The circuit diagram of each block is shown at introduction.

CHAPTER 5

RESULTS AND DISCUSSION

The Avantwaves simulator is used to model the current and planned architecture. The performance of the current CLB and the proposed CLB was compared, and it is concluded that the proposed architecture consumes less power than the existing design. Hspice UI is used for the synthesis.

5.1 Simulation results for MOSFET technology

5.1.1 Simulation results for 130nm CLB without sleep

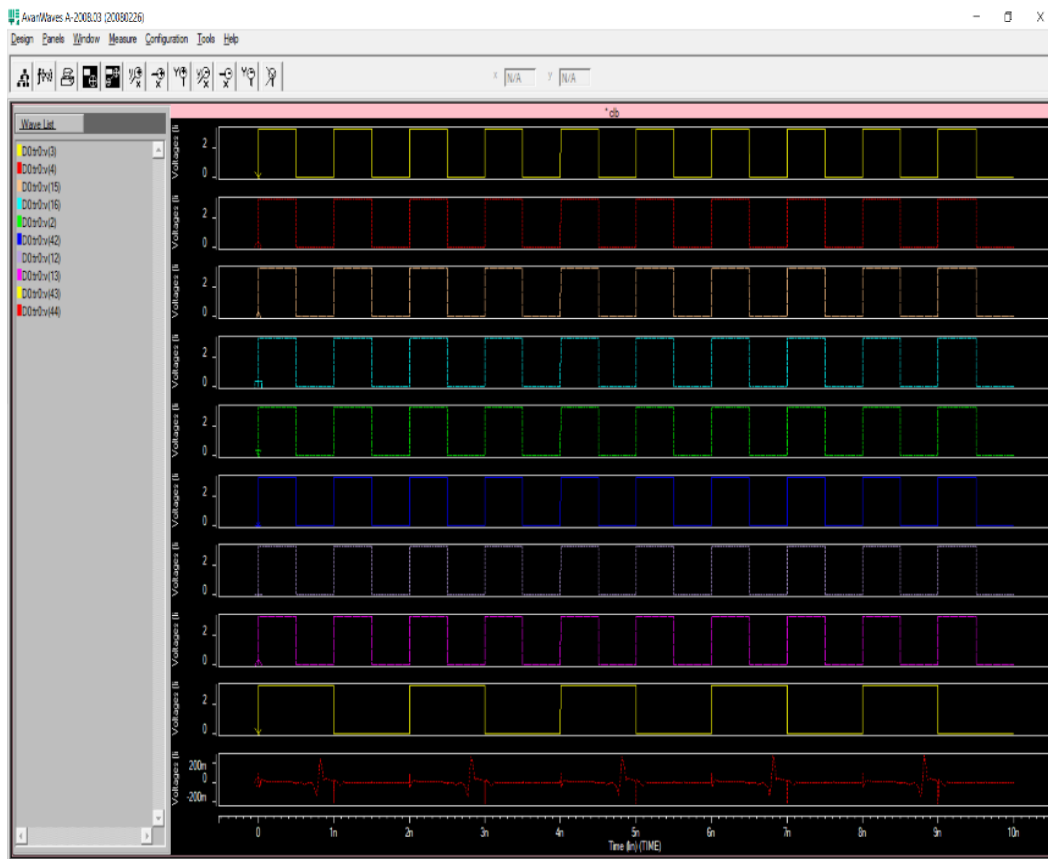


Fig 5.1 simulation output of a CLB 130nm without sleep.

Figure 5.1 shows the simulation of a CLB 130 nm without sleep, the inputs given were v (3), v (4), v (15), v (16) and selection lines given were v (2), v (42), v (12), v (13) and CLK signal given was v (43) and the output is taken by v (44).

5.1.2 Simulation results for 32nm CLB without sleep

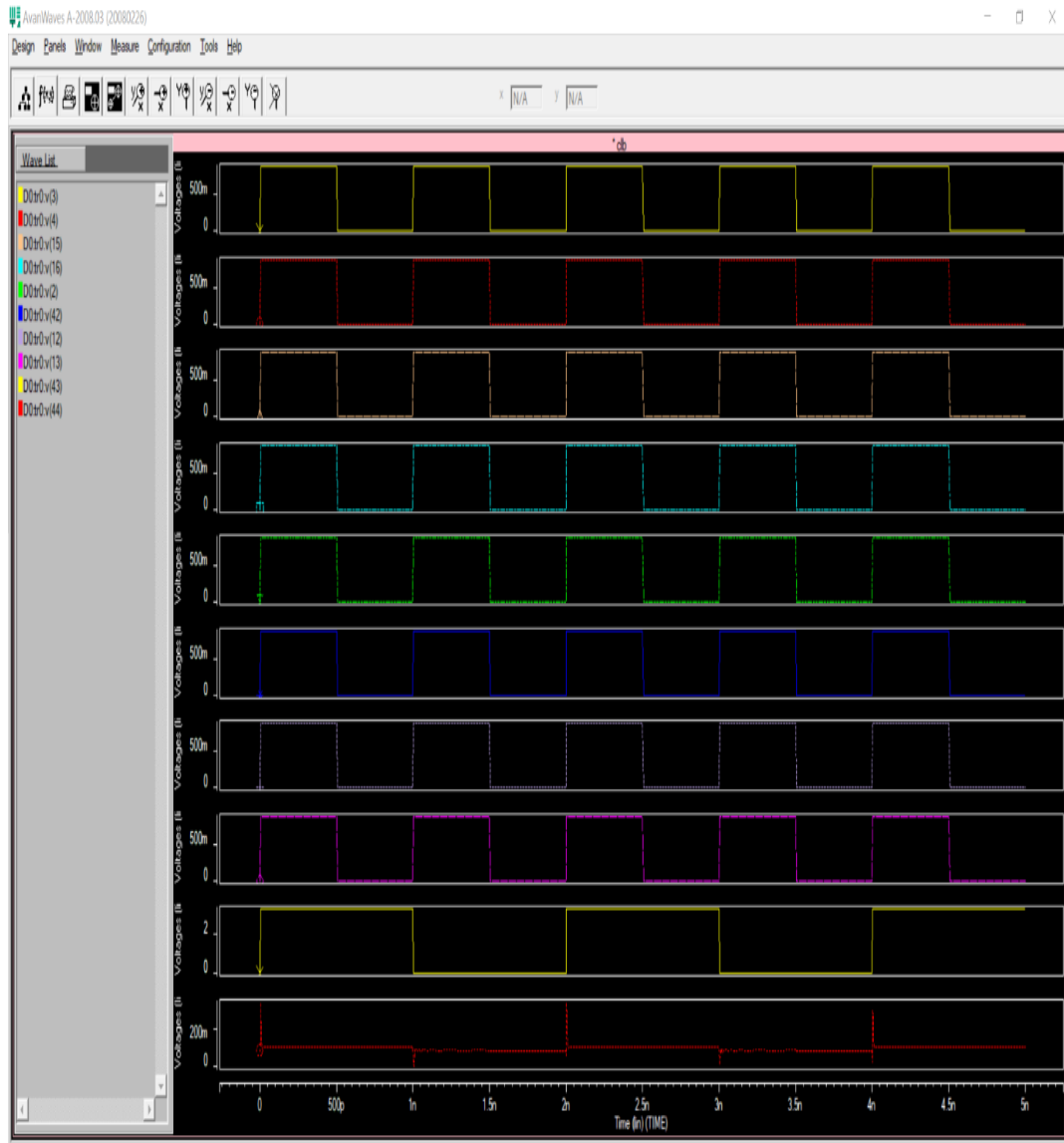


Figure 5.2 Simulation output of a CLB 32nm without sleep.

Figure 5.2 shows the simulation output of a CLB 32nm without sleep shows, the inputs given were v (3), v (4), v (15), v (16) and selection lines given were v (2), v (42), v (12), v (13) and CLK signal given was v (43) and the output is taken by v (44).

5.1.3 Simulation results for 32nm CLB with P-HALF sleep



Figure 5.3 Simulation output of a CLB 32nm with P-HALF SLEEP.

Figure 5.3 shows the simulation output of a CLB 32nm with P-HALF SLEEP, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (40) and the output is taken by v (38).

5.1.4 Simulation results for 32nm CLB with N-HALF sleep

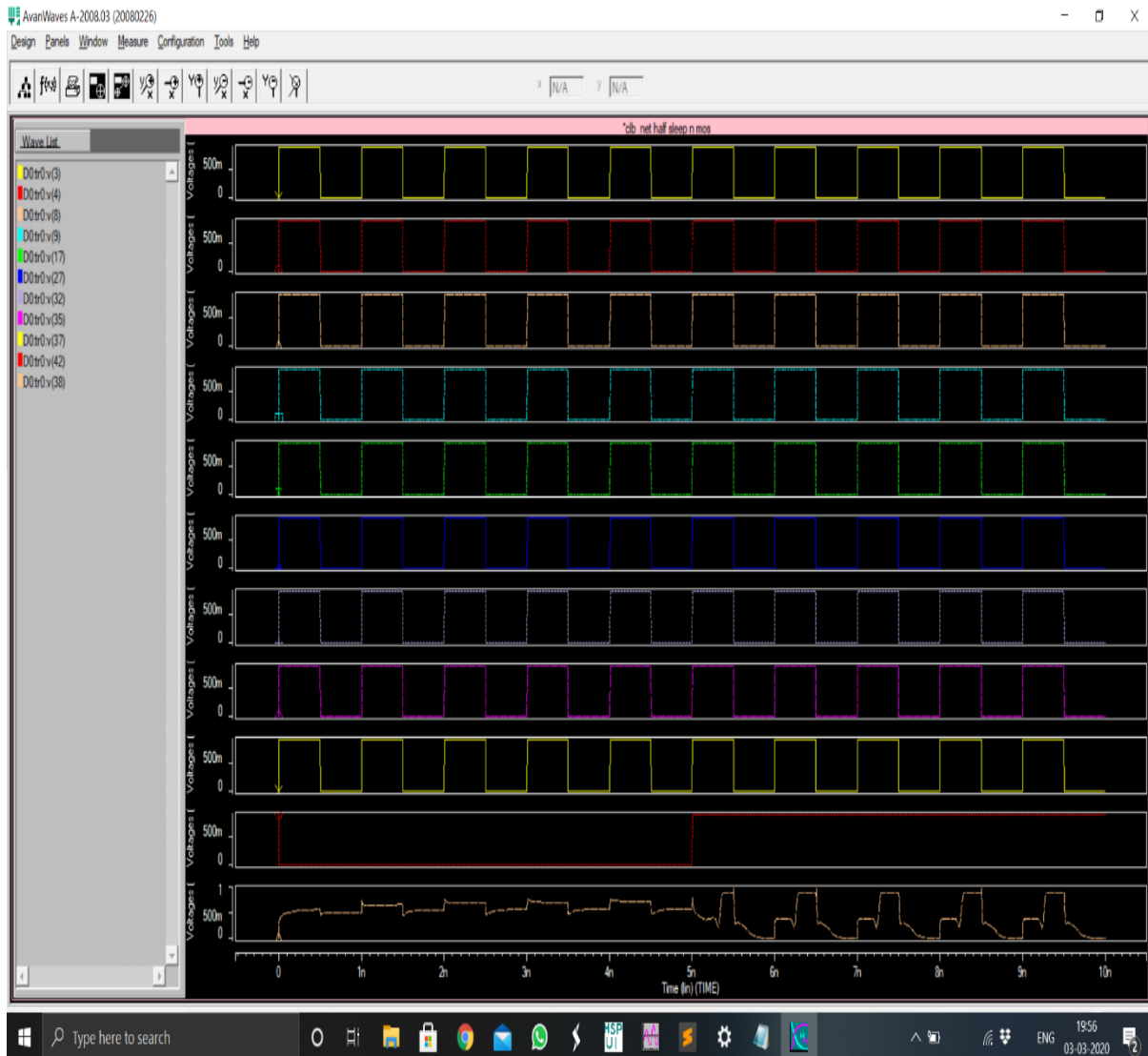


Figure 5.4 Simulation output of a CLB 32nm with N-HALF sleep.

Figure 5.4 shows the simulation output of a CLB 32nm with N-HALF sleep, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (42) and the output is taken by v (38).

5.1.5 Simulation results for 32nm CLB with full sleep

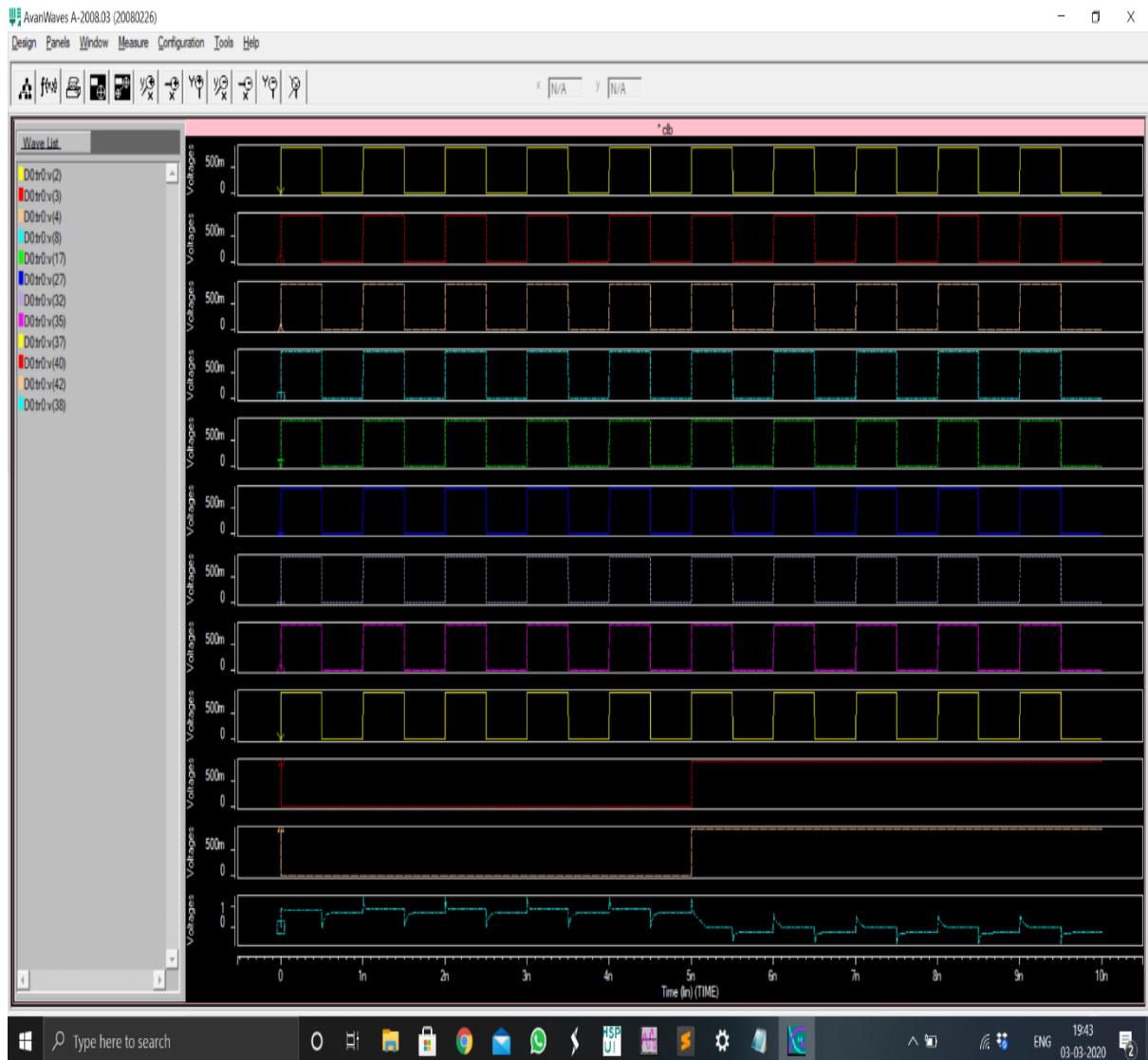


Figure 5.5 Simulation output of a CLB 32nm with sleep.

Figure 5.5 shows the simulation output of a CLB 32nm with sleep, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (40), v (42) and the output is taken by v (38).

5.2 Simulation results for CNFET technology

5.2.1 Simulation results for 32nm CLB without sleep signal

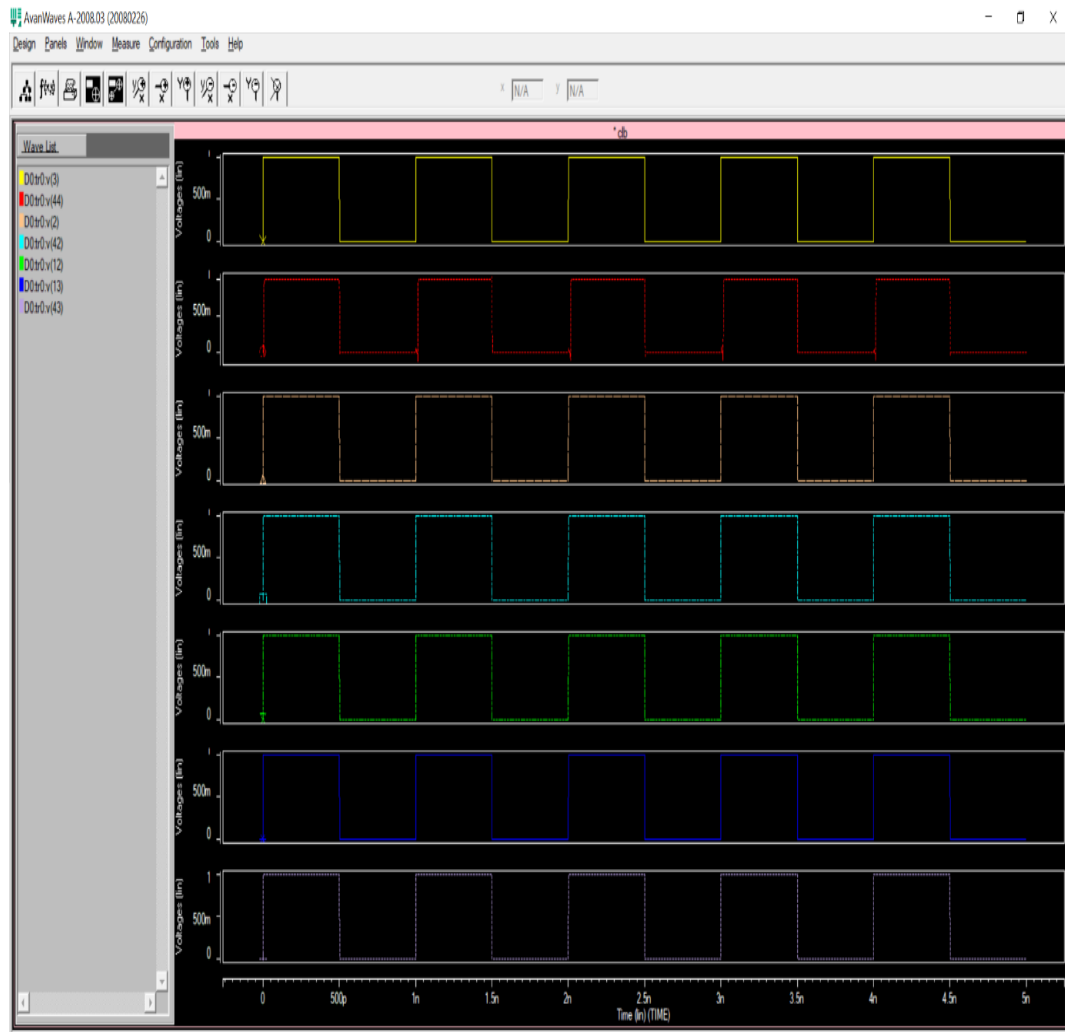


Figure 5.6 Simulation output of a CLB 32nm without sleep.

Figure 5.6 shows the simulation output of a CLB 32nm without sleep, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (40), v (42) and the output is taken by v (38).

5.2.2 Simulation results for 32nm CLB with P-HALF sleep

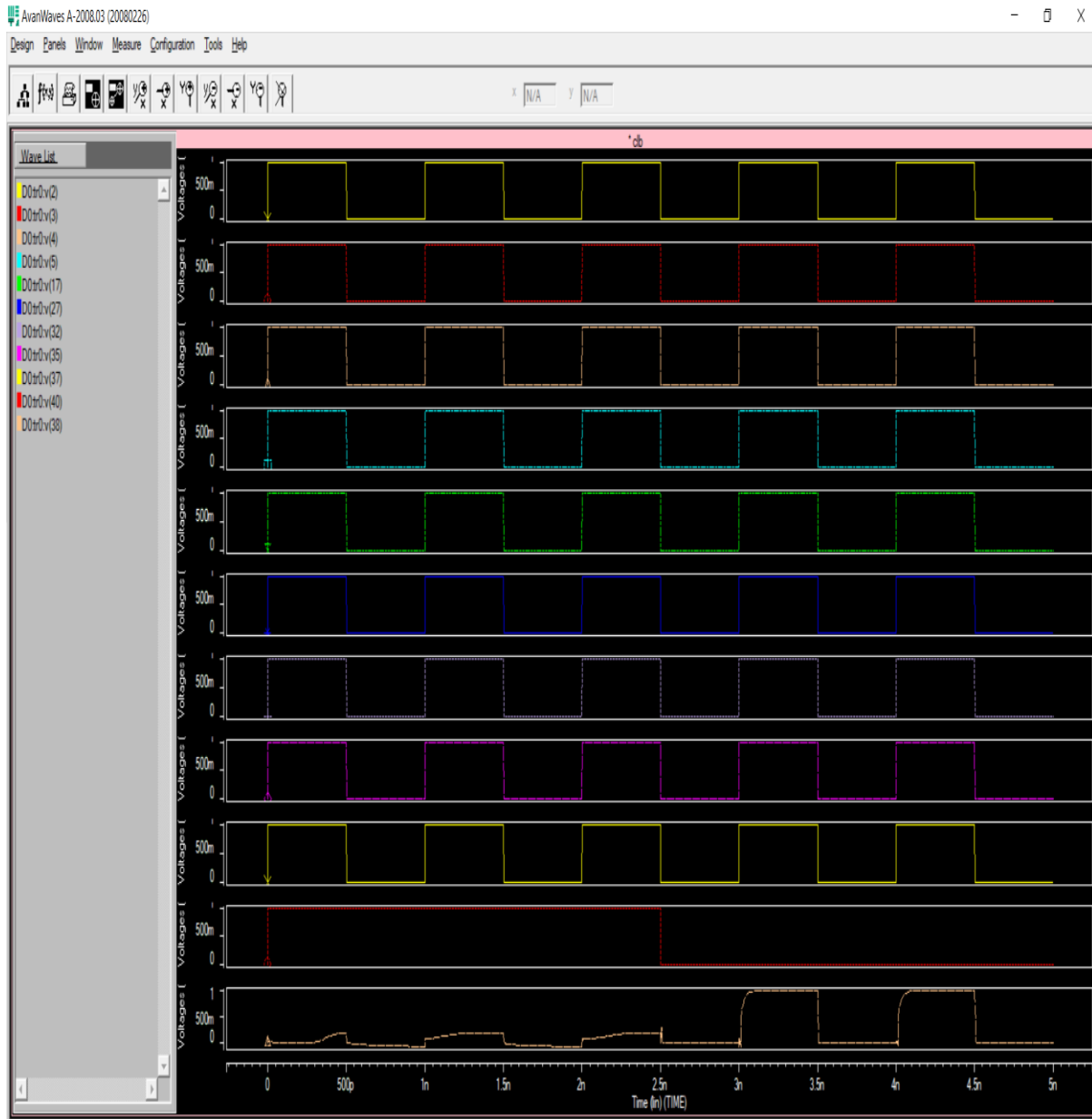


Figure 5.7 Simulation output of a CLB 32nm with P-HALF sleep.

Figure 5.7 shows the simulation output of a CLB 32nm with P-HALF sleep, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (40) and the output is taken by v (38).

5.2.3 Simulation results for 32nm CLB with N-HALF sleep

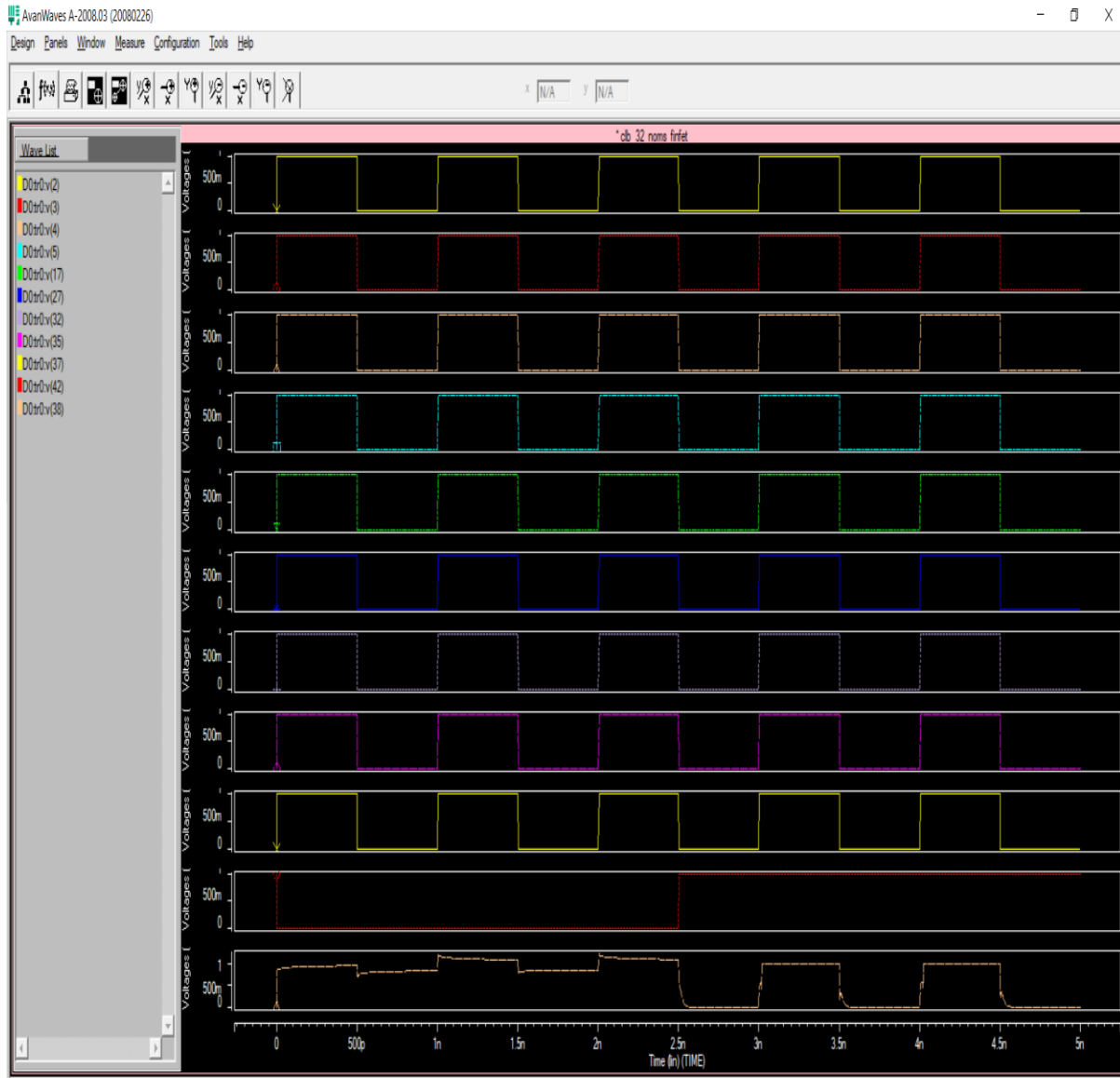


Figure 5.8 Simulation output of a CLB 32nm with N-HALF sleep.

Figure 5.7 shows the simulation output of a CLB 32nm with P-HALF sleep, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (42) and the output is taken by v (38).

5.2.4 Simulation results for 32nm CLB with FULL sleep

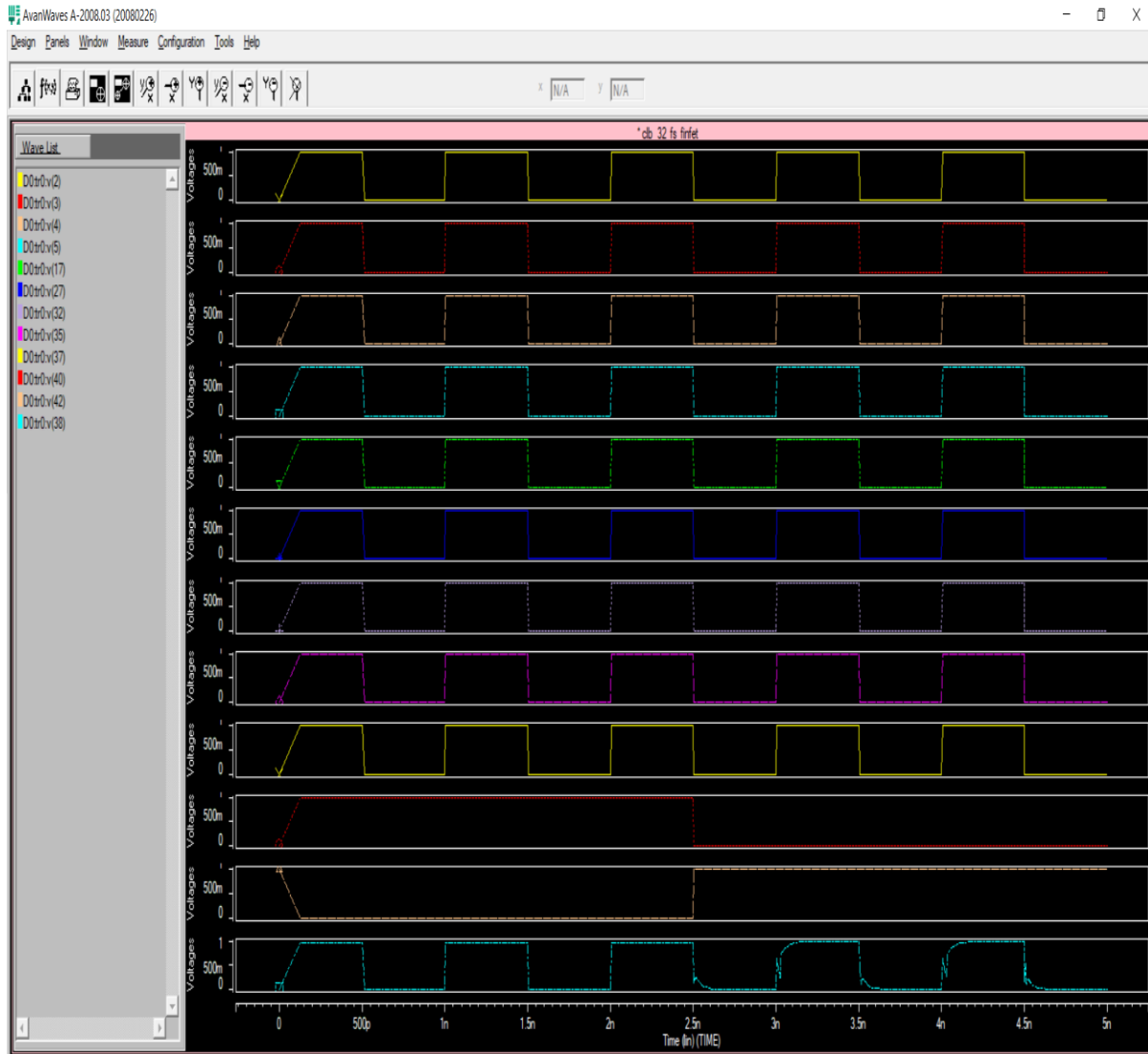


Figure 5.9 Simulation output of a CLB 32nm with sleep.

Figure 5.2.4 shows the simulation output of a CLB 32nm with sleep, the inputs given were v (2), v (3), v (4), v (5) and selection lines given were v (17), v (27), v (32), v (35) and CLK signal given was v (37) and the sleep signal given was v (40), v (42) and the output is taken by v (38).

5.3 PERFORMANCE ANALYSIS (MOSFET)

The performance analysis of Multiplexer, D flip flop, CLB in terms of power, delay and PDP.

5.3.1 POWER ANALYSIS OF DFF, MUX AND CLB 130nm without sleep

From the Table 5.1 the power from existing work.

Table 5.1: Design analysis of DFF, MUX AND CLB 130nm without sleep

Components	Power (w)	Delay (sec)	PDP (J)
2:1 Multiplexer	6.167 e^{-5}	57.131 e^{-12}	352.32 e^{-17}
D flip flop	7.898 e^{-5}	63.243 e^{-12}	499.49 e^{-17}
Configurable logic block	1.215 e^{-3}	103.4 e^{-12}	5.67 e^{-15}

5.3.2 POWER ANALYSIS OF DFF, MUX AND CLB 32nm without sleep

From the Table 5.2 the power from existing work.

Table 5.2: Design analysis of DFF, MUX AND CLB 32nm without sleep

Components	Power (W)	Delay (sec)	PDP (J)
2:1 Multiplexer	1.25 e^{-6}	48.257 e^{-12}	60.8 e^{-18}
D flip flop	1.414 e^{-6}	41.64 e^{-12}	59.70 e^{-18}
Configurable logic block	0.3308 e^{-4}	683.73 e^{-15}	226.17 e^{-19}

5.3.3 POWER ANALYSIS OF DFF, MUX AND CLB 32nm with P-HALF sleep

From the Table 5.3 the power from proposed work.

Table 5.3: Design analysis of DFF, MUX AND CLB 32nm with P-HALF sleep

Components	Power (W)	Delay (sec)	PDP (J)
2:1 Multiplexer	1.596 e^{-6}	10.736 e^{-12}	17.13 e^{-18}
D flip flop	1.327 e^{-6}	3.9503 e^{-12}	5.24 e^{-18}
Configurable logic block	1.652 e^{-5}	32.047 e^{-12}	52.94 e^{-17}

5.3.4 POWER ANALYSIS OF DFF, MUX AND CLB 32nm with N-HALF sleep

From the Table 5.4 the power from proposed work.

Table 5.4: Design analysis of DFF, MUX AND CLB 32nm with N-HALF sleep

Components	Power (W)	Delay (sec)	PDP (J)
2:1 Multiplexer	6.534 e^{-7}	6.5826 e^{-12}	43.01 e^{-19}
D flip flop	2.574 e^{-8}	1.3754 e^{-12}	3.54 e^{-20}
Configurable logic block	3.133 e^{-7}	11.022 e^{-12}	34.53 e^{-19}

5.3.5 POWER ANALYSIS OF DFF, MUX AND CLB 32nm with full sleep

From the Table 5.5 the power from proposed work.

Table 5.5: Design analysis of DFF, MUX AND CLB 32nm with full sleep

Components	Power (W)	Delay (sec)	PDP (J)
2:1 Multiplexer	9.217 e^{-7}	17.36 e^{-12}	160.00 e^{-19}
D flip flop	2.944 e^{-7}	639.85 e^{-15}	1883.71 e^{-22}
Configurable logic block	2.7 e^{-6}	16.115 e^{-15}	3.51 e^{-21}

5.4 PERFORMANCE ANALYSIS (CNTFET)

The performance analysis of Multiplexer, D flip flop, CLB in terms of power, delay and PDP.

5.4.1 POWER ANALYSIS OF DFF, MUX AND CLB 32nm without sleep

From the Table 5.6 the power from existing work.

Table 5.6: Design analysis of DFF, MUX AND CLB 32nm without sleep

Components	Power (W)	Delay (sec)	PDP (J)
2:1 Multiplexer	2.555 e^{-7}	81.36 e^{-15}	207.48 e^{-22}
D Flip Flop	2.417 e^{-7}	$2.77.06 \text{ e}^{-15}$	669.65 e^{-22}
Configurable Logic Block	5.430 e^{-6}	818.19 e^{-15}	4442.77 e^{-22}

5.4.2 POWER ANALYSIS OF DFF, MUX AND CLB 32nm P-HALF sleep

From the Table 5.7 the power from proposed work.

Table 5.7: Design analysis of DFF, MUX AND CLB 32nm P-HALF sleep

Components	Power(W)	Delay(sec)	PDP(J)
2:1 Multiplexer	5.889 e^{-7}	10.736 e^{-12}	$63224.304 \text{ e}^{-19}$
D Flip Flop	6.536 e^{-7}	3.9503 e^{-12}	25.81 e^{-19}
Configurable Logic Block	5.345 e^{-6}	32.47 e^{-13}	17.219 e^{-19}

5.4.3 POWER ANALYSIS OF DFF, MUX AND CLB 32nm N-HALF sleep

From the Table 5.8 the power from proposed work.

Table 5.8: Design analysis of DFF, MUX AND CLB 32nm N-HALF sleep

Components	Power(W)	Delay(sec)	PDP(J)
2:1 Multiplexer	6.088 e^{-7}	244.56 e^{-15}	1488.88 e^{-21}
D Flip Flop	7.065 e^{-7}	745.25 e^{-15}	5265.19 e^{-21}
Configurable Logic Block	2.457 e^{-6}	676.24 e^{-15}	1661.52 e^{-21}

5.4.4 POWER ANALYSIS OF DFF, MUX AND CLB 32nm FULL sleep

From the Table 5.9 the power from proposed work.

Table 5.9: Design analysis of DFF, MUX AND CLB 32nm FULL sleep

Components	Power(W)	Delay(sec)	PDP(J)
2:1 Multiplexer	9.485 e^{-8}	2.5708 e^{-12}	24.38 e^{-20}
D Flip Flop	9.428 e^{-8}	3.5312 e^{-12}	33.19 e^{-20}
Configurable Logic Block	1.856 e^{-6}	2.8283 e^{-15}	5.249 e^{-19}

5.5 PERFORMANCE ANALYSIS OF EXISTING WORK AND PROPOSED WORK

From the Table 5.10 the Power from existing to the proposed one.

Table 5.10 Design Analysis of Proposed CLB (MOSFET)

Components	Power with 130nm technology without sleep technology (W)	Power with 32nm technology without sleep technology (W)	Power with 32nm technology with full sleep technology (W)
2:1 Multiplexer	6.167×10^{-5}	1.25×10^{-6}	9.217×10^{-7}
D flip flop	7.898×10^{-5}	1.414×10^{-6}	2.944×10^{-7}
Configurable logic block	1.215×10^{-3}	0.3308×10^{-4}	2.7×10^{-6}

From the above table 5.10 we have the comparison between the power obtained when sleep signals are given and when the sleep signal is not given for 32nm technology. From the table we can conclude that power consumed by the circuit is less when the sleep technique is applied and when the sleep technique is not applied.

From the Table 5.11 the Power from existing to the proposed one.

Table 5.11 Design Analysis of Proposed CLB (CNTFET)

Components	Power with 32nm technology without sleep technology (W)	Power with 32nm technology with full sleep technology (W)
2:1 Multiplexer	2.555 e^{-7}	9.485 e^{-8}
D Flip Flop	2.417 e^{-7}	9.428 e^{-8}
Configurable Logic Block	5.430 e^{-6}	1.856 e^{-6}

From the above table 5.11 we have the comparison between the power obtained when sleep signals are given and when the sleep signal is not given for 32nm technology. From the table we can conclude that power consumed by the circuit is less when the sleep technique is applied and when the sleep technique is not applied

CHAPTER 6

CONCLUSION

Various Configurable Logic Block (CLB) architecture were analysed in terms of power and delay and PDP of various CLB architecture by modifying the existing architecture. We compared the results on both existing and proposed CLB using 130nm, 32nm MOSFET and CNTFET technology in terms of power.

The power consumed by the existing architecture of CLB by applying 32nm MOSFET technology is 0.3308×10^{-4} W. The power consumed by the proposed architecture of CLB by applying 32nm MOSFET technology is 2.7×10^{-6} W.

The power consumed by the existing architecture of CLB by applying 32nm CNTFET technology is 5.430×10^{-6} W. The power consumed by the proposed architecture of CLB by applying 32nm CNTFET technology is 1.856×10^{-6} W.

From the analysis of both MOSFET and CNTFET technologies we concluded that CNTFET technology applied architecture CLB has more Power efficiency than MOSFET technology applied architecture CLB.

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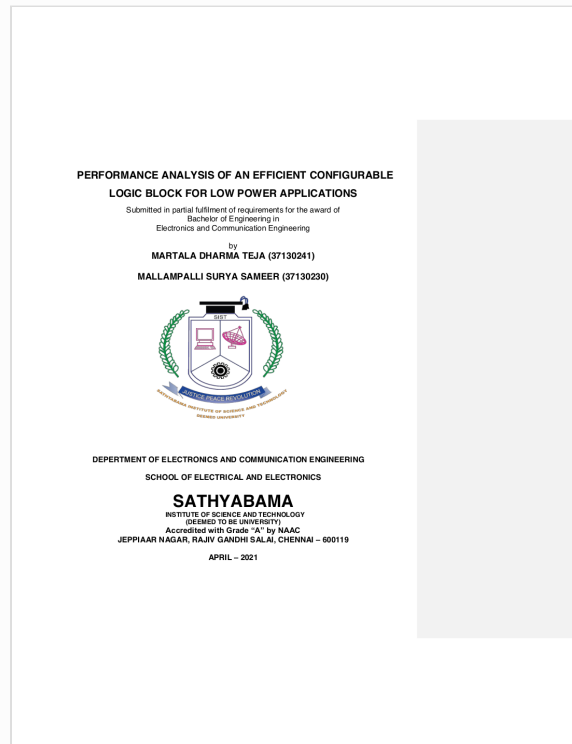


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