

REPORT ON PCB DESIGN

Bachelor of
Engineering Degree in Electrical and Ele
ctronics Engineering

By
SUJOY HALDER (39140058)



DEPARTMENT OF ELECTRICAL AND ELECTRONICS
SCHOOL OF ELECTRICAL AND ELECTRONICS
SATHYABAMA INSTITUTE OF SCIENCE AND TECHNOLOGY
PEEPA NAGAR, RAJIV GANDHI SALAI,
CHENNAI - 600119, TAMIL NADU.

SEPTEMBER-2021



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)

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Ref:SHD/2021/06/28/R3

28June2021

TOWHOMSOEVERITMAYCONCERN

Thisistocertifythat**Mr.SUJOYHALDER**,RegisterNumber**39140058**isaBonafidestudentofourInstitutionpursuing**BACHELOROFENGINEERING**in**ELECTRICALELANDELECTRONICSENGINEERING**duringtheacademicyear**2020-2021**.Hewillbecompletingthecourseintheyear**2023**.

Thiscertificateisissuedfor thepurposeof **Applying**
INTERNSHIP.

DEAN (STUDENT AFFAIRS)
Dr. G. SUNDARI, M.E., Ph.D.,
DEAN (STUDENT AFFAIRS)
SATHYABAMA
INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)
Jeppiaar Nagar, Rajiv Gandhi Salai
Chennai - 600 119.

ACKNOWLEDGEMENT

The satisfaction and elation that accompany the successful completion of any task would be incomplete without the mention of the people who have made it possible. It is our great privilege to express our gratitude and respect to all those who have guided me during the course of my Professional Training.

First and foremost, we would express our sincere gratitude to our beloved Founder Chancellor **Col. Dr. JEPPIAAR, M.A., B.L., Ph.D.**, and Chancellor **Dr. Mariazeena Johnson, B.E., M.B.A., M.Phil., Ph.D.**, I extend my sincere thanks to our President **Dr. Marie Johnson, B.E., M.B.A., M.Phil., Ph.D.**, and for providing me the necessary facilities for the completion of the professional training. I also acknowledge our Vice Chancellor **Dr. T. Sasiprabha, M.E., Ph.D.**, and the Pro Vice Chancellor **Dr. E. Logashanmugam, M.E., Ph.D.**, the Pro Vice Chancellor **Dr. Wilson Aruni Ph.D., FAMPV**, for their constant support and endorsement.

I would like to express our gratitude to our Registrar **Dr. S. S. Rao, MBA, Ph.D.** and Controller of Examinations **Dr. Igni Sabasti Prabu M.E., Ph.D.**, for their valuable support offered to complete my professional training successfully.

I like to express our gratitude to **Dr. V. Sivachidambaramanathan M.E., Ph.D.**, Head of the Department of Electrical and Electronics Engineering, Sathyabama Institute of Science and Technology for having been a constant source of support and encouragement for the completion of the professional training.

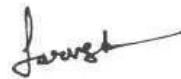
I would also like to express our sincere thanks to our internal guide who guided me in the preparation of the report.

Also, I thank the **Almighty** and my **Parents** for supporting me in the completion of the professional

Certificate of Training

Sujoy Halder

from Sathyabama Institute Of Science And Technology, has successfully completed a eight weeks online training on PCB Design. The training consisted of Introduction to Autodesk Eagle, Project 1 – ASTABLE 555 Timer, Warnings and Layers, Project 2 – Shift Register 74595 LED Controller, Special and Miscellaneous Topics, Case Study and Final Project modules. In the final assessment, Sujoy scored 51% marks. We wish Sujoy all the best for the future endeavours.



Sarvesh Agarwal

FOUNDER & CEO, INTERNSHALA

Date of certification: 2021-08-03

Certificate no.: C1AB6E6E-64A0-BDD7-DD24-

90BFF7F7921E For certificate authentication, please visit https://trainings.internshala.com/verify_certificate

Abstract

All bachelor degree students are required to undergo industrial training for eight months as a part of curriculum to complete their 4 year course for bachelor of electronics and communication engineering.

For my industrial training I did at **INTERNSHALA TRAINING**

I was assigned to the quality section. My Supervisor name was **“Mr. Mohannad Rawashdeh”** who gave me knowledge about how to design and modify the PCB either it is single sided or double sided PCBs. I learnt a lot of basic procedures of manufacturing of PCBs in production section.

Contents

Electronics component:

- ***Resistor***
- ***Capacitor***
- ***Transformer***
- ***IC 555***
- ***Diode***
- ***Single stand wire***
- ***IC 78XX***
- ***IC 79XX***
- ***TRANSISTOR***
- ***LED***

Apparatus:

- ***Breadboard***
- ***CRO***
- ***Multi-meter***
- ***Cutter***
- ***Power supply***

AC to DC converter:

- ***Rectifier***

Projects:

- ***Timer using IC555***
- ***Positive and Negative power supply***
- ***7 Segments Display***
- ***NOT Gate using Transistor(n-p-n)***
- ***PCB (Printed Circuit Board)***

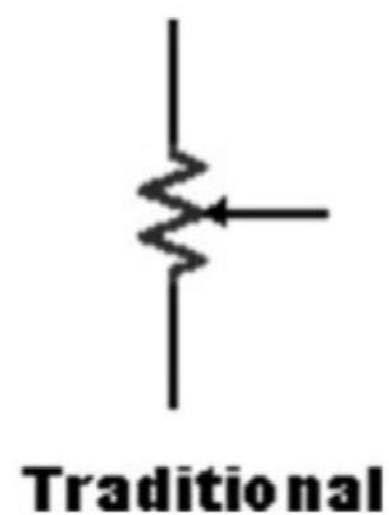
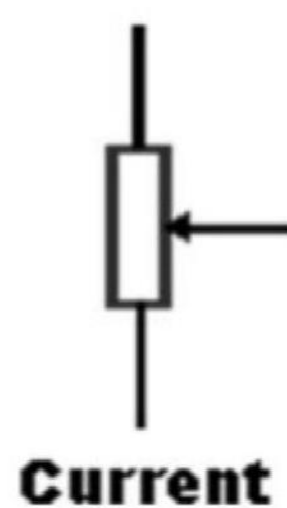
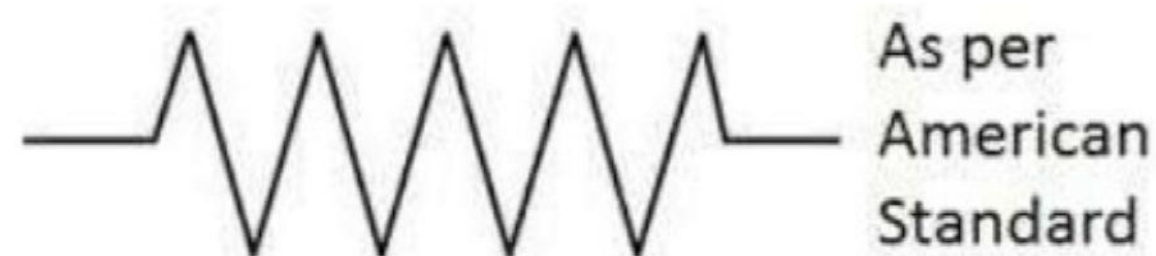
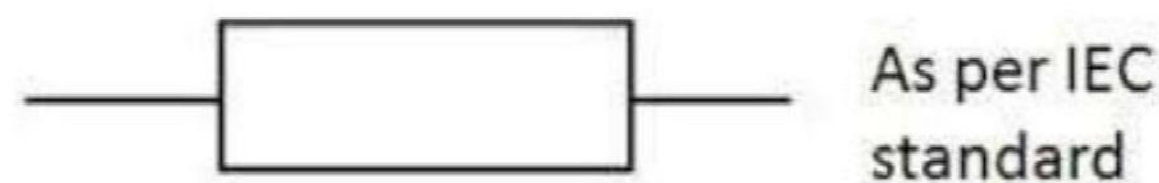
ELECTRONICS COMPONENT

RESISTOR: *A resistor is a passive two-terminal electrical component that implements electrical resistance as a circuit element. In electronic circuits, resistors are used to reduce current flow.*

Types of Resistor

- *Carbon Composition Resistor – Made of carbon dust or graphite paste, low wattage values*
- *Film or Cermet Resistor – Made from conductive metal oxide paste, very low wattage values*
- *Wire-wound Resistor – Metallic bodies for heatsink mounting, very high wattage ratings*
- *Semiconductor Resistor – High frequency/precision surface mount thin film technology*

Symbol of Resistor



Example of Resistor



Resistors

Nowdays Resistors very small in size known as Embedded Resistors are used in electronics.

Embedded Resistors:

Resistors can be embedded in PCBs either by use of special layers laminated. Those types of Resistors are known as Embedded Resistors.

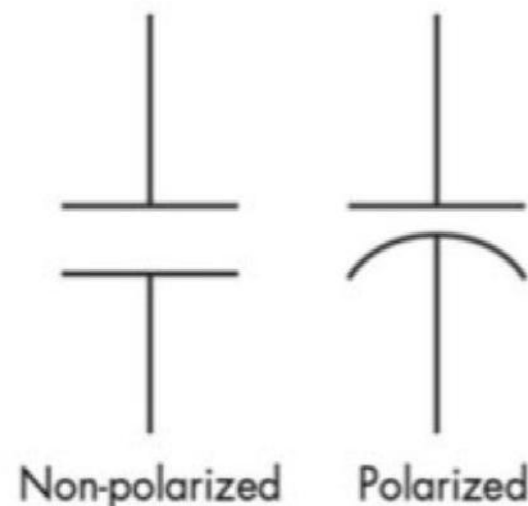
Example:



Embedded Resistor

CAPACITOR: *A capacitor is a passive two-terminal electrical component that stores electrical energy in an electric field. The effect of a capacitor is known as capacitance.*

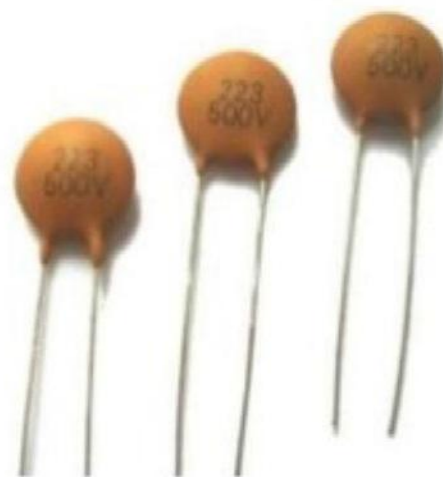
Symbol:



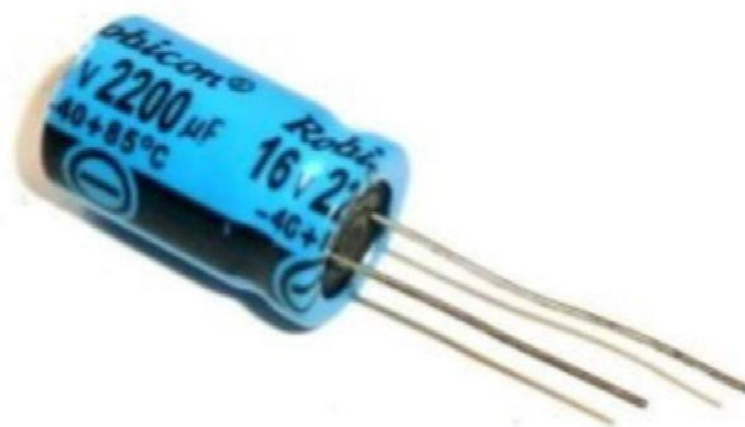
Types of Capacitors:

- *Ceramic capacitor*
- *Electrolytic capacitor*

CERAMIC CAPACITORS: *This type of capacitors are non-bised. So we can use any terminal as positive or negative terminal. This is also known as paper capacitor.*



ELECTROLYTIC CAPACITOR: *This type of capacitor that is polarised. So there is a positive and a negative terminal.*

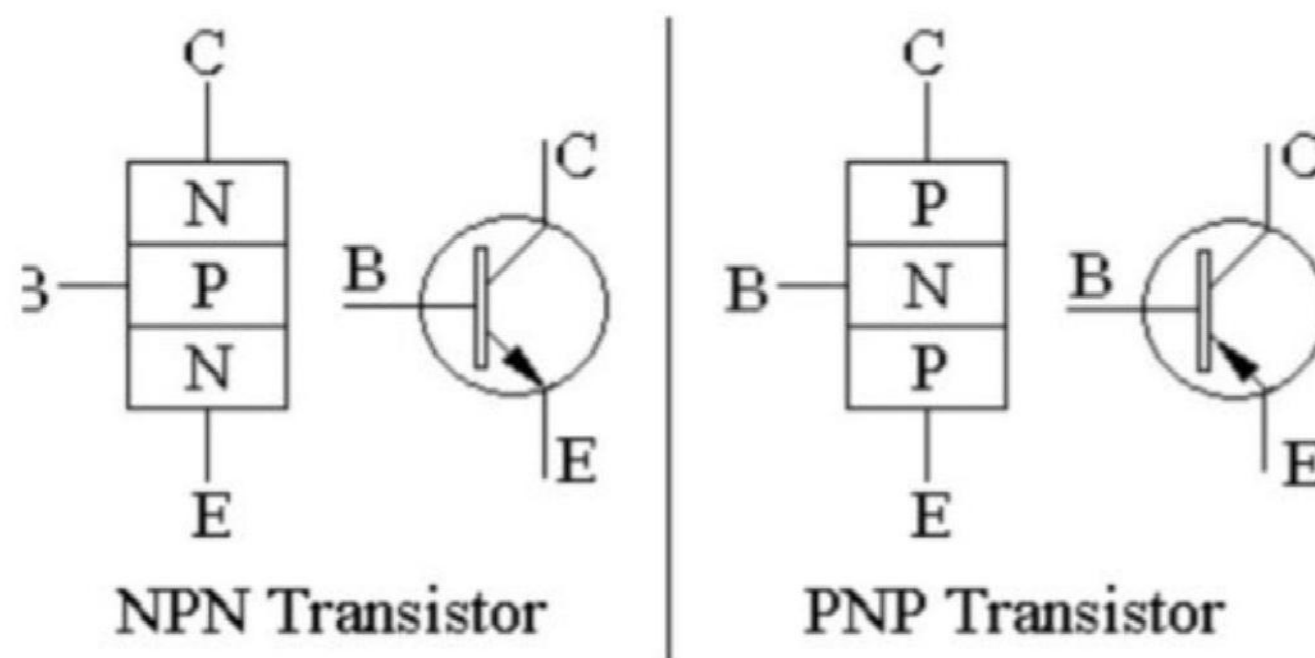


TRANSISTOR: Transistor is a 3 terminal semi-conductor device.
The terminals are base, emitter and collector.

Types:

- ❖ *p-n-p Transistor*
- ❖ *n-p-n Transistor*

Symbol

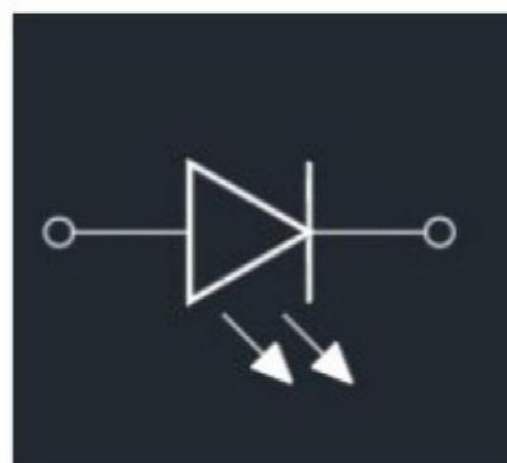


Uses:

- *Use as switches in digital TTL circuits.*
- *Use in amplifier circuit.*
- *Use in oscillator circuit.*

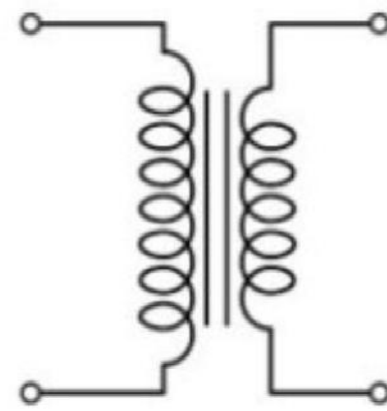
LED: Light emitting diode, whenever forward current pass through diode it emits light.

Symbol:



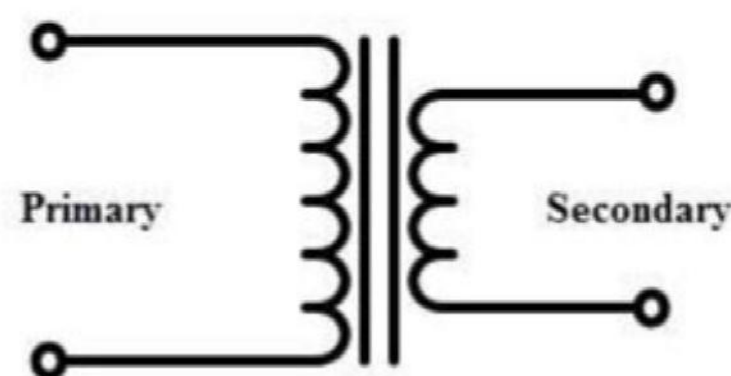
Transformer: A transformer is an electrical device that transfers electrical energy between two or more circuits through electromagnetic induction.

Symbol:



Types of Transformers:

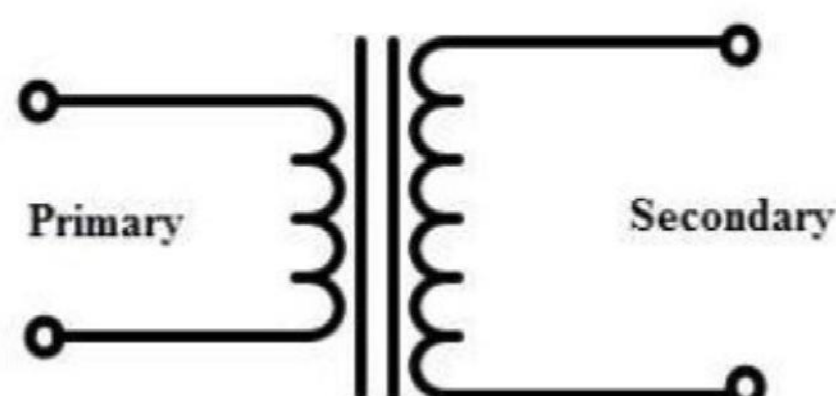
- ❖ **Step-down Transformers:-** In Step-down transformer secondary windings are fewer than the primary windings. So the transformer's secondary voltage is less than the primary voltage.



Step-down Transformer

- ❖ **Step-up Transformers:-**

The step-up transformer is the direct opposite of a step-down transformer. There are many turns on the secondary winding than in the primary winding in the step-up transformers. Thus, the voltage supplied in the secondary transformer is greater than the one supplied across the primary winding.

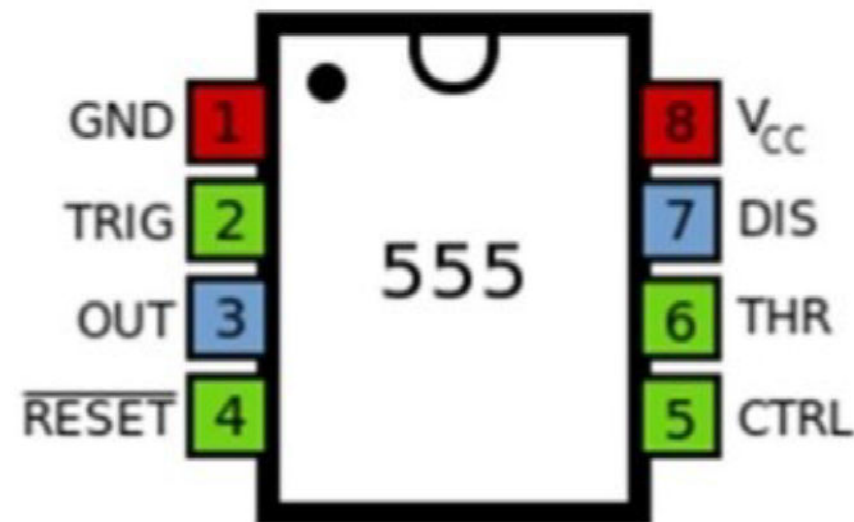


Step-up Transformer

555 TIMER:

The 555 timer IC is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications. It has 8 pins and can be operated within 5v to 15v range.

PIN DIAGRAM:



PIN DESCRIPTION:

PIN 1: Ground supply, ground reference voltage (zero volts).

PIN 2: Trigger, Output of the timer totally depends upon the amplitude of the external trigger voltage applied to this pin.

PIN 3: Output, the output of the pin is obtain in this pin.

PIN 4: Reset, this pin is used to reset the timer ic.

PIN 5: Control, this pin provides "control" access to the internal voltage divider.

PIN 6: Threshold

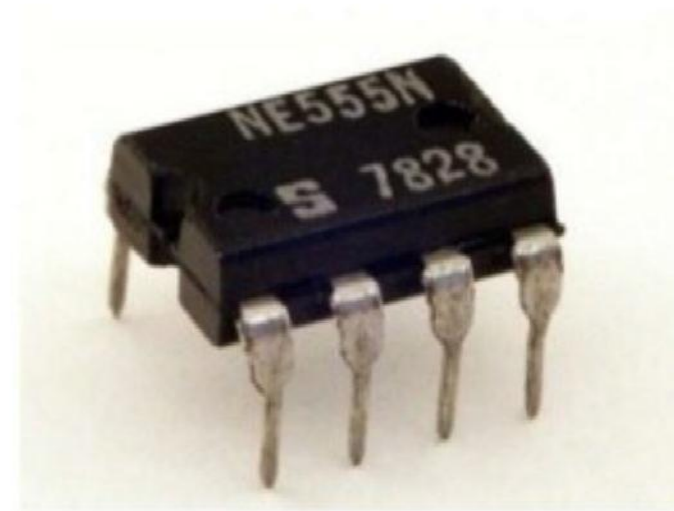
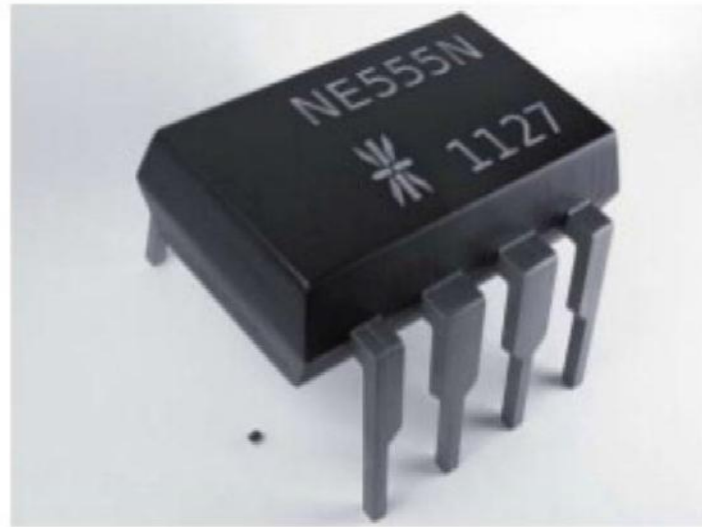
PIN 7: Discharge, open-collector output, which may discharge a capacitor between intervals.

PIN 8: Positive supply, the guaranteed voltage range of bipolar parts are typically 4.5 volt to 15 volts.

Use of 555 IC:

1. *It is used to build timer or ON-OFF pulse generator.*
2. *It is also used in multivibrator(astable,monostable,bistable).*

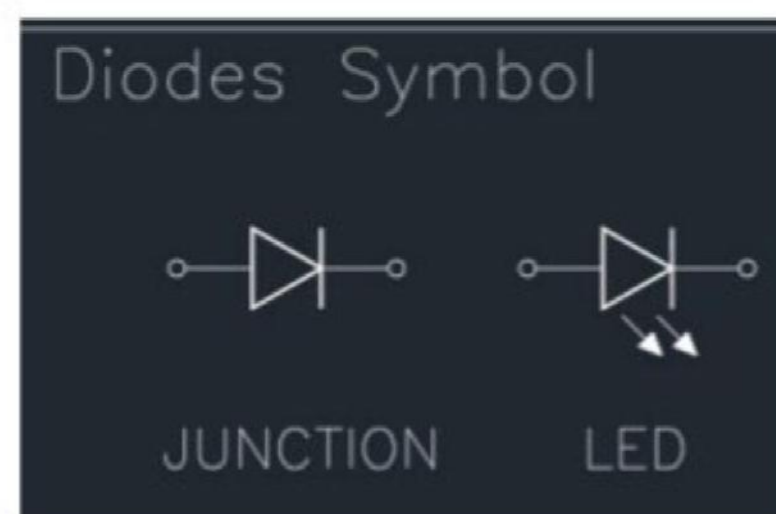
Example:



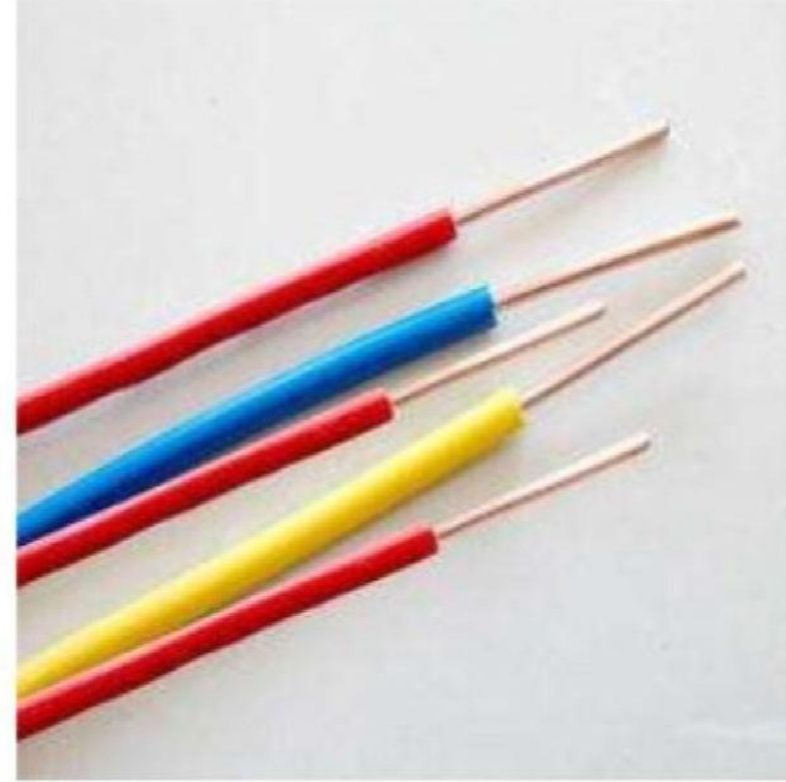
IC 555

DIODES: *Diode is 2 terminal semi-conductor devices, which allow to flow current in only one direction with low resistance.*

Symbol:

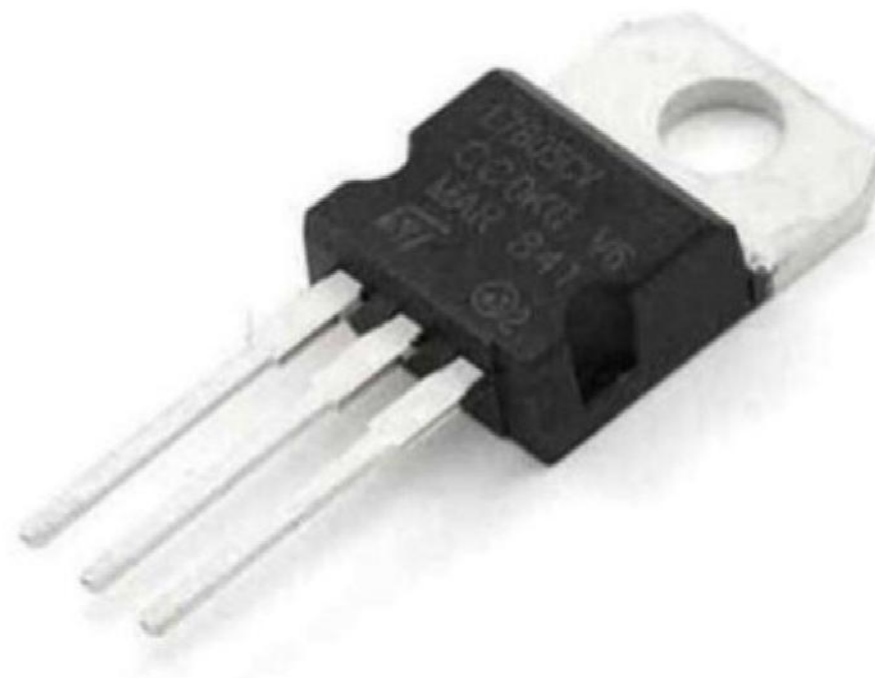


Single stand wire: *This wire consists of only one copper core. Which Used in electronics lab.*



IC 78XX & IC 79XX

IC 78XX: *IC 78XX is a family of self-contained fixed linear voltage regulator integrated circuits. The 78xx family is commonly used in electronic circuits requiring a regulated power supply due to their ease-of-use and low cost.*



IC 79XX: *IC 79XX is a family of self-contained fixed linear voltage regulator integrated circuits. IC 7905 output is 1A at 5V.*



AC TO DC CONVERTER

RECTIFIER

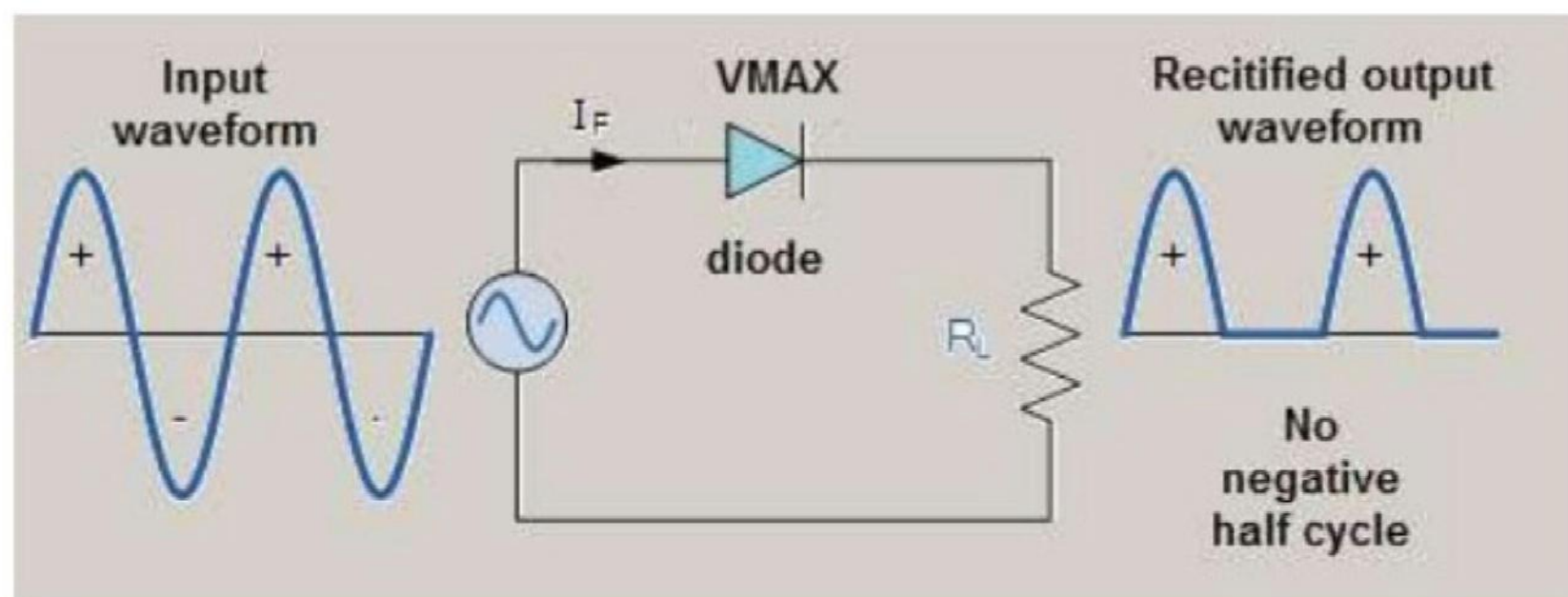
A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC).

Types of Rectifiers:

- *Half wave Rectifier*
- *Full wave Rectifier*

Half wave Rectifier:

The half wave rectifier is a circuit which converts AC signal to DC signal, but it convert only half cycle of a full wave signal so efficiency is very low.



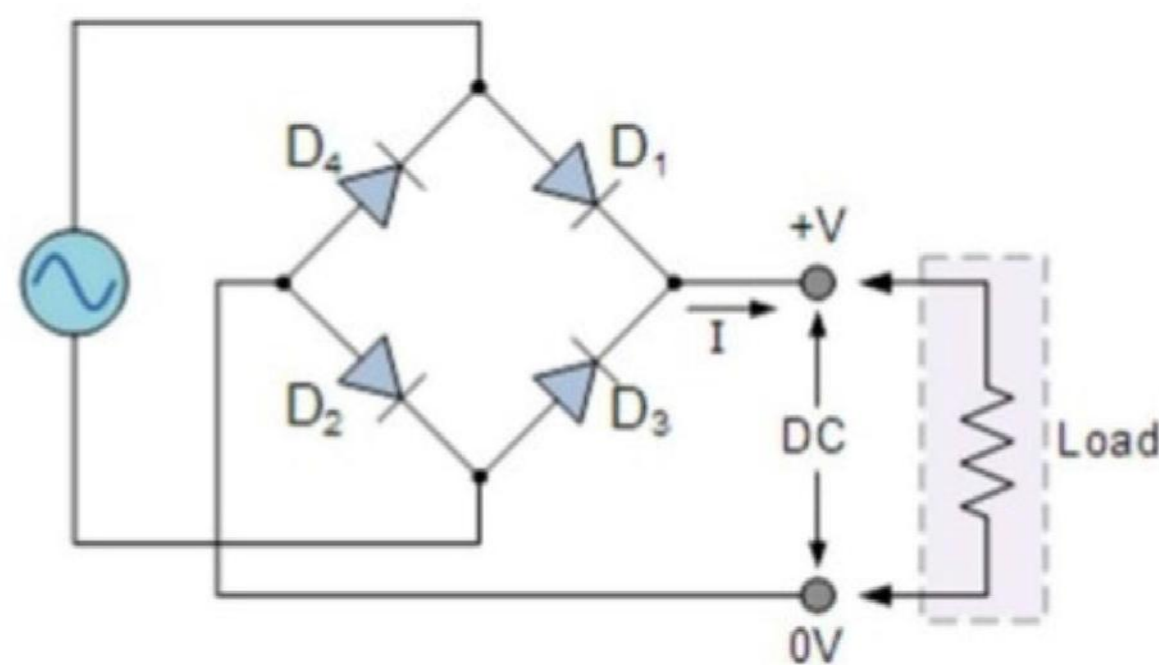
Full wave Rectifier:

Full wave rectifier is a circuit which converts AC signal to DC signal and it converts both negative and positive half cycle to DC, so its efficiency is high and it is commonly used in AC to DC converters.

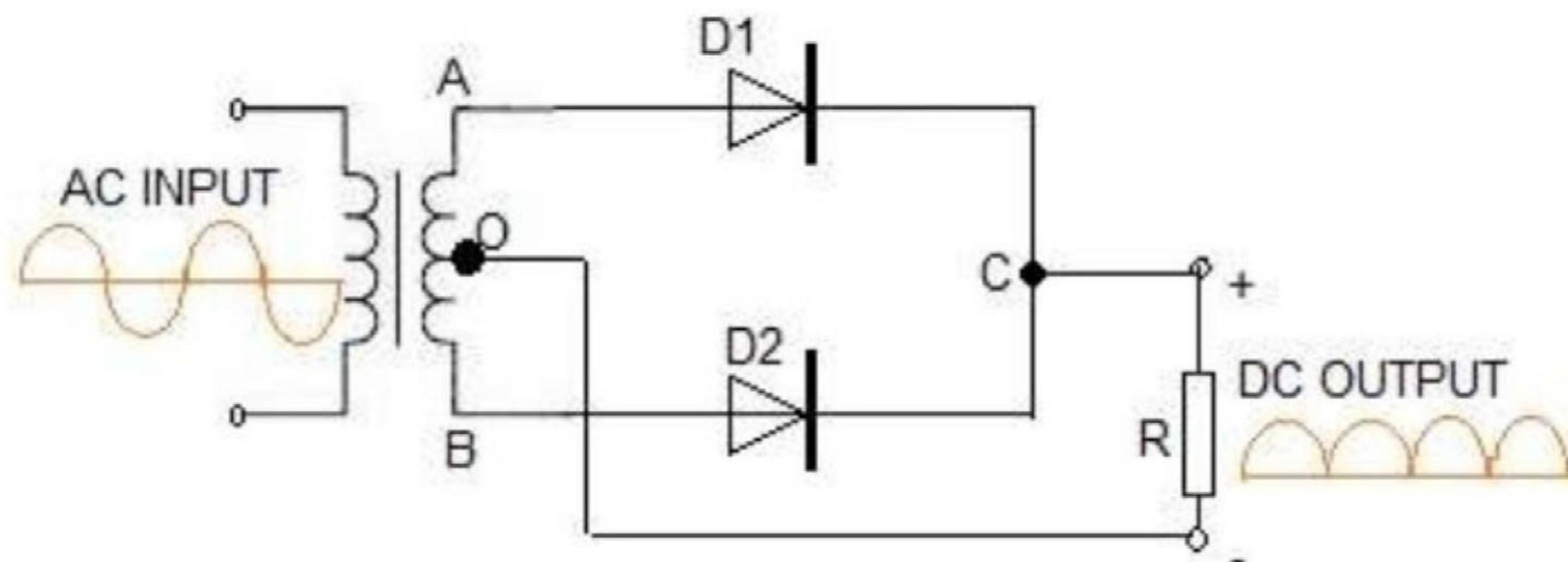
Now full wave rectifier is two types. Those are-

- ❖ *Bridge rectifier*
- ❖ *Center-tapped rectifier*

Bridge rectifier: A bridge rectifier is a full wave rectifier, it use 4 diode to rectify the full signal.



Center-tapped rectifier: A center-tapped rectifier is also a full wave rectifier, it use a center tapped transformer and 2 diodes to rectify the full signal.

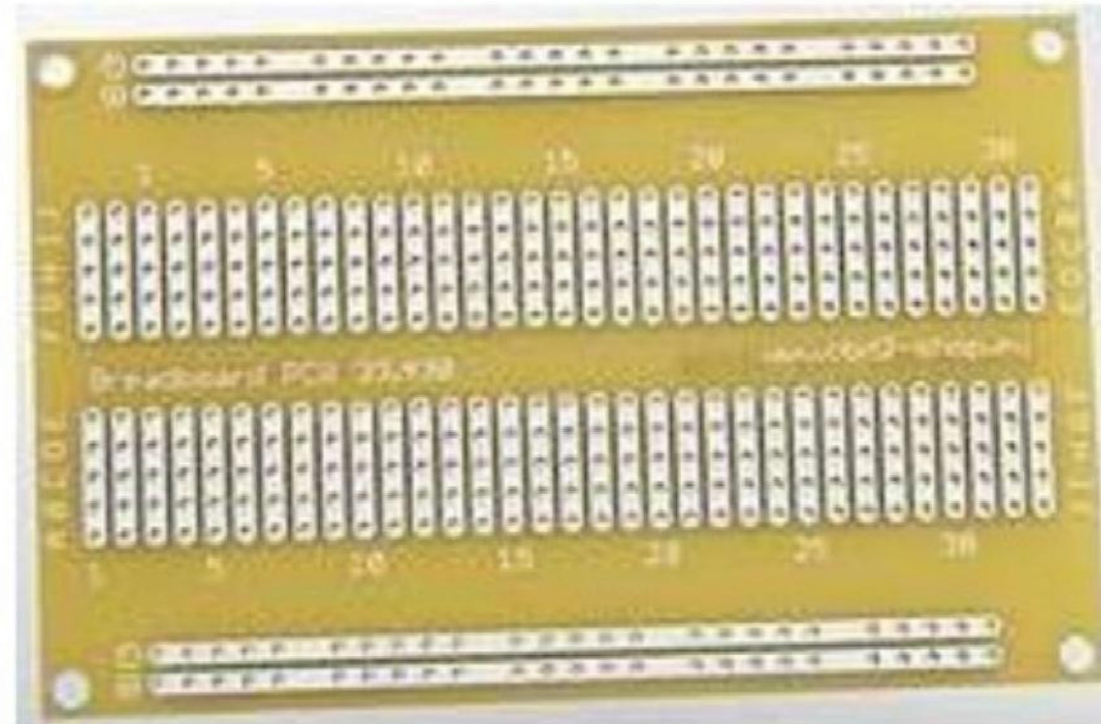


Full Wave rectifier (Centre tap)

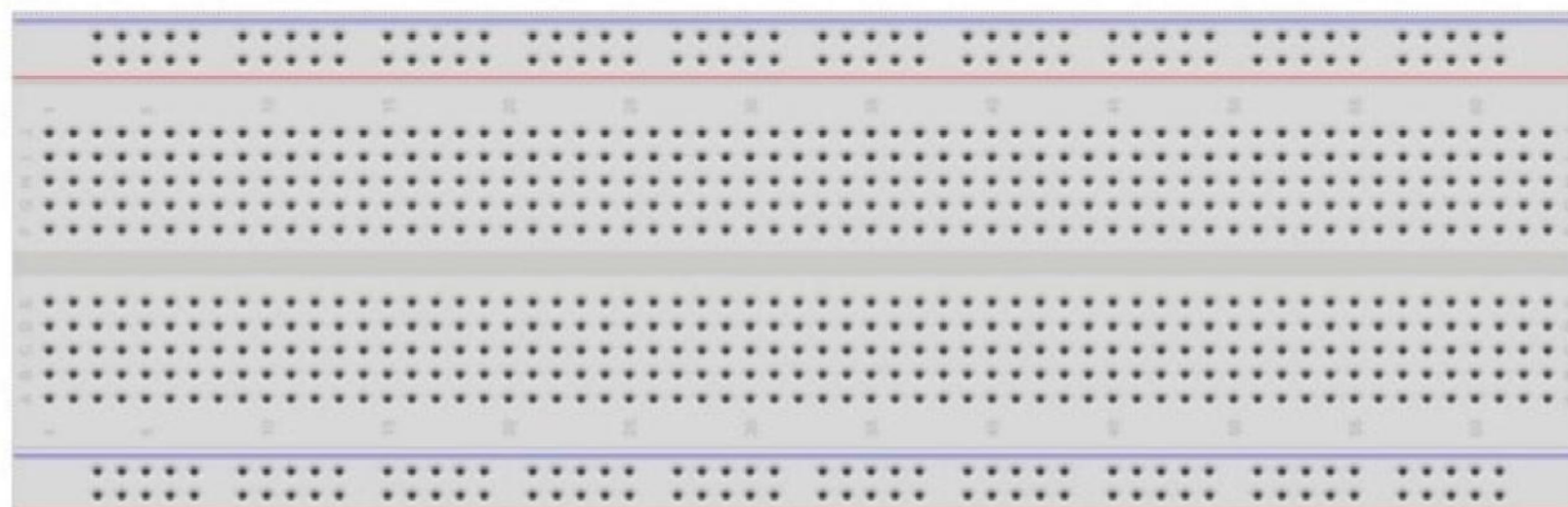
APPARATUS

BREAD BOARD: A breadboard is a construction base for prototyping electronics circuit. It does not need any soldering so it is very useful for circuit testing.

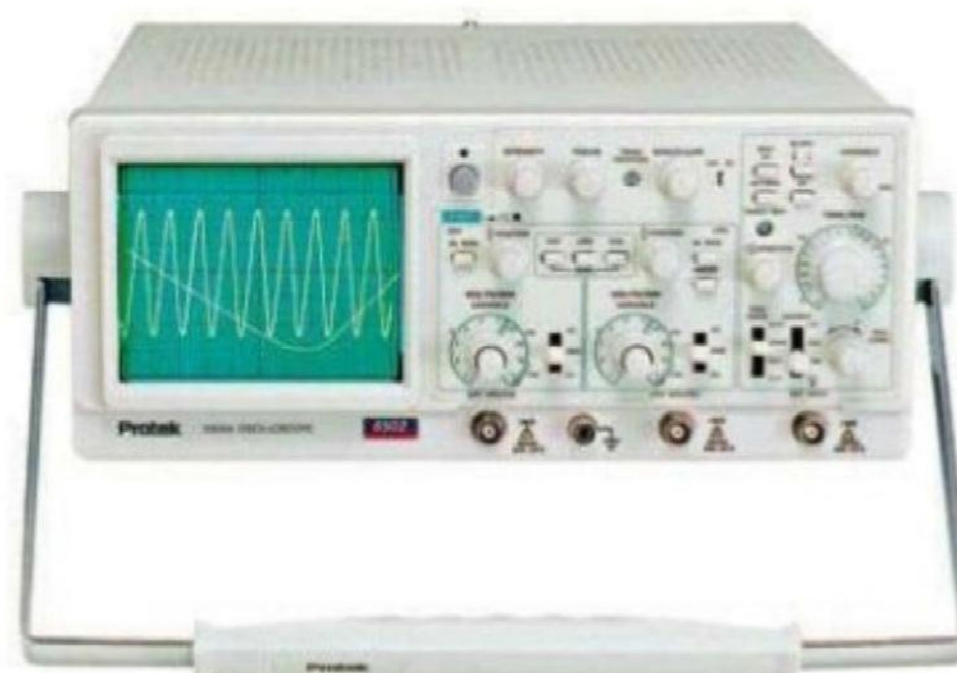
Internal Circuit:



Example:



CRO: Oscilloscope is used to observe the change of an electrical signal over time, such that voltage and time describe a shape which is continuously graphed against a calibrated scale. The observed waveform can be analyzed for such properties as amplitude, frequency, rise time, time interval, distortion and others.



Multimeter: *A multimeter, is an electronic measuring instrument that combines several measurement functions in one unit. A typical multimeter can measure voltage, current, resistance etc.*



Wire-Cutter: *A wire cutter is a small, hand-held device used to cut electrical wire or to strip the electrical insulation from electric wires.*



Power Supply: *A power supply is usually a piece of electronic test equipment or software used as different voltage and current supply.*

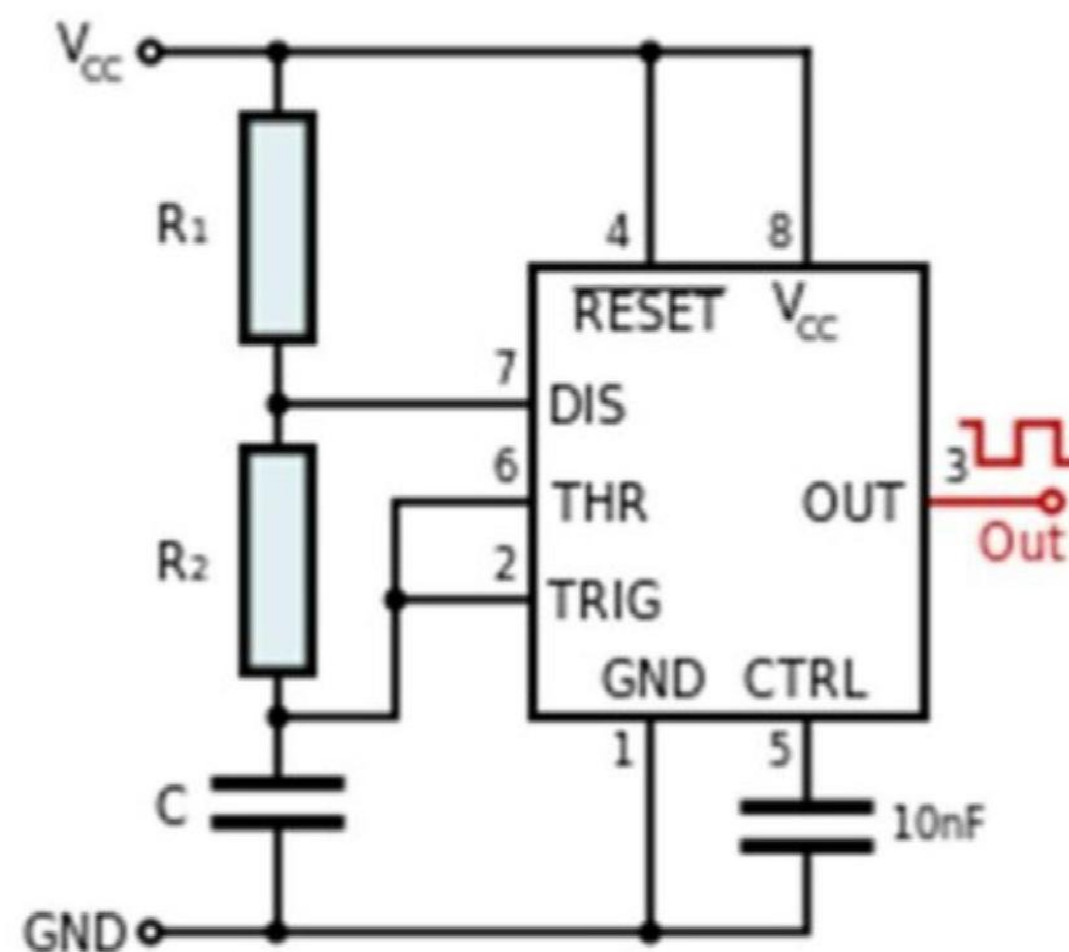


PROJECTS

PROJECTS

1. Timer using IC555

Circuit Diagram:



Calculation: $T_{ON} = 0.693(R_1 + R_2)C$

$$T_{OFF} = 0.693R_2C$$

Used Components Value:-

$$R_1 = 4.7\text{K}\Omega, R_2 = 22\text{k}\Omega$$

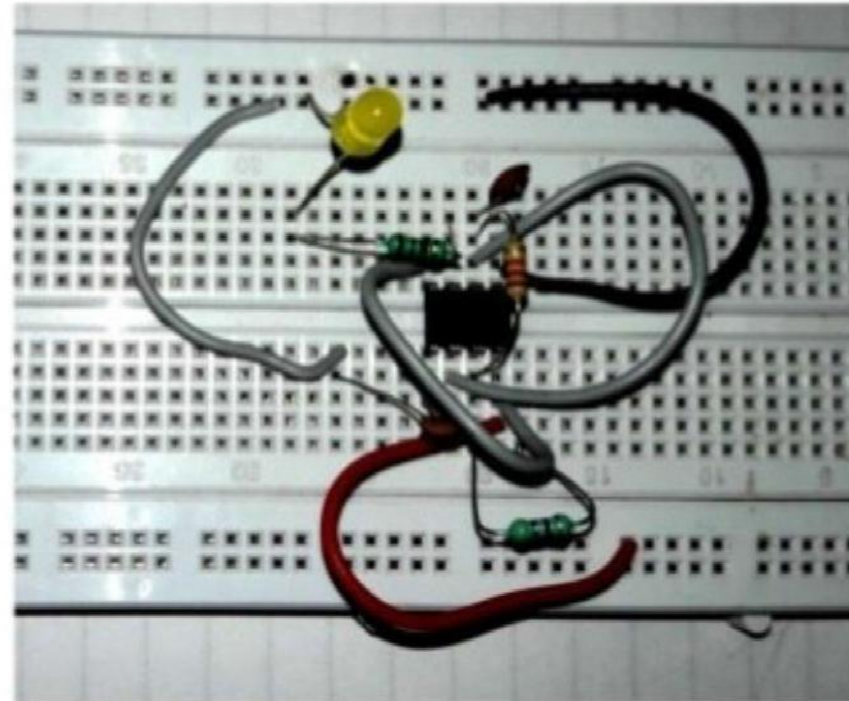
$$C = 0.0047\mu\text{F}, C_1 = 0.01\mu\text{F}$$

Calculated $T_{ON} = 86.96\mu\text{Sec}$, $T_{OFF} = 71.65\mu\text{Sec}$

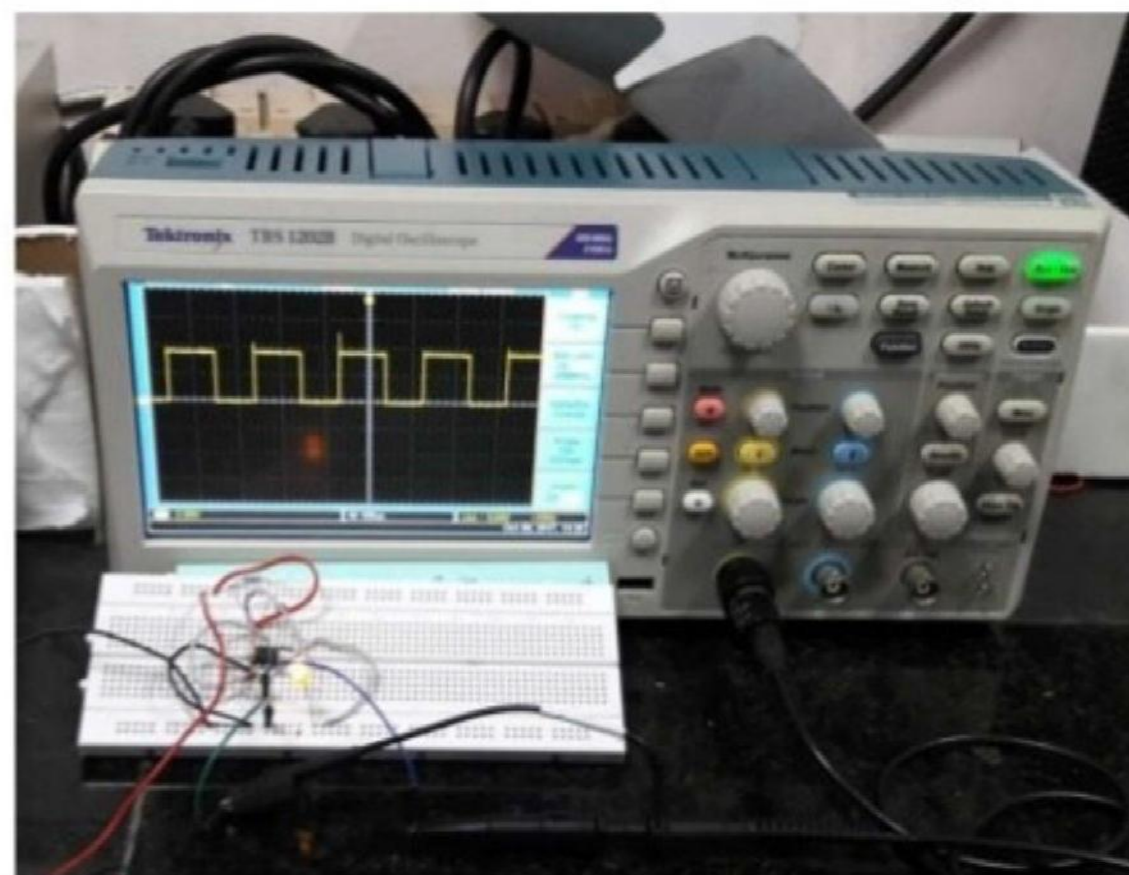
Measured $T_{ON} = 110\mu\text{Sec}$, $T_{OFF} = 63\mu\text{Sec}$

Circuit on Breadboard:

Before Running Condition:



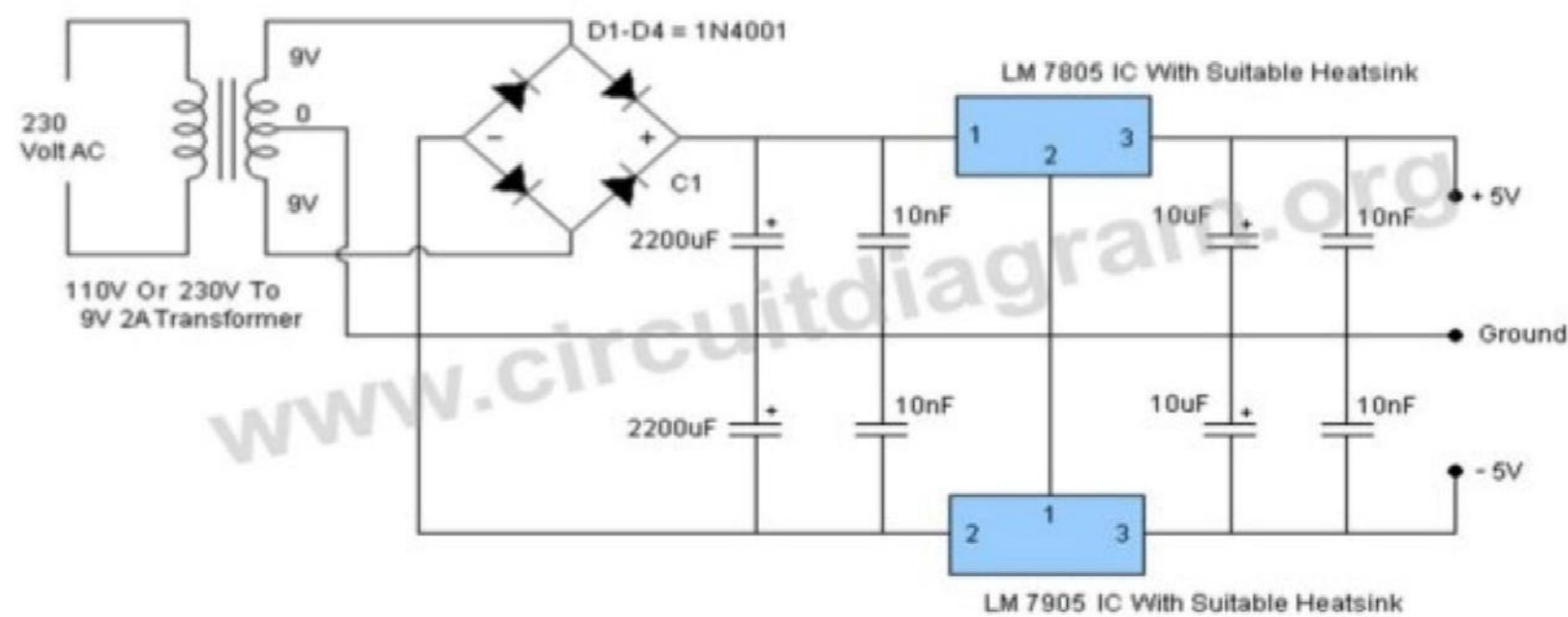
Running Condition:



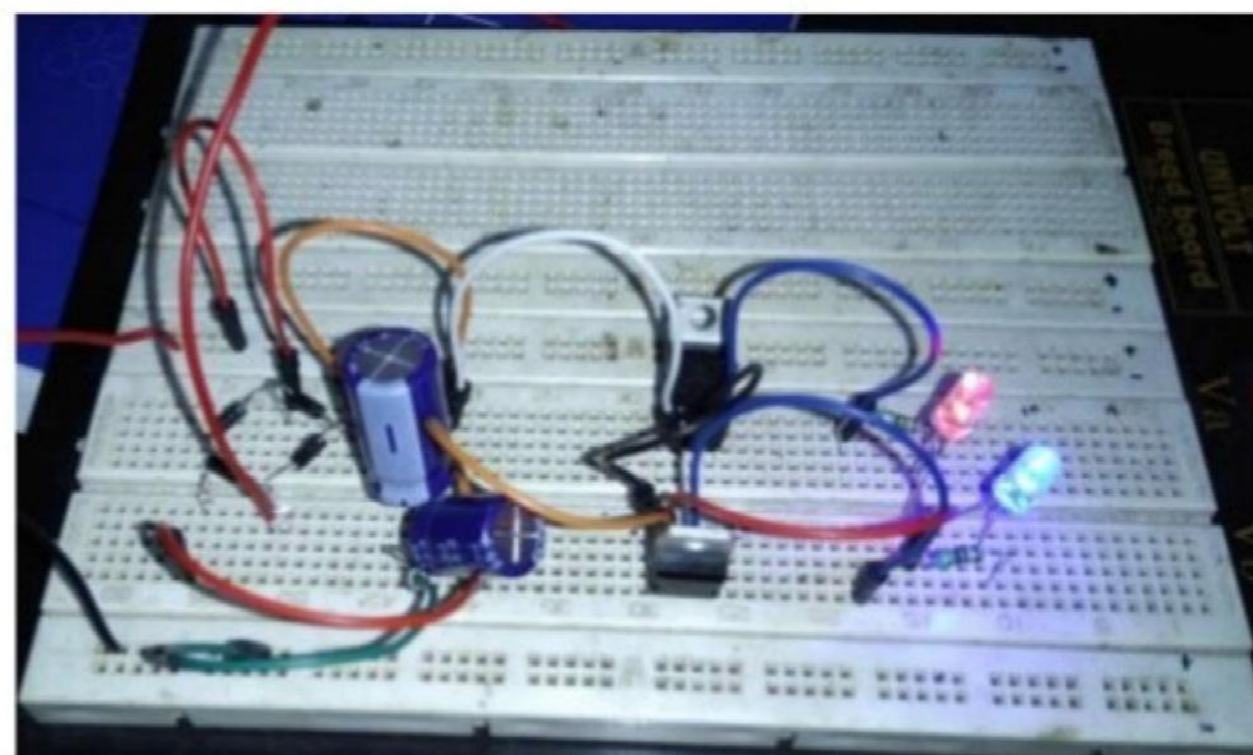
Conclusion: The output freq is above 10Hz so we can't observe the on and off time with eyes, so we use CRO.

2. Positive and Negative power supply: A positive voltage regulator (7805) and a negative voltage regulator (7905) is used in this circuit. Seperate power supplies (9V Transistor battery) are given to both regulators individually.

Circuit:

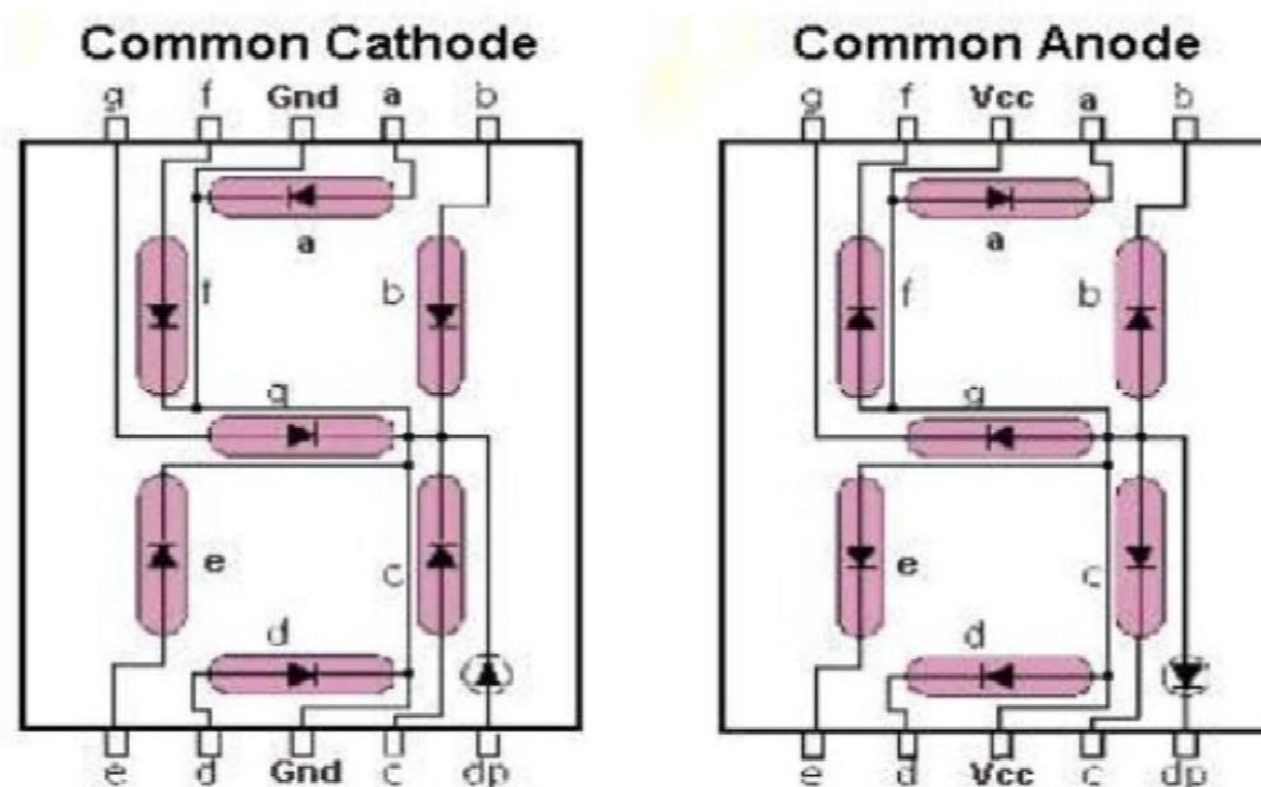


Running Condition:



3. SEVEN SEGMENT DISPLAY: A seven-segment display (SSD), or seven-segment indicator, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot matrix displays.

Seven-segment displays are widely used in digital clocks, electronic meters, basic calculators, and other electronic devices that display numerical information

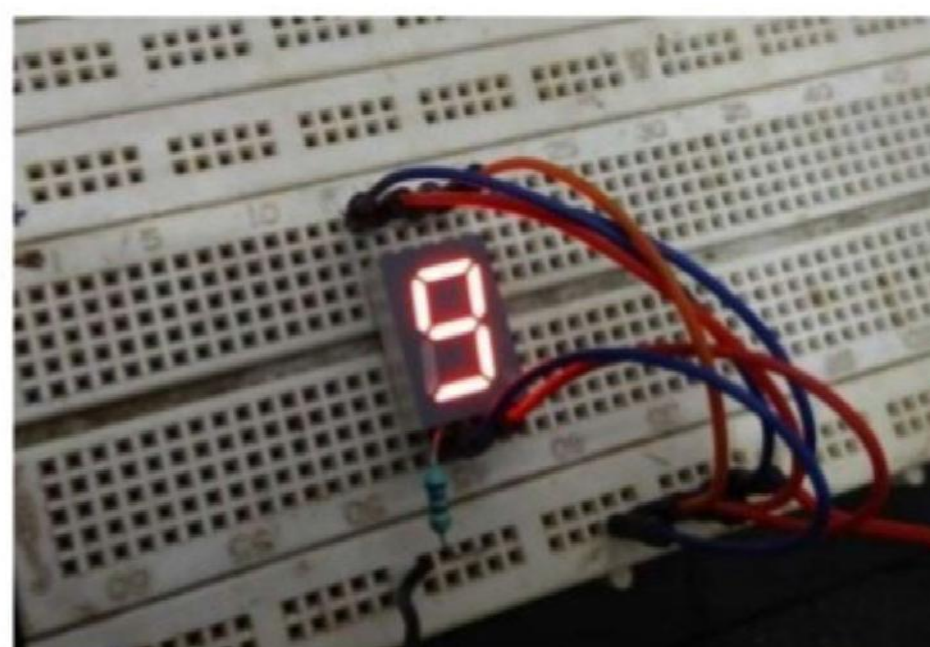


Truth Table of Seven Segment Display:-

Common Cathode							
Decimal Digit	Individual Segments Illuminated						
	a	b	c	d	e	f	g
0	1	1	1	1	1	1	
1		1	1				
2	1	1		1	1		1
3	1	1	1	1			1
4		1	1			1	1
5	1		1	1		1	1
6	1		1	1	1	1	1
7	1	1	1				
8	1	1	1	1	1	1	1
9	1	1	1	1		1	1

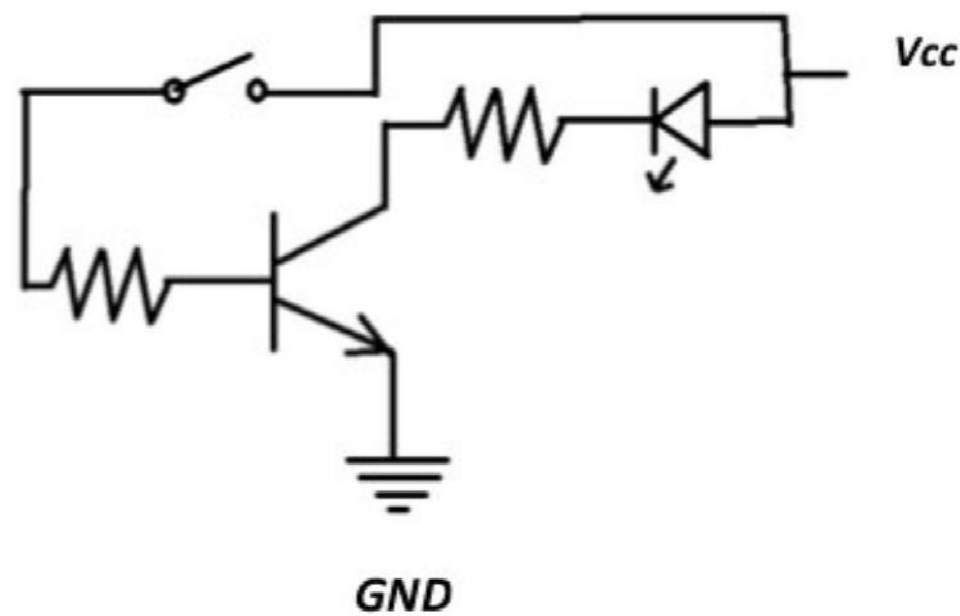
Common Anode							
Decimal Digit	Individual Segments Illuminated						
	a	b	c	d	e	f	g
0	0	0	0	0	0	0	
1		0	0				
2	0	0		0	0		0
3	0	0	0	0			0
4		0	0			0	0
5	0		0	0		0	0
6	0		0	0	0	0	0
7	0	0	0				
8	0	0	0	0	0	0	0
9	0	0	0	0		0	0

Running Condition:

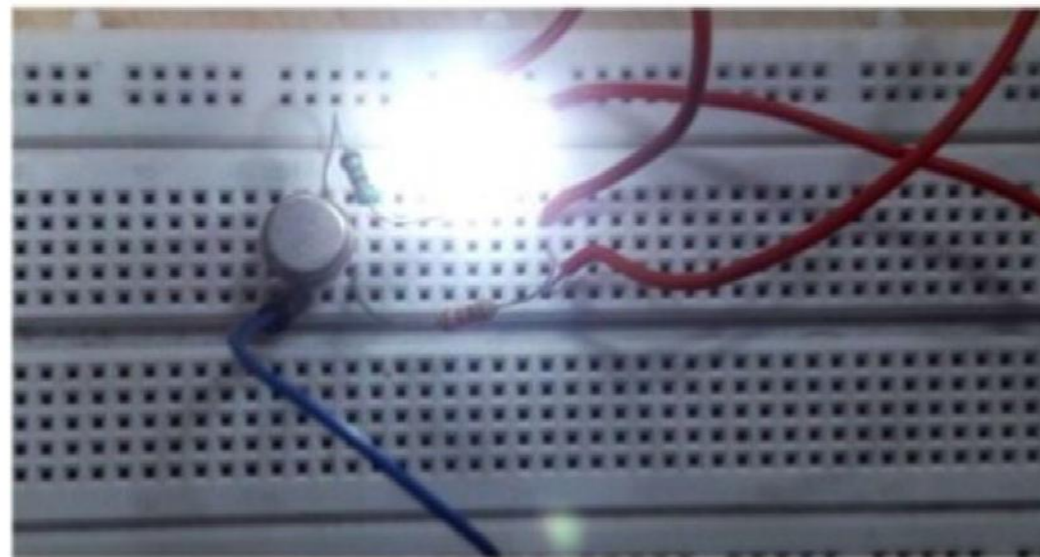


NOT GATE USING N-P-N TRANSISTOR:

Circuit:



Runing Condition:



PCB DESIGN:

Softwares used:-

- TINA

Hardware used:-

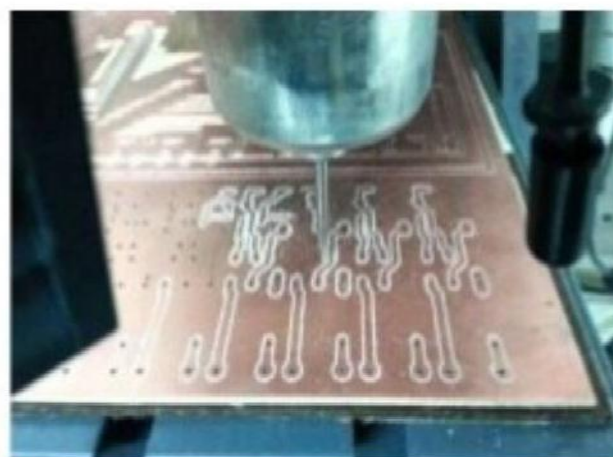
- PCB PROTOTYPE MACHINE

PCB Making Operation:-

- **Milling (*Cut or shape (metal) with a rotating tool*)**



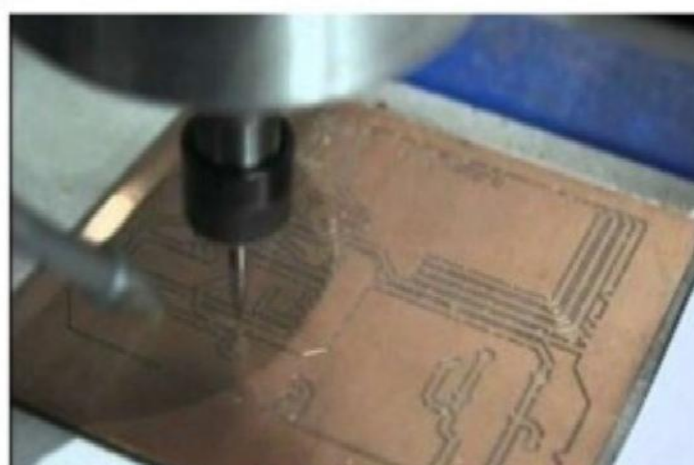
- **Engraving (Engraving is the practice of incising a design onto a hard, usually flat surface by cutting grooves into it)**



- **Drilling (*Drilling is a cutting process that uses a drill bit to cut a hole of circular cross-section in solid materials*)**



- **Routing (Cut only the designed area)**



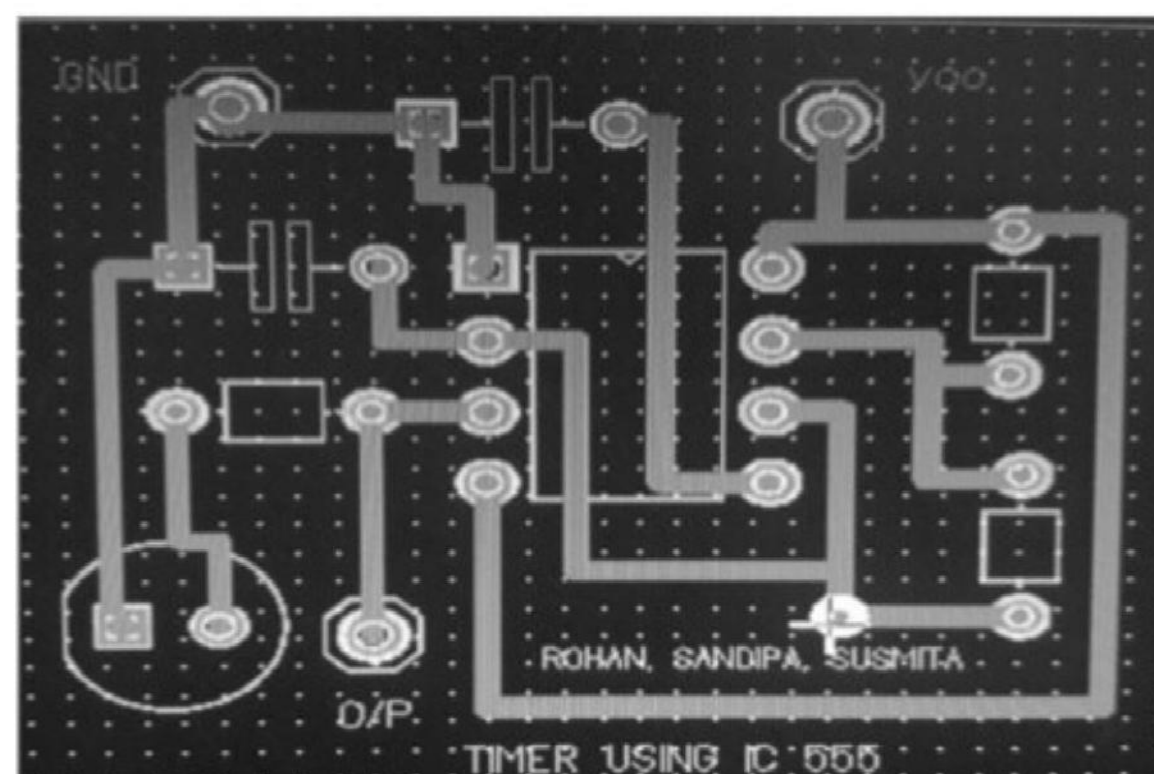
PCB Production Technique:-

1. Dry Technique
2. Wet Lab Technique
 - a. Photoresist Based/Photolithographic Technique
 - b. Silk Screen Paint Technique

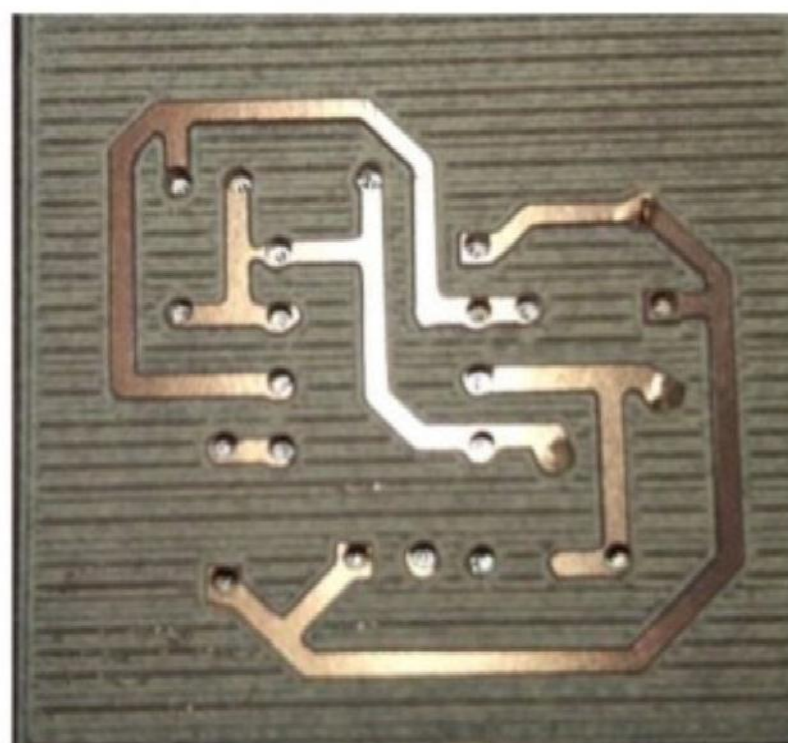
Hands on Design on TINA software

Circuit:- Timer using IC 555

Design on TINA:



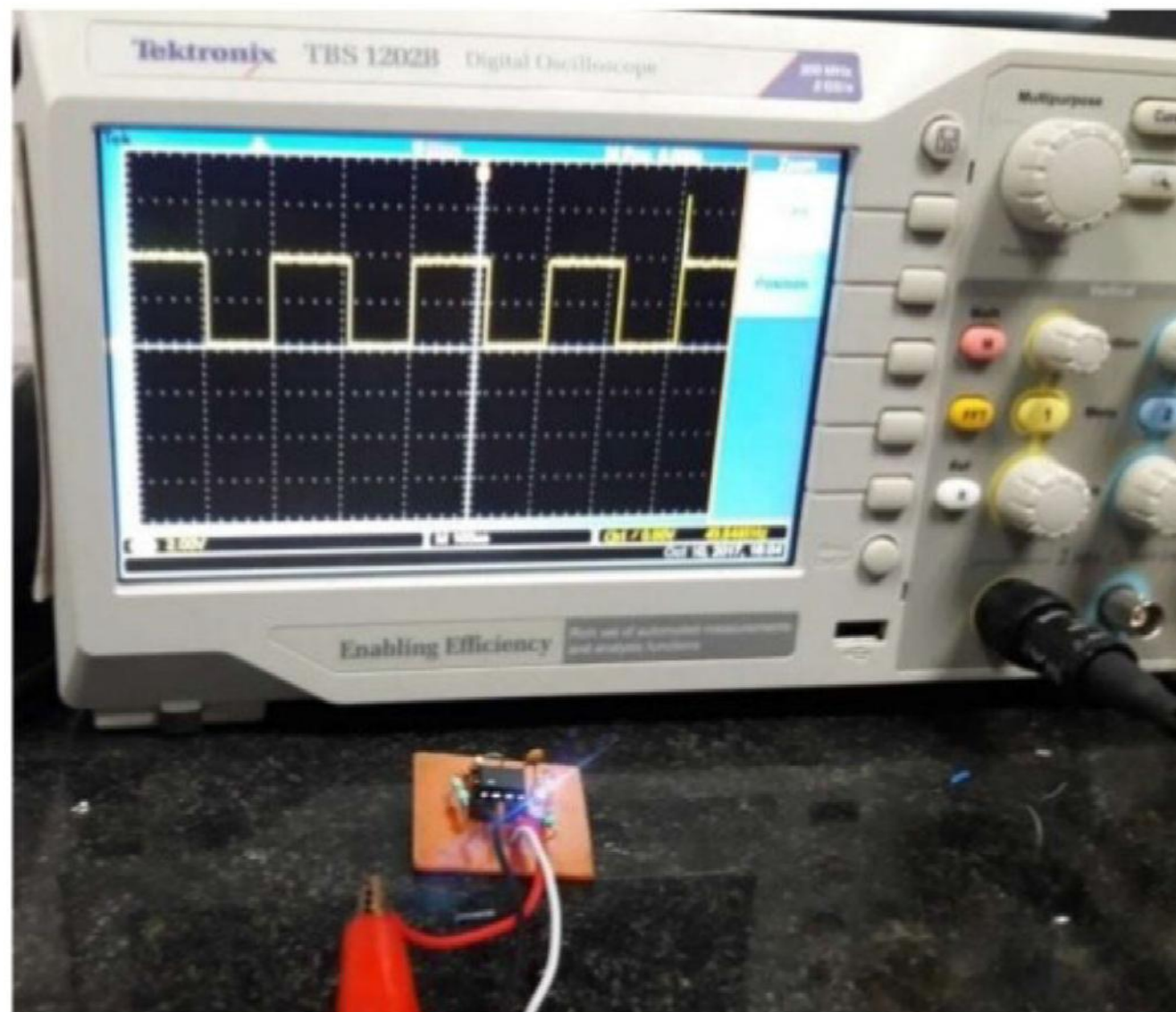
Design on PCB:



Circuit on PCB:



PCB Circuit on Running Condition:



xx555 Precision Timers

1 Features

- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up to 200 mA
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

2 Applications

- Fingerprint Biometrics
- Iris Biometrics
- RFID Reader

3 Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC} . These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

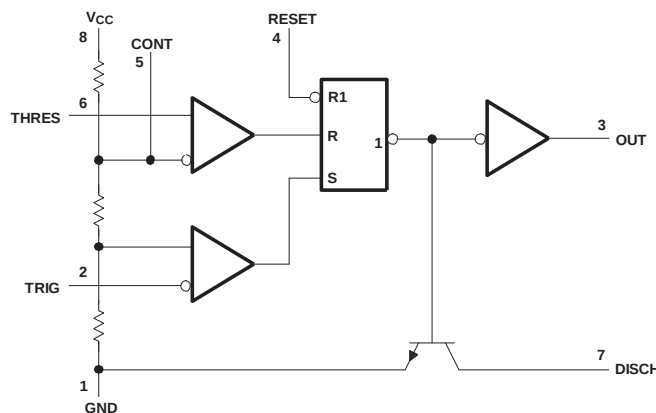
The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5 V to 15 V. With a 5-V supply, output levels are compatible with TTL inputs.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
xx555	PDIP (8)	9.81 mm × 6.35 mm
	SOP (8)	6.20 mm × 5.30 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic





An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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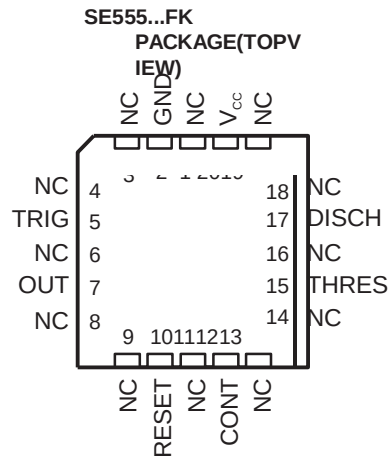
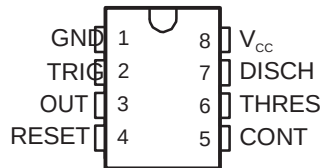
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5 Revision History

Changes from Revision H (June 2010) to Revision I	Page
• Updated document to new TI enhanced data sheet format	1
• Deleted Ordering Information table.	1
• Added Military Disclaimer to Features list	1
• Added Applications.	1
• Added Device Information table.	1
• Moved T_{stg} to Handling Rating table.	4
• Added DISCH switch on-state voltage parameter.	5
• Added Device and Documentation Support section.	19
• Added ESD warning.	19
• Added Mechanical, Packaging, and Orderable Information section.	19

6 Pin Configuration and Functions

NA555...D OR P
PACKAGE NE555...D, P, PS, OR PW
PACKAGE SA555...D OR P
PACKAGE SE555...D, JG, OR P
PACKAGE (TOP VIEW)



NC – No internal connection

Pin Functions

NAME	PIN		I/O	DESCRIPTION
	D, P, PS, P W, JG	FK		
	NO.			
CONT	5	12	I/O	Controls comparator thresholds, Outputs 2/3V _{CC} , allows bypass capacitor connection
DISCH	7	17	O	Open collector output to discharge timing capacitor
GND	1	2	–	Ground
NC		1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	–	No internal connection
OUT	3	7	O	High current timer output signal
RESET	4	10	I	Active low reset input forces output and discharge low.
THRES	6	15	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	5	I	Start of timing input. TRIG < ½ CONT sets output high and discharge open
V _{CC}	8	20	–	Input supply voltage, 4.5V to 16V. (SE555 maximum is 18V)

7 Specifications

7.1 AbsoluteMaximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage ⁽²⁾			18	V
V _I	Input voltage	CONT, RESET, THRES, TRIG		V _{CC}	V
I _O	Output current			±225	mA
θ _{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	D package		97	°C/W
		P package		85	
		PS package		95	
		PW package		149	
θ _{JC}	Package thermal impedance ⁽⁵⁾⁽⁶⁾	FK package		5.61	°C/W
		JG package		14.5	
T _J	Operating virtual junction temperature			150	°C
	Case temperature for 60s	FK package		260	°C
	Lead temperature 1.6mm (1/16in) from case for 60s	JG package		300	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_J(max) - T_A) / θ_{JA}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD51-7.
- (5) Maximum power dissipation is a function of T_J(max), θ_{JC}, and T_C. The maximum allowable power dissipation at any allowable case temperature is P_D = (T_J(max) - T_C) / θ_{JC}. Operating at the absolute maximum T_J of 150°C can affect reliability.
- (6) The package thermal impedance is calculated in accordance with MIL-STD-883.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T _{stg}	Storage temperature range	-65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage	NA555, NE555, SA555	4.5	16	V
		SE555	4.5	18	
V _I	Input voltage	CONT, RESET, THRES, and TRIG		V _{CC}	V
I _O	Output current			±200	mA
T _A	Operating free-air temperature	NA555	-40	105	°C
		NE555	0	70	
		SA555	-40	85	
		SE555	-55	125	

7.4 Electrical Characteristics

 $V_{CC}=5V$ to $15V$, $T_A=25^{\circ}C$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	$V_{CC}=15V$		9.4	10	10.6	8.8	10	11.2	V
	$V_{CC}=5V$		2.7	3.3	4	2.4	3.3	4.2	
THRES current ⁽¹⁾				30	250		30	250	nA
TRIG voltage level	$V_{CC}=15V$		4.8	5	5.2	4.5	5	5.6	V
		$T_A = -55^{\circ}C$ to $125^{\circ}C$		3	6				
	$V_{CC}=5V$		1.45	1.67	1.9	1.1	1.67	2.2	
		$T_A = -55^{\circ}C$ to $125^{\circ}C$			1.9				
TRIG current	TRIG at 0V			0.5	0.9		0.5	2	μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	$T_A = -55^{\circ}C$ to $125^{\circ}C$				1.1				
RESET current	RESET at V_{CC}			0.1	0.4		0.1	0.4	mA
	RESET at 0V			-0.4	-1		-0.4	-1.5	
DISCH switchoff-state current				20	100		20	100	nA
DISCH switchon-state voltage	$V_{CC}=5V$, $I_O=8mA$						0.15	0.4	V
CONT voltage (opencircuit)	$V_{CC}=15V$		9.6	10	10.4	9	10	11	V
		$T_A = -55^{\circ}C$ to $125^{\circ}C$	9.6		10.4				
	$V_{CC}=5V$		2.9	3.3	3.8	2.6	3.3	4	
		$T_A = -55^{\circ}C$ to $125^{\circ}C$	2.9		3.8				
Low-level output voltage	$V_{CC}=15V$, $I_{OL}=10mA$			0.1	0.15		0.1	0.25	V
		$T_A = -55^{\circ}C$ to $125^{\circ}C$			0.2				
	$V_{CC}=15V$, $I_{OL}=50mA$			0.4	0.5		0.4	0.75	
		$T_A = -55^{\circ}C$ to $125^{\circ}C$			1				
	$V_{CC}=15V$, $I_{OL}=100mA$			2	2.2		2	2.5	
		$T_A = -55^{\circ}C$ to $125^{\circ}C$			2.7				
	$V_{CC}=15V$, $I_{OL}=200mA$			2.5			2.5		
	$V_{CC}=5V$, $I_{OL}=3.5mA$	$T_A = -55^{\circ}C$ to $125^{\circ}C$			0.35				
	$V_{CC}=5V$, $I_{OL}=5mA$			0.1	0.2		0.1	0.35	
		$T_A = -55^{\circ}C$ to $125^{\circ}C$			0.8				
High-level output voltage	$V_{CC}=5V$, $I_{OL}=8mA$			0.15	0.25		0.15	0.4	V
	$V_{CC}=15V$, $I_{OH}=-100mA$		13	13.3		12.75	13.3		
		$T_A = -55^{\circ}C$ to $125^{\circ}C$	12						
	$V_{CC}=15V$, $I_{OH}=-200mA$			12.5			12.5		
	$V_{CC}=5V$, $I_{OH}=-100mA$		3	3.3		2.75	3.3		
		$T_A = -55^{\circ}C$ to $125^{\circ}C$	2						
Supply current	Output low, No load	$V_{CC}=15V$		10	12		10	15	mA
		$V_{CC}=5V$		3	5		3	6	
	Output high, No load	$V_{CC}=15V$		9	10		9	13	
		$V_{CC}=5V$		2	4		2	5	

(1) This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when $V_{CC}=5V$, the maximum value is $R_A+R_B \leq 3.4M\Omega$, and for $V_{CC}=15V$, the maximum value is $10M\Omega$.

7.5 Operating Characteristics

 $V_{CC}=5V$ to $15V$, $T_A=25^{\circ}C$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS ⁽¹⁾	SE555			NA555 NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval ⁽²⁾	Each timer, monostable ⁽³⁾	$T_A=25^{\circ}C$		0.5	1.5 ⁽⁴⁾		1	3	%
	Each timer, astable ⁽⁵⁾			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable ⁽³⁾	$T_A=MIN$ to MAX		30	100 ⁽⁴⁾		50		ppm/ $^{\circ}C$
	Each timer, astable ⁽⁵⁾			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable ⁽³⁾	$T_A=25^{\circ}C$		0.05	0.2 ⁽⁴⁾		0.1	0.5	%/V
	Each timer, astable ⁽⁵⁾			0.15			0.3		
Output-pulse rise time		$C_L=15pF$, $T_A=25^{\circ}C$		100	200 ⁽⁴⁾		100	300	ns
Output-pulse fall time		$C_L=15pF$, $T_A=25^{\circ}C$		100	200 ⁽⁴⁾		100	300	ns

(1) For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

(2) Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

(3) Values specified are for a device in a monostable circuit similar to [Figure 9](#), with the following component values: $R_A=2k\Omega$ to $100k\Omega$, $C=0.1\mu F$.

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(5) Values specified are for a device in an astable circuit similar to [Figure 12](#), with the following component values: $R_A=1k\Omega$ to $100k\Omega$, $C=0.1\mu F$.

7.6 Typical Characteristics

Data for temperatures below -40°C and above 105°C are applicable for SE555 circuit only.

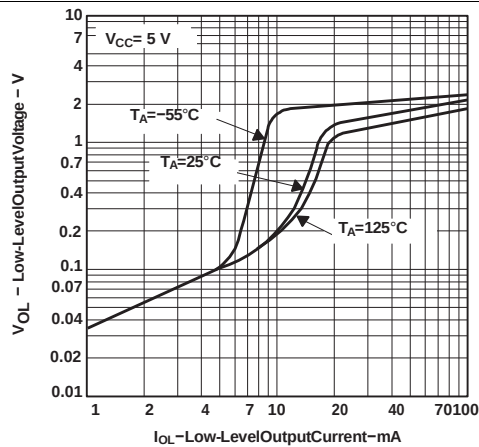


Figure 1. Low-Level Output Voltage vs Low-Level Output Current

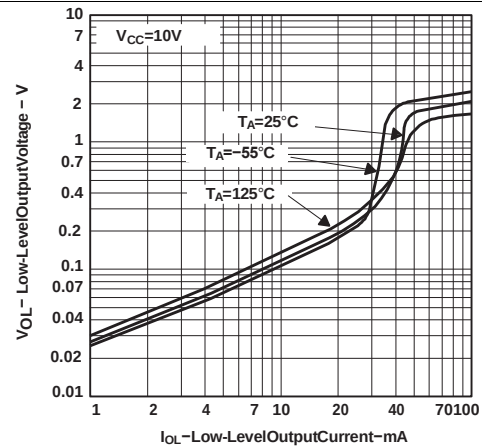


Figure 2. Low-Level Output Voltage vs Low-Level Output Current

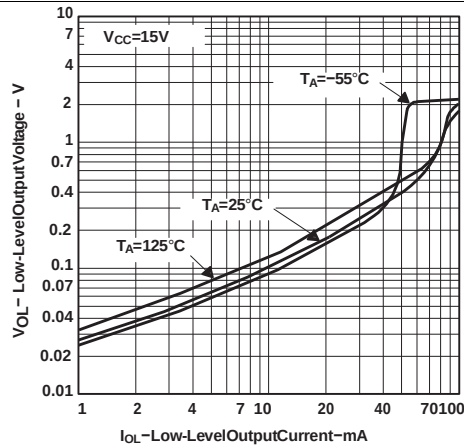


Figure 3. Low-Level Output Voltage vs Low-Level Output Current

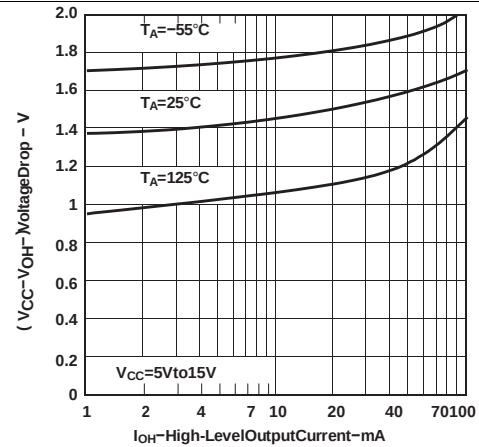


Figure 4. Drop Between Supply Voltage and High-Level Output Current

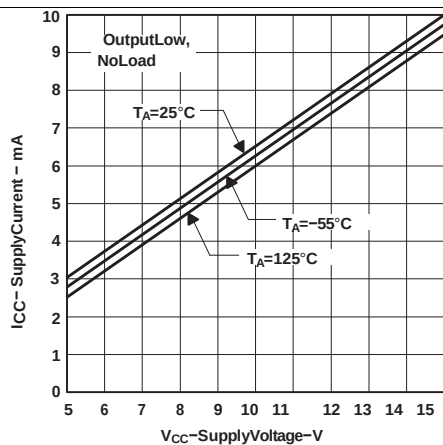


Figure 5. Supply Current vs Supply Voltage

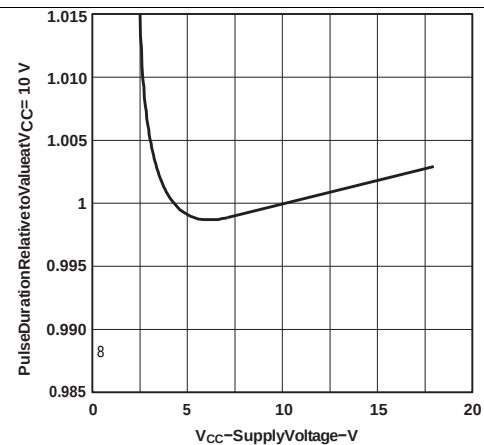


Figure 6. Normalized Output (Monostable Operation) vs Supply Voltage

Typical Characteristics (continued)

Data for temperatures below -40°C and above 105°C are applicable for SE555 circuit only.

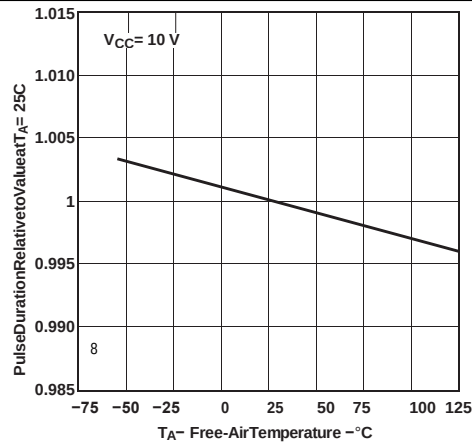


Figure 7. Normalized Output Pulse Duration (Monostable Operation) vs Free-Air Temperature

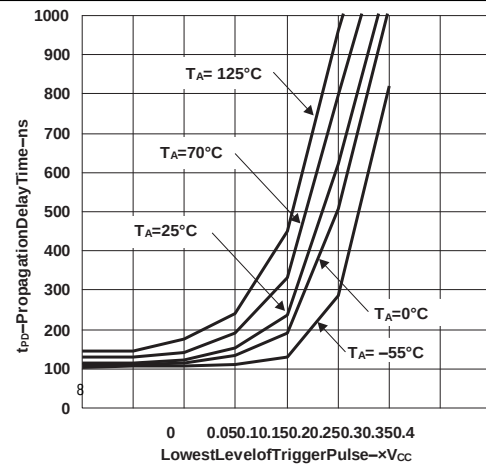


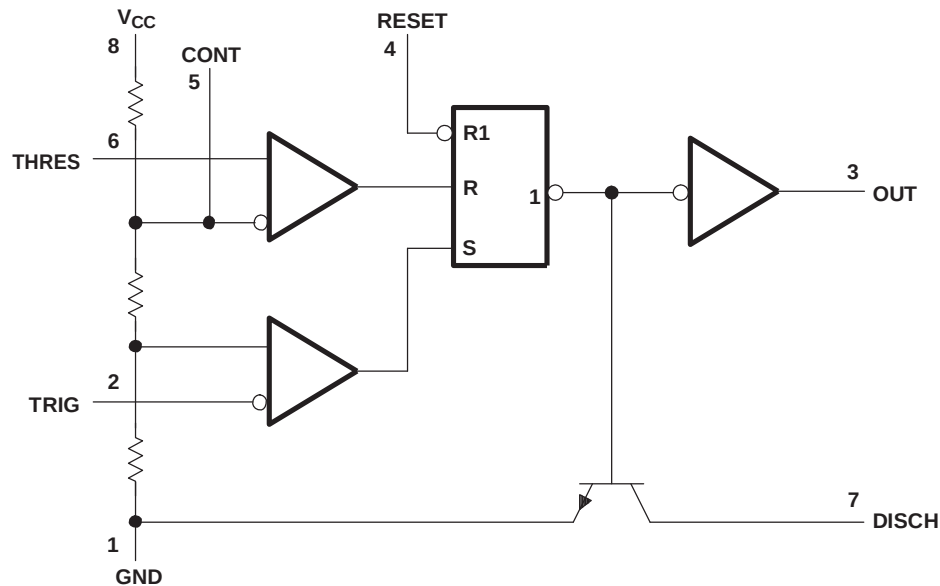
Figure 8. Propagation Delay Time vs Lowest Voltage Level of Trigger Pulse

8 Detailed Description

8.1 Overview

The xx555 timer is a popular and easy to use for general purpose timing applications from 10 μ s to hours or from <1 mHz to 100 kHz. In the time-delay or mono-stable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor. Maximum output sink and discharge sink current is greater for higher VCC and less for lower VCC.

8.2 Functional Block Diagram



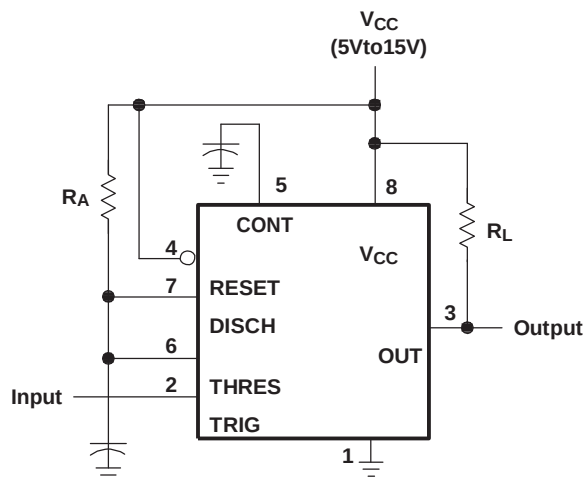
- A. Pin numbers shown are for the D, JG, P, PS, and PW packages.
- B. RESET can override TRIG, which can override THRES.

8.3 Feature Description

8.3.1 Mono-stable Operation

For mono-stable operation, any of these timers can be connected as shown in Figure 9. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop (Q goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop (Q goes high), drives the output low, and discharges C through Q1.

Feature Description (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Figure 9. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least $10\mu\text{s}$ before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as $10\mu\text{s}$, which limits the minimum monostable pulse width to $10\mu\text{s}$. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately $t_w = 1.1R_A C$. Figure 11 is a plot of the time constant for various values of R_A and C . The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC} . The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used, it should be connected to V_{CC} .

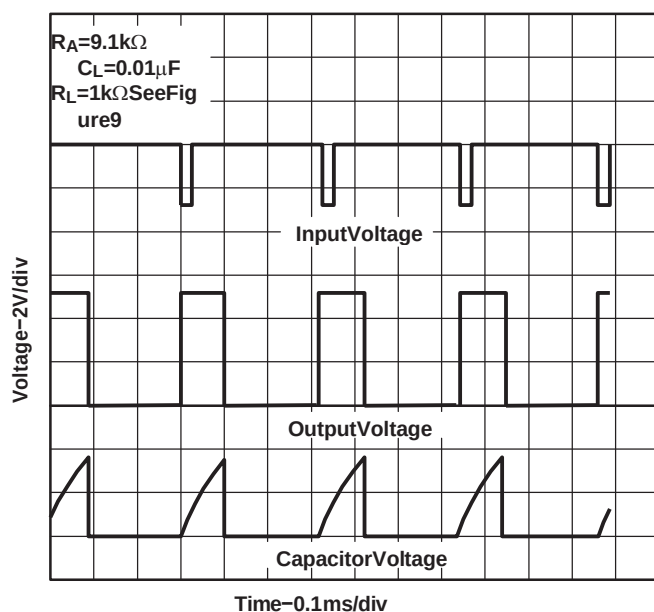


Figure 10. Typical Monostable Waveforms

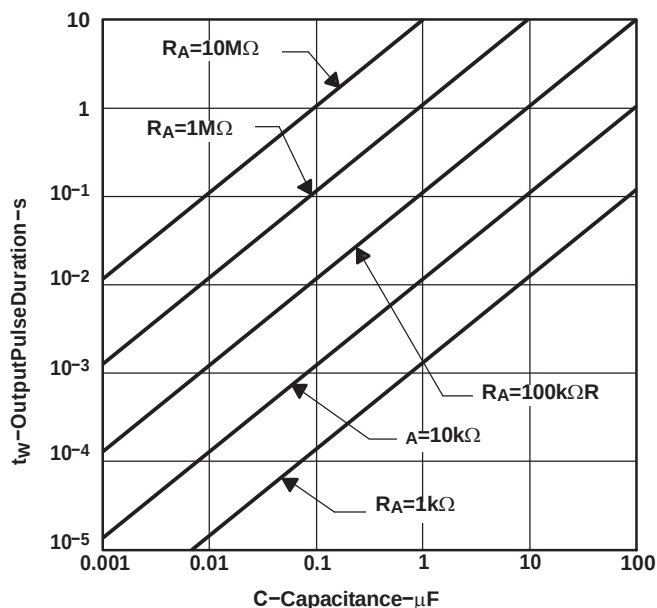


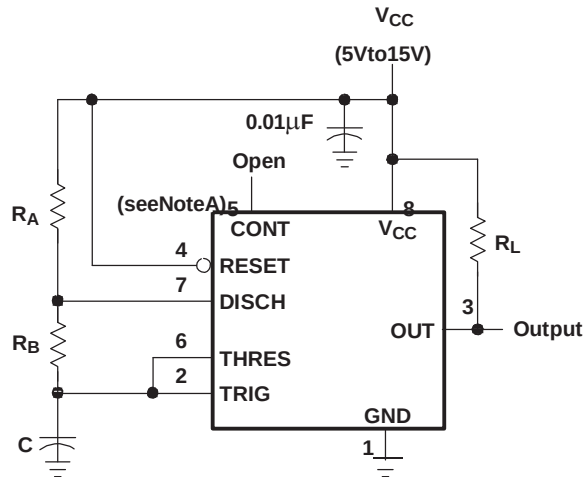
Figure 11. Output Pulse Duration vs Capacitance

FeatureDescription(continued)

8.3.2 A-stableOperation

As shown in Figure 12, adding a second resistor, R_B , to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B .

This astable connection results in capacitor C charging and discharging between the threshold-voltage level ($\approx 0.67 \times V_{CC}$) and the trigger-voltage level ($\approx 0.33 \times V_{CC}$). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

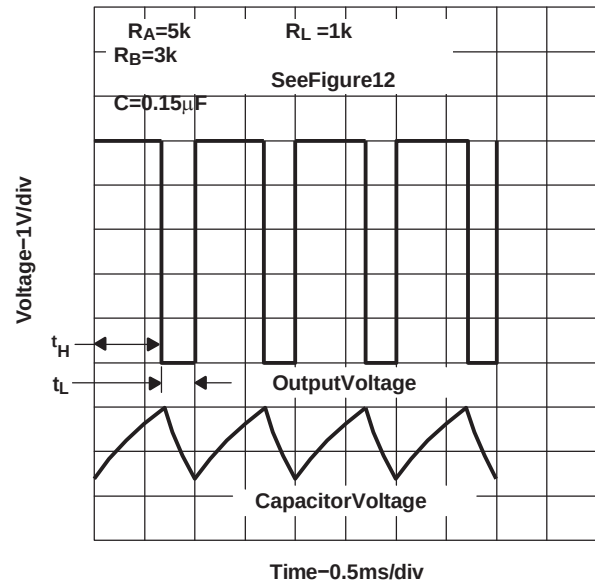


Figure 13. Typical Astable Waveforms

Figure 12 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693(R_A + R_B)C_B \quad (1)$$

$$t_L = 0.693(R_B)C_B \quad (2)$$

Other useful relationships are shown below:

$$\text{period} = t_H + t_L = 0.693(R_A + 2R_B)C \quad (3)$$

$$\text{frequency} \approx \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

$$\text{Output driver duty cycle} = \frac{t_L}{t_H + t_L} = \frac{R_B}{R_A + 2R_B} \quad (5)$$

$$\text{Output waveform duty cycle} = \frac{t_H + t_L}{t_H + t_L} = 1 - \frac{R_B}{R_A + 2R_B} \quad (6)$$

$$\text{Low-to-high ratio} = \frac{t_L}{t_H} = \frac{R_B R_A}{R_B + R_A} \quad (7)$$

Feature Description (continued)

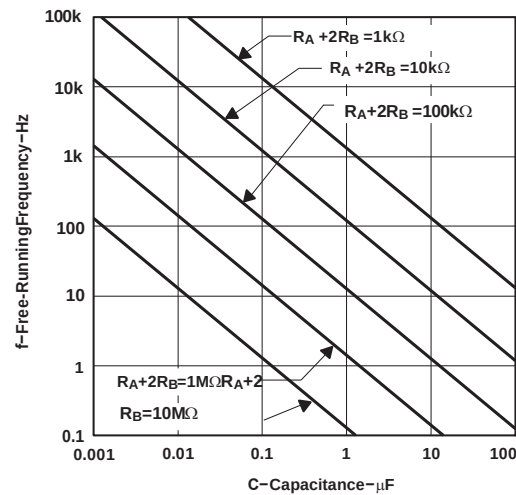


Figure 14. Free-Running Frequency

8.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 15 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

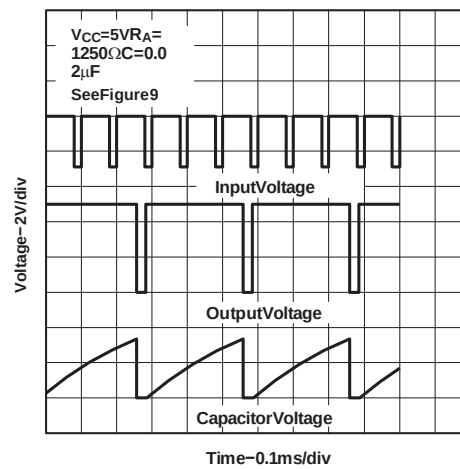


Figure 15. Divide-by-Three Circuit Waveforms

8.4 Device Functional Modes

Table 1. Function Table

RESET	TRIGGER VOLTAGE ⁽¹⁾	THRESHOLD VOLTAGE ⁽¹⁾	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V _{CC}	Irrelevant	High	Off
High	>1/3 V _{CC}	>2/3 V _{CC}	Low	On
High	>1/3 V _{CC}	<2/3 V _{CC}	As previously established	

(1) Voltage level shown are nominal.

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI components specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

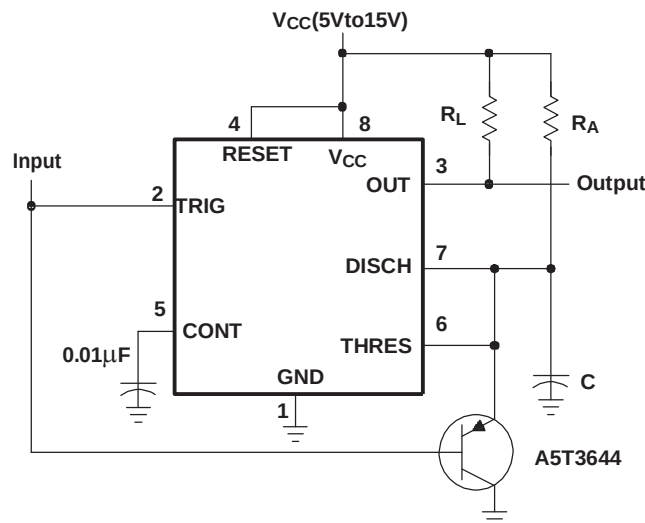
9.1 Application Information

The x555 timer devices use a resistor and capacitor charging delay to provide a programmable time delay or operating frequency. This section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Missing-Pulse Detector

The circuit shown in Figure 16 can be used to detect a missing pulse or an abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 17.



Pin numbers shown are shown for the D, JG, P, PS, and PW packages.

Figure 16. Circuit for Missing-Pulse Detector

9.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. Input stuck low will not be detected because timing capacitor "C" will remain discharged.

9.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C > [\text{maximum normal input high time}]$. R_L improves V_{OH} , but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.1.3 Application Curves

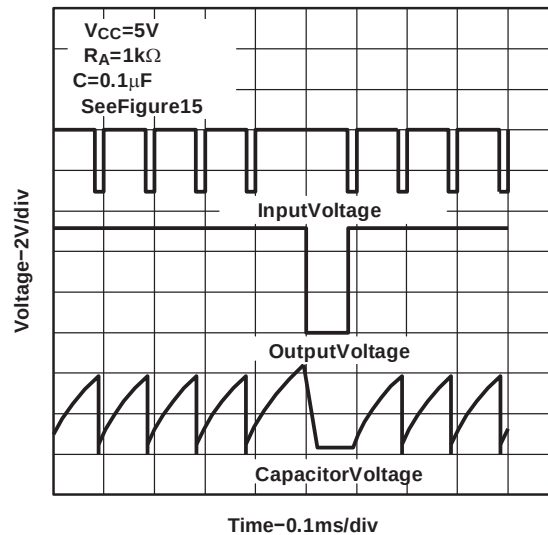
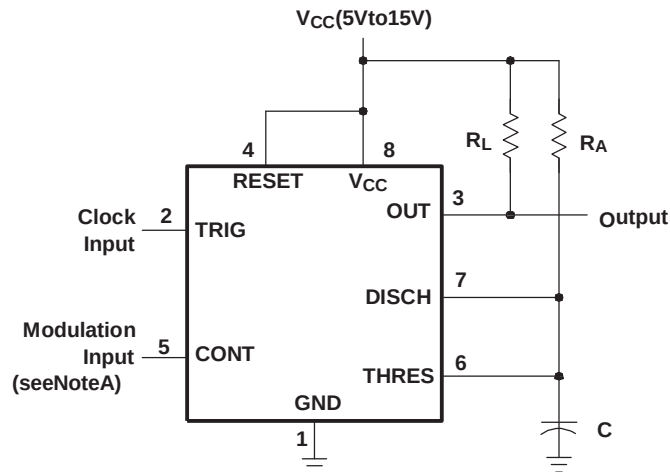


Figure 17. Completed Timing Waveforms for Missing-Pulse Detector

9.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse trains trigger the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any waveshape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.
 NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

Typical Applications (continued)

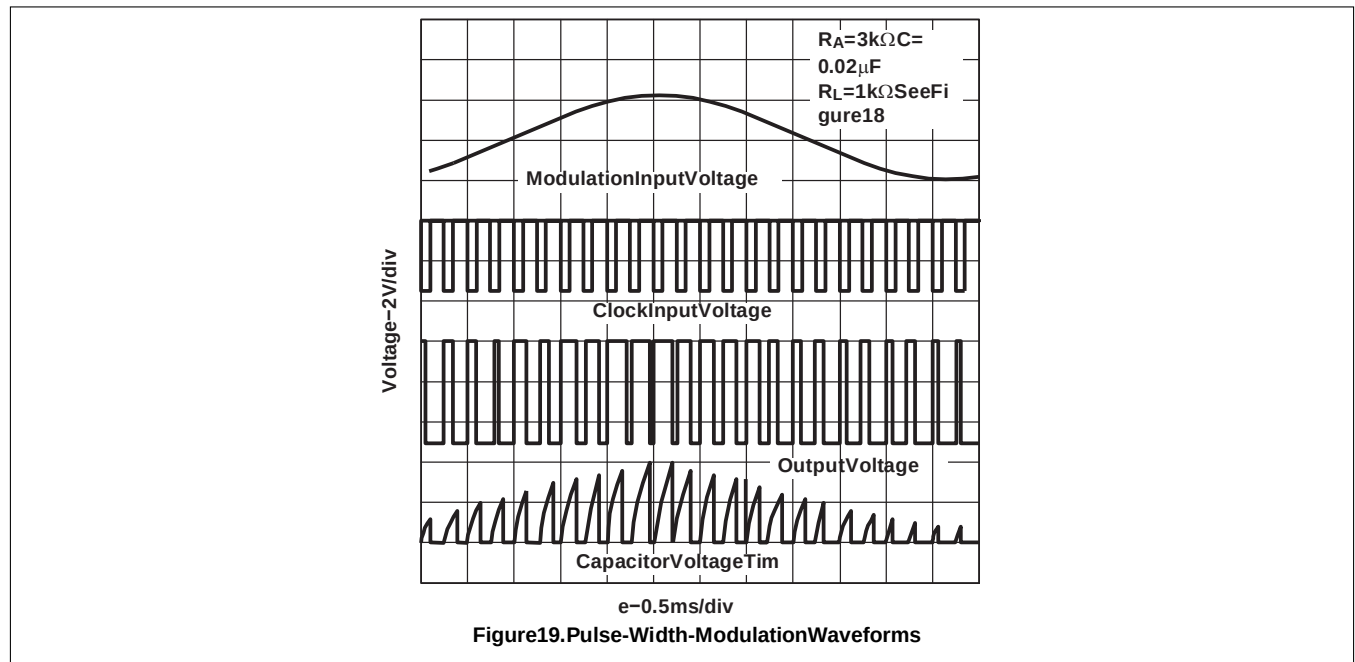
9.2.2.1 Design Requirements

Clock input must have V_{OL} and V_{OH} levels that are less than and greater than $1/3V_{CC}$. Modulation input can vary from ground to V_{CC} . The application must be tolerant of an nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is based on an negative exponential curve.

9.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH} , but it is not required for TTL compatibility.

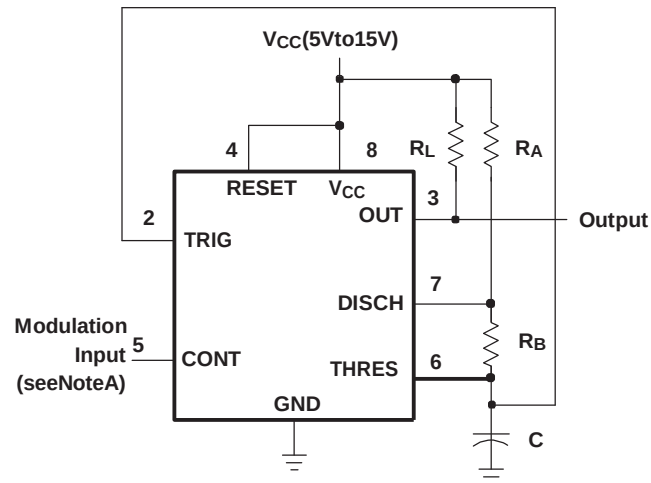
9.2.2.3 Application Curves



9.2.3 Pulse-Position Modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.

Typical Applications (continued)



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

9.2.3.1 Design Requirements

Both DC and AC coupled modulation input will change the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle will vary with the modulation voltage.

9.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in the Astable Operation section. R_L improves V_{OH} , but it is not required for TTL compatibility.

Typical Applications (continued)

9.2.3.3 Application Curves

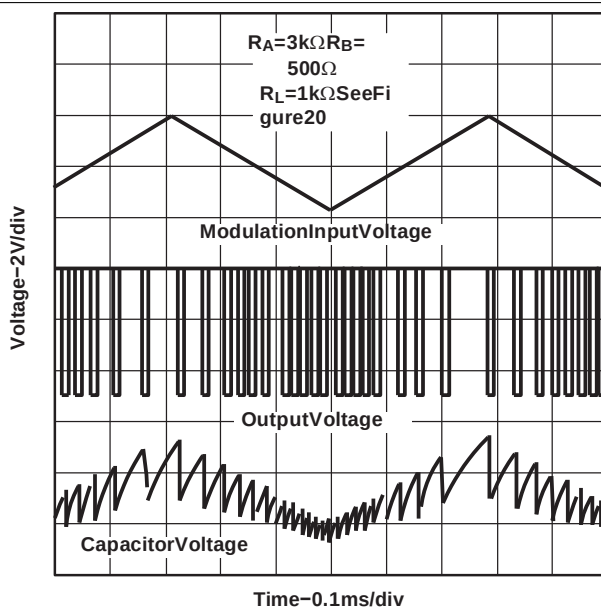
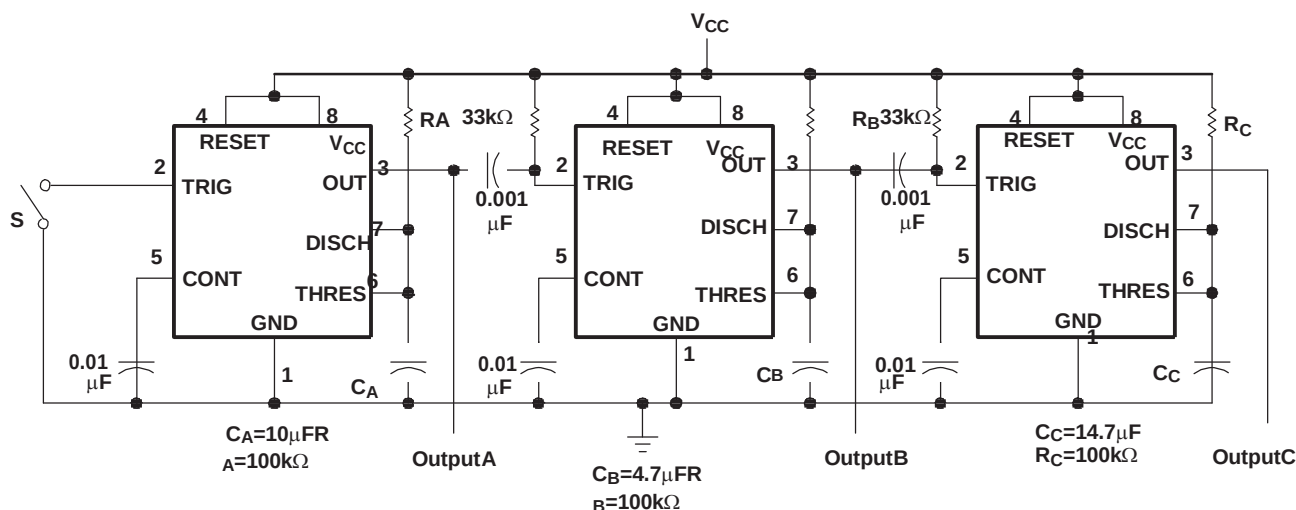


Figure 21. Pulse-Position-Modulation Waveforms

9.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require reactivation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of fastable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



Pin numbers shown are for the D, JG, P, PS, and PW packages. NOTE
A: S closes momentarily at t=0.

Figure 22. Sequential Timer Circuit

Typical Applications (continued)

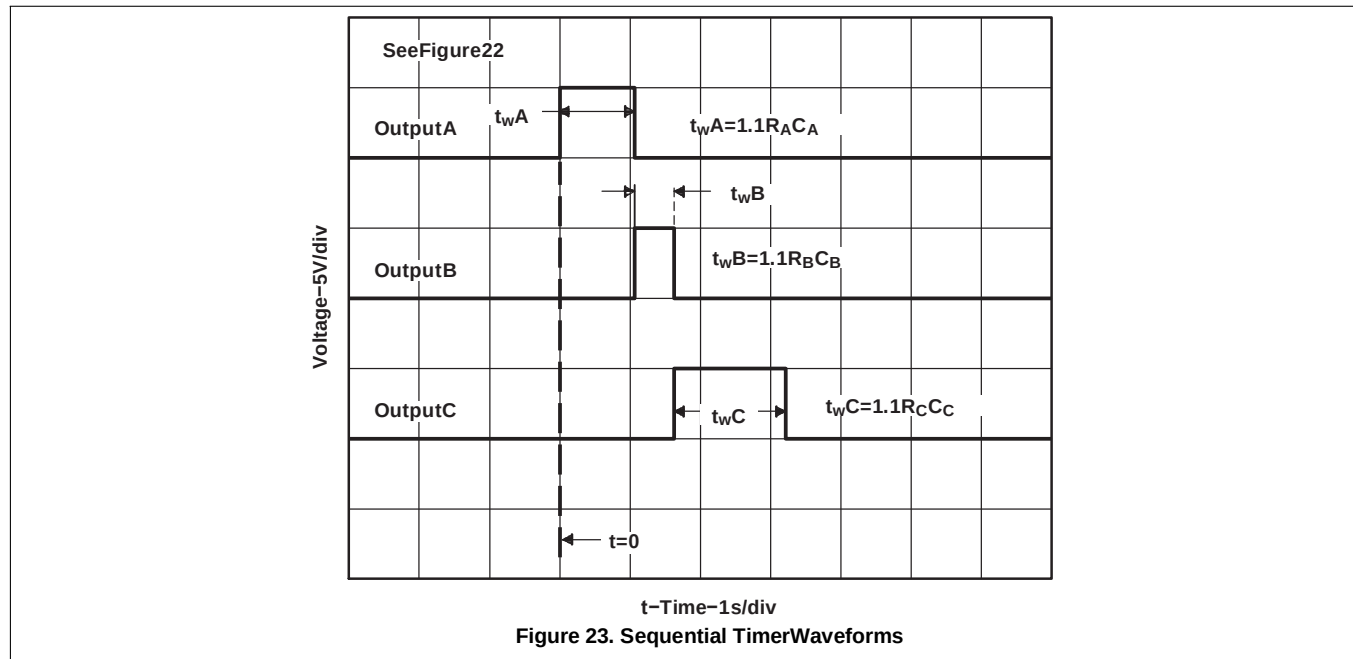
9.2.4.1 Design Requirements

These sequential timer application chains together multiple mono-stable timers. The joining components are the 33-kΩ resistors and 0.001-μF capacitors. The output high-to-low edge passes a 10-μs start pulse to the next monostable.

9.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula. $t_w = 1.1 \times R \times C$.

9.2.4.3 Application Curves



10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5V and 16V. (18V for SE555). A bypass capacitor is highly recommended from VCC to ground pin; ceramic 0.1μF capacitor is sufficient.

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
NA555	Click here	Click here	Click here	Click here	Click here
NE555	Click here	Click here	Click here	Click here	Click here
SA555	Click here	Click here	Click here	Click here	Click here
SE555	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

[SLYZ022](#)—*TIGlossary*.

This glossary lists and explains terms, acronyms and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
JM38510/10901BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10901BPA	Samples
M38510/10901BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /10901BPA	Samples
NA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	NA555	Samples
NA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU CU SN	N / A for Pkg Type	-40 to 105	NA555P	Samples
NA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 105	NA555P	Samples
NE555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555DRG3	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	NE555	
NE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	NE555	Samples
NE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU CU SN	N / A for Pkg Type	0 to 70	NE555P	Samples
NE555PE3	PREVIEW	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70	NE555P	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	NE555P	Samples
NE555PSLE		SO	PS	8		TBD	Call TI	Call TI	0 to 70		
NE555PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	N555	Samples
NE555Y				0		TBD	Call TI	Call TI	0 to 70		
SA555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU CU SN	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA555	Samples
SA555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA555P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SA555PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SA555P	Samples
SE555D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	SE555	Samples
SE555FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SE555FKB	Samples
SE555JG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SE555JG	Samples
SE555JGB	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SE555JGB	Samples
SE555N		PDIP	N	8		TBD	Call TI	Call TI	-55 to 125		
SE555P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	SE555P	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) EcoPlan-Theplannedeco-friendlyclassification:Pb-Free(RoHS),Pb-Free(RoHSExempt),orGreen(RoHS&noSb/Br)-pleasecheck<http://www.ti.com/productcontent>forthelatestavailability information and additional product content details.

TBD:The Pb-Free/Green conversion plan has not been defined.

Pb-Free(RoHS):TI'sterms"Lead-Free"or"Pb-Free"meansemiconductorproducts thatarecompatiblewiththecurrentRoHSrequirementsforall6substances,includingtherequirementthat lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free(RoHSExempt):ThiscomponenthasaRoHSExemptionforeither1)lead-basedflip-chipsolderbumpsusedbetweenthedieandpackage,or2)lead-baseddieadhesiveusedbetween the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green(RoHS&noSb/Br):TIdefines"Green"tomeanPb-Free(RoHScompatible),andfreeofBromine(Br) andAntimony(Sb)basedflameretardants(Br orSb donot exceed0.1%byweight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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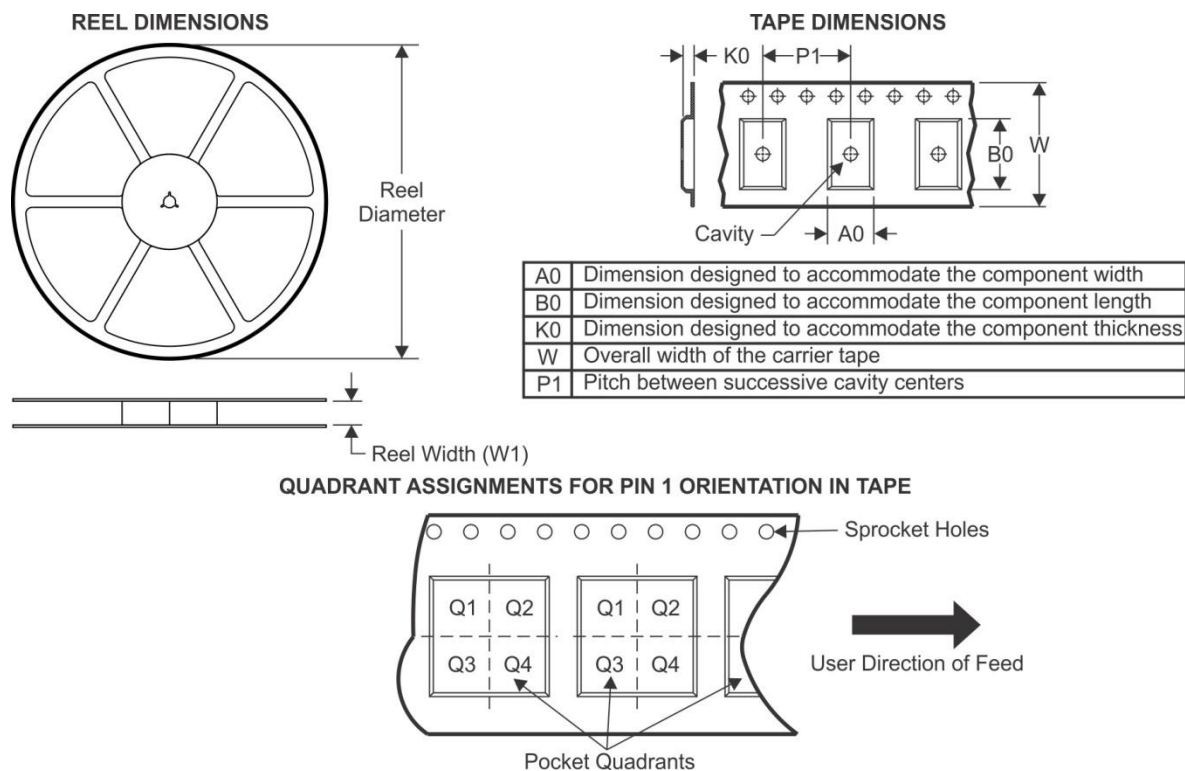
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SE555, SE555M :

- Catalog: [SE555](#)
- Military: [SE555M](#)
- Space: [SE555-SP](#), [SE555-SP](#)

NOTE: Qualified Version Definitions:

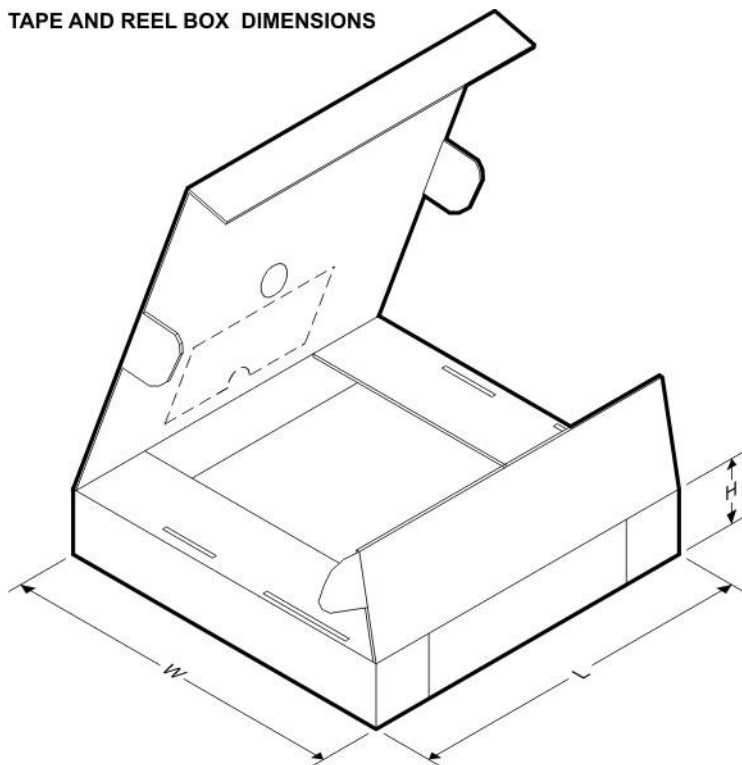
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
NE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE555PSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
NE555PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
SA555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SE555DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SE555DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

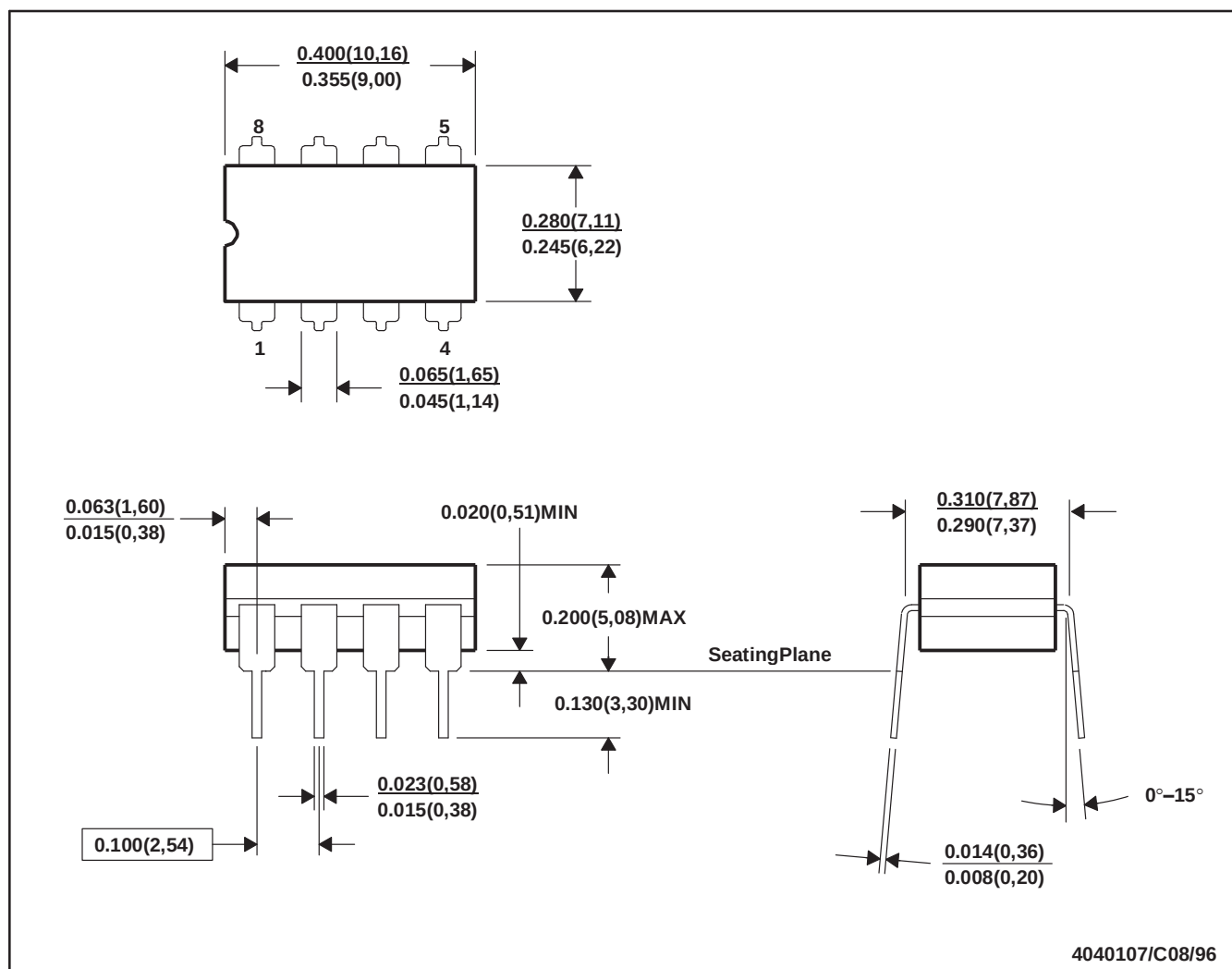


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NA555DR	SOIC	D	8	2500	340.5	338.1	20.6
NA555DR	SOIC	D	8	2500	367.0	367.0	35.0
NE555DR	SOIC	D	8	2500	367.0	367.0	35.0
NE555DR	SOIC	D	8	2500	364.0	364.0	27.0
NE555DR	SOIC	D	8	2500	340.5	338.1	20.6
NE555DRG4	SOIC	D	8	2500	367.0	367.0	35.0
NE555DRG4	SOIC	D	8	2500	340.5	338.1	20.6
NE555PSR	SO	PS	8	2000	367.0	367.0	38.0
NE555PWR	TSSOP	PW	8	2000	367.0	367.0	35.0
SA555DR	SOIC	D	8	2500	340.5	338.1	20.6
SA555DRG4	SOIC	D	8	2500	340.5	338.1	20.6
SE555DR	SOIC	D	8	2500	367.0	367.0	35.0
SE555DRG4	SOIC	D	8	2500	367.0	367.0	35.0

JG(R-GDIP-T8)

CERAMIC DUAL-IN-LINE

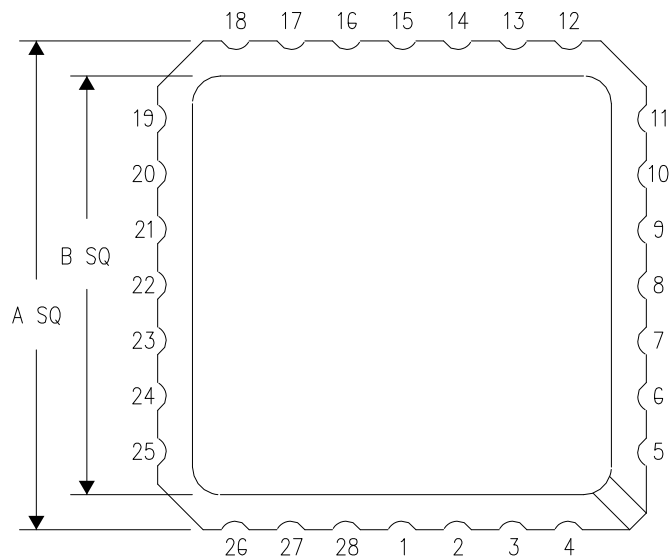


- NOTES: A. All lineardimensionsareinches(millimeters).
 B. Thisdrawingissubjecttochangewithoutnotice.
 C. Thispackagecanbehermeticallysealedwithaceramiclidusingglassfrit.
 D. Indexpointisprovidedoncapforterminalidentification.
 E. Falls withinMILSTD1835GDIP1-T8

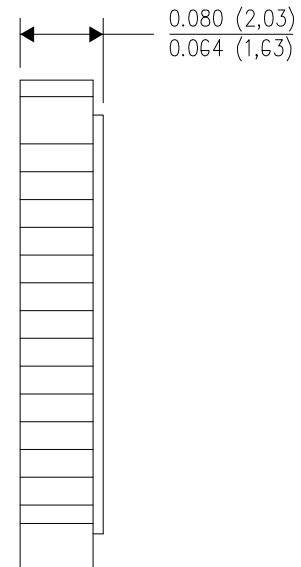
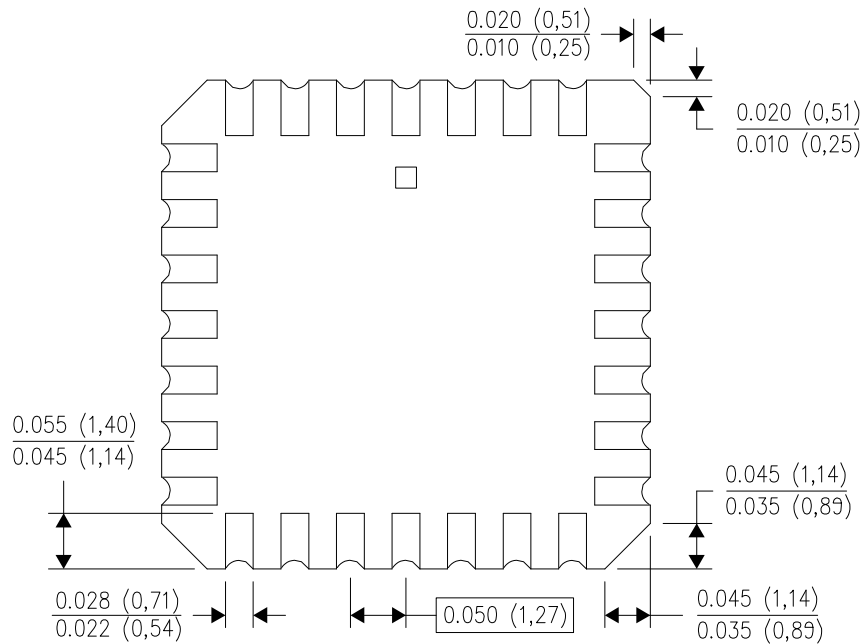
FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

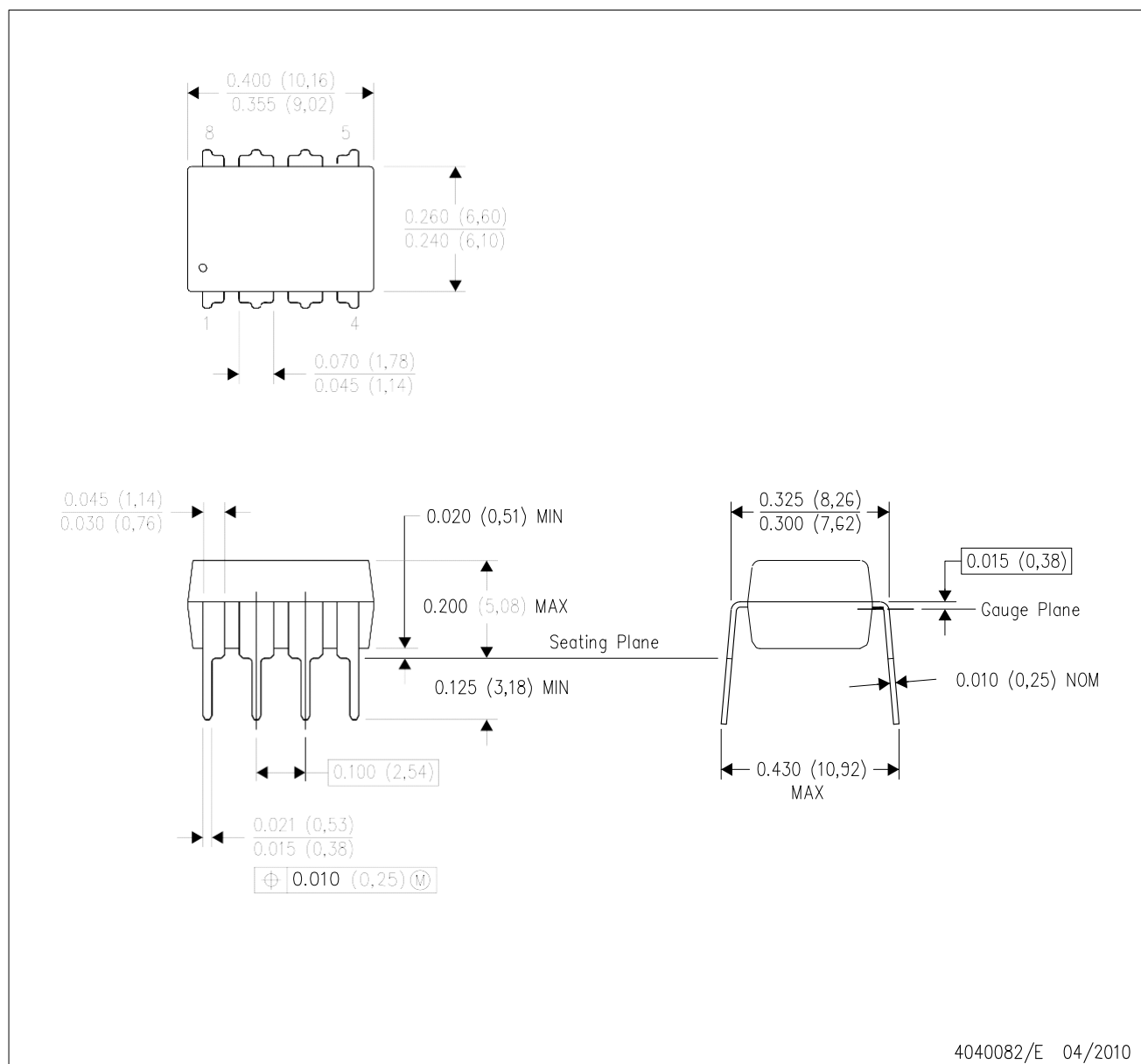


4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE

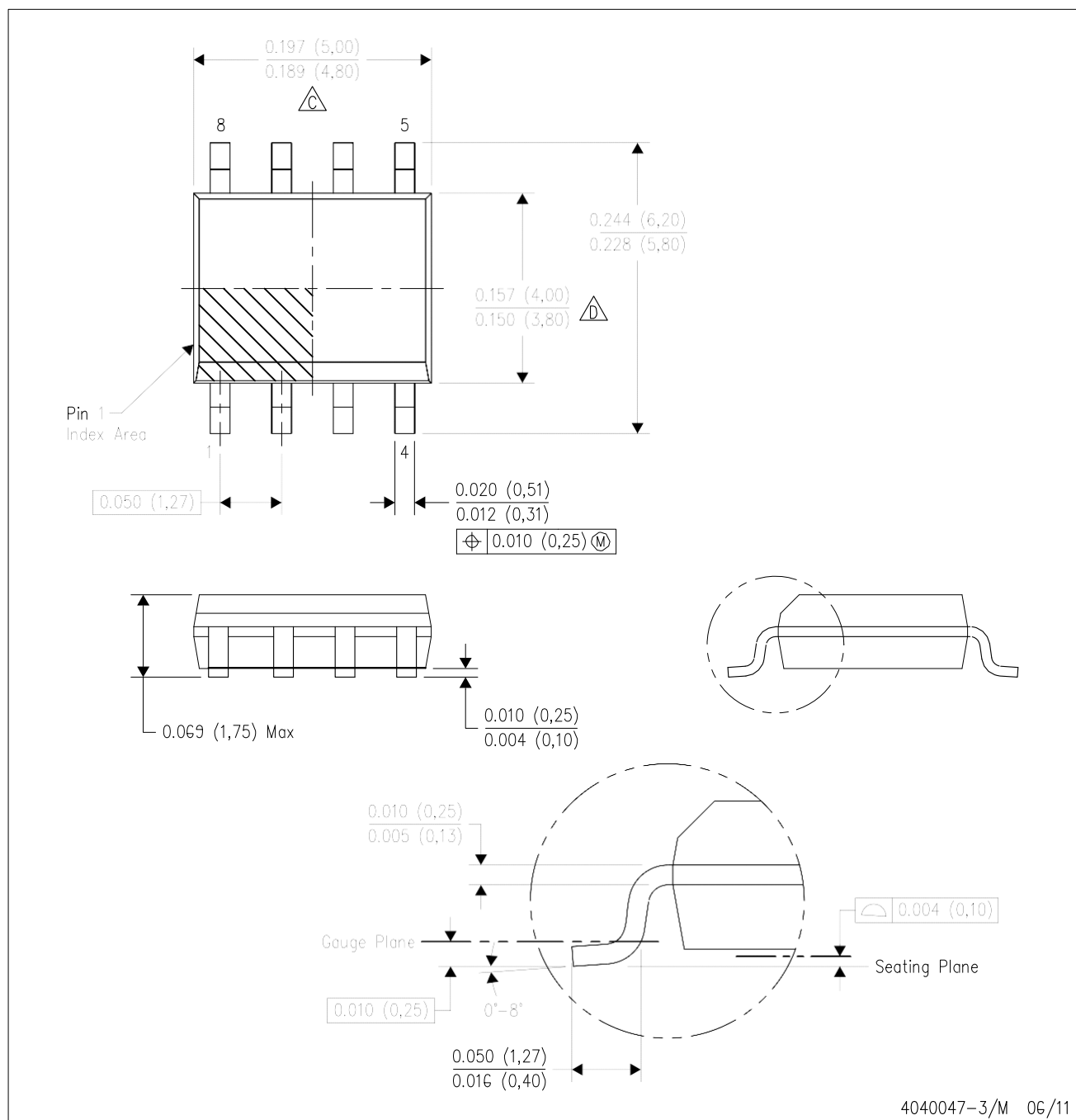


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



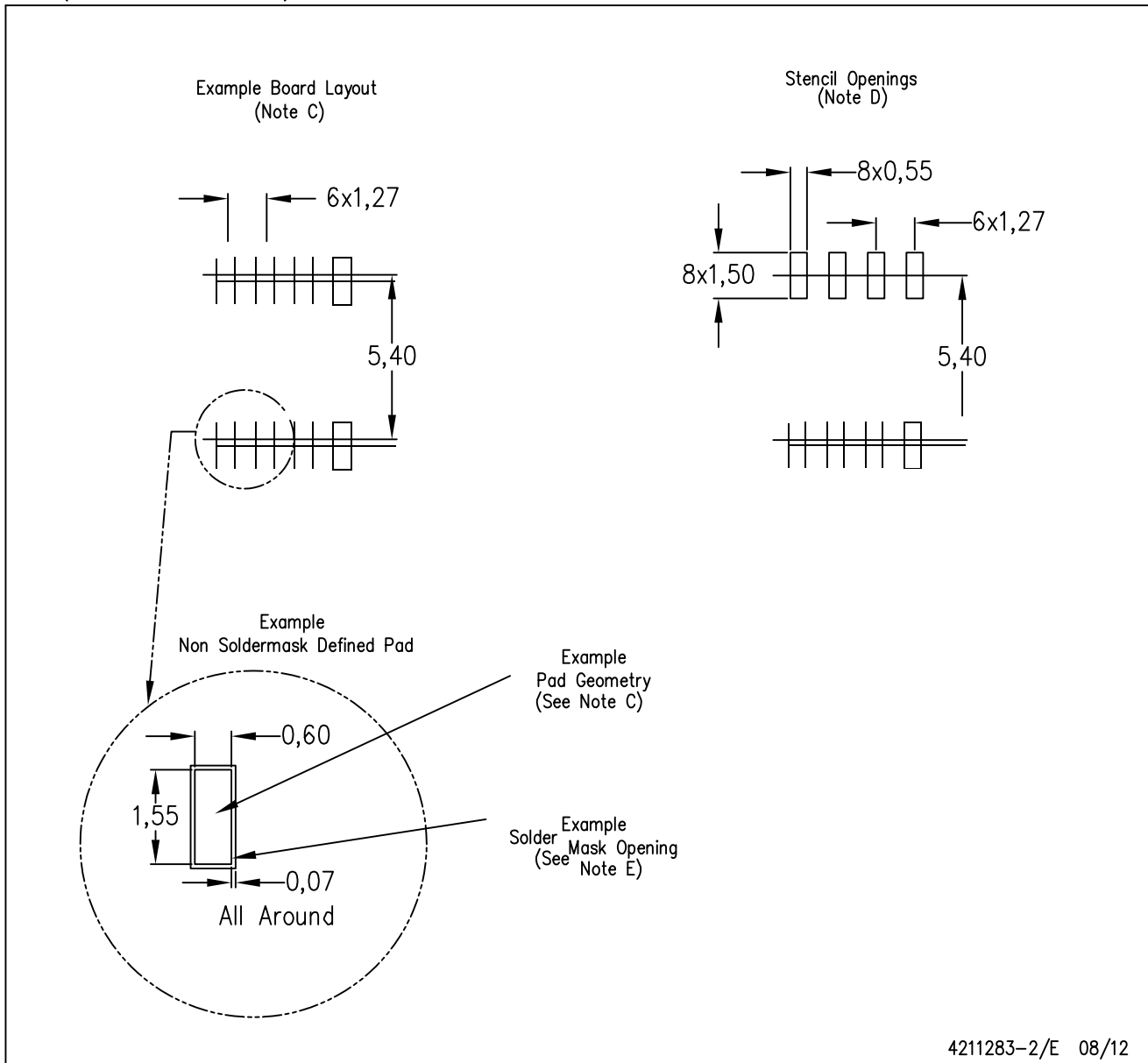
NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.



orgateburrs. Mold flash, protrusions, orgateburrrsshall

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE

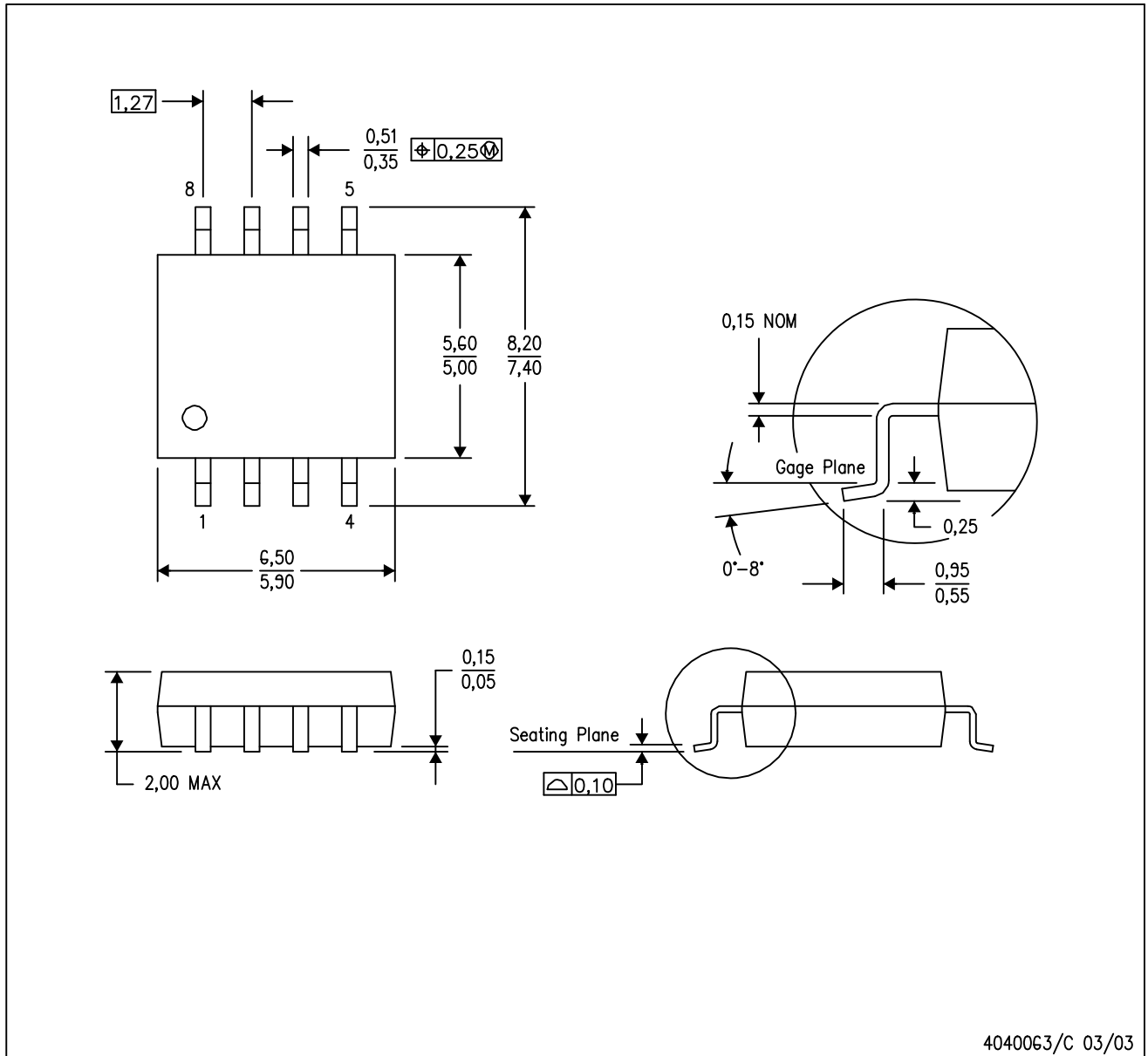


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

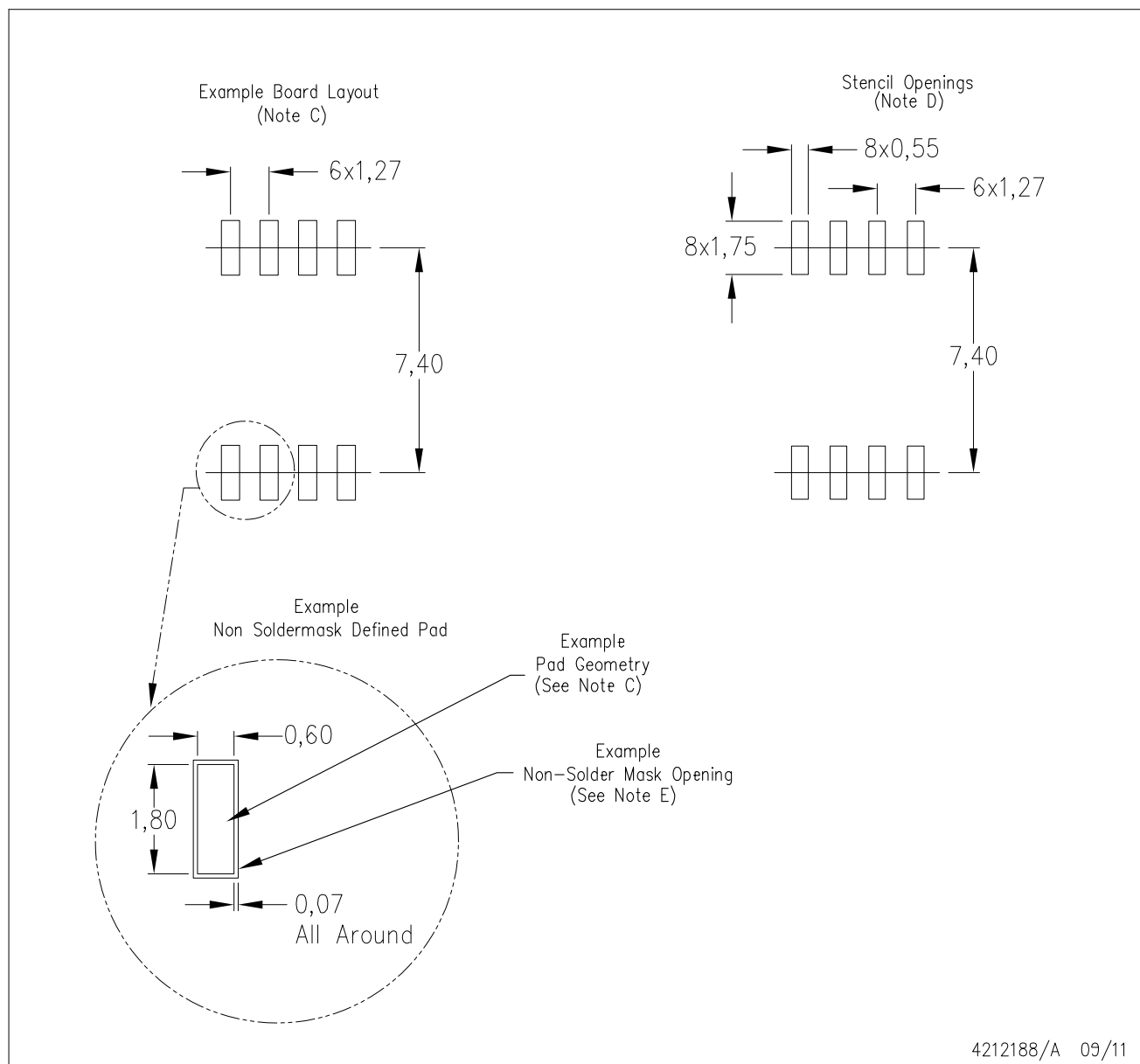


NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion, nottoexceed0,15.

PS (R-PDSO-G8)

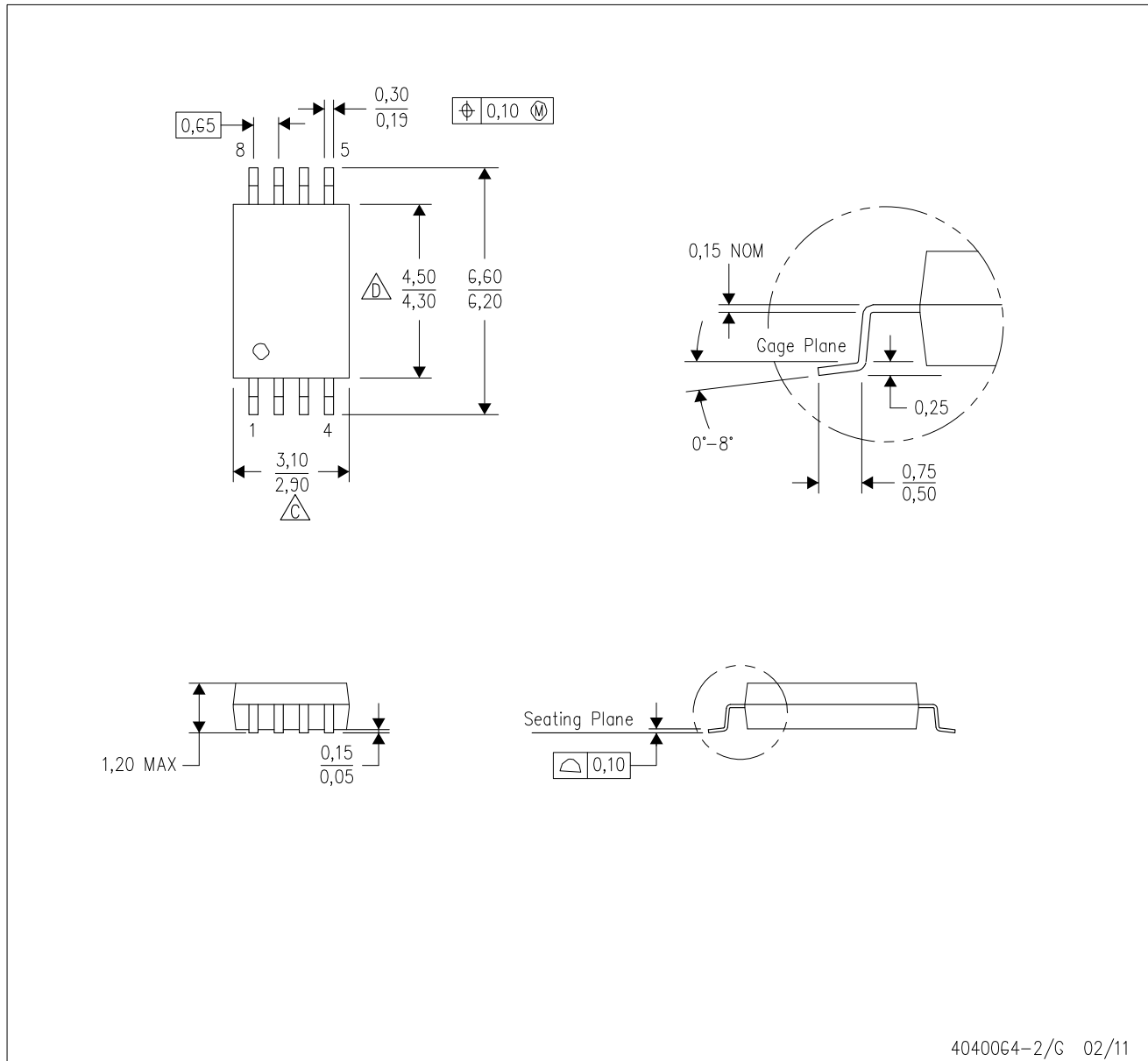
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

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CONCLUSION

The following observations can be drawn from the detailed study on PCB, The Printed Circuit Board (PCB) is very important in all electronic gadgets, which are used either for domestic use, or for industrial purpose. PCB design services are used to design the electronic circuits. Apart from electrically connecting, it also gives mechanical support to the electrical components. Thus, an effective PCB design can help in reducing the possibilities of errors and the chances of short circuit. Therefore, learning to design circuit in a PCB has great chance to explore in the field of electronics.

This eight-week training program on PCB design at INTERNSHIP AT TRAINING has been one of the most interesting, productive and instructive experience in my life. Through this training, I have gained new insight and more comprehensive understanding about the real industrial working condition and practice. It also improved my soft and functional skills.

All these valuable experiences and knowledge that we have gained were not only acquired through the direct involvement in task but also through the other aspects of training such as work observation, interaction with mentors, and others related to the laboratory.

Here I am concluding, this training program has satisfied my primary objectives, and as a result I am more confident practically and theoretically on my respective subjects, which in future will become helpful to build my career.

THANK YOU