

HIGH-PERFORMANCE PATTERN TEST GENERATOR FOR BIST

Submitted in partial fulfillment of the requirements for
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This is to certify that this Project Report is the bonafide work of **RESHMI NAIR** (38130187) and **NANDINI MAHESHWARI** (38130149) who carried out the project entitled "**HIGH-PERFORMANCE PATTERN TEST GENERATOR FOR BIST**" under our supervision from December 2021 to March 2022.

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ABSTRACT

When compared to the best-to-date built-in self-test (BIST)-based pseudorandom test pattern generators, this research proposes a low-power (LP) programmable generator capable of creating pseudorandom test patterns with appropriate toggling levels and better fault coverage gradient. It consists of a linear finite state machine (a linear feedback shift registers or a ring generator) that drives an appropriate phase shifter, and it has a number of features that allow it to generate binary sequences with preselected toggling (PRESTO) activity. We provide a method for selecting multiple generator settings automatically, allowing for easy and accurate adjustment. The generator is then deterministically guided toward test sequences with superior fault-coverage-to-pattern-count ratios using the same approach. Furthermore, by adopting the PRESTO-based logic BIST (LBIST) infrastructure, this paper offers an LP test compression approach that allows customising the test power envelope in a completely predictable, accurate, and flexible manner. The suggested hybrid approach effectively integrates test compression with LBIST, allowing both strategies to perform high-quality tests in a synergistic manner. The practicality of the suggested test systems is demonstrated by experimental results acquired for industrial designs, which are presented here.

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LIST OF ABBREVIATIONS

• DFT	⇒	Design For Testability
• BIST	⇒	Built in Self Test
• CUT	⇒	Circuit Under Test
• LFSR	⇒	Linear Field Shift Register
• BS-LFSR	⇒	Bit Swapping LFSR
• BCU	⇒	BIST Control Unit
• FPGA	⇒	Field Programmable Gate array
• RTL	⇒	Register Transistor Level
• HDL	⇒	Hardware Descriptive Language
• VHDL	⇒	Very High Speed Integrated Circuit
• ISE	⇒	Integrated Synthesis Environment
• TPG	⇒	Test Pattern Generator
• TRE	⇒	Test Response Evaluator
• FC	⇒	Fault Coverage
• BIT	⇒	Built In Test
• SFF	⇒	Scan Flip Flops

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CHAPTER 1

INTRODUCTION

In this project core goal of factory testing will stay roughly the same in the coming years, to assure dependable and high-quality semiconductor devices, test solutions may experience substantial modification. This development will be influenced by semiconductor technology, design features, and the design process, among other things. With new forms of flaws to address in order to achieve the requisite test quality for future technological nodes, such as 3-D, it's only natural to wonder what design-for-test (DFT) methodologies would be required. Test compression, which was first used a decade ago, has fast become the standard DFT approach. However, it's questionable if test compression will be able to keep up with the tremendous pace of technological development in the coming decade. Interestingly, logic built-in self-test (LBIST), which was initially designed for board, system, and in-field testing, is now being accepted for production testing since it delivers highly robust DFT and is increasingly being utilised with test compression. This hybrid technique appears to be the natural next step in DFT advancement. It has the potential to increase test quality, enhance the ability to execute at-speed power conscious testing, and lower the cost of manufacturing tests while maintaining all LBIST and scan compression benefits.

The notion of merging LBIST with test data compression has become a crucial research and development topic as attempts to overcome the bottleneck of test data bandwidth between the tester and the chip have become a vital research and development area. Several hybrid BIST methods, in instance, compress deterministic top-up patterns (used to detect random pattern resistant flaws) on the tester and then decompress these test patterns using existing BIST hardware. Some strategies use compressed weights or modify pseudorandom vectors in various ways to include deterministic stimuli. If BIST logic is used to give compressed test data, the underlying encoding algorithms often take advantage of low fill rates, as advocated in LFSR coding, which later evolved into static and dynamic LFSR reseeding. There are extensive assessments of relevant test compression methodologies available.

Due to the high data activity involved with scan-based test procedures, hybrid systems, like traditional scan-based test, may consume far more power than a circuit under test was designed to operate under. Reductions in the operational power of ICs in a test mode have been a source of worry for years due to overstressing devices beyond the mission mode.

Full-toggle scan patterns can consume many times the power of a normal functional mode, and this tendency is expected to continue, especially at the mission mode's peak power. Thermal difficulties, voltage noise, power droop, or high peak power over numerous cycles may result in yield loss due to quick device damage, severe drop in chip dependability, reduced product lifespan, or device malfunction due to timing faults following a considerable circuit delay increase. Fully functioning chips may also fail during testing due to phenomena such as IR-drop, crosstalk, or a di/dt issue caused by abnormal switching activity. Power reduction strategies for scan testing have been created in a variety of ways. There are ways designed for BIST to maintain the average and peak power below a certain level among them. For example, by preventing transitions at memory elements from propagating to combinational logic during scan shift, the test power can be lowered. This is accomplished by putting gating logic between the scan cell outputs and the logic they control. This logic is visible during regular operations and capture. Scan cells with gates have also been proposed. In a synergistic test power reduction solution, available on-chip clock gating circuitry is used to selectively block scan chains, while test scheduling and planning are used to reduce BIST power in the Cell processor.

Not all created vectors, which are typically quite long, detect faults, a test vector blocking system of masks is used to examine patterns generated by an LFSR. Eliminating such tests can minimise switching activity while leaving fault coverage unaffected. The introduction of low-transition test pattern generators has given power conscious BIST solutions a whole new dimension. An LFSR, for example, is used to feed scan chains via biassing logic and a T-type flip-flop in one of the devices shown. The same value is continually scanned through scan chains until the value at the output of biassing logic (e.g., a k-input AND gate) reaches 1.

Depending on k , the number of transitions at the scan chain inputs can be greatly reduced.

A dual-speed LFSR is made up of two LFSRs, one for standard clocks and the other for slow clocks. The circuit inputs coupled to the slow-speed LFSR have less switching activity, but the overall design still provides enough fault coverage. As illustrated, mask patterns reduce switching activity in LFSR-produced patterns, but bit swapping accomplishes the same result at CUT's major inputs. A gated LFSR clock allows only half of the LFSR stages to be activated at a time. Only half of the circuit inputs change every cycle, which reduces power usage. As proven, combining a low transition generator (managing easy-to-detect faults) with a 3-weight pseudorandom test pattern generator (PRPG) (detecting random pattern resistant faults) can minimise BIST switching activity.

LFSR-generated sequences are monitored statistically and transitions are suppressed by introducing intermediate and strongly correlated patterns. Finally, in a parallel BIST context, a random single-input change generator may yield low power patterns. Because the BIST power consumption while testing at speed can rapidly surpass the maximum ratings, scan patterns must be shifted at a programmed low speed, with just the final few cycles and the capture cycle applied at the maximum frequency. Typically, five consecutive clock cycles are employed in the burst-mode technique provided. The first four cycles are for shifting purposes, while the fifth and final cycle is for capture. Before applying the last shift and capture pulses, which are crucial for at-speed testing, the goal is to stabilise the power supply. A burst clock controller slows down portion of the shift cycles to prevent voltage droop caused by increased circuit activity. It permits a progressive rise in circuit activity, lowering the di/dt impact.

Depending on the necessity for progressive circuit warming, the controller can gate the shift clocks. Low power (LP) test compression techniques use LFSR reseeding to decrease scan-in transitions since low fill rates allow identical test data to be sent to scan chains directly from the decompressor for a period of shift cycles, lowering the number of transitions. Because the input vectors in functional mode are frequently closely coupled compared to statistically independent sequential input vectors during testing, power dissipation during test mode might

be much higher than in functional mode. Zorian demonstrated that the test power might be twice as high as the usual mode power. In hand-held electronic devices with built-in self-test (BIST) circuits for periodic self-test, test power is an essential design consideration to extend battery life. Reduced test power of a module permits concurrent testing of several integrated cores in an IC, therefore it's also necessary to lower test costs. By producing a reduction in supply voltage, increased peak power is likely to cause noise difficulties in a semiconductor. During the test, lowering the peak and average power helps to increase the test's reliability and yield. As a result, it's critical to keep power dissipation low during the test mode.

Scan architectures are a popular way to test digital circuits using the Design for Testability (DFT) method. Power is dissipated in both the sequential scan parts and the combinational logic during test application in a scan-based circuit. The impact of scan-ripple propagates to the combinational block as scan values are put into a scan chain, and redundant switching occurs in the combinational gates during the scan-in/out time. It is estimated that the combinational block alone dissipates around 78 percent of total test energy. As a result, strategies to decrease power dissipation in the combinational block should be addressed in a low-power scan design. A lot of study has gone into finding effective ways to minimise test power in scan-based circuits. In order to reduce power dissipation during scan testing, Wang et al. suggested an automated test pattern generating approach to redesign test vectors. Repetitive transitions in combinational logic can be mitigated, but not totally avoided, using their automated test pattern generation (ATPG).

Furthermore, in order to trade off power, test application time may rise. For test power reduction, scan-latch reordering or input vector reordering approaches have been suggested. These strategies, on the other hand, are aimed at reducing transitions at the output of scan flip-flops and are unable to reduce redundant switching in the combinational block. Whetsel proposed a method for lowering average and peak power consumption by converting traditional scan architecture into a desired number of selectable, distinct scan routes. Each scan route is loaded with input and then depleted of responses in turn. Sankar lingam et al.

advocated deactivating the scan chain selectively during external testing to solve the peak power problem. The test set is constructed and organised in this fashion such that only the changing sections of successive tests are relocated into the scan chains. The authors propose adopting scan chain partitioning to prevent peak power violation during both the shift and capture cycles.

Inserting blocking logic into the scan flip-flops' stimulus path to prevent scan ripple effect propagation to logic gates is a simple and effective way to dramatically lower test power, regardless of test set. Werstendorfer et al. suggested a blocking approach based on NOR or NAND gates in. The test enable signal controls blocking gates (of the types NOR or NAND), and the stimulus pathways remain locked at either logic "0" or logic "1" throughout the scan shift operation. Multiplexers at the output of the scan cells were employed by Zhang et al. to hold the prior states of the scan register during shifting, preventing activity in combinational logic.

A scan hold circuit as a sequential element is another approach for reducing combinational power utilising blocking. This approach is known as enhanced scan [9], and it aids in the latency of fault testing by permitting the use of any two-pattern test. Each sequential element in a scan-hold design has an extra storage cell called the hold latch, and the stimulus path for the combinational section is coupled to the output of the hold latch, which is not utilised in scan shifting. As a result, superfluous switching in combinational logic is avoided.

A system-on-a-chip (SoC) often has memory cores, processor cores, interface cores, mixed-signal, and analogue cores, all of which have been predesigned and prevalidated. The SoC design approach boosts the designer's productivity, but it also raises the chip's test complexity and reduces the cores' accessibility to chip pins. To test the chip, additional test pins and a larger ATE-chip bandwidth are required to keep test times short, while higher timing resolution is required to minimise yield loss. The ITRS roadmap expects a considerable cost rise for ATE capable of testing the next generation of systems-on-a-chip, making it more appealing to invest in approaches that complement ATE.

Design-for-testability, design and test automation tools, and ATE architecture are three areas where the test complexity problem might be solved. The solution given here handles all three issues at the same time. The application of a test set created by an ATPG tool optimised to limit the number of test patterns by statically and dynamically compacting test vectors in order to reduce test application time and storage needs for the ATE is a typical test approach. A designer must now choose between utilising advanced ATPG tools to generate very small test sets and using a strong ATE architecture. Lower limitations of compressed test set minimum sizes demonstrate that upgrading ATPG algorithms alone will not considerably reduce test data volume, i.e., addressing merely the field of design and test automation tools will not enough.

Some Built-In-Self-Test (BIST) approaches use a concise representation of the test patterns to produce the test patterns on-chip¹. These encoded test data may also be saved on an ATE, resulting in a significant reduction in test data storage. In order to achieve greater compression of the test patterns, a specialised ATPG algorithm for these BIST schemes was devised. The tool creating an encoded representation of the deterministic patterns must make a trade-off between the size of the test pattern generator, the ATE storage need, the test duration^{2,3}, and the test production time. The LFSR-based techniques compress data well and may be used in standard-scan designs, but they require test controllers and on-chip pattern generators.

Furthermore, because linear dependencies may prevent the production of certain test patterns with the provided LFSR, a little modification in the test requirements and test set after tape out may be difficult. RESPIN (Reusing Scan Chains for Test Pattern Decompression IoN) is a novel test architecture that was just introduced. A series of precomputed test patterns is applied to a core under test in the RESPIN architecture, which are produced from encoded test data stored on an ATE. In terms of space and control overhead, the RESPIN design is equivalent to systems that include a testwrapper on each core and use a test access method to apply condensed test sets to each embedded core (TAM). It is comparable to BIST techniques in terms of ATE storage and ATE-chip bandwidth needs.

The advantages of built-in self-testing techniques are well known. They include, among other things, field reusability, cost savings for automated test equipment (ATE), excellent coverage of non-target problems, and IP protection. Because BIST is applied outside to the scan chains in a BIST method like STUMPS (Self-Test Using MISR and Parallel Shift register sequence generator), its influence on design cost is minimised. The ATE is in charge of the test session and reads out the results. The scan chains are loaded across numerous scan clock cycles, with each clock producing a vector of k bits that is shifted into the chains by the shift register SR. t vectors are put into the chains to construct a complete test pattern, with t being the maximum scan chain length.

The advantages of built-in self-testing techniques are well known. They include, among other things, field reusability, cost The scan flip-flops have collected the response bits of the core-under-test (CUT) after a system clock cycle, which are unloaded into the MISR with the following t scan clock cycles. Built-in self-test (BIST), also known as serial or scan-based BIST, is an ideal solution for the issues of today's integrated circuit testing. Even for externally inaccessible components in complicated systems-on-a-chip, the built-in capabilities of test pattern development and test response assessment enable for an efficient test (SOCs).

The traditional architecture, which uses an LFSR to feed pseudo-random patterns into the scan route, is simple to construct and has a low impact on system performance. A variety of sophisticated strategies have been developed in the literature to tackle the problem of random pattern resistant defects.

These methods include anything from test point insertion to weighted random pattern and mixed mode testing, and they all have various trade-offs in terms of fault coverage, hardware overhead, performance degradation, and test time. Mixed mode systems employ a small number of pseudorandom patterns to remove faults that are simple to detect, and deterministic patterns to conceal the remaining defects that are resistant to random patterns. The deterministic patterns are compressed on the chip and then expanded during BIST ("store and generate"), or they are immediately incorporated into an LFSR sequence using "bit-fixing" or "bit-flipping" techniques.

The BIST design, on the other hand, is particularly specialised to the individual circuit, and changing the test set necessitates resynthesis of the whole BIST hardware. The store and produce techniques provide a cost-effective option for applications that require a more flexible BIST architecture. Simple test pattern generators, such as LFSRs, multiple polynomial LFSRs, counters, or twisted ring (Johnson) counters, are used to encode deterministic patterns (or groups of patterns). The amount of test data necessary to evaluate more sophisticated system-on-chip (SOC) designs is quickly rising, outpacing ATE capabilities (automated test equipment).

The usage of built-in self-test is a well-known solution to this problem (BIST). On the semiconductor, BIST entails test pattern creation and output response compression. Pseudorandom pattern testing is used in the most cost-effective BIST methods. However, because of the prevalence of random-pattern-resistant (r.p.r.) faults, pseudo-random pattern testing often does not offer adequate fault coverage. Two options are there for dealing with this issue. The first is to alter the circuit by installing test points to minimise random pattern resistance, and the second is to modify the test pattern generator by adding additional hardware to produce patterns that identify hard defects. Both strategies have severe flaws. Inserting test points necessitates changing the function logic, which can reduce system performance, and changing the test pattern generator can necessitate a significant amount of extra silicon space.

A hybrid strategy combining external testing with BIST can be used to decrease the hardware overhead for BIST. To accomplish the necessary fault coverage, a "hybrid BIST" system combines certain external data from the tester with the BIST hardware. In comparison to complete external testing, a hybrid BIST scheme reduces the amount of test data retained on the tester, but it does not require as much hardware as full stand-alone BIST. A basic BIST approach is to apply pseudo-random patterns to identify random pattern testable faults using a STUMPS architecture, and then use deterministic vectors from the tester to discover random pattern resistant (r.p.r.) faults using deterministic vectors from the tester. When compared to standard external testing, the results of employing this

approach on big industrial designs reveal that it only provides a 30-50 percent reduction in tester storage needs. Using hybrid patterns, folding counters, two-dimensional compression weighted pattern testing, and RESPIN, more advanced hybrid BIST systems have been constructed.

As the size and complexity of systems-on-chip (SOCs) develop, power dissipation during testing becomes a serious issue. There are more transitions in the flip-flops during scan shifting than during regular functional operation. When pseudorandom filling of the unassigned input values is used, the problem becomes even worse. Excessive power dissipation during testing can raise production costs by necessitating the adoption of more costly chip packaging or resulting in unneeded yield loss. A novel test-data-compression strategy based on linear feedback shift register (LFSR) reseeding is suggested in this study, which dramatically decreases power usage during testing.

As the size and complexity of chips have expanded, so has the volume of test data. As a result, a lot of effort has gone into developing test-data compression algorithms that may be utilised to minimise tester storage and bandwidth needs. Commercial test data compression technologies based on LFSR reseeding have been launched, including Mentor Graphics' Test Compress, Synopsys' SOC BIST, and Logic Vision's ELT-Comp. The primary idea behind LFSR reseeding is to enlarge seeds to create deterministic test cubes.

A seed is the LFSR's starting state, which is enlarged by executing the LFSR. A similar seed may be calculated from a deterministic test cube by solving a sequence of linear equations (one equation for each specified bit) based on the LFSR's feedback polynomial. Because just 1%–5% of the bits in a test vector are normally defined, the majority of bits in a test cube do not need to be taken into account when a seed is generated because they are don't care bits. As a result, the size of a seed is significantly lower than that of a test vector. As a result, reseeding can drastically minimise the amount of test data stored and bandwidth used.

Several strategies for reducing test storage have been offered. The first was introduced in, where it was demonstrated that if s_{max} is the highest number of

specified bits in any test cube, then for an LFSR of length $s_{max} + 20$ bits, the chance of not being able to identify a seed for any test cube is less than 10^6 for an LFSR of length $s_{max} + 20$ bits. To improve the encoding efficiency of the basic system, several techniques have been proposed, such as using multiple-polynomial LFSRs, test cube concatenation, and variable-length seeds.

Dynamic LFSR reseeding, in which the seed is progressively updated while the LFSR runs, has been the subject of more recent research. The size of a seed doesn't depend on s_{max} in dynamic LFSR reseeding, hence it can be any size. Recent research has focused on dynamic LFSR reseeding, in which the seed is changed progressively as the LFSR runs. The size of a seed does not rely on s_{max} in dynamic LFSR reseeding, hence it can be even less than the size of an LFSR. While reseeding is a good way to condense test data, it is wasteful in terms of power consumption. When moved into a scan chain, the don't care bits in each test cube are filled with random values, resulting in excessive switching activity. Only a small number of flip-flops make transitions throughout each clock cycle in normal operation.

When scanning test vectors with random values filled in 95 percent–99 percent of the bits, however, a substantial number of the flip-flops will undergo transitions, resulting in excessive power consumption throughout the test. Because the chip may be built to only manage power usage during normal operation, high power consumption during testing may cause overheating. Reduce the scan frequency as a remedy to this problem; nevertheless, this results in longer test periods. The automated test equipment (ATE) used to test today's integrated circuits is being strained by higher circuit density and increased design complexity (ICs).

The incorporation of complicated embedded cores in system-on-a-chip (SOC) designs has resulted in a considerable rise in test-data volume, necessitating a significant increase in ATE channel memory depth. Another restriction encountered in the testing of SOC's with high clock rates, big test-data volumes, and a large number of I/O pins is ATE channel bandwidth. To address these concerns, the literature has presented a number of solutions based on test-data compression, built-in self-test (BIST), and a combination of the two's. A

deterministic test set is compressed and stored in ATE memory using the test-data compression technique. The compressed test set is sent to the IC through ATE channels, where it is decompressed and decoded before being applied to the circuit under test (CUT) via decoding hardware. Run-length coding techniques based on statistical coding To minimise test data storage, Golomb coding, frequency-directed run-length (FDR) coding, and variable-input Huffman coding (VIHC) coding. Techniques for reducing test data capacity based on on-chip pattern decompression are also discussed. The renewed interest in test-data compression has resulted in the development of new commercial solutions that can compress huge industrial designs significantly. The IBM OPMISR and Smart BIST tools, as well as Mentor Graphics' Test Compress tool, employ test-data compression and on-chip decompression to minimise test-data volume and testing time. Test patterns are created by an on-chip pseudorandom pattern generator, which is often a linear feedback shift register, in BIST solutions (LFSR).

BIST solves a variety of test interface issues, including as signal bandwidth limitations and a large pin count. Techniques based on test point insertion, reseeding, bit-flipping, bit-fixing, and weighted random pattern testing have been proposed to identify random-pattern resistant defects and obtain comprehensive coverage of single stuck-at faults. To increase random pattern testability, test point insertion approaches necessitate design adjustments such that 100 percent fault coverage may be obtained with an acceptable amount of pseudorandom test patterns.

The other BIST procedures are nonintrusive in that they generally apply a small number of random patterns; for the remaining hard-to-test defects, deterministic test patterns are acquired by modifying the state of the pattern generator or changing the pattern generator's output. A number of research on the usage of logic BIST for large industrial circuits have recently been published. Recently, techniques using a mix of data compression and BIST have been developed. To achieve 100 percent fault coverage, the hybrid BIST approach introduced in uses a weighted pseudorandom patterns circuit. The compressed weight set is kept on the ATE, and it is decompressed using an on-chip look-up table. Statistical coding is used to condense the seeds for the LFSR.

CHAPTER 2

LITERATURE SURVEY

S. Pathak, et.al [2017] ; The author introduced a novel approach to scan cell stitching based on logic cluster controllability (LoCCo). By identifying flip-flops which would require more test combinations to test the logic and the creator called them as flip-flops of higher controllability. Further, these Flip Flops were then placed at the beginning of scan chains while flip-flops with lower required combinations or lower controllability flip flops are placed at the end of the circuit. It is, therefore, needed to have a solution that does not increase the hardware cost and keeps the software iterations to a minimum. Therefore, the creators intention was to provide the same by their new power-aware scan stitching method.

S. Ukey, et.al [2016]; S. Ukey, S. Rathkanthiwar, and S.Kakde, [April 2016], In this paper the authors proposes a novel scanning cell architecture for low power scanning technique that provides combined solution to reduce total average power in both combined part and scan cell during acquisition mode and move mode. Thus the novel method instigates implemented on the different combinational Tanner circuits and the experimental results were observed. It is inferred by the creators to save total average power in shift and capture mode to about 20%.

S.A.Pathak, et.al [2016]; The author proposed a designs verifications are growing in complexity, chip design cycle is desired to be shorter. Hence, methods has been implemented by the designers The scope of the work is also extended to reduce the cycle time of a derivative product from a base design. The author describes a technique which can modify the existing spare cells in the design for logic corrections or modifications during ECO.

Sungyoul, et.al [2015]; The author rectified two main problems with low power testing. These two questions must therefore be treated differently. Thus the creator aimed blocking the malfunction during at-speed testing, the capture Power must be lowered not to generate excessive IR-drop and resulting . The major point is to capture power and shift delay in a nutshell the scan chain reordering (SR)-aware X-filling and the low power scan stitching, are specifically introduced to serve this purpose.

Satyadev Ahlawat and Jaynaryan Tuduseri[2010]; The author tried to scan design has become the de-facto design for testability technique. Ease of testing and high test coverage widely accepted by the industry Those scan-shift transitions can be further reduced by selectively using the inverse connections between scan cells. In addition, the trade-off between routing overhead and power consumption can also be controlled by the proposed scan-cell reordering techniques.

Elif Alpaslan, et.al [2010]; In this paper the author, propose a DFT-based approach for reducing circuit switching activity during the scan shifting process. Instead of inserting additional logic at the gate level which leads to introducing extra delay on critical paths, this method modifies the design at the register transfer level (RTL) and uses the synthesis tools to automatically deal with timing analysis and optimization.

Y.Z.Wu and M. C. T. Chao[2010]; In this author did a common practice to lower the power consumption during scan-based testing is to reduce the number of scan cell's signal transitions, which can be classified into the following three types: (1) capture transitions and (2) scan-out transitions. Hence, to reduce these critical problems the scan shift is combined with a pattern-filling technique. In addition, the trade-off between routing overhead and power consumption can also be controlled by the proposed scan-cell reordering techniques.

M. Elm, et.al [2008]; The author focuses on power consumption during the test. An effective power-saving technique when analyzing testicles is to shut down unused analysis chains. It is not dependent on a test set and can improve the performance of any test power reduction technique as a result. The approach does not specify any sorting within strings and fits well with any standard scanning string integration tool. The approach produced but the proposed system does not imply any scan chain reordering but partitions the flip flop into sets.

J.T.Zhang and Q. Zuo[2007]; The author found the requirements for testing these portable products are so strict since the test power dissipation and reliability directly determine the quality of chips. In this paper, the MPC-SCAN (Multi-phase clock scan) technique has been proposed to reduce the average as well as the peak power of multiple scan circuits in a device. Unlike those previous methods

proposed , MPC-SCAN technique has many unique advantages which maintains the fault coverage and dissipation limits.

Swarup Bhunia, et.al [2005]; In this paper the author discusses about the power dissipation during test mode can be significantly higher .The author showed that the test power could be twice as high as the power consumed during the normal mode. Therefore the main concept is that test power is an important design concern to increase battery Adding an extra transistor in only one logic level renders significant advantages with respect to area, delay, and power overhead compared to existing methods, which use gating logic at the output of scan flip-flops. Simulation results proposed by the author signifies ISCAS89 benchmarks show an average improvement of 62% in area overhead, 101% in power overhead (in normal mode), and 94% in delay overhead, compared to the lowest cost existing method.

Min Hao Chiu and J.C.M.Li[2005]; This paper presents a Jump scan technique or also know as a J-scan technique for low power testing. The J-scan/Jump Scan shifts two bits of scan data per clock cycle so the scan clock frequency is reduced without evaluating the test time. Consecutively, the experimental data show that the proposed technique effectively reduces the test power by two thirds compared with the traditional MUX scan. The presented technique requires very few changes in the existing MUX-scan design for testability methodology and needs no extra computation. The penalties are area overhead and speed degradation.

Kenneth M. Butler, et.al [2004]; In recent years structural (mostly scan-based) tests have come to be the predominant procedure for mass IC production. When adding speed structural tests to the standard production tests presents an series of new problems. In this paper, the author will begin by presenting pattern generation approaches to minimize power consumption that would be used if power-related problems were discovered after design completion. Hence investigates various heuristics for modifying test content to address power concerns.

S. Ghosh and N. A. Touba[2003];Two of the main drawbacks of scan testing are the power dissipation and the area overhead. In CMOS circuits, power dissipation is proportional to the amount of switching activity that takes place. During scan

testing, a much larger percentage of the scan cells will change value. In order to overcome this defect the paper focuses on technique for minimizing power dissipation that is also capable of reducing the circuit head area, relative to a random order of scan cells for a given set of test vectors. The experiments show that with a proper choice of the parameter λ , the creators algorithm is quite effective in reducing the power in a circuit.

P.Gupta, et.al [2003]; A scan chain is commonly used to implement the shift registers that store the input and output vectors during the testing phase of manufacturing. In this paper a routing-driven and timing-aware methodology for scan insertion with minimum wirelength is used. We take into account timing slacks at all sinks that are affected by scan insertion, to achieve a scan chain ordering that meets timing and has smallest wirelength. For the case where sink timing is not met, we also propose a buffer insertion methodology with minimum wirelength objective. The key contribution of this paper is a method to compute a timing-driven incremental connection suited to scan insertion.

Patrick Girard [2002]; Production of current efforts by the creators are focused on leveraging the available on-chip scan design for-test (DFT) capability to afford effective and low cost structural timing tests based on the transition delay fault (TDF) gate delay and path delay fault models. He started with a discussion of power consumption which provides the reasons and consequences for the increase in power during the test. Thus concludes it with a discussion of the opportunity to use such techniques in varying situations.

Y. Bonhomme, et.al [2002]; With ever decreasing geometry sizes and increasing clock speeds, ascertaining correct operation of digital circuits at the desired speed becomes a necessity rather than an option to maintain the quality level of the product. Detecting a delay fault normally requires the application of a pair of test patterns. Reductions of average and peak power consumption during scan testing are up to 58% and 24% respectively for experimented ISCAS benchmark circuits.

Chein-Chung Tsai, et.al [2002]; this paper the author presents a methodology to insert scan paths in a functional Register Transfer Level also known as (RTL) which specifies a design that can damage existing functional paths between sequential elements in the original circuit for establishing scan chains. . This may

prove to be very expensive cause of re optimization. Scan path insertion at Register Transistor Level is a step towards achieving RTL DFT.

M. Bushnell and V. Agrawal [2000]; A client intercession based progressed method for the recognition of the effectiveness of the ILS architecture depends on the actual configuration of individual scan chains. Consecutively, results on the ISCAS'89 benchmark circuits show that the proposed ILS configuration method can achieve on an average 5% more fault coverage in the Broadcast Mode and an average 15% more reduction in total test data volume and test application time than the existing methods.

R. Sankaralingam and N. A. Toubia [2000]; has introduced a compaction procedure which can be used to find a minimal set of scan vectors that satisfies constraints on both average power and peak power. This proposed mechanism is simple yet effective and can be easily implemented and used in the conventional test vector generation flow which is increasingly used in industries today. And also controlled or minimized the amount of heat that can be safely dissipated without damaging the chip.

S. Gerstendorfer and H.-J. Wunderlich [1999]; Power dissipation is a major concern for many designers. Power supply and packaging of a circuit are cost-intensive parts which must be sized corresponding to the peak power consumption and power dissipation during BIST limits the optimization potential of so-called "low power" designs. Secondly, It shorten the life of batteries. The authors use the switching activity of the circuit nodes as a metric for the energy consumption since in static CMOS circuits the switching energy contributes to over 90 % of the total energy consumption

L. H. Goldstein and E. L. Thigpen [1980]; A method for analyzing the testability of digital circuits was described in detail. This paper describes the SCOAP program implementation of the testability analysis algorithms at Sandia Laboratories. First, related work in the area of design for testability is summarized. Next, the test-ability analysis method is reviewed. Two major approaches have emerged in recent years to facilitate the development of testable structured design for testability and testability measure analysis.

CHAPTER 3

OBJECTIVES AND AIM OF THE PROJECT

3.1. OBJECTIVES

- ☐ To reduce the power and power delay product in BIST for low power application.
- ☐ To compare the characteristics of MOSFET technology in terms of power, delay and energy.
- ☐ To identify the feasibility of high performance test pattern generator for BIST.
- ☐ To increase the efficiency of test pattern generator for BIST.

3.2. AIM

In order to assess the efficiency of the test pattern generator, it should be examined and modified in terms of power, delay, and power delay products.

CHAPTER 4

METHODOLOGY OF THE PROJECT

4.1 METHODOLOGY

A PRESTO generator has an essential structure. The generator's kernel is an n-bit PRPG coupled to a phase shifter feeding scan chains, which creates real pseudorandom test patterns. A linear feedback shift register or a ring generator can be used to construct a PRPG. The placement of n hold latches between the PRPG and the phase shifter, on the other hand, is more crucial. The matching stage of an n-bit toggle control register controls each hold latch individually. As long as the enable input is asserted, the supplied latch is transparent for data travelling from the PRPG to the phase shifter, and it is said to be in toggle mode. When the latch is turned off, it catches and saves the relevant bit of PRPG for a number of clock cycles, giving the phase shifter a constant value (and potentially certain scan chains). For the time being, it has been placed on hold. It's worth noting that each phase shifter output is created by XORing the outputs of three different hold latches.

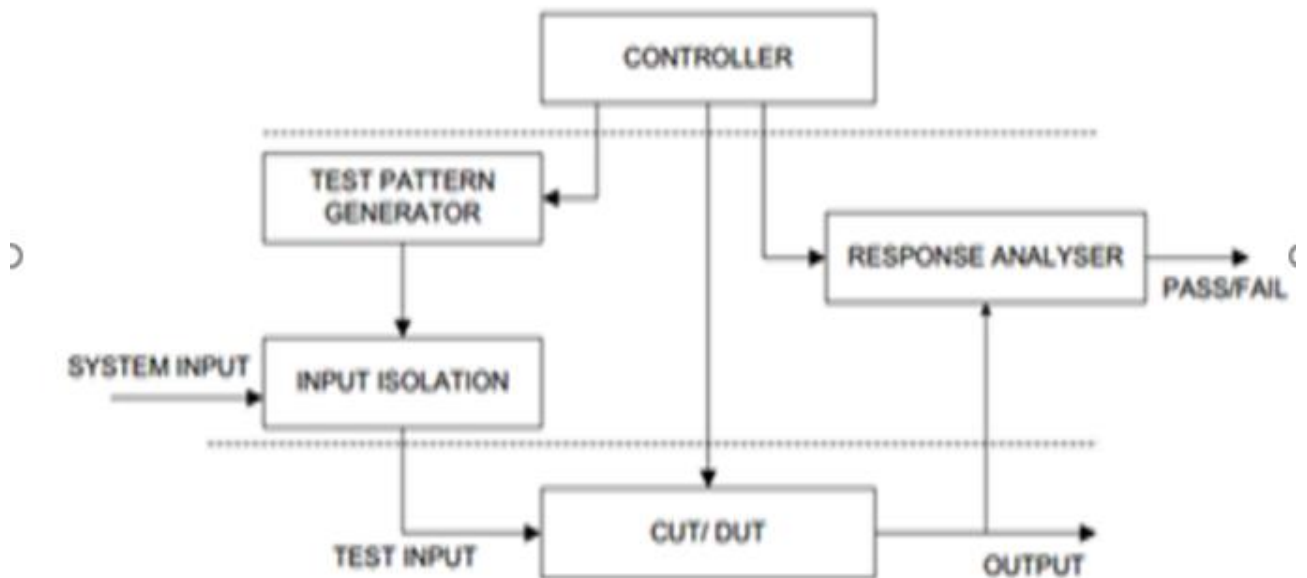


Fig.4.1. Internal block diagram of the circuit

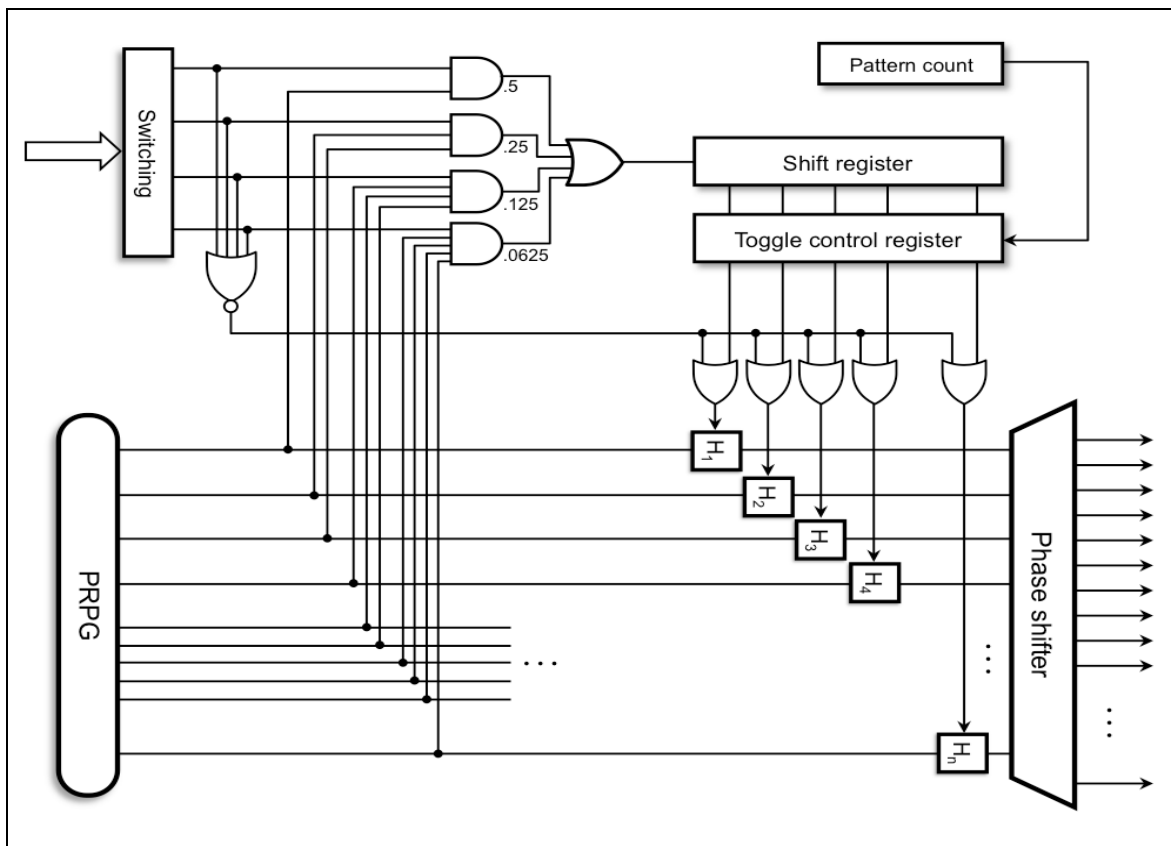


Fig.4.2. Basic architecture of a PRESTO generator.

As previously explained, the toggle control register supervises the hold latches. Its data is made up of 0s and 1s, with 1s representing latches in toggle mode, rendering it invisible to PRPG data. The fraction of scan switching activity determines the activity. The control register is reloaded with the contents of an additional shift register after each pattern. The enable signals sent into the shift register are produced probabilistically using the original PRPG with a variable set of weights. To compute the weights, four AND gates yield 1s with probability of 0.5, 0.25, 0.125, and 0.0625, respectively. You can use the OR gate to select probabilities that aren't just powers of two. A four-bit register is one that has four bits. Switching activates AND gates, allowing for a user-defined quantity of switching activity. For example, the switching code 0100 will activate 25% of the control register stages on average, resulting in 25% of the hold latches being

enabled. The number of scan chains achieving constant values, and hence the projected toggling ratio, may be estimated given the phase shifter architecture.

An additional 4-input NOR gate detects the switching code 0000, which is used to turn off the LP capability. When operating in the weighted random mode, the switching level selector ensures statistically constant content of the control register in terms of the number of 1s it holds. As a result, despite the fact that a set of actual low toggling chains will continue to vary from one test pattern to the next, about the same percentage of scan chains will remain in LP mode. It will correspond to a certain number of scan chain toggles. However, with just 15 potential switching codes, the available toggling granularity may be too coarse to be always suitable. When it comes to generating low-toggling test patterns, a method like this one could provide you a lot more flexibility. Essentially, this approach separates each test pattern's shifting time into a sequence of alternating hold and toggle periods while keeping the primary solution's working principles. When the generator's data input is a 1, we use a T-type flip-flop to transition it between these two states. The generator enters the hold phase with all latches temporarily disabled if it is set to 0, regardless of the control register state. AND gates on the control register outputs, which freeze all phase shifter inputs, are used to do this. Because only one scan chain covers a core in SoC designs, erratic toggling might result in locally unacceptable heat dissipation that can only be managed by brief hold periods. If the T flip-flop is set to 1, the latches operated by the control register can pass test data flowing from the PRPG to the scan chains (the toggle period).

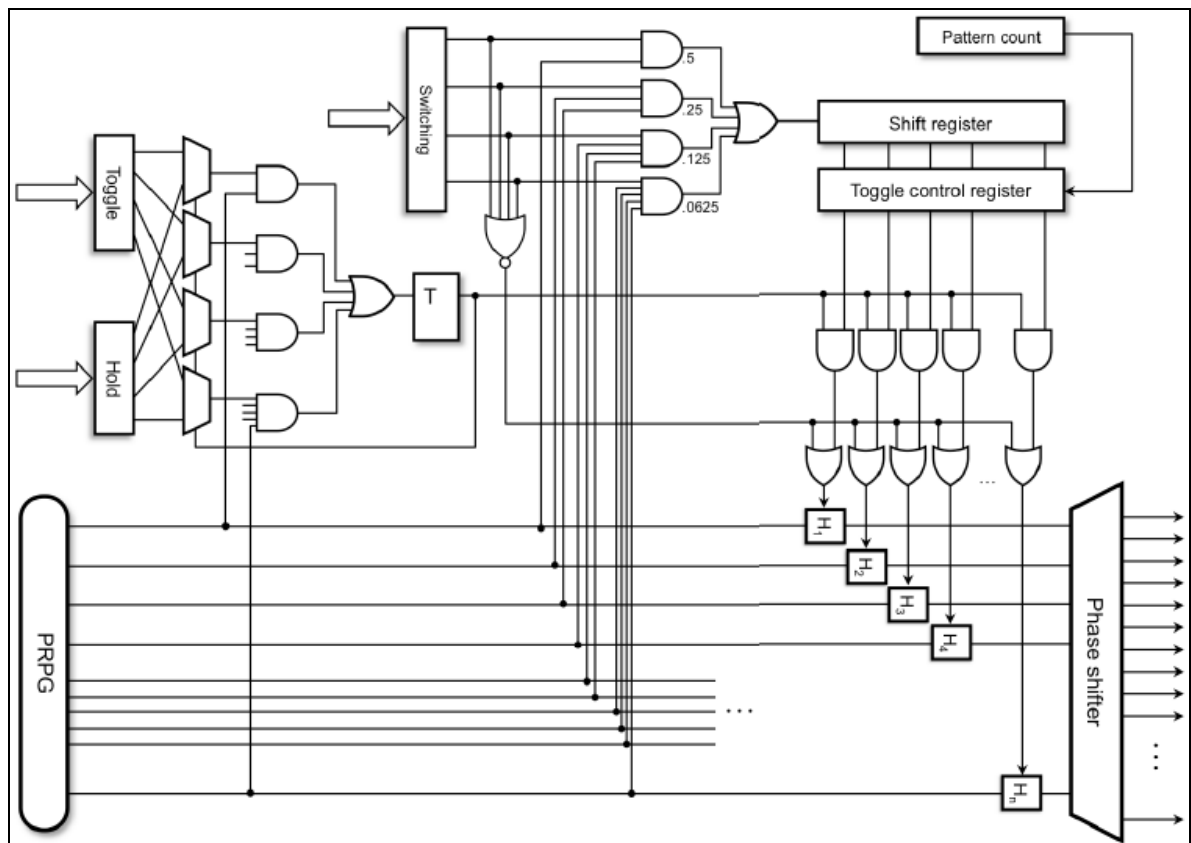


Fig. 4.3. Fully operational version of PRESTO.

Two additional parameters stored in 4-bit Hold and Toggle registers govern how long the whole generator remains in either the hold or toggle mode. A 1 on the D flip-flop input must be received to end either mode. This weighted pseudorandom signal is generated in the same way that the shift register is fed with weighted logic. The D flip-flop controls also four 2-input multiplexers routing data from the Toggle and Hold registers. It allows you to choose a source of control data that will be utilised in the following cycle to modify the generator's operational mode. The input multiplexers, for example, watch the Toggle register while in toggle mode. The flip-flop toggles and, as a result, all hold latches freeze in the previous recorded state once the weighted logic outputs 1. They'll stay in this state until the weighted logic output shows another 1.

The content of the Hold register, which defines when the hold mode should be terminated, is now linked to the random occurrence of this event. All LP registers are loaded once every test or per test pattern when utilising the PRESTO generator with an established DFT flow. The test setup method initialises the

registers loaded just once, which operate as test data registers or are elements of an IJTAG network. They're activated by a slow scan shift clock and run at a very low speed, so there's no need to worry about time. Because shallow logic generates bits to be fed serially into the registers, time is not affected even when the remaining registers are loaded once per test pattern (also at scan shift speed). Values are kept constant during capture thanks to shadow registers. It's obvious that it's best for LBIST applications with fast shift speeds. The LP registers are also included in the IP creation and insertion for embedded deterministic test (EDT). Along with the EDT logic, the related logic is incorporated into the design. There is no impact on the functional mode of operation because the EDT logic (including LP) is only introduced in the scan routes.

The following three elements are most important to the PRESTO generator (notice that in the BIST mode, they are only supplied once, at the start of the whole test session):

- 1) the switching code (which is stored in the switching register).
- 2) the hold duty cycle (HC).
- 3) the toggle duty cycle (TC).

The switching code, as well as the HC and TC values, may be automatically calculated based on the size of the PRPG, the number of scan chains, and the related phase shifter selected so that the entire generator produces pseudorandom test patterns with a desired level of toggling T, assuming the scan chains are balanced.

In the past, an enormous amount of research was conducted in order to attain larger BIST fault coverage with quicker test application time. LFSR-based pseudorandom test sequences were typically modified by putting a mapping logic between the PRPG outputs and the inputs of a circuit under test, or by adjusting the probabilities of outputting 0s and 1s, as in various forms of weighted-random testing, so that the resultant vectors capture characteristics of test patterns for hard-to-detect faults.

Test patterns that exit a PRPG can be modified in a more predictable manner as well. In a similar vein, we'll show how PRESTO-created LP test patterns can improve the fault coverage-to-pattern-count ratio. Test patterns with better-than-average fault coverage can be developed if the toggle control register can also be driven by deterministic test data.

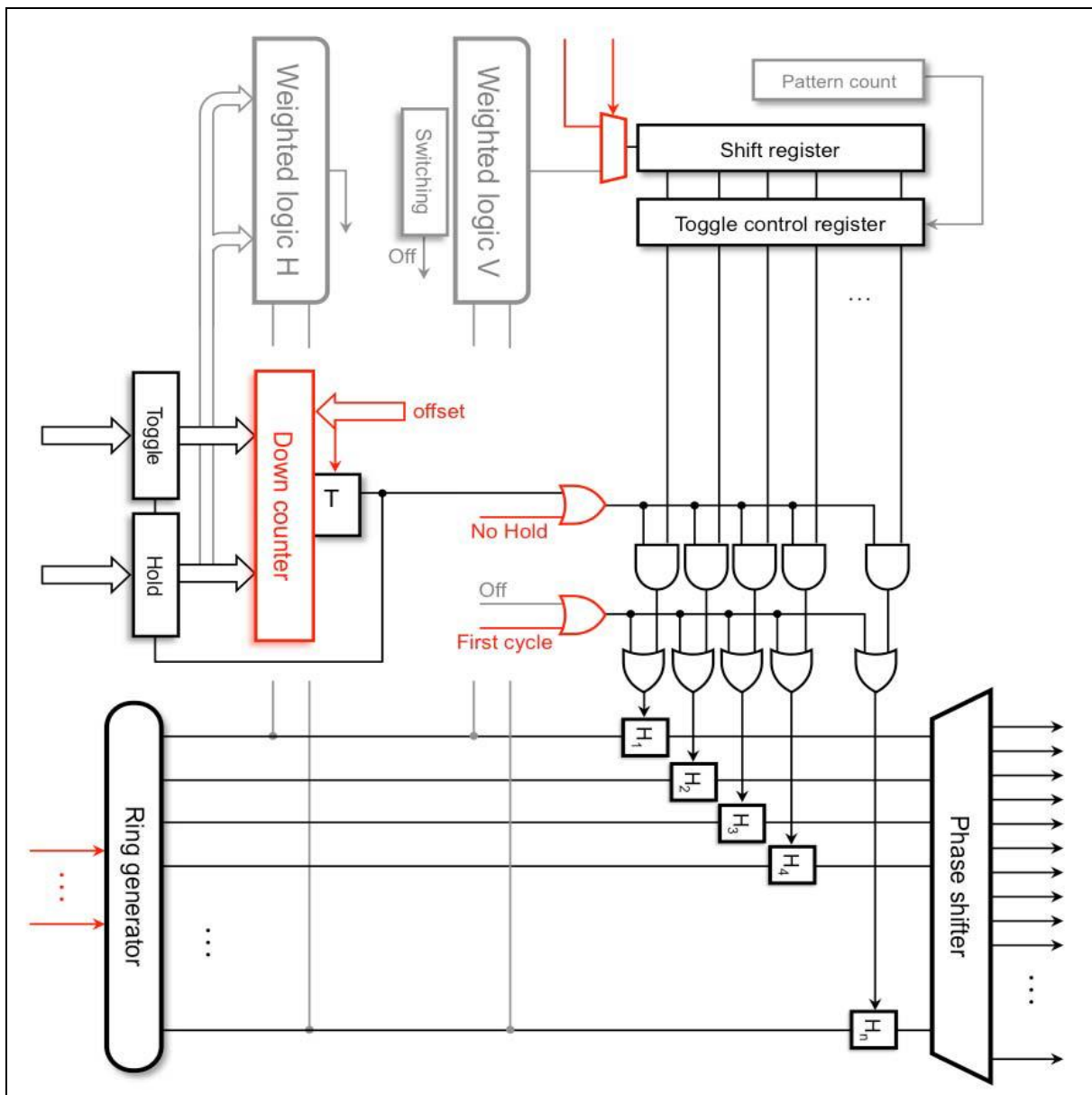


Fig. 4.4 LP decompressor—modules in gray are disabled. The red items have been added.

After that, ATPG is called again and again until the appropriate PRESTO pattern count or fault coverage limit is attained. The ATPG generates test cubes one by one for each fault. For performance reasons, the number of created test cubes is

restricted (in each loop). Many investigations have shown that a properly chosen restriction has no effect on test quality. As explained below, the obtained test cubes are now deployed to arrive with the content of the control register. Our aim now is to discover the matching distribution of 1s in the control register that optimises the fault detection probability using the PRESTO switching algorithm. To begin, each ATPG-created test cube is reduced to a collection of scan chains having more than one required bit. This collection will also be referred to as a foundation. Consider the following scan cells in a test cube where s is a scan chain and c is a cell location inside the scan chain. A argument for omitting any base scan chains housing a single defined bit is that there is a considerable likelihood (50 percent) of getting a particular logic result in a totally pseudorandom method. As a result, multiple bases can be integrated to create a single control setting in the future.

Given the phase shifter architecture, the minimum number of phase shifter inputs—or, equivalently, the number of 1s in the toggle control register— needed to activate the given scan chains may be calculated for each base. We identify the minimal set of phase shifter inputs that overlaps all subsets of phase shifter inputs capable of activating specified scan chains of a particular base by addressing the minimum hitting set issue in a greedy manner. Remember that the preselected switching code limits the amount of such inputs (and consequently the number of 1s in the control register). The switching code 0100, for example, restricts the number of 1s in the 32-bit control register to eight. Where s is a scan chain and c is a cell location inside the scan chain. The basis note that chain 45 is not included because it only has one scan cell defined. A argument for omitting any base scan chains housing a single defined bit is that there is a considerable likelihood (50 percent) of getting a particular logic result in a totally pseudorandom method. As a result, multiple bases can be integrated to create a single control setting in the future. Let C be a collection of bases that is initially empty. After we've calculated all of the weights, we'll add a minimum-weight basis to C . The cost value for each remaining base B is set to the least number of 1s in the control register that would be necessary to activate all scan chains in $C \cup B$. The cost of the other bases is recalculated when a minimum-cost base (or a minimum-weight base if there are two or more bases with the same minimal cost) is added to C . The basis is thus 4, 13; note that chain 45 is not included because it only has one scan

cell defined. A argument for omitting any base scan chains housing a single defined bit is that there is a considerable likelihood (50 percent) of getting a particular logic result in a totally pseudorandom method. As a result, multiple bases can be integrated to create a single control setting in the future depicts this. The decompressor's main premise is to deactivate both weighted logic blocks (V and H) and instead use deterministic control data. Due to a multiplexer set in front of the shift register, the content of the toggle control register may now be picked in a deterministic way. Furthermore, the Toggle and Hold registers are used to alternately preload a 4-bit binary down counter, allowing the lengths of the hold and toggle phases to be determined. When the value of this circuit approaches zero, it triggers a dedicated signal to go high, which toggles using the D flip-flop. The counter can have the input data retained in the Toggle or Hold register as the next state using the same signal. Every test pattern necessitates the initialization of both the down counter and the D flip-flop. The starting value of the T flipflop defines whether the decompressor will work in toggle or hold mode, and the initial value of the counter, also known as an offset, controls the length of that mode.

4.2. TYPES OF THE LANGUAGE AND SOFTWARE.

4.2.1 HDL

HDL is an advanced computing language for describing the structure and behaviour of electrical circuits, mainly digital logic circuits. A hardware description language, like a programming language like C, is a written description consisting of expressions, statements, and control structures. HDLs are essential parts of electronic design automation (EDA) systems, especially for complex circuits such as application-specific integrated circuits, microprocessors, and programmable logic devices.

4.2.2. VHDL

VHDL (VHSIC Hardware Description Language) is a hardware description language for digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits used in electrical design automation. VHDL may also be used to write general-purpose parallel programming code. VHDL is a programming language that is often used to create text models of logic circuits.

Only if the model is part of the logic design is it handled by a synthesis software. The logic design is tested using a simulation tool that uses simulation models to mimic the logic circuits that interface with the design. A testbench is a term used to describe a collection of simulation models. VHDL supports file input and output and may be used as a general-purpose language for text processing, however files are most typically utilised by a simulation test bench to store stimulus or verification data.

When used for systems design, VHDL has the benefit of allowing the behaviour of the needed system to be specified (modelled) and tested (simulated) before the design is translated into physical hardware via synthesis tools (gates and wires). Another advantage is that VHDL may be used to describe a concurrent system. Unlike procedural computer languages like BASIC, C, and assembly code, which run one instruction at a time, VHDL is a dataflow language.

4.2.2.1. TYPES OF REPRESENTATION OF VHDL

A text file describing a digital system can be represented by VHDL. A behavioural or structural model can be used to depict the digital system. These levels, sometimes referred to as levels of abstraction, aid the designer in effectively developing complicated systems.

4.2.2.2. Behavioural Model

Instead of a lower abstraction of the system's connectivity, the behavioural level explains how it acts. A Register Transfer Level (RTL), an Algorithmic (series of instructions), or basic Boolean Equations can be used to describe a behavioural model.

4.2.2.3. Register transfer level

Data flow inside a system, such as data flow between registers, is often represented by RTL. RTL is mostly used to create combinational logics.

4.2.2.4. Algorithmic level

The systems are described at a structural level as gates or component blocks that are coupled to accomplish the necessary activities. The structural level is

essentially a graphical depiction of the digital system, which is closer to the system's real physical representation.

4.2.2.5. Structural Model

The systems are described at the structural level as gates or component blocks that are coupled to accomplish the necessary actions. The structural level is essentially a graphical depiction of the digital system and is closer to the system's real physical representation.

4.2.3. MODELSIM

ModelSim is a Mentor Graphics multi-language HDL simulation environment that includes a built-in C debugger for simulation of hardware description languages like as VHDL, Verilog, and SystemC. ModelSim may be used on its alone or in tandem with Altera Quartus or Xilinx ISE. Simulation can be done manually or automatically using a graphical user interface (GUI). Figure 4.2 depicts the ModelSim environment. ModelSim comes in several different editions, including ModelSim PE, ModelSimSE, and ModelSim XE. ModelSim SE is a high-performance simulator with sophisticated debugging features, whereas ModelSim PE is a beginner's simulator for hobbyists and students. ModelSim SE is utilised in big multi-million gate designs and is available in 32-bit and 64-bit architectures for Microsoft Windows and Linux.

ModelSim XE stands for Xilinx Edition and was created specifically for use with Xilinx ISE. ModelSim XE allows HDL programmes created for Xilinx Virtex/Spartan family FPGAs to be tested without the requirement for actual hardware.

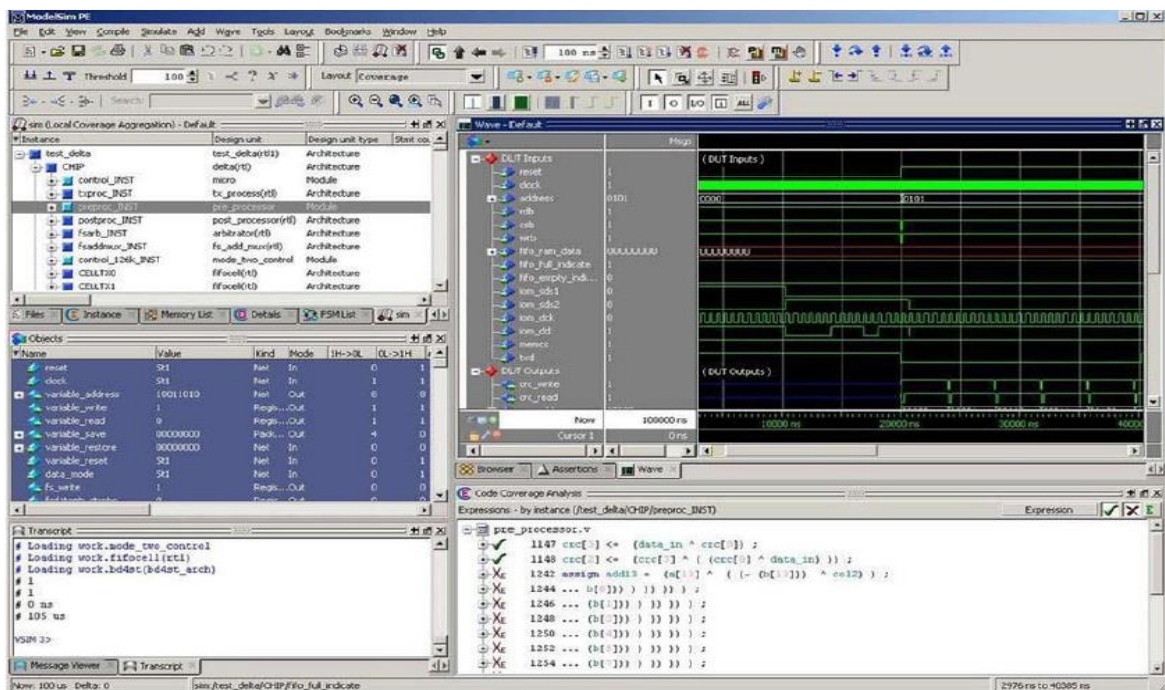


Fig.4.5. ModelSim Environment

Link for ModelSim allows ModelSim to be used with MATLAB/Simulink. Link for ModelSim is a bidirectional co-simulation interface for Simulink and ModelSim that is quick and easy to use. ModelSim provides tools to evaluate the hardware implementation and temporal features of such designs, while MATLAB provides a numerical simulation toolkit. With an intelligently constructed debug environment, ModelSim simplifies the process of detecting design flaws. ModelSim's debug environment conveniently presents design data for all languages' analysis and debugging. Many debug and analysis features are available in ModelSim, both post-simulation on stored data and during live simulation sessions.

4.3.1. Features of ModelSim

- For simplicity of usage and performance, a unified mixed language simulation engine has been developed.
- For successful verification of advanced design environments, native support of Verilog, System Verilog for design, and VHDL.
- Advanced code coverage and analysis tools for rapid time to coverage closure.
- Fast time to debug, easy to use, multi-language debug environment.

- Due to the availability of both interactive and post-sim debugging, the same debug environment is used for both.
- Waveform Compare is a powerful tool for analysing discrepancies and bugs.
- Unified Coverage Database with full interactive and HTML reporting and processing to help you understand and debug coverage throughout your project.

4.4. XILINX ISE DESIGN SUITE

The design may be submitted in a variety of methods with the Xilinx ISE tools, including graphical schematics, state machine diagrams, VHDL, and Verilog. The ISE® Design Suite manages the whole design process. You may access all of the design entry and design implementation capabilities through the Project Navigator interface. You can also have access to the files and papers related to your project.

4.4.1. Project Navigator Interface

By default, the Project Navigator interface is divided into four panel sub-windows. On the top left are the Start, Design, Files, and Libraries panels, which include display and access to the source files in the project as well as access to running processes for the currently selected source. The Start panel provides quick access to opening projects as well as frequently access reference material, documentation and tutorials. At the bottom of the Project Navigator are the Console, Errors, and Warnings panels, which display status messages, errors, and warnings. To the right is a multi-document interface;e (MDI) window referred to as the Workspace. The Workspace enables you to view design reports, text files, schematics, and simulation waveforms. Each window can be resized, undocked from Project Navigator, moved to a new location within the main Project Navigator window, tiled, layered, or closed. You can use the **View > Panels** menu commands to open or close panels. You can use the **Layout > Load Default Layout** to restore the default window layout.

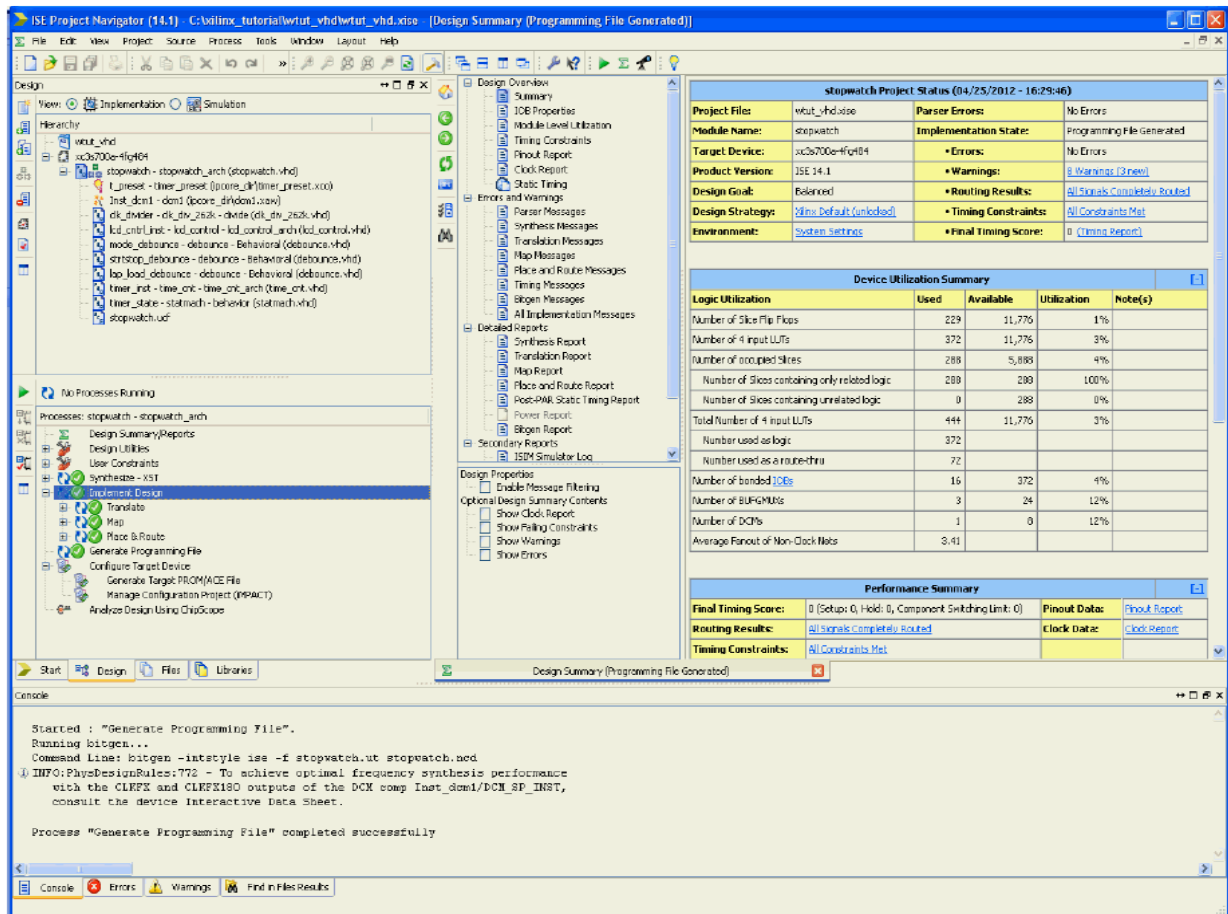


Fig.4.6. Project Navigator Interface

4.4.1.1. Design Panel

The following are accessible from the Design panel:

- View pane
- Hierarchy pane
- Processes pane

4.4.1.2. View Panel

In the Hierarchy pane, the Examine pane radio buttons allow you to view the source modules connected with the implementation or the Simulation Design View. If Simulation is chosen, you must choose a simulation phase from the drop-down menu.

4.4.1.3. Hierarchy Panel

The project name, target device, user documents, and design source files connected with the selected Design View are displayed in the Hierarchy pane.

Only those source files related with the selected Design View, such as Implementation or Simulation, may be viewed in the View window at the top of the Design panel. In the Hierarchy pane, each file has its own icon. The file type is indicated by the icon (HDL file, schematic, core, or text file, for example). See the ISE Help page on Source File Types for a comprehensive list of available source types and their related icons. To access the ISE Help, go to Project Navigator > Help > Help Topics. The icon bears a plus symbol (+) to the left of the name if the file contains lower levels of hierarchy. By clicking the plus symbol (+), you may extend the hierarchy. By double-clicking on the filename, you may open it for modification.

4.4.1.4. Processes Panel

The Processes pane is context-sensitive, changing depending on the source type selected in the Sources pane and the project's top-level source. You may execute the functions required to define, run, and analyse your design from the Processes window.

4.4.1.5. Workspace

In the Workspace, you'll find design editors, viewers, and analytic tools. ISE Text Editor, Schematic Editor, Constraint Editor, Design Summary/Report Viewer, RTL and Technology Viewers, and Timing Analyzer are just a few of the tools on offer. Other tools, such as Plan Ahead planning and floor planning, ISim, third-party text editors, XPower Analyzer, and iMPACT, open in separate windows outside of the Project Navigator context when they are engaged.

CHAPTER 5

RESULT AND OUTPUT

The project's VHDL source code was utilised in Xilinx and ModelSim, and the code produced the intended results.

Circuit	n	m	PI	RF%	FC%	Test length			
						Det.	LFER	BS-LFSR no ordering	BS-LFSR with order
S641	32	19	35	0	98.0	53	5120	4910	4970
S838	32	32	35	0	86.5	90	8160	8460	7910
S1196	30	18	14	0	97.0	131	3750	3680	3370
S1238	30	18	14	5.09	91.3	141	3890	3560	3610
S5378	40	179	35	.88	98.0	244	30110	33700	28900
S9234	40	228	19	6.52	90.0	367	397800	401930	398170
S13207	60	669	31	1.54	95.0	455	49660	47400	48110
S35932	64	1728	35	10.19	89.8	63	18700	16640	16520
S38417	64	1636	28	.53	96.5	849	118580	125520	117080
S38584	64	1452	12	4.15	94	632	43530	39660	40090

TABLE 5.1 Test Length Needed To Get Target Fault Coverage For LFSR And BSLFSR

A group of experiments was performed benchmark circuit In the first series of experiments, the BSLFSR is evaluated as a function of the length of the test sequence required to achieve some fault coverage with and without the scan chain ordering algorithm. Table 5.1 shows the results for a set of ten benchmark circuits. The columns labeled n, m and PI refer to the size of the LFSR, there respectively the number of flip-flops in the scanning chain and the number of primary inputs of the CUT.

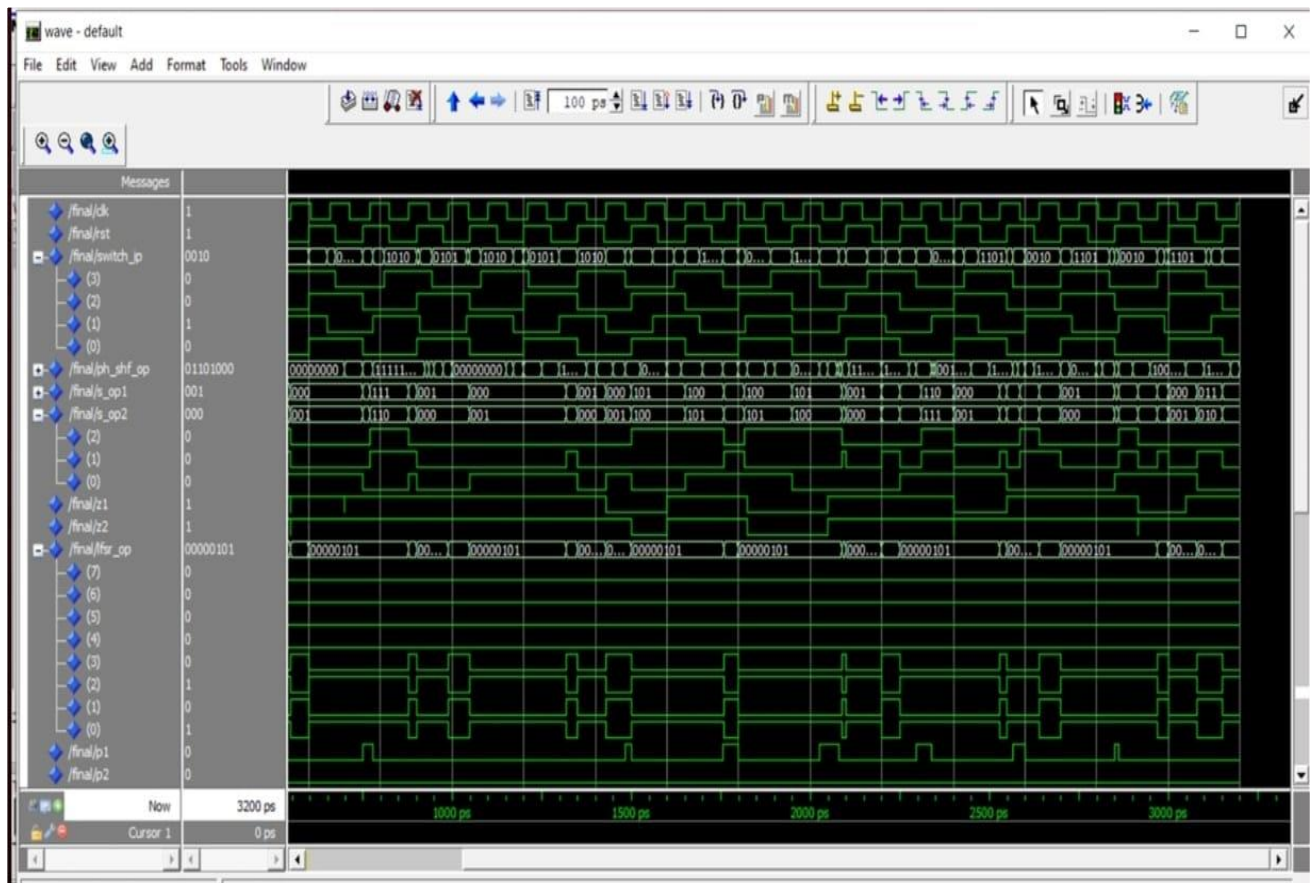


Fig 5.1 the output wave formed in ModelSim Software

The waveform view contains waves (binary 0's and 1's, hexadecimal digits, binary digits, enumerated types, etc) for all of the signals in your design. It shows how your module reacts to different stimulus.

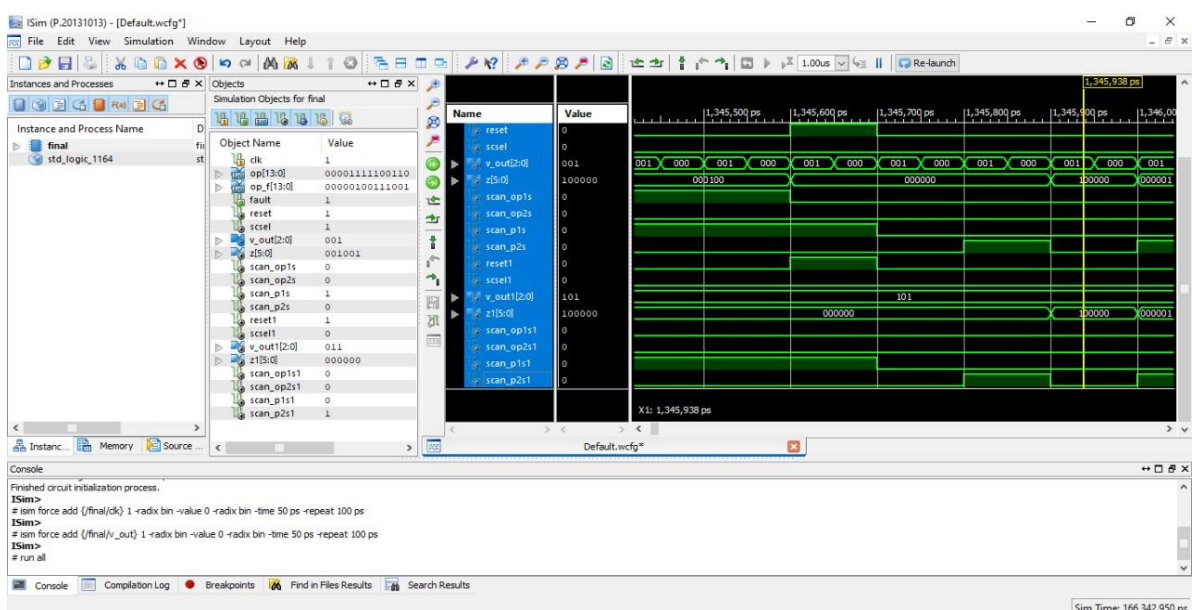


Fig 5.2 Output waveform in the Project navigator

The Drawing Management environment within the Project Navigator helps you organize, create, and access all your project drawings in one unified interface. The output waveform is produced in Xilinx version 14.7.

After XST synthesis is completed, helps to view both RTL and technology schematic.

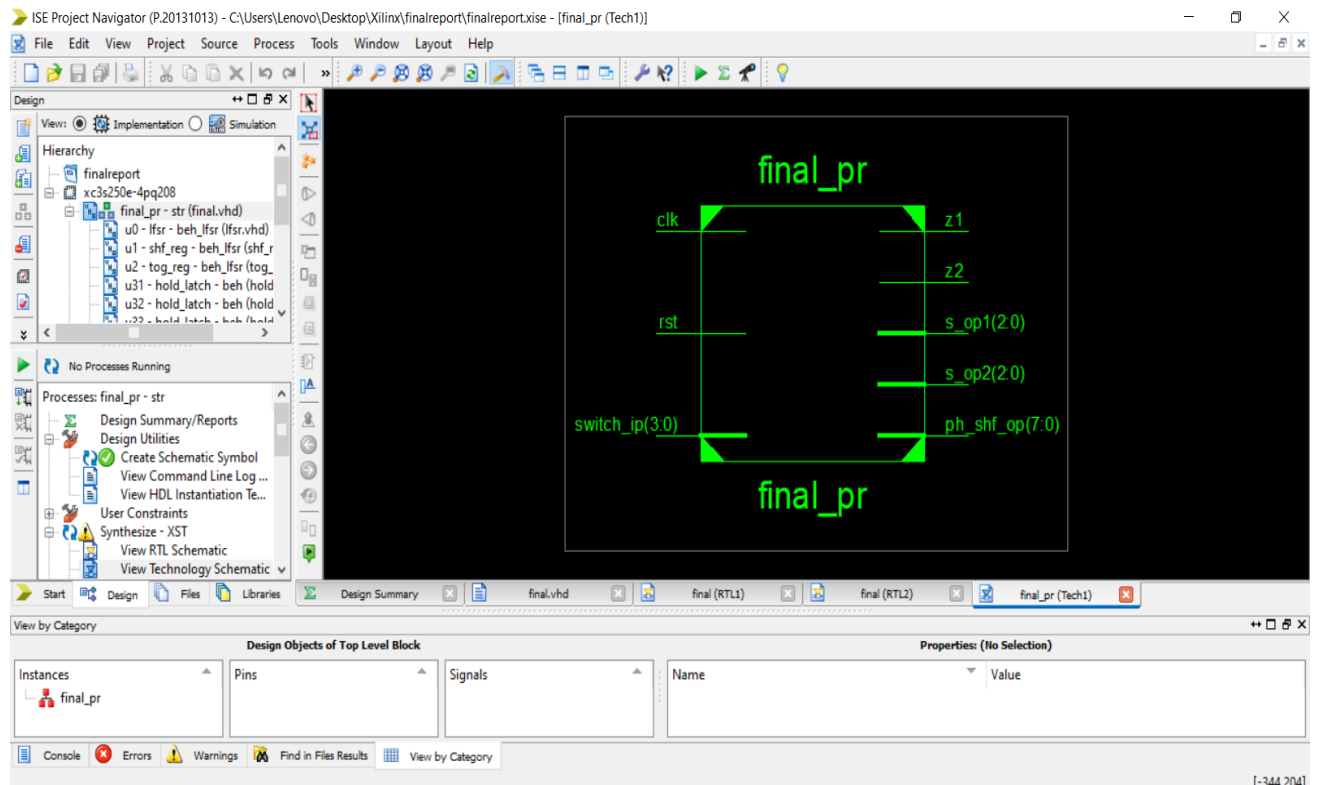


Fig 5.3 Technology Schematic

It is frequently observed discrepancies between these two schematics. RTL View shows you the representation of your design in terms of generic symbols means like AND Gates, OR Gates, adders, multipliers, etc.

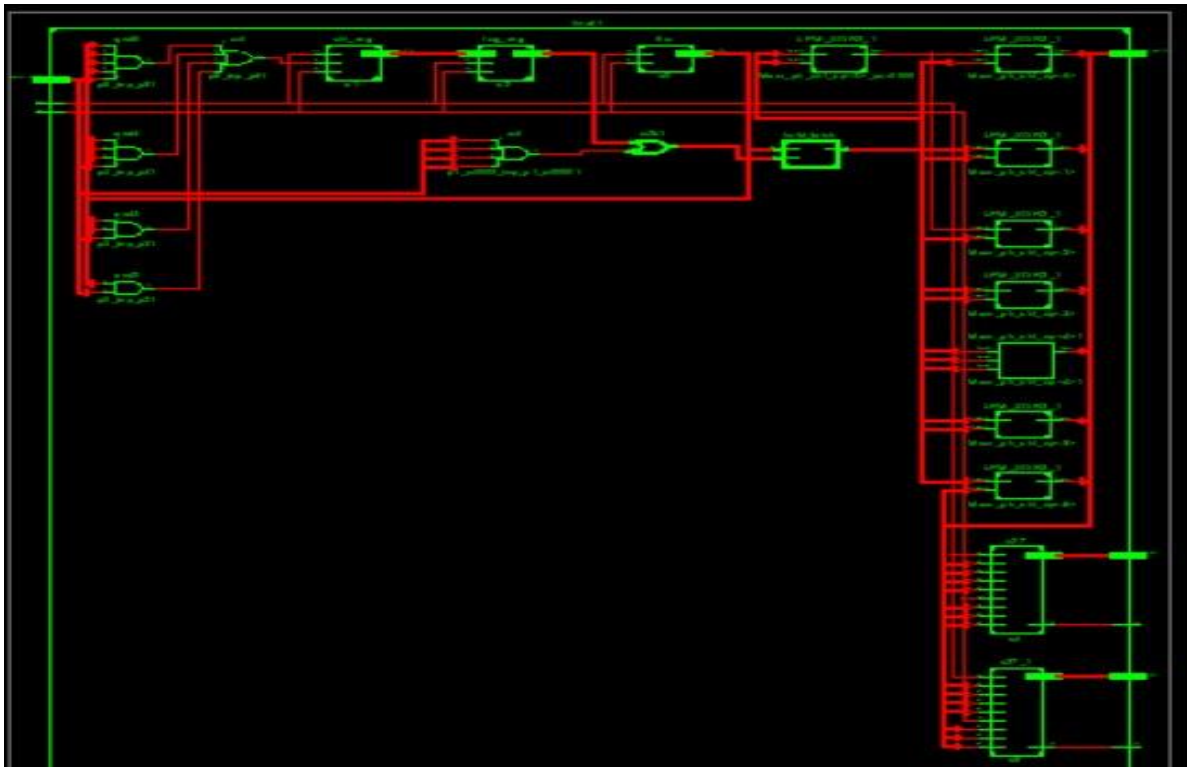


Fig 5.4 The schematic circuit is formed in Xilinx ISE Software

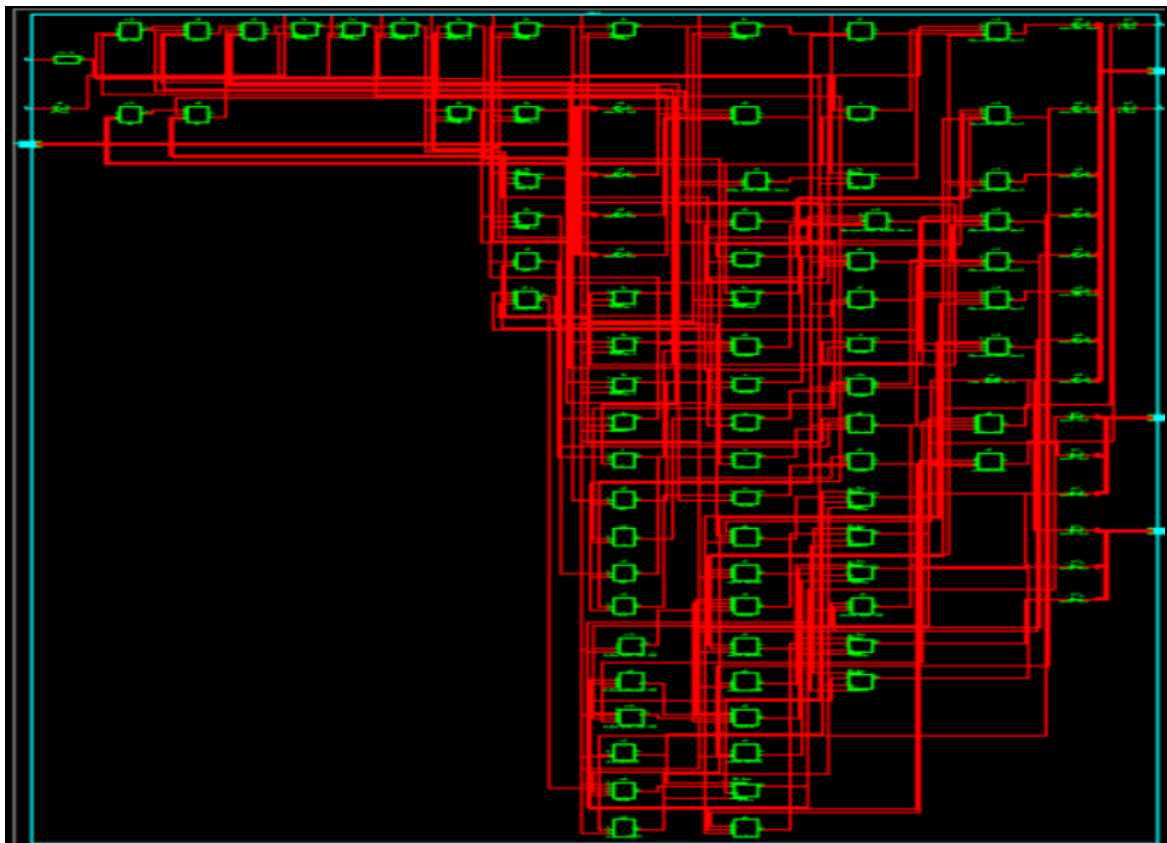


Fig 5.5 The RTL Technology circuit formed in Xilinx ISE Software

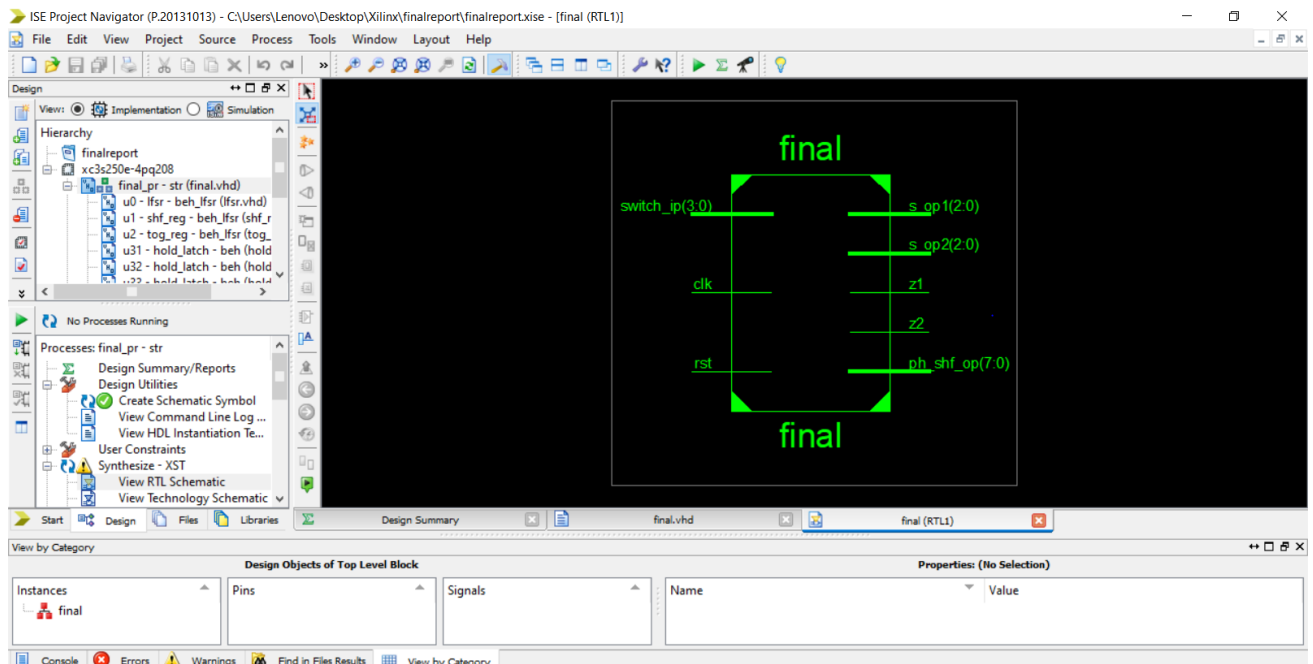


Fig 5.6 RTL schematic

5.4.1 Difference between Schematic

Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic. This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

5.4.2 Technology View

Viewing a technology diagram opens an NGC file that can be viewed as an architecture-specific diagram. This diagram is generated after the optimization and technological targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized for the Xilinx target device or "technology"; for example, in terms of LUTs, transport logic, I/O buffers, and other technology-specific components. Viewing this diagram allows you to see a technology-level representation of your HDL optimized for specific Xilinx architecture, which might help you uncover design issues early in the design process.

Xilinx Power Estimator (XPE) can be used during the pre-design and pre-implementation phases of the power analysis design cycle. With the increasing complexity and computing power of modern programmable devices, the first analysis of electrical and thermal specifications is essential for successful product design.

XPE is also commonly used later in the design cycle when implementing and power closure to, for example, evaluate power implications of engineering change orders (ECO). For large designs implemented by multiple teams, the project leader can use XPE to import utilization and activity for each team's module, then monitor the total power and reallocate the power budget to ensure constraints.

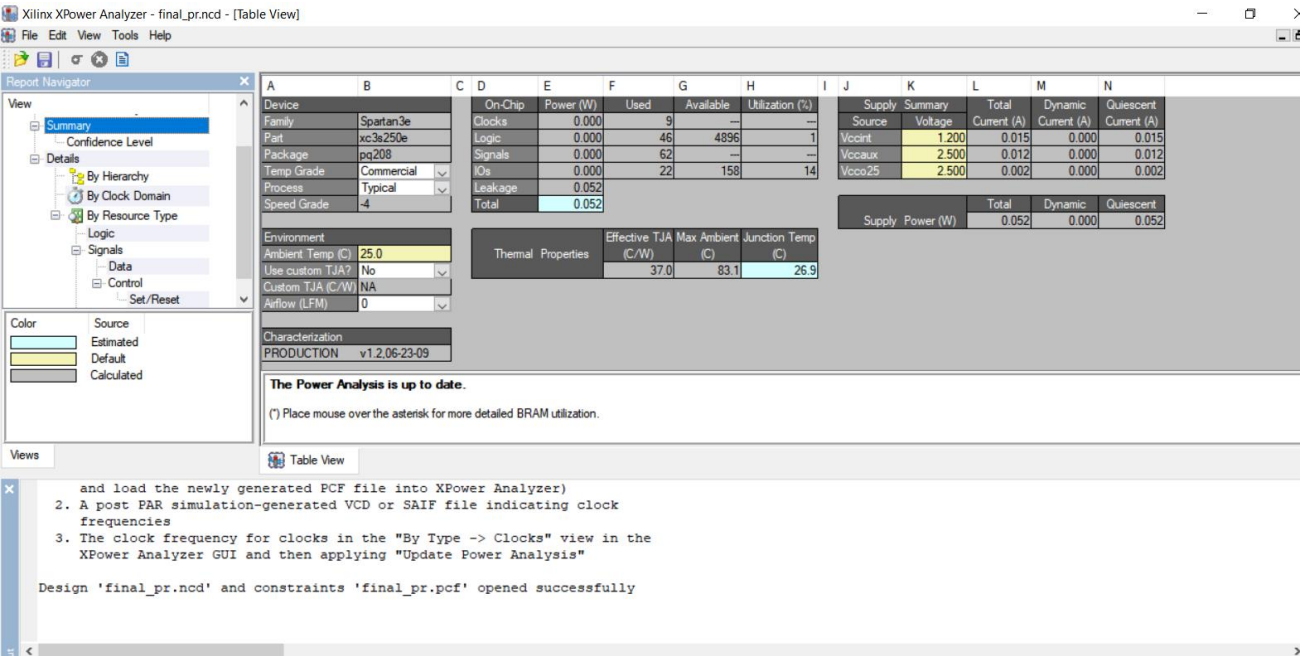


Fig 5.7 Power Analysis

CHAPTER 6

CONCLUSION

Although the automated programming, the PRESTO generator may generate pseudorandom test patterns with scan shift-in switching activity carefully chosen. The same features can be used to control the generator, resulting in test vectors that either yield the desired fault coverage faster than conventional pseudorandom patterns while still lowering toggling rates to desired levels, or offer visibly higher coverage numbers if run for comparable test times. This LP PRPG may also work as a full-featured test data decompressor, with the ability to manage scan shift-in switching activity throughout the encoding process. The suggested hybrid system enables the efficient combination of test compression and logic BIST, where both techniques may function in tandem to provide high-quality tests. As a result, it's a highly appealing LP test method that lets you trade-off test coverage, pattern counts, and rate toggling in a very flexible way.

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