

HIGH PERFORMANCE DIGITAL COMPARATOR FOR VLSI ARCHITECTURE

Submitted in partial fulfilment of the requirements of the award of
Bachelor of Engineering Degree
in Electronics and Communication Engineering

by

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION
ENGINEERING**

SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

Accredited with Grade “A” by NAAC

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APRIL 2022



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BONAFIDE CERTIFICATE

This is to certify that this project report is the bonafide work of SANKU REVATHI (38130194) and Y. VENKATA SREEKAVYA (38130236) who carried out the project entitled **“HIGH PERFORMANCE DIGITAL COMPARATOR FOR VLSI ARCHITECTURE”** under my supervision from DECEMBER 2021 to APRIL 2022.

Internal Guide & Head of the Department

Dr. T. RAVI M.E., Ph.D.,

Submitted for Viva voce Examination held on_____

Internal Examiner

External Examiner

DECLARATION

We SANKU REVATHI (38130194) and Y. VENKATA SREEKAVYA (38130236) hereby declare that the Project Report entitled “**HIGH PERFORMANCE DIGITAL COMPARATOR FOR VLSI ARCHITECTURE**” done by us under the guidance of Dr. T. RAVI M.E., Ph.D., is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

DATE:

PLACE:

1

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SIGNATURE OF THE CANDIDATE

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Abstract

Comparator forms a fundamental component of processors and digital systems. For processors, in order to achieve high throughput with fast clock rates, it is necessary that such devices have less delay. Hence, Proposed EX-OR-NOR Cell based 4 bit Digital Comparator is designed. These comparators are first simulated in Synopsis Hspice using 130nm technology and then compared with the traditional design. Simulation results show that the proposed architecture has 5.442 μ W average power consumption whereas Existing 4 bit Digital Comparator has 6.346 μ W Average power consumption. Therefore the proposed digital comparator shows less power consumption when compared to the existing comparator. Also, the number of gates transistors get reduced in the proposed ex-or-nor cell based digital comparator.

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1. INTRODUCTION

1.1 COMPARATOR

Comparator is a basic arithmetic unit that compares the magnitude of two binary numbers, say A and B, and produces output bits: $A > B$ or $A < B$ or $A = B$. It is an important data-path element for any general purpose architecture as well as an essential device for application-specific and signal processing architectures [1, 2]. Comparators are also used in sorting networks which play an important role in areas such as parallel computing, multi-access memories and multiprocessing [3, 4, 5, 6]. Comparator forms a fundamental component of processors and digital systems. For processors, in order to achieve high throughput with fast clock rates, it is necessary that such devices have less delay. Consequently, the designing of high speed comparator architecture becomes a relevant and essential research topic. Previously published comparator implementations having serial and parallel architecture can both be found in literature. The serial architecture is suitable for short inputs (i.e. when both the inputs have lesser number of bits). For longer inputs (say, 32 bit, 64 bit inputs), the circuit complexity and the combinational delay increase drastically. As a result, parallel approach is generally preferred for comparators with longer inputs. The comparator designs presented in this paper are based on parallel approach.

Comparator is a combinational logic circuit that compares the magnitudes of two binary quantities to determine which one has the greater magnitude. In other word, a comparator determines the relationship of two binary quantities. A exclusive-OR gate can be used as a basic comparator. Digital comparators are also called as binary or logic comparators. Comparator is a very useful combinational circuit capable of comparing two numbers as input in binary form and determines whether one number is greater than, less than or equal to other number. This logic circuit is used for testing whether the binary number at one input is greater than or less than or equal to another binary number. There are two types of comparators:

1. Equality or Identity Comparator
2. Magnitude or inequality comparator.

Output of the comparator is at logic '1' if the two input words A and B match otherwise the output remains at logic '0'. Out of the 2^n combinations, there is only one input combination that is correct and other combinations will result in inequality. This comparator can be used for simple circuits like electronic lock and security systems where binary password consisting of n bits compared with another preset code. Let us discuss the implementation of simple 1-bit equality comparator.

Let us study 1-bit equality comparator using simple XOR circuit. The truth table of XOR indicates the operation of Identity or Equality comparator. When both the inputs of the comparator are equal then the output is active LOW indicating matching of the input code, other wise output is at logic '1' indicating the mismatch.

In two bit equality comparator, two bit binary numbers A and B represented as A_1A_0 and B_1B_0 are compared. Here A_1 and B_1 are the most significant bits, and A_0 and B_0 are the least significant bits of numbers A and B respectively. A_1 is compared with B_1 and A_0 is compared the B_0 . If A_1 is equal to B_1 and A_0 is equal to B_0 output of a two bit comparator will be HIGH. If A_1 is not equal to B_1 or A_0 is not equal to B_0 output will be LOW

In recent year, high speed & low power device designs have emerged as principal theme in electronic industry due to increasing demand of portable devices. This tremendous demand is due to popularity of battery operated portable equipments such as personal computing devices, wireless communication, medical applications etc. Demand & popularity of portable electronic devices are driving the designers to strive for higher speed, smaller power consumption and smaller area.

The logic style used in logic gates basically influences the speed, size, power dissipation, and the wiring complexity of a circuit. Circuit size depends on the number of transistors and their sizes and on the wiring complexity. The wiring complexity is determined by the number of connections and their lengths. All these characteristics may vary considerably from one logic style to another and thus proper choice of logic style is very important for circuit performance.

1.2 Literature survey

High-speed and area-efficient scalable N-bit digital comparator

An area-efficient N-bit digital comparator with high operating speed and low-power dissipation is presented in this work. The proposed comparator structure consists of two separate modules. The first module is the comparison evaluation module (CEM) and the second module is the final module (FM). Independent from the input operand bitwidths, stages present in CEM involve the regular structure of repeated logic cells used for implementing parallel prefix tree structure. The FM validates the final comparison based on results obtained from the CEM. The presence of regular very large-scale integration topology in the proposed structure allows the analytical derivation of the area in terms of total number of transistors present in the design and total delay encountered in input–output flow as the function of input operand bit width. Spectre simulation results have been presented using 0.18 μm complementary metal–oxide–semiconductor (CMOS) technology at 1 GHz. The main advantages of the proposed comparator are minimum input–output delay of 0.57 ns, minimum fan-out-of-4 delay of 9.5 ns and low-power dissipation of 1.03 mw as compared with existing comparators designed using 180 nm CMOS technology for 64 bit comparison.

A Low Power 1V Supply Dynamic Comparator

This paper presents a low power dynamic comparator for ultra low power applications. The prototype is designed in a 65nm CMOS process with a supply voltage of 1V and is compared against the widely used double tail latch comparator in terms of power consumption and input referred rms noise. This reduces the power consumption while achieving similar noise levels. Measurements demonstrate that the proposed comparator achieves an input referred rms noise voltage of 220 μV against 210 μV for the conventional comparator with a 30% reduction in power. The proposed circuit consumes 0.19pJ energy per comparison.

An In-Comparator Aperture-Time Equalization in a 7nm FinFET CMOS 40Gb/s Receiver

This paper proposes an in-comparator aperture-time equalization scheme using the impulse response of a clocked comparator. The technique is applied in a wireline link receiver prototype, implemented in CMOS 7nm FinFET technology. The proposed method controls the aperture properties of the slicers by shaping their impulse sensitivity functions. We demonstrate an aperture skew control range of 4.7ps with 147fs accuracy for NRZ signaling at 40Gb/s. PAM4 signaling at 80Gb/s is also showcased using the proposed technique. These results serve as a proof of concept for next-generation source-synchronous chip-to-chip dense I/O links where aperture-time skews could be fine adjusted inside each comparator.

A Low-Power Low-Voltage Dynamic Comparator in 180nm CMOS Technology

This paper presents a new design for a dynamic comparator that its combined of the PMOS Bulk-driven input differential stage. The main advantage is low consumed power by connecting the input signal to the bulk of the transistors in the proposed circuit. The proposed comparator has the power consumption in the range of nanowatts. The presented circuit is simulated and designed in a standard 180 nm CMOS technology and post-layout

simulation results at 0.5 V supply voltage and frequency of 20 KHz, consumed power is only 8.86 nW with 3.5 ns delay time.

High-Speed Comparator Architectures for Fast Binary Comparison

This paper proposes the design of digital comparator with two different parallel architectures. These comparators are first realized in Verilog and simulated with Xilinx ISE 8.2i platform and then compared with the traditional design. Simulation results show that the first proposed architecture has 23.769 % less combinational delay (logic + interconnect) and the second proposed architecture is even much faster and has a combinational delay of 35.218 % less compared to the traditional design.

An Energy-Efficient Comparator With Dynamic Floating Inverter Amplifier

This article presents an energy-efficient comparator design. The pre-amplifier adopts an inverter-based input pair powered by a floating reservoir capacitor; it realizes both current reuse and dynamic bias, thereby significantly boosting gm/ID and reducing noise. Moreover, it greatly reduces the influence of the process corner and the input common-mode voltage on the comparator performance, including noise, offset, and delay. A prototype comparator in 180 nm achieves 46- μ V input-referred noise while consuming only 1 pJ per comparison under a 1.2-V supply. This represents greater than seven-time energy efficiency boost compared with a strong-arm (SA) latch. It achieves the highest reported comparator energy efficiency to the best of our knowledge.

A Three-Stage Comparator and Its Modified Version With Fast Speed and Low Kickback

This brief presents a three-stage comparator and its modified version to improve the speed and reduce the kickback noise. Unlike the traditional two-stage structure that uses pMOS input pair in the regeneration stage, the three-stage comparator makes it possible to use nMOS input pairs in both the regeneration stage and the amplification stage, further increasing the speed. Furthermore, in the proposed modified version of three-stage comparator, a CMOS input pair is adopted at the amplification stage. This greatly reduces the kickback noise by canceling out the nMOS kickback through the pMOS kickback. It also adds an extra signal path in the regeneration stage, which helps increase the speed further. For easy comparison, both the conventional two-stage and the proposed three-stage comparators are implemented in the same 130-nm CMOS process. Measured results show that the modified version of three-stage comparator improves the speed by 32%, and decreases the kickback noise by ten times. This improvement is not at the cost of increased input.

1.3 PROBLEM DEFINITION

- To design and analysis of High Performance Digital Comparator for VLSI Architecture.

1.4 OBJECTIVES

- To analyze the performance of Existing Digital Comparator
- To design a high performance digital comparator for VLSI architecture.
- To analyze the performance in terms of power, delay, energy consumption and area.
- To compare the performance analysis with the existing comparator.

2. EXISTING METHODOLOGY

Traditional magnitude comparator is shown in Fig.1. The design is a parallel architecture. The circuit has three output bits: $A > B$, $A < B$, $A = B$. In many applications, only two output signals $A > B$, $A < B$ are sufficient. The output bit ($A = B$) goes high if all the bits of A are equal to the corresponding bits of B. The two output signals $A > B$ and $A < B$, are determined based on the following two conditions.

- If MSBs of the two numbers are unequal, i.e when $A_i = 1$, $B_i = 0$ then $A > B$ or $A_i = 0$, $B_i = 1$ for $A < B$.
- OR if the pair of bits in the significant bit positions are equal, and LSBs are different i.e. $A_i = B_i$ and $A_{i-1} = 1$, $B_{i-1} = 0$ then $A > B$ or $A_i = B_i$ and $A_{i-1} = 0$, $B_{i-1} = 1$ then $A < B$.

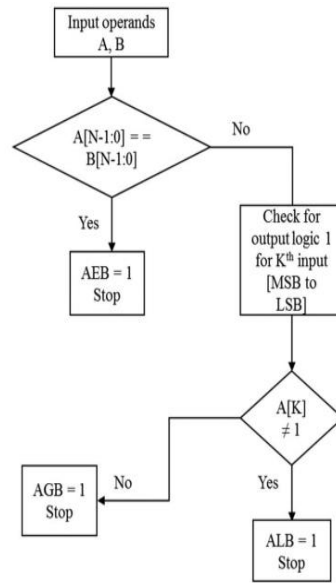


Fig. 2.1: Comparison between two N-bit operands

3. PROPOSED ARCHITECTURE

The proposed N-bit digital comparator is shown in Fig. 2. For performing a comparison between two N-bit binary operands, the proposed structure is divided into the comparison evaluation module (CEM) and final module (FM). These modules serve as a high-level and low-level architectures. The CEM incorporates parallel prefix tree structure that is intended for performing a bitwise comparison of two N-bit operands A and B depicted by $A_{N-1}A_{N-2}, \dots, A_0$ and $B_{N-1}B_{N-2}, \dots, B_0$. To explore the regularity of the proposed comparator for arbitrary bitwidths, two operands A and B are applied into 4 bit partitions as $A_{N-1}A_{N-2}A_{N-3}A_{N-4}, \dots, A_3A_2A_1A_0$ and $B_{N-1}B_{N-2}B_{N-3}B_{N-4}, \dots, B_3B_2B_1B_0$. The complete process of comparison is divided into five sets, in which CEM contains sets 1–4 and FM contains only set 5.

All the sets in the design are placed in four hierarchal prefix orders according to their functionality; therefore, the output of each set in this approach serves as the input of another set with an exclusion of set 1, whose outputs act as the inputs of sets 2 and 3.

In set 1, bitwise comparison of two N-bit binary operands is carried out by the novel EX–OR–NOR cell. The proposed structure of EX–OR–NOR cell shown in Fig. 3 is based on the pass transistor logic and CMOS logic. It uses seven transistors for EX–OR and EX–NOR operations as compared with the conventional eight transistors model. The transistor M5 is used to obtain full output voltage swing of EX–NOR operation as shown in Fig. 6. The six transistors model has also been reported in but it gives limited output voltage swing when applied input operands are (0, 0) or (1, 1). Optimum aspect ratios of the seven transistors (M1–M7) consisting of four P-channel MOS (PMOS) and three N channel MOS transistors of the proposed EX–OR–NOR

cell are carried out to avoid the universal drive constraint faced by the pass transistor logic. The novel structure uses a PMOS transistor in the feedback to maintain the logic level on the EX–NOR output terminal and the CMOS logic to boost up the output for achieving the full voltage swing on the EX–OR output terminal. The outputs of novel EX–OR–NOR cells provide the termination and comparison bits intended for sets 2 and 3 structures.

Set 2 comprises of cells, which operates on the termination bits (TK) obtained from set 1. The logic cells present in set 2 combine the termination bits obtained from the nibble partitions (partition used for the comparison of every 4 bit of the operands starting from the MSB) present in set 1 and the outputs obtained from the preceding AND-type logic cells present in the same level of set 2. Equal flags $E[(N/4)-1]$ to $E0$ generated from set 2 control the switching activities of the next subsequent partitions of set 3. Comparison request from set 2 generates if and only if all the results obtained from the bitwise comparison performed by preceding cells of set 1 are 'equal'; otherwise, termination bits as logic 0 will be generated.

Set 3 includes cells, which combine the outputs obtained from sets 1 and 2. The number of inputs increases in the ascending order from left to right for each cell in their respective partition and ending with the maximum fan-in of six. The combination of sets 1 and 3 architectures forms the pre-encoder structure. If most significant unequal bits are received in the comparison process of two operands, then the output bits obtained from sets 1 and 2 allow the termination of the subsequent bitwise comparison activity of the logic cells present in set 3.

Set 4 contains NAND-type logic cells, which receive the inputs from set 3 and set 4 requires $(N/4)$ cells to combine the outputs from each partition of set 3.

Set 5 contains two NOR-type logic cells to decide the final results of the proposed digital comparator in terms of 'ALB' and 'AGB'. First NOR gate uses outputs of set 4 and 'AEB' as inputs to decide 'ALB', whereas second NOR gate uses the output of first NOR gate and 'AEB' as inputs to decide 'AGB'.

To explain the process of the proposed methodology, two input operands $A = 1010101010101010$ and $B = 1001100110011001$ are chosen for 16 bit comparison and the pictorial view of the process is illustrated in Fig. 4. The complete process is divided into five sets. Set 1 includes a bitwise comparison of input operands for the examination of equal and unequal bit pairs. The outputs of set 1 are '1100110011001100' and '0011001100110011' using novel EX–OR–NOR cells. From the output, it is clear that the first two bit pairs $A_{15} B_{15} = '11'$ and $A_{14} B_{14} = '00'$ are equal bit pairs, whereas the third bit pair $A_{13} B_{13} = '10'$ is the unequal most significant bit pair. The set 2 examines the presence of equal bit pairs but due to the presence of unequal most significant bit pair, the outputs of set 2 are $E3 = '1'$, $E2 = '0'$, $E1 = '0'$, $E0 = '0'$ and $AEB = '0'$ due to logical AND operation. Since, unequal most significant bit pair $A_5 B_5 = '10'$ is encountered during the comparison

process, the output of set 3 is obtained as $C3,1C3,2C3,3C3,4$, $C2,1C2,2C2,3C2,4, C1,1C1,2C1,3C1,4, C0,1C0,2C0,3C0,4 =$ '1101,1111,1111,1111'. Set 4 combines four nibbles obtained from the four partitions of set 3 into 4 bit data as '1000'. Finally, set 5 acquires the 4 bit input pattern from set 4 and output bit 'AEB' from set 2 to give the final decision. Since A is greater than B, the proposed comparator structure provides the outputs $AGB = '1'$, $ALB = '0'$ and $AEB = '0'$.

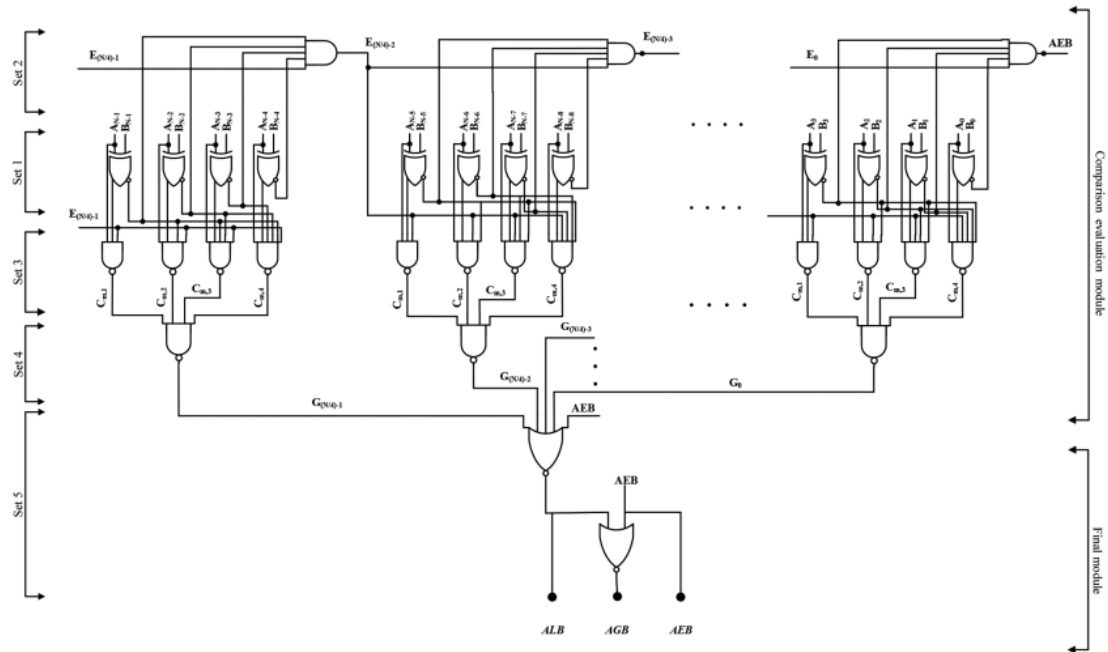


Fig 3.1: N-Bit Digital Comparator

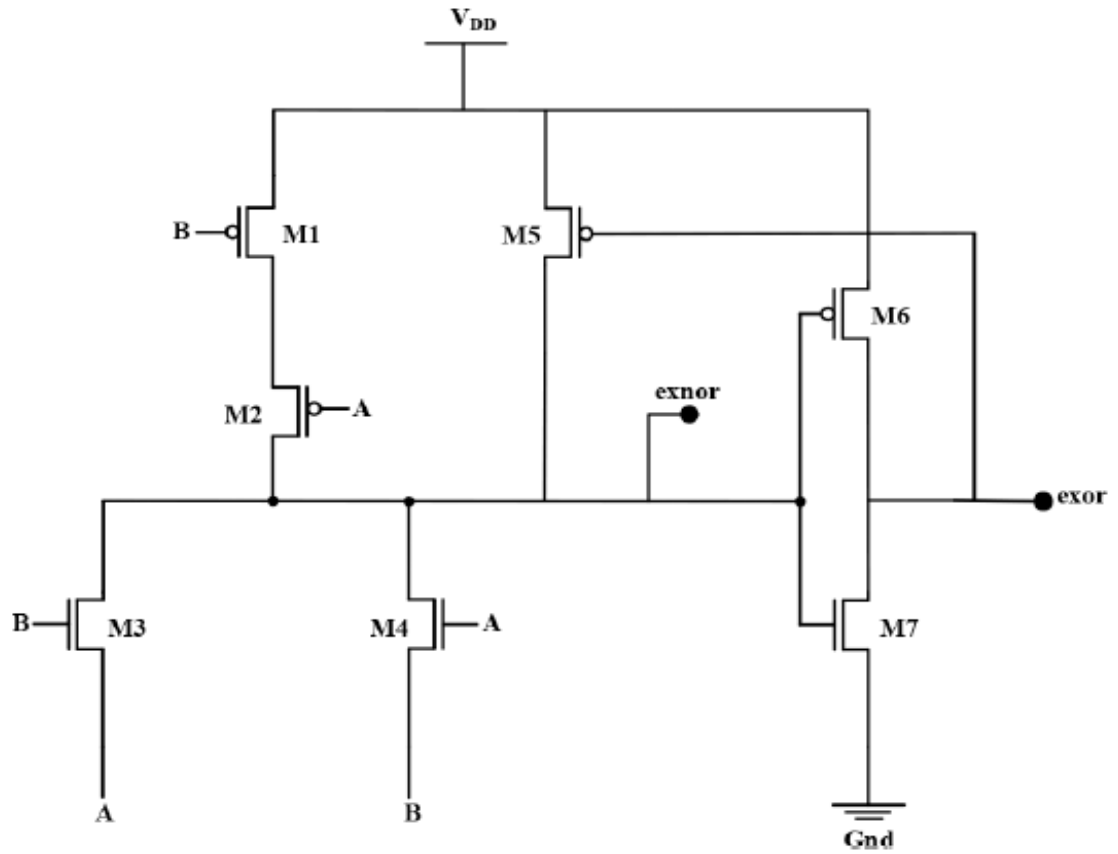


Fig 3.2: Proposed EX-OR-NOR Cell

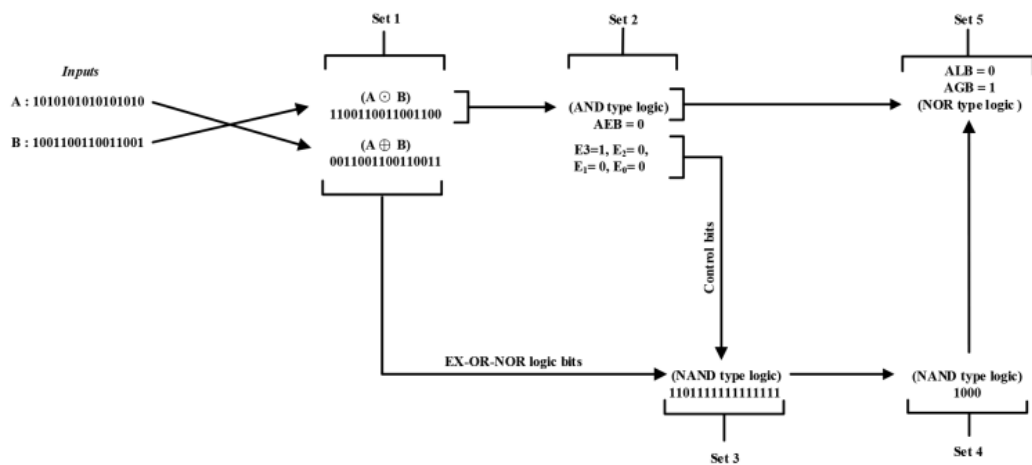


Fig 3.3: 16 bit comparison using the proposed N-bit digital comparator

4. SOFTWARE DESCRIPTION

4.1 Overview

HSPICE is the industry's "gold standard" for accurate circuit simulation and offers foundry-certified MOS device models with state-of-the-art simulation and analysis algorithms. With extensive usage in analog/RF/mixed-signal IC design, cell and memory characterization, and chip/package/ board/backplane signal integrity simulation, HSPICE is the industry's most popular, trusted and comprehensive circuit simulator.

4.2 Foundry-Certified Models

Device models are the ingredients for accurate circuit simulation. HSPICE is consistently first to provide new advanced device models and HSPICE models are first to be foundry-certified. Over the years, HSPICE has consistently engineered leading-edge modeling technology for advanced node CMOS, FinFET and FDSOI processes that ensures the most advanced and accurate set of industry-standard device-model implementations. Synopsys collaborates closely with leading commercial and proprietary foundries to ensure that their HSPICE model parameters are timely and accurately validated to their fabrication process. The comprehensive set of HSPICE models have been extensively proven over the broadest set of semiconductor technologies, ranging from the Compact Modeling Council (CMC) standardized models (BSIM, PSP, HiSIM, etc.) on the latest technology nodes to proprietary models (HVMOS, TFT, etc.) for specialized applications (high voltage, display, etc.)

4.3 Analog/RF/Mixed-signal IC Design

Runtime Performance - Single and Multicore simulation

HSPICE's simulation accuracy, "out of the box" convergence, and runtime performance across all circuit types continue to be the number one focus of the HSPICE R&D team. Release to release, Synopsys R&D improves HSPICE's runtime performance without sacrificing accuracy. Over the last 2 years, HSPICE's runtime performance on one core has improved, on average, over 5X on large pre and post layout analog, mixed-signal, and memory designs. In addition, HSPICE delivers superior multi-core scalability with an average of additional 8X speed up on 16 cores.

Integration with Synopsys Custom Compiler™ and Custom WaveView™

Synopsys Custom Compiler provides Analog, RF, and mixed-signal designers with a front-to-back, schematic-to-layout, modern era design cockpit with full HSPICE

support. Please see: www.Synopsys.com > Silicon Design & Verification > Custom Design.

Verilog-A Behavioral Modeling

Verilog-A has been shown to be an ideal language for describing analog circuit behavior and complicated test bench input stimuli. Using HSPICE's compiled LRM 2.4 compliant Verilog-A simulation, users can mix transistor level and Verilog-A behavioral descriptions in the same netlists and improve runtime performance.

4.4 Reliability Aware Verification - Process Variability and MOSRA Device Reliability Analysis Sophisticated analyses such as HSPICE MOSRA, worst case corners, Monte Carlo, ACMatch, and DCMatch allow a user to optimize a circuit that satisfies the design constraints across various processes, voltages, temperature ranges and device ages. In addition to device process variation, HSPICE and StarRC together can support interconnect variation. HSPICE not only reports the effect of variation on yield but also identifies the critical yield limiting devices and parameters. HSPICE design for yield features include:

- Corner Case Analysis: HSPICE can easily explore process corners and operating conditions for a design in order to analyze its yield, power, and performance
- Smart Monte Carlo sampling: Latin Hypercube sampling and Low Discrepancy Sequences for efficient and accurate yield analysis
- Sigma Amplification: increases process variation in SPICE model by a scale factor to cover high σ variation analysis with fewer samples and faster turn-around time. Ideal for large mixed-signal IP robustness validation
- ACMatch and DCMatch: for analyzing parameter mismatch effects due to local variation
- Variation Block: powerful and flexible mechanism for defining process variation effects
- MOSRA device reliability analysis: simulate HCI and NBTI device aging effects

Loop Stability Analysis

HSPICE's loop stability analysis enables users to analyze loop gain and phase characteristics on feedback circuits in frequency domain.

Transient Noise Analysis

HSPICE's transient noise analysis enables users to predict the effects of device noise (channel, thermal, flicker, and shot noise) on time domain waveforms. Transient noise analysis can be used to characterize phase noise and jitter for PLL applications. Multi-sample Monte Carlo samples generate an ensemble of noise

stimulated waveforms for statistical evaluation. HSPICE supports noise bandwidth and scaling controls and enables the user to plot histograms of the simulation results.

Large Signal Periodic Steady-State Analysis

HSPICE can perform key large signal analyses including periodic steady-state (PSS) analysis, periodic noise and phase-noise analysis, and periodic AC analysis and much more using either the Shooting Newton (SN) engine (for strongly non-linear circuits) or the Harmonic Balance (HB) engine (for weakly non-linear circuits). HSPICE can quickly and accurately simulate large non-linear, highfrequency designs. With a complete array of specialized analyses, HSPICE is the clear choice for both traditional RFIC applications and high-frequency phase noise and jitter analysis.

4.5 Cell and Memory Characterization

HSPICE is ideal for performing accurate cell and memory characterization and provides versatile waveform measurement functions based on simulation data. A data-driven parameter sweep automates characterization by simultaneously varying parameters to conveniently handle hundreds of HSPICE simulations parameters.

Improved Performance

HSPICE has significantly enhanced its performance (read-in, simulation, and total throughput) while maintaining the same high level of accuracy. The improved simulation performance is achieved by an enhanced time-step control algorithm, combined with a simplified simulation control interface. The user can scale simulation options simultaneously using a single control option eliminating the need for users to adjust multiple option settings. HSPICE automatically adjusts each time-step size and other simulation options to meet the desired accuracy level.

Improved Integration

HSPICE's client server mode option enables users to speed up simulation and total turnaround time. When running HSPICE with the client server mode option, HSPICE shortens total turnaround time by minimizing the re-reading of models and netlists and minimizing the number of license check-ins and check-outs. With improved performance and integrations with cell and memory characterization environments, HSPICE can quickly and easily explore multiple process corners and operating conditions across large cell and memory libraries.

4.6 Chip/Package/Board/Backplane Signal Integrity (SI) Simulation

Advanced Elements and Sources

As chip and board speeds continue to increase, new design and verification challenges emerge. HSPICE reveals signal integrity problems caused by jitter, crosstalk, ringing, ground bounce, and other noise sources. With extensive model and element support, HSPICE is the only simulator that can satisfy your silicon-to-package-to-board-to-backplane SI simulation needs.

Statistical Eye Diagram Analysis (with IBIS AMI)

With HSPICE's new StatEye analysis, designers can accurately simulate bit error rate measurements in a single simulation and display bathtub plots in what used to require a million transient simulations to attain the same coverage. For accurate modeling of SERDES equalizers, HSPICE's StatEye supports the Algorithm Modeling Interface (AMI), part of the IBIS 6.0 specification.

S-element

Users can readily create accurate S-parameter models based on direct measurements from a network analyzer or the solutions of a field solver. HSPICE supports S-parameter models with an arbitrary number of differential and single-ended ports. HSPICE's recursive convolution algorithm can quickly and accurately simulate S-parameters with over 1000 ports for large packages and other applications. HSPICE provides for S-parameter extraction directly using the .LIN command, resulting in more accurate, detailed measurements.

W-element

By handling dielectric loss, HSPICE's W-element can accurately simulate 50-inch, 50-GHz transmission lines. In addition, S-parameters can be incorporated in the W-element for interconnect simulation. More Sources, Elements and Models HSPICE supports pseudo-random and bit-pattern sources, E & G elements, IBIS models and much more for all your SI simulation needs.

4.7 Operating Systems

- Redhat Enterprise Linux v6.6-6.8, v7.1-7.3
- SUSE Linux 11-SP4, 12, 12-SP2
- Windows 7, 10, Server 2016

5. RESULTS AND CONCLUSION

Synopsis HSpice with 130 nm technology is used to perform Transient analysis.

5.1 INVERTER GATE

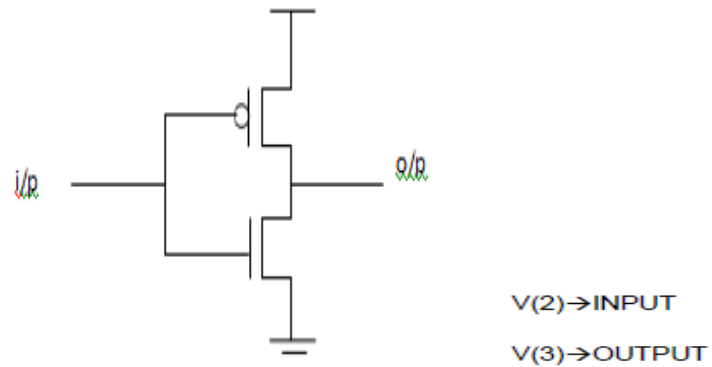
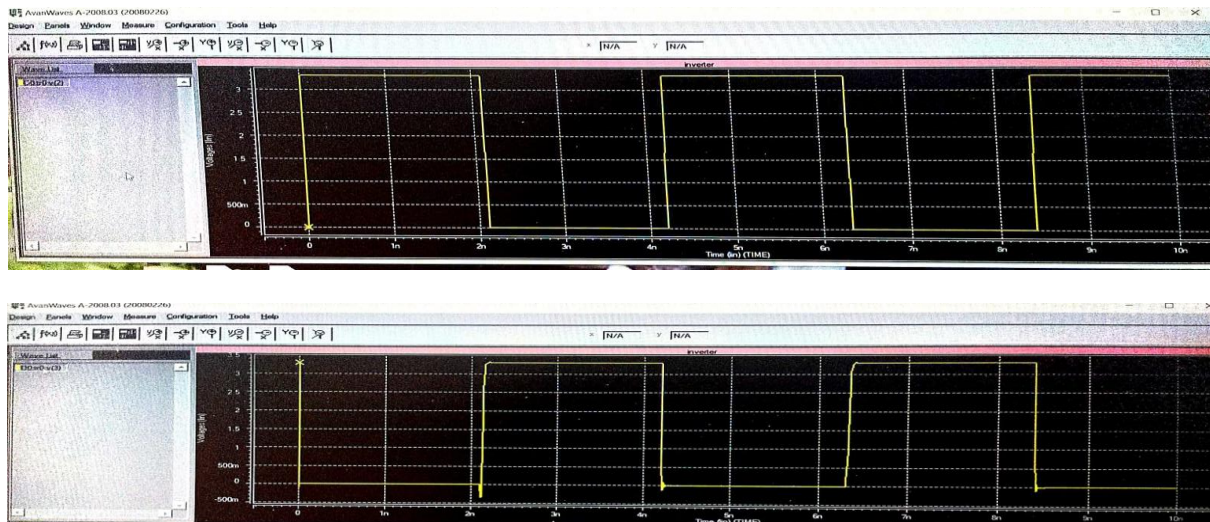


Fig 5.1.1 Inverter



5.2 AND GATE

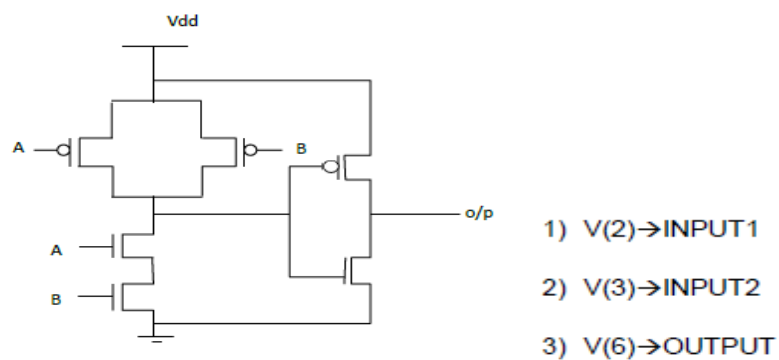


Fig 5.2.1 AND gate

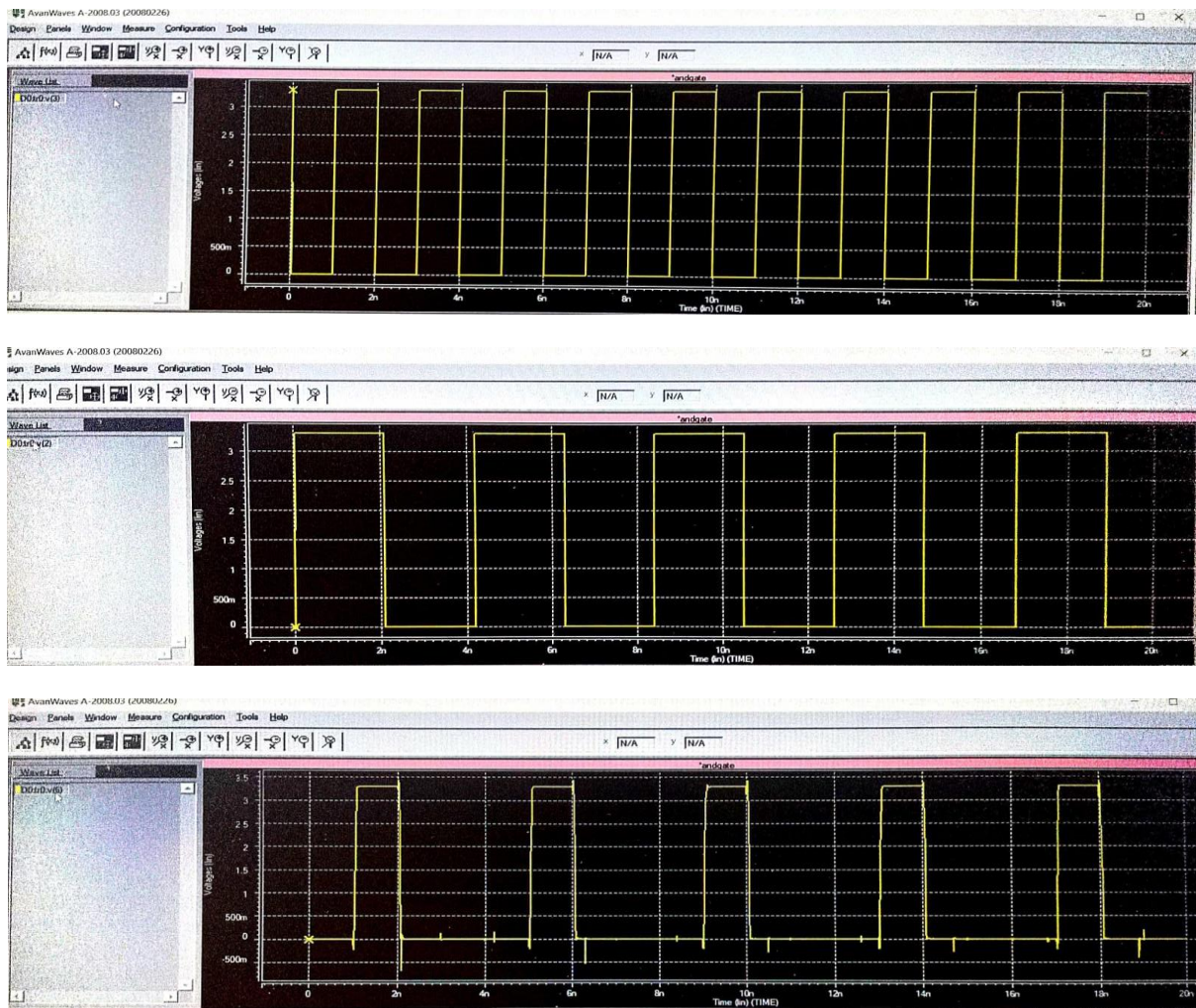
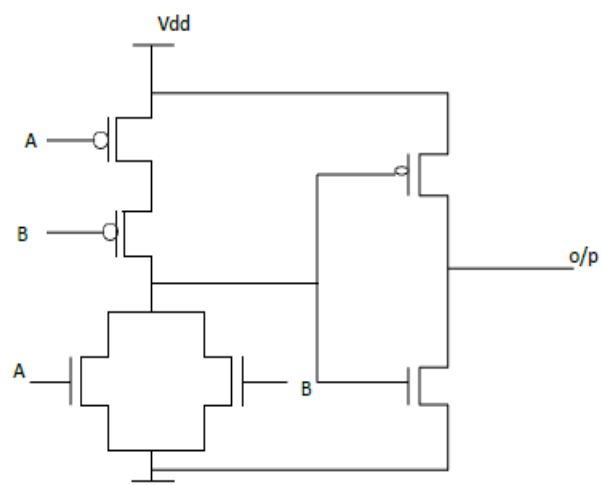


Fig 5.2.2 Transient analysis of AND gate

5.3 OR gate



- 1) V(2)→INPUT1
- 2) V(3)→INPUT2
- 3) V(6)→OUTPUT

Fig 5.3.1 OR gate

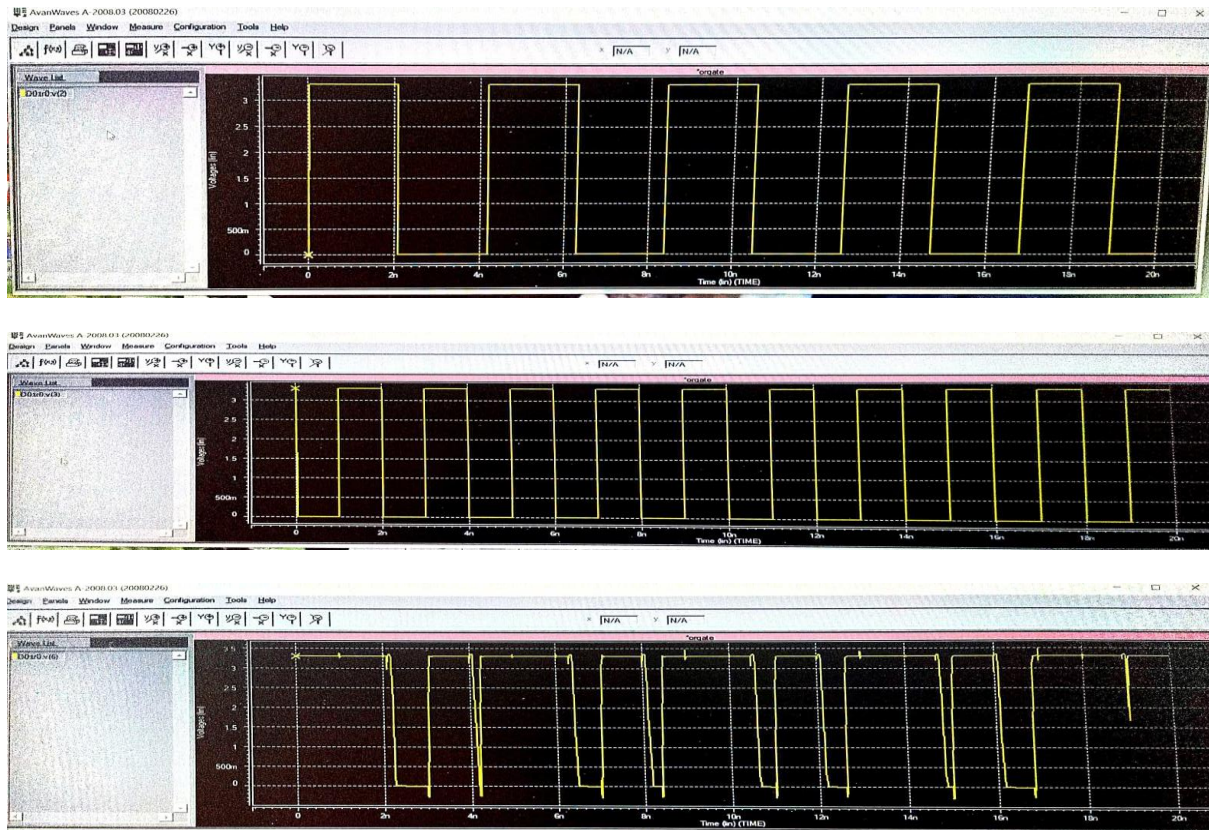


Fig 5.3.2 Transient analysis of OR gate

5.4 NOR gate

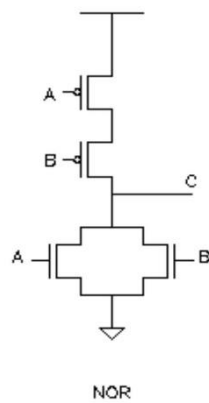


Fig 5.4.1 NOR gate

1. V(2)- INPUT1
2. V(3)- INPUT 2
3. V(5)- OUTPUT

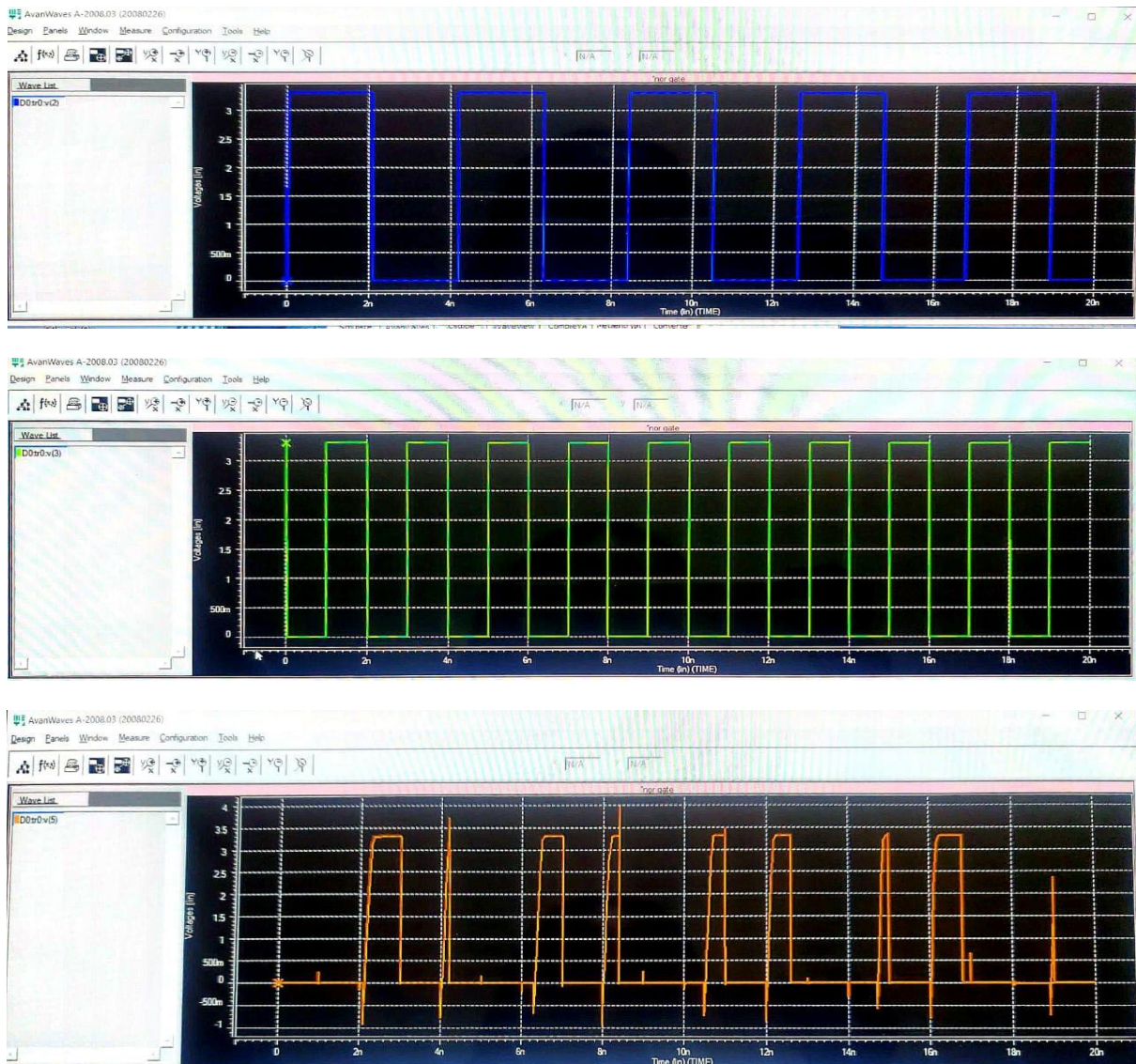


Fig 5.4.2 Transient analysis of NOR gate

5.5 NAND gate

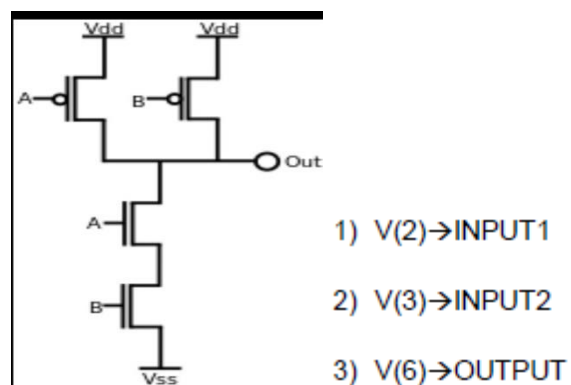


Fig 5.5.1 NAND gate

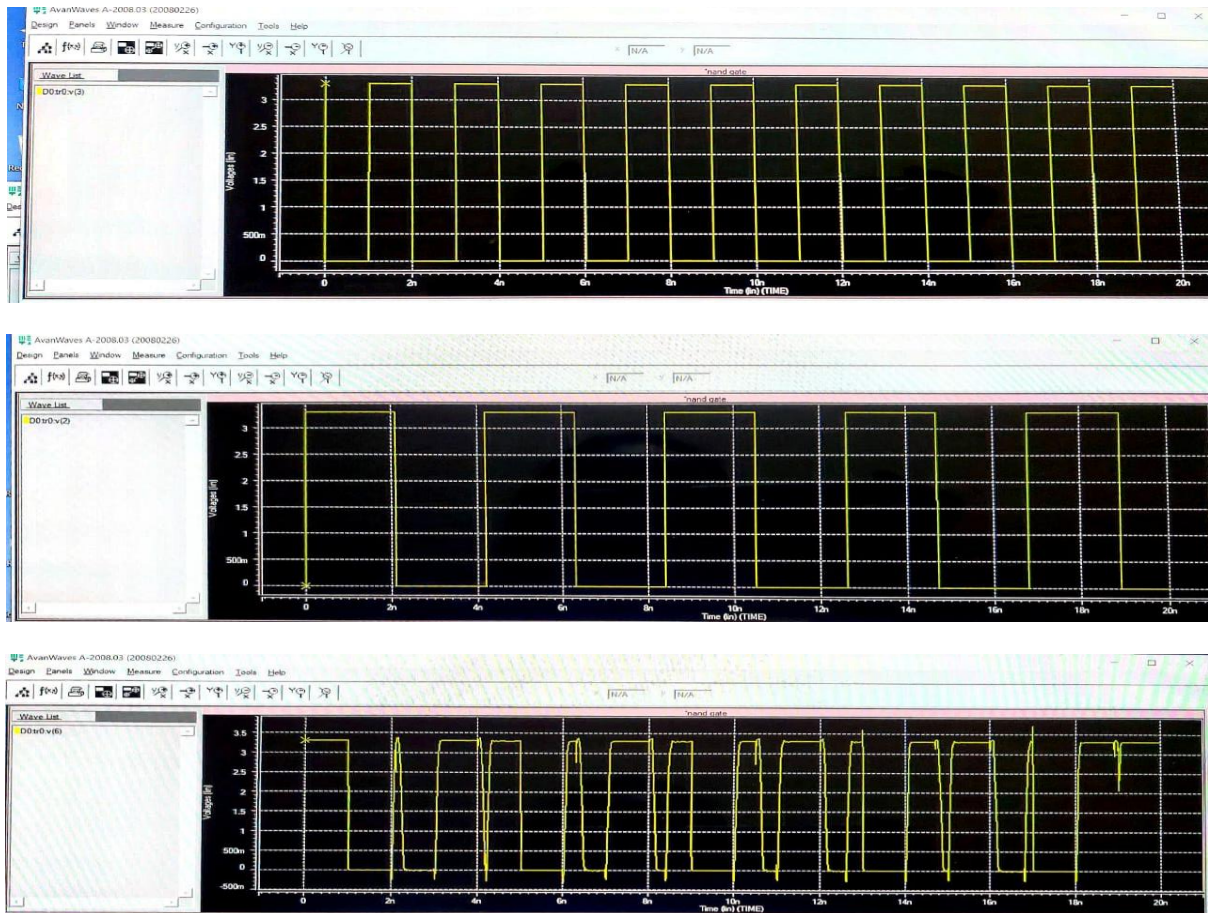


Fig 5.5.2 Transient analysis of NAND gate

5.6 XOR gate

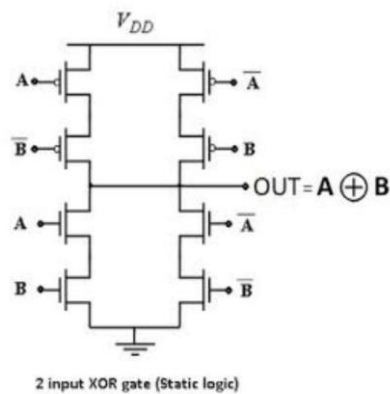


Fig 5.6.1 XOR gate

1. V(2)- INPUT1
2. V(3)- INPUT 2
3. V(5)- OUTPUT

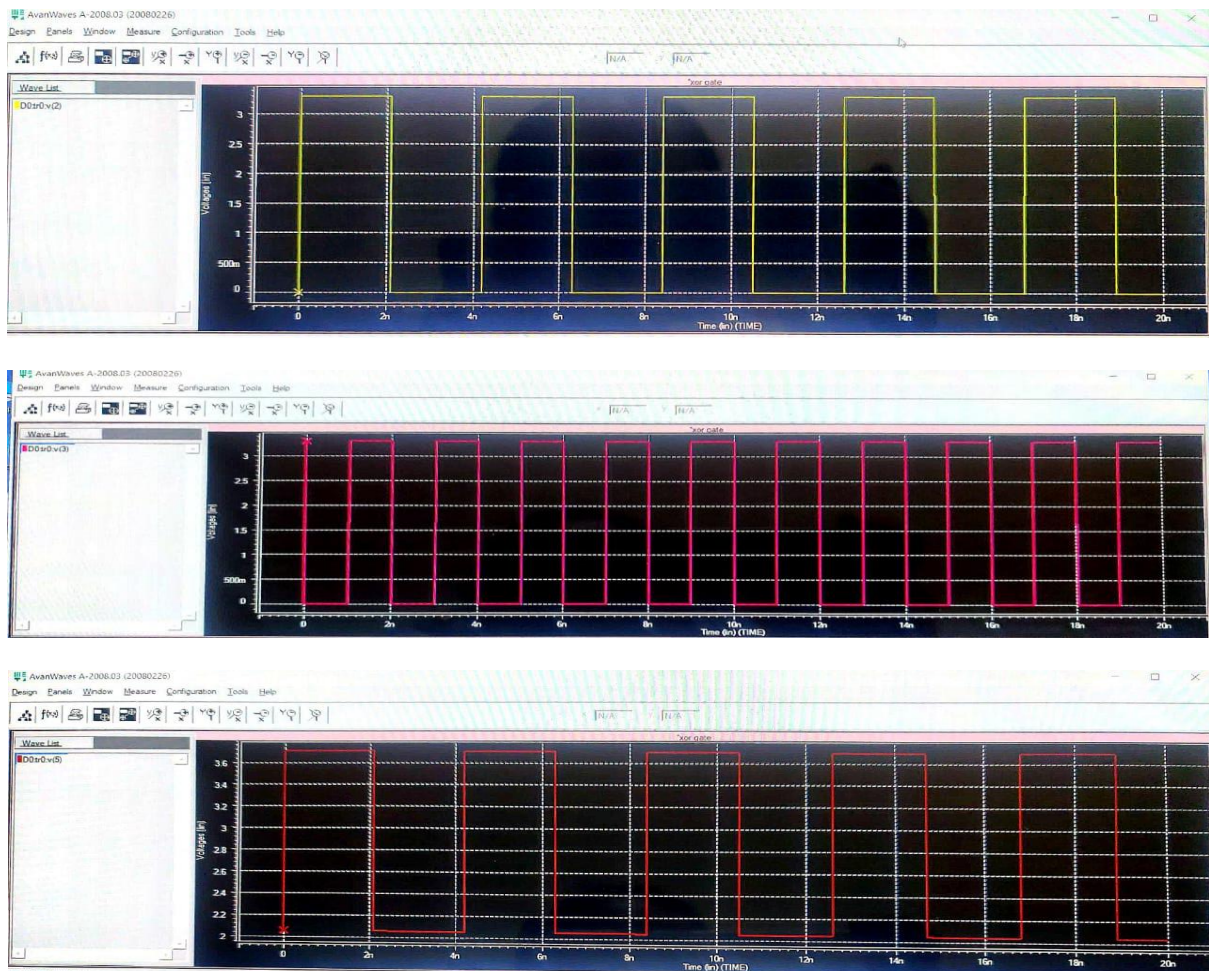
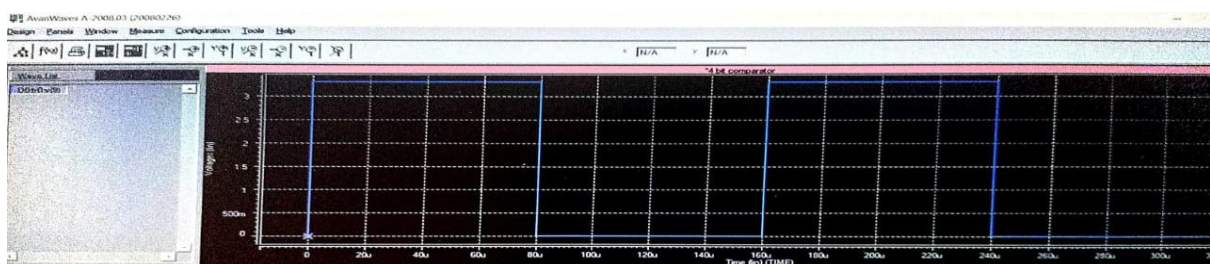
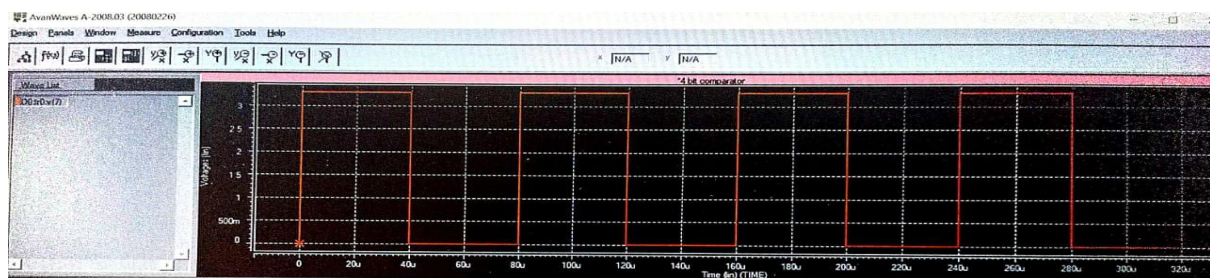
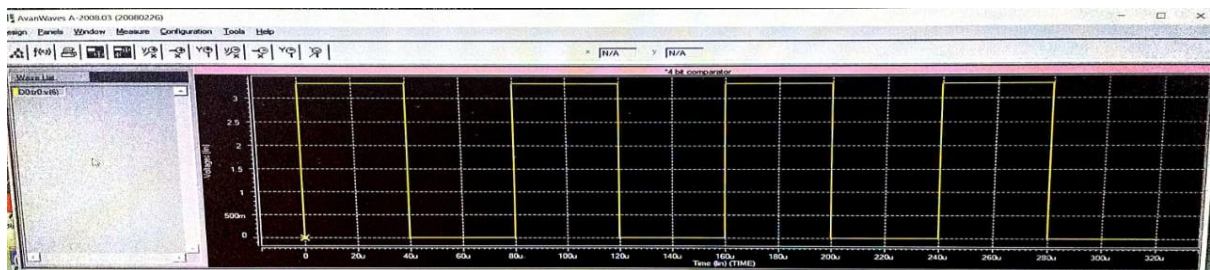
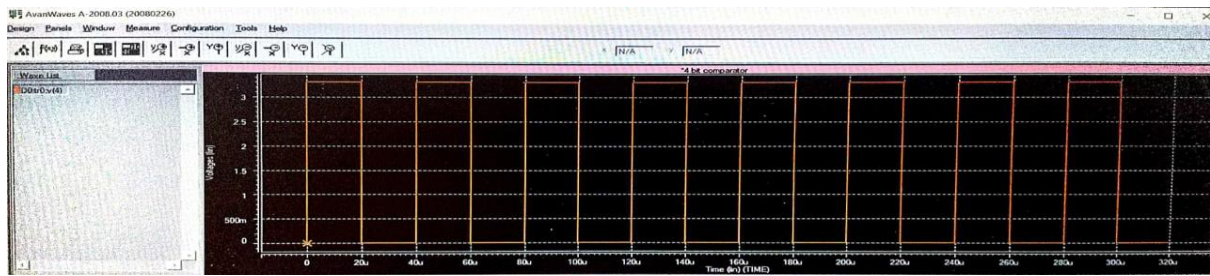


Fig 5.6.2 Transient analysis of XOR gate

5.7 Conventional 4-bit Comparator (Existing)





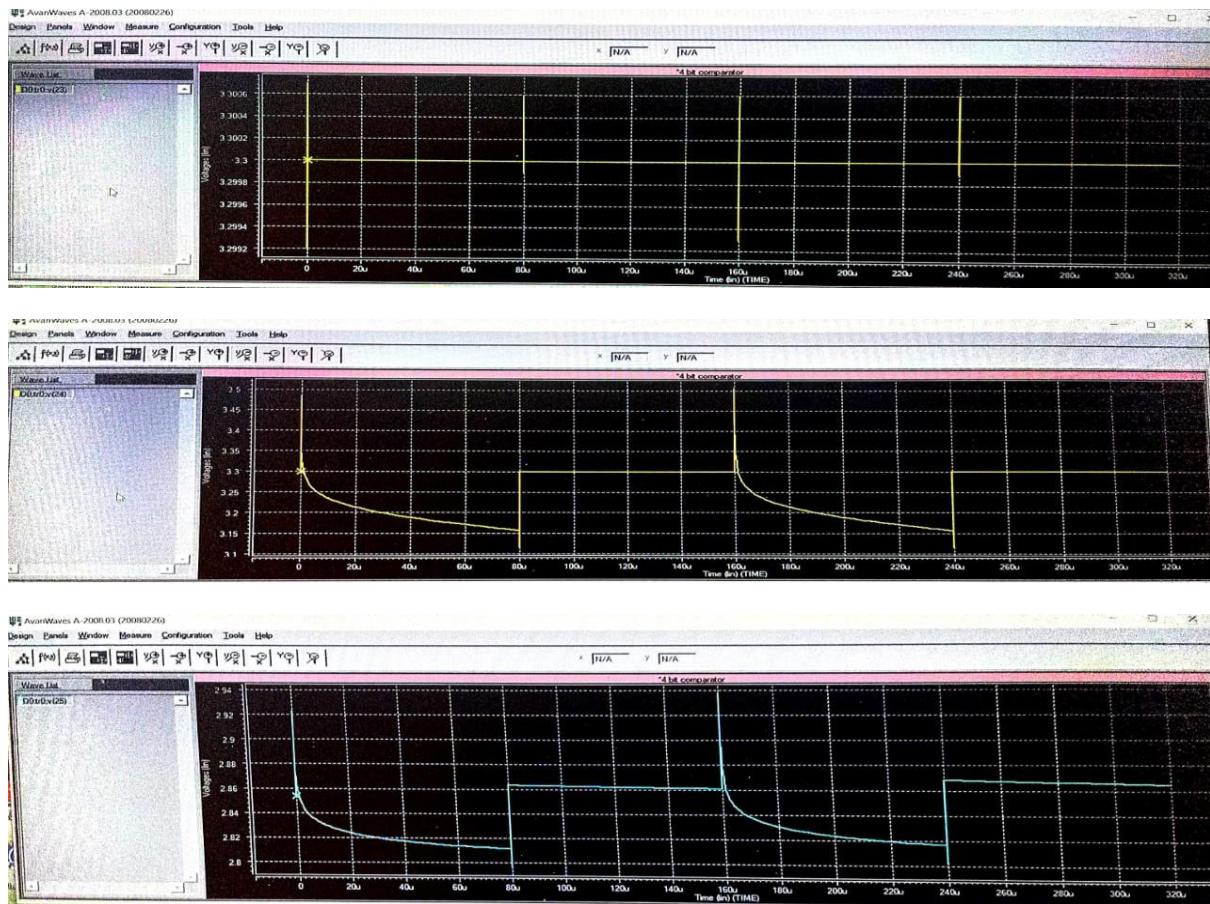


Fig 5.7 Transient analysis of Conventional 4-bit Comparator (Existing)

5.8 Proposed EX-OR-NOR Cell – Transient Analysis



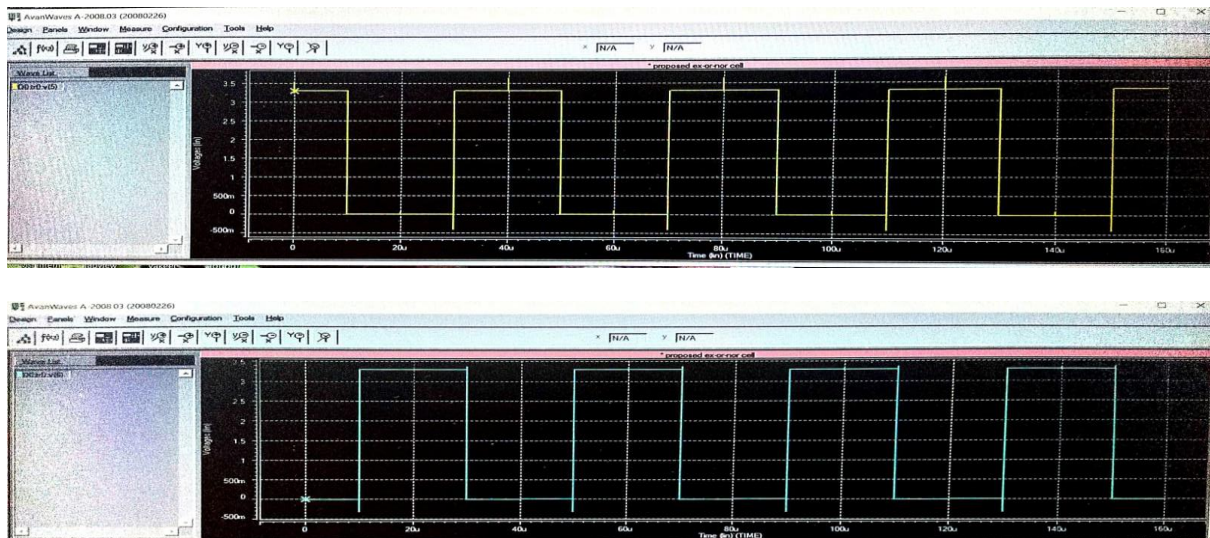


Fig 5.8 Transient Analysis of Proposed EX-OR-NOR Cell

5.9 Proposed 4-bit Comparator

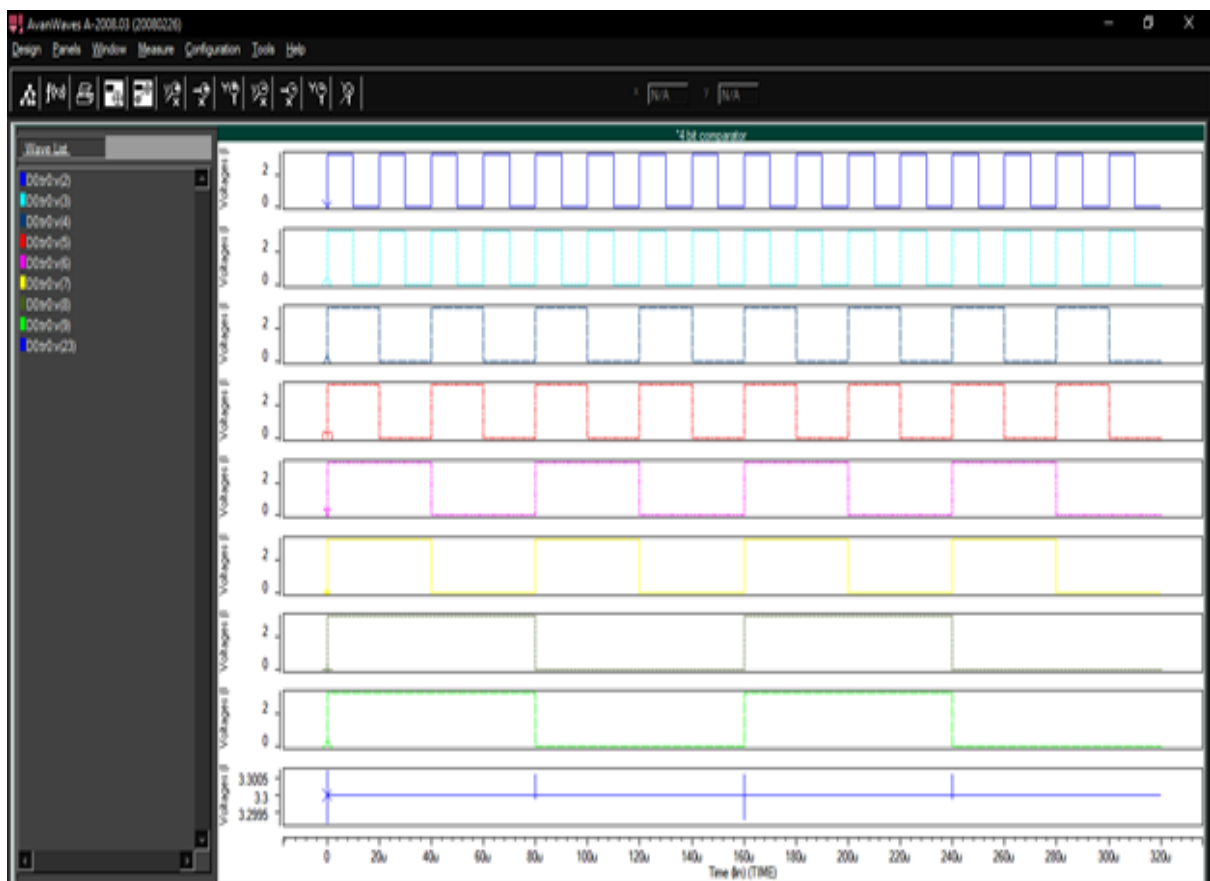


Fig 5.9 Transient analysis of proposed 4 bit comparator

5.10 POWER ANALYSIS

Average Power consumption by proposed EX-OR-NOR CELL is 0.825 microwatts.

In the case of Existing 4 bit digital comparator, the average power consumption is about 6.346 microwatts.

Whereas, in the case of proposed EX-OR-NOR CELL based 4 bit digital comparator, the average power consumption is about 5.442 microwatts. The objective of power analysis is fulfilled here and reduction in average power consumption is observed.

6. CONCLUSION

The existing 4bit digital comparator has been designed and analyzed in Synopsis H-Spice environment. The proposed EX-OR-NOR cell based 4bit digital comparator has designed and power analysis has been performed in H-Spice environment. In the proposed design, 0.904 microwatt power consumption has been reduced when compared to the existing design. Therefore, around 15% of the power consumption has been reduced in the proposed design.

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