

DESIGN AND ANALYSIS OF CUSTOM STANDARD-CELL LIBRARY FOR MIXED-SIGNAL APPLICATIONS

Submitted in partial fulfilment of the requirements of the award of
Bachelor of Engineering Degree
in Electronics and Communication Engineering

by

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SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

**Accredited with Grade "A" by NAAC
JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI- 600 119.**

MAY 2022



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BONAFIDE CERTIFICATE

This is to certify that this project report is the bonafide work of ANIRUDH LAKSHMANAN (38130010) and GAURAV KUMAR MISHRA (38130068) who carried out the project entitled “**DESIGN AND ANALYSIS OF CUSTOM STANDARD-CELL LIBRARY FOR MIXED-SIGNAL APPLICATIONS**” under my supervision from AUGUST 2021 to MAY 2022.

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Submitted for Viva voce Examination held on _____

Internal Examiner

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DECLARATION

We ANIRUDH LAKSHMANAN (38130010) and GAURAV KUMAR MISHRA (38130068) hereby declare that the Project Report entitled “**DESIGN AND ANALYSIS OF CUSTOM STANDARD-CELL LIBRARY FOR MIXED-SIGNAL APPLICATIONS**” done by us under the guidance of Dr. T. RAVI M.E., Ph.D., is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

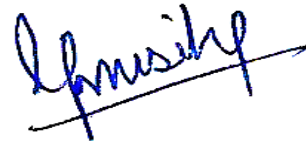
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ABSTRACT

This project describes the construction of 7nm FinFET full custom standard cell library, and hence evaluating the performance based on various parameters. The ASAP7 PDK is used as it is open-source tool provided by Arizona state University. The library consists of basic gates with variable inputs and load driving force. Layouts are optimized in a very predictive manner to increase performance and get desired applications. Given also is a brief definition of process on how to make standard cells using a PDK. A continuous effort was made to reduce the area occupancy of the standard cell to minimum as to get maximum parametric performance.

Implementation of any complex digital circuit requires digital synthesis and therefore a digital standard cell library. Absence of the standard cell libraries in core design kits provided by the foundries is a significant hurdle for academic institutions to design complex electronic systems. Therefore, design of a custom digital library becomes a necessary step for a successful mixed-signal design. In this project, the design of such a custom digital library is presented. The library was designed in 7nm FinFET technology. The composition of available cells and its effect on the performance and area of the synthesized block are discussed. Moreover, different approaches to the transistor dimensioning are compared regarding design effort and performance. The primary aim for designing and analyzing this 7nm FinFET Full Custom Standard Cell Library is to save time for a lot of IC Design engineers since they can make use of this library.

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LIST OF SYMBOLS AND ABBREVIATIONS

ASIC	Application Specific Integrated Circuit
CMOS	Complementary Metal oxide Semiconductor
CNTFET	Carbon Nanotube Field-Effect Transistor
DRC	Design Rule Check
FET	Field-Effect Transistor
FinFET	Fin Field-Effect Transistor
GaAs	Gallium arsenide
GDS	Graphic Data Stream
GND	ground
GNRFET	Graphene Nanoribbon Field-Effect Transistor
IC	Integrated Circuits
JFET	Junction Field-Effect Transistor
LIG	Local Interconnect Gate
LISD	Local Interconnect Source-Drain
LVS	Layout versus Schematics
MESFET	Metal–Semiconductor Field-Effect Transistor
MODFET	Modulation-Doped Field Effect Transistor
MOL	Metal Oxide Layer
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
nm	nanometer
NMOS	n-channel, enhancement mode Metal–Oxide–Semiconductor Field-Effect Transistor
PMOS	p-channel, enhancement mode Metal–Oxide–Semiconductor Field-Effect Transistor
PDK	Process Design Kit

PnR	Placement and Route
PTM	Predictive Technology Models
QFET	Quantum Field Effect Transistor
SD	Source-Drain
SDT	Source-Drain Trench
VDD	Voltage Drain Drain
VLSI	Very Large-Scale Integration
VSS	Voltage Source Source

CHAPTER 1

INTRODUCTION

Very-large-scale integration (VLSI) is the process of integrating or embedding hundreds of thousands of transistors on a single silicon semiconductor microchip. VLSI technology was conceived in the late 1970s when advanced-level computer processor microchips were under development.

VLSI is one of the most widely used technologies for microchip processors, integrated circuits (IC), and component designing. It was initially designed to support hundreds of thousands of transistor gates on a microchip which, as of 2012, exceeded several billion. All of these transistors are remarkably integrated and embedded within a microchip that has shrunk over time but still can hold enormous amounts of transistors.

1.1 MOORE'S LAW

Moore's law states that the number of transistors per square inch in integrated circuits had doubled every year since the integrated circuit was invented. This law is named after Intel co-founder Gordon E. Moore. Because of his prediction now the law is used in the semiconductor industry to guide long-term planning. Moore's Law is the foundation for exciting new technological capabilities and improved energy efficiency [35].

Several measures of digital technology are improving at exponential rates related to Moore's law, including the size, cost, density, and speed of components. Moore himself wrote only about the density of components (or transistors) at minimum cost. The capabilities of many digital electronic devices are strongly linked to Moore's law: processing speed, memory capacity, sensors, and even the number and size of pixels in digital cameras. All of these are improving at roughly exponential rates as well.

1.1 FIELD-EFFECT TRANSISTOR

The field-effect transistor (FET) is a unipolar transistor that uses an electric field to control the shape and the conductivity of a channel of one type of charge

carrier in a semiconductor material. FETs can be majority-charge-carrier devices, in which the current is carried predominantly by majority carriers, or minority-charge-carrier devices, in which the current is mainly due to a flow of minority carriers. FET consists of four terminals namely source, drain, gate, and substrate. The device consists of an active channel through which charge carriers, electrons or holes, flow from the source to the drain. Source and drain terminal conductors are connected to the semiconductor through ohmic contacts. The conductivity of the channel is a function of potential applied across the gate and source terminals.

1.1.1 Types of FET

The channel of a FET is doped to produce either an n-type semiconductor or a p-type semiconductor. The drain and source may be doped of opposite type to the channel, in the case of depletion mode FETs, or doped of a similar type to the channel as in enhancement mode FETs. Field-effect transistors are also distinguished by the method of insulation between channel and gate. The types of FETs are,

- The JFET (junction field-effect transistor) uses a reverse-biased p–n junction to separate the gate from the body.
- The MOSFET (metal-oxide-semiconductor field-effect transistor) utilizes an insulator (typically SiO₂) between the gate and the body.
- The MESFET (Metal–Semiconductor Field-Effect Transistor) substitutes the p–n junction of the JFET with a Schottky barrier; and is used in GaAs and other III-V semiconductor materials.
- The MODFET (Modulation-Doped Field Effect Transistor) uses a quantum well structure formed by graded doping of the active region.
- The NOMFET is a Nanoparticle Organic Memory Field-Effect Transistor.
- The QFET (Quantum Field Effect Transistor) takes advantage of quantum tunneling to greatly increase the speed of transistor operation by eliminating the traditional transistor's area of electron conduction.

- The GNRFET (Graphene Nanoribbon Field-Effect Transistor) uses a graphene nanoribbon for its channel.
- The CNTFET (Carbon Nanotube Field-Effect Transistor).
- The FinFET (A fin-like structure enclosing the gate on 3 sides)

1.2 FINFET

1.2.1 Structure of FinFET

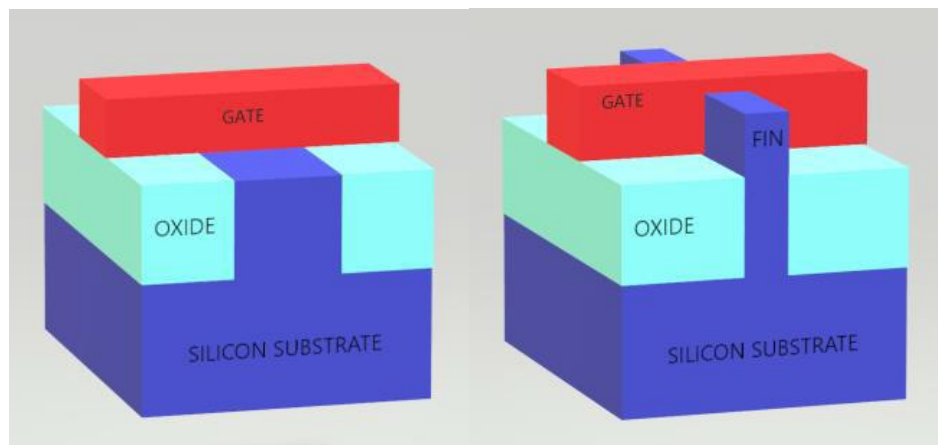


Figure 1.1 structure of MOSFET and FinFET

CMOS is a type of VLSI technology that is used in almost all semiconductor fabricated devices nowadays. In CMOS, the source-drain channel is controlled by a single gate, but in FinFET transistors, the channel is a narrow vertical fin with the gate surrounded by three sides of the channel.

1.2.2 Significance of FinFET recently

FinFETs have been increasingly popular in recent years as a way to reduce short channel effects, optimize leakage, and allow for ongoing VDD scaling. PDKs and Commercial libraries, particularly for advanced nodes, are typically difficult to come by for academic usage, and access to physical layouts is much more limited. As a result, since it is an open-source PDK, the ASAP7 Predictive Technology Models (PTM) PDK created by Arizona State University is used. In advanced nodes, it enables realistic physical design. [10] ASAP7 PDK in general is used to model 7nm FinFET process technology by synthesizing technological data from open source. In November of 2016, the ASAP7 PDK was launched for the first time. The PDK has

been widely utilized in the creation of custom circuits and layouts by many researchers and academicians. [11] FinFET technology provides numerous advantages over the traditional planar CMOS, for example, very less potential is required to drive a FinFET because a channel can be controlled from all sides of the fin. The performance of the FinFET was compared in terms of power delay product, energy-delay product, and power dissipation with the findings indicating that the FinFET is superior. [12]

1.3 TRANSISTOR SCALING

Over the past decades, the MOSFET has continually been scaled down in size, typical MOSFET channel lengths were once several micrometers, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometers. Intel began production of a process featuring a 32 nm feature size in late 2009. The semiconductor industry maintains a "roadmap", the ITRS, which sets the pace for MOSFET development. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and poorer electrical performance necessitating circuit redesign and innovation. Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuit is mainly related to the number of chips that can be produced per wafer.

1.4 STANDARD CELLS IN ASIC DESIGN

Standard cells are well-defined and pre-characterized cells used in ASIC (Application Specific Integrated Circuit) Design flow as basic building blocks. All these cells are equal in height and can easily fit into the standard cell row. Standard cells are highly reusable and save lots of ASIC design time.

1.4.1 *Standard Cell Layout*

All the Standard cells are equal in height and varying width. The main characteristics of a standard cell have been explained with the help of the following figure.

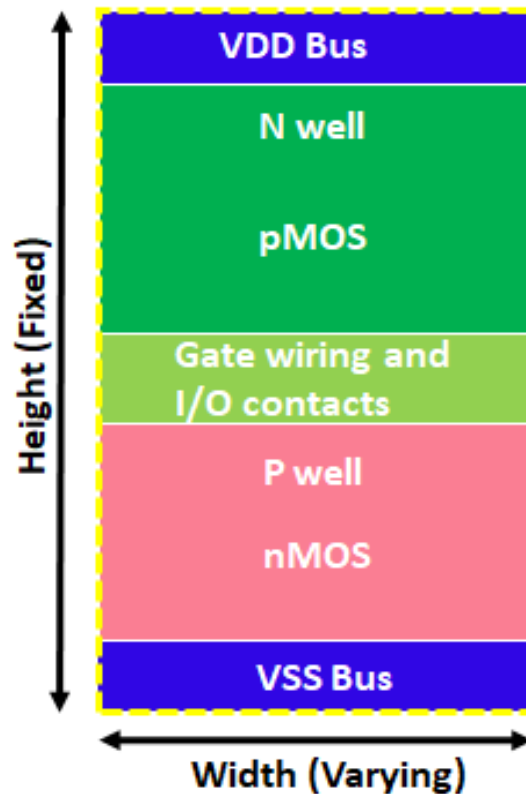


Figure 1.2 Standard Cell layout style

At the top of the standard cell, there is a VDD rail, and bottom there is a VSS rail. Both the Power rails are drawn in the Metal-1 layer. In between the VDD rail and VSS rail, there are three main regions, a nwell region, a gap of nwell and pwell and pwell region. The n-well region is near the VDD rail and the p-well region is near the VSS rail. PMOS transistors are built inside the nwell, so all the PMOS transistors are in the top half of the cell and similarly, all NMOS are in the bottom half of the standard cell.

1.4.2 Tracks in standard cells

The track can be defined as a line on which metal layers are drawn. A track means one M1 Pitch. The height of a Standard cell is generally measured in terms of no. of tracks inside it. like a 6T standard cell means that the height of the standard cell is 6 Track of M1.

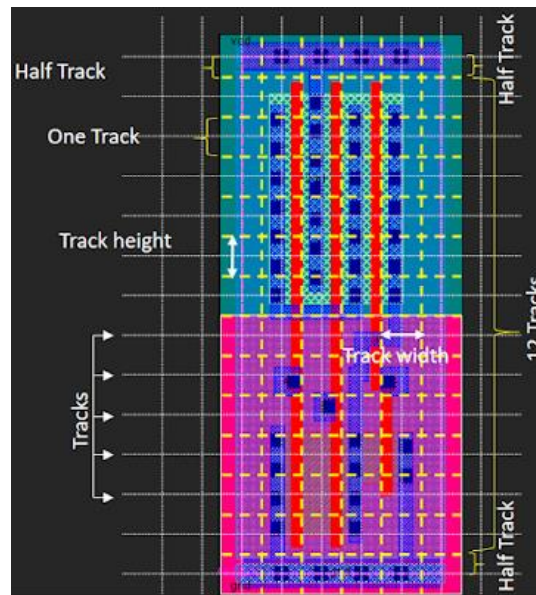


Figure 1.3 A 13T height standard cell

1.4.3 Heights in Standard cell library

Generally, there are various sets of standard cell libraries having different track sizes of standard cells. Depending on the use of ASIC, the track height a standard library has selected. There are generally three sets of standard cell libraries characterized as small transistor standard cell, large transistor standard cell, and medium transistor standard cell.

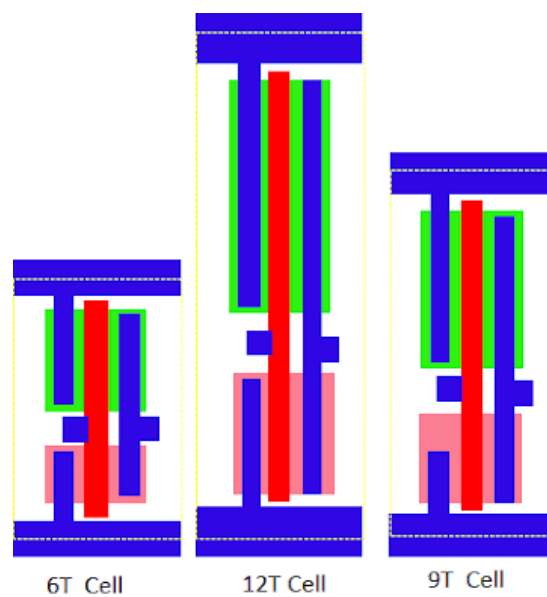


Figure 1.4 Various heights of the standard cell

1.5 PROCESS DESIGN KIT (PDK)

A process design kit (PDK) is a set of files used within the semiconductor industry to model a fabrication process for the design tools used to design an integrated circuit. The PDK is created by the foundry defining a certain technology variation for their processes. It is then passed to their customers to use in the design process. The customers may enhance the PDK, tailoring it to their specific design styles and markets. The designers use the PDK to design, simulate, draw and verify the design before handing the design back to the foundry to produce chips. The data in the PDK is specific to the foundry's process variation and is chosen early in the design process, influenced by the market requirements for the chip. An accurate PDK will increase the chances of first-pass successful silicon.

1.6 LITERATURE SURVEY

J. Pliva et al. (2017) described that for decades, the evolution of CMOS (Complementary metal-oxide-semiconductor) technology has been dominated by continuous scaling. This tendency, however, has distinct consequences for digital and analog circuits. Digital circuits that have been scaled are growing quicker, and the decrease in size and leakage power enable more complicated systems. Since advanced node design criteria must assure compliance with process phases including double-patterning and optical correction, the layout effort is getting increasingly complicated. [1]

Q. Xie et al. (2015) inform that the gradual downscaling of CMOS feature sizes has fueled the steady growth in cost per functionality and circuit speed over the last few decades. Significant challenges (i.e., reducing device-to-device variability, lowering leakage current, and minimizing short channel effects) are encountered with planar CMOS transistor downscaling beyond 22 nm owing to process technology and fundamental material limits. As a result, at technology nodes below 22 nm, a FinFET (Fin Field-effect transistor) has been proposed as an alternative to the planar CMOS device. A FinFET is a type of multi-gate device with a process flow and layout similar to that of a standard planar CMOS device. FinFET devices are said to have superior scalability, lower gate leakage current, better control of short-channel effects, and are less susceptible to gate line-edge coarseness. [2]

S. Ilin et al. (2018) state that adherence to technological and design rules, regulations, and restrictions in semi-custom and bespoke design schemes using 22 nm and lower technology is a difficult technical problem. Synthesis of FinFET technologies is an alternative solution, in particular for advanced technologies. [3]

E. Amr et al. (2016) describe the most significant part of creating Application-Specific Integrated Circuits (ASIC) as Standard Cells. The efficient area, fast speed, and low power consumption are all factors in this efficiency factor. As a result, additional effort, including people, money, and manufacturing capabilities, is always poured into improving the design of standard cell libraries for ASICs. In today's rapidly expanding digital Integrated Circuit (IC) architecture, standard cells with high-efficiency factors are required. Hence, using FinFET devices for standard cell design in 7nm technology would be more advantageous than using other planar CMOS devices. [4]

X. Xu et al. (2017) describe that in most cases, a single standard cell is created and optimized in two stages: schematic and layout design. The presence of FinFET limits the flexibility of a schematic design when turning a gate/circuit into a transistor-level netlist. Furthermore, geometric scaling creates significant challenges in traditional cell layout design, especially when lithography-imposed design limitations are included. Standard cell layout design, for instance, is constrained to a fixed height, i.e., standard cell architecture, resulting in a lengthier routing turnaround time and transistor-level placement. [5]

1.7 LITERATURE SUMMARY

FinFETs have been increasingly popular in recent years as a way to reduce short channel effects, optimize leakage, and allow for ongoing VDD scaling.

FinFET technology provides numerous advantages over the traditional planar CMOS, for example, very less potential is required to drive a FinFET because a channel can be controlled from all sides of the fin. The performance of the FinFET was compared in terms of power delay product, energy-delay product, and power dissipation with the findings indicating that the FinFET is superior.

1.8 PROBLEM DEFINITION

The project is titled “Design and Analysis of 7nm FinFET Full Custom Standard Cell Library using ASAP7 PDK”. PDKs and Commercial libraries, particularly for advanced nodes, are typically difficult to come by for academic usage, and access to physical layouts is much more limited. That is why our goal is to generate a standard cell library that can be utilized by anyone to learn and create new complex layout designs.

1.9 OBJECTIVES OF THE PROJECT

- To undergo a proper literature survey on FinFET, CMOS, 7nm, layouts.
- Learn tools to make circuit diagrams for various gates.
- Learning tools to do a simulation to determine the parameters of the device used.
- Learning tools to do the layout.
- Verification of layout using DRC and LVS.
- Generation of the library by repeating the above steps for all basic gates.

1.10 ORGANIZATION OF REPORT

The project report is organized into five chapters.

Chapter 1 focuses on the FinFET devices and how it works. This chapter also provides a detailed literature survey related to the project.

Chapter 2 depicts the existing process of how a library is created like pre simulations, schematic, layout design, and post simulations.

Chapter 3 describes the proposed schematics and layouts in 7nm technology.

Chapter 4 provides the simulation results and performance analysis of the proposed layout designs using CMOS technology. The performances of proposed designs are analyzed.

Chapter 5 altogether summarizes the project. This chapter as a whole explains the total work that has been performed. This chapter as a whole concludes the project. Finally, the references referred to precede the project are given in brief. The next part of the project report comprises the publications in national/international journals and conferences with proper proofs and attachments.

CHAPTER 2

EXISTING PROCESS OF CONSTRUCTION OF CELL LIBRARY

A standard cell library is a collection of low-level electronic logic functions such as AND, OR, INVERT, flip-flops, latches, and buffers. These cells are realized as fixed-height, variable-width full-custom cells. It helps to reduce the design time drastically. Standard cells used in the ASIC design are a part of a standard cell library along with some other file sets.

As a standard cell library is a collection of well-defined and appropriately characterized logic gates that can be used to implement a digital design. A structured design process is followed every time a standard cell/library is constructed. The device characteristics, model card, and layout rules which are used to make the cell are provided by ASAP 7 PDK.

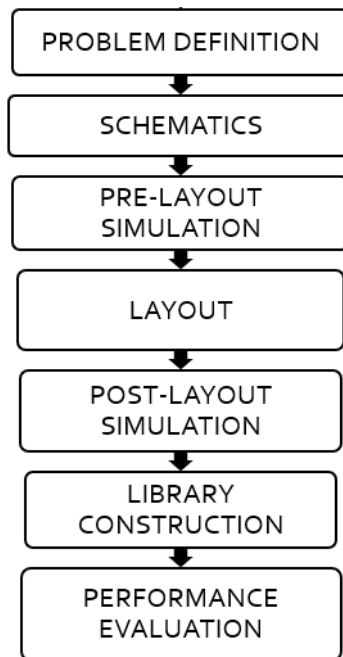


Figure 2.1 Process of library construction

2.1 PROBLEM DEFINITION

Standard cells are the building blocks in integrated circuit design. standard cells must meet predefined specifications to be flawlessly manipulated by synthesis, place, and route algorithms.

Standard cell library contains all and every little factor/attribute (area, timing, power, voltage, temperature, transistor parameters, other geometrical information, etc.) of every cell which will be useful for other calculations and inference in synthesis optimization.

A good standard library should contain:

- A variety of drive strengths for all cells
- Larger varieties of drive strengths for inverters and buffers
- Cells with the balanced rise and fall delays (for clock tree buffers/gated clocks)
- Same logical function and its inversion as separate outputs, within the same cell
- Complex cells (e.g., AOI, OAI)
- High fan in cells
- Variety of flip-flops, both positive and negative edge triggered, preferably with multiple drive strengths
- Single or Multiple outputs available for each flip-flop (e.g., Q only, or Qbar only, or both), preferably with multiple drive strengths.
- Flops to contain different inputs for Set and Reset (e.g., Set only, Reset only, both)
- Variety of latches, both positive and negative level sensitive.
- Several delay cells. Useful for fixing hold time violations.
- To enable scan testing of the designs, each flip-flop should have an equivalent scan flop.

- Flexible to constrain

2.2 SCHEMATICS

First of all, a circuit diagram is formulated that should work as per our desired scope, in our case basic gates like NOT, AND, OR, XOR, etc. As the circuit should work for both digital and analog signals, we have used a static CMOS logic with a pull-up and a pull-down network that complement each other. In Complementary logic, the pull-up network is formed by PMOS and the pull-down network by NMOS. Bodies of the FET device are shorted to VDD and VSS to remove any static voltage deposition on the device.

2.2.1 CMOS Logic Gates

In general, a static CMOS gate has an NMOS pull-down network to connect the output to 0 (GND) and a PMOS pull-up network to connect the output to 1 (VDD), as shown in Figure. The networks are arranged such that one is ON and the other OFF for any input pattern.

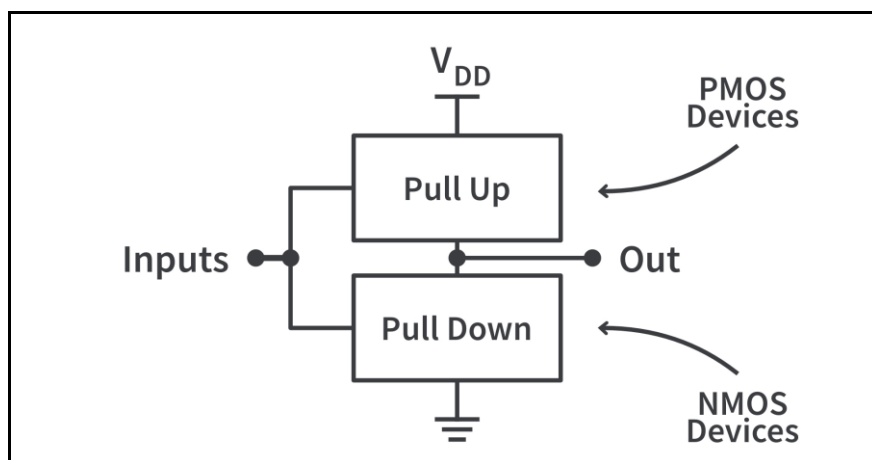


Figure 2.2 CMOS Logic

2.2.2 Inverter as an example

The figure shows the schematic and symbol for a CMOS inverter or NOT gate using one NMOS transistor and one PMOS transistor.

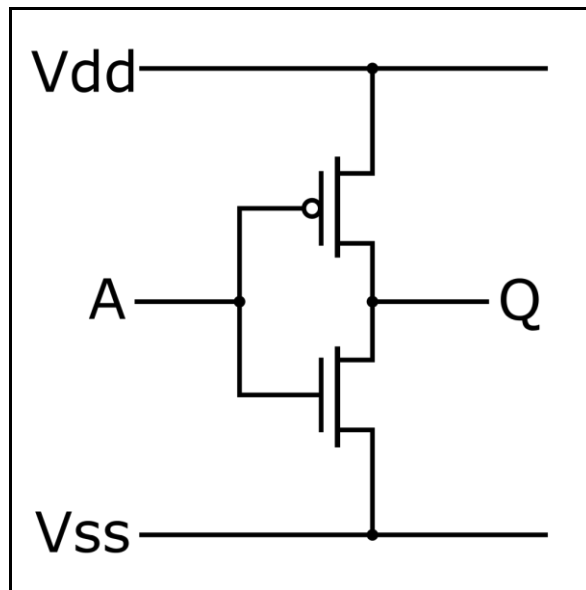


Figure 2.3 Inverter CMOS Logic

The bar at the top indicates VDD and the triangle at the bottom indicates GND. When the input A is 0, the NMOS transistor is OFF and the PMOS transistor is ON. Thus, the output Y is pulled up to 1 because it is connected to VDD but not to GND. Conversely, when A is 1, the NMOS is ON, the PMOS is OFF, and Y is pulled down to '0.'

A	Q
1	0
0	1

Table 2.1 Inverter truth table

"Input 0 makes Output 1" suggests a P-SWITCH connected from a "1" source (VDD) to the output. "Input 1 makes Output 0" suggests an N-SWITCH connected from a "0" source (VSS) to the output.

2.2.3 Combinational Logic

The pull-up and pull-down networks in the inverter each consist of a single transistor. The NAND gate uses a series pull-down network and a parallel pull-up network. More elaborate networks are used for more complex gates. Two or more transistors in series are ON only if all of the series transistors are ON. Two or more transistors in parallel are ON if any of the parallel transistors are ON. By using combinations of these constructions, CMOS combinational gates can be constructed. Although such static CMOS gates are most widely used, it explores alternate ways of building gates with transistors.

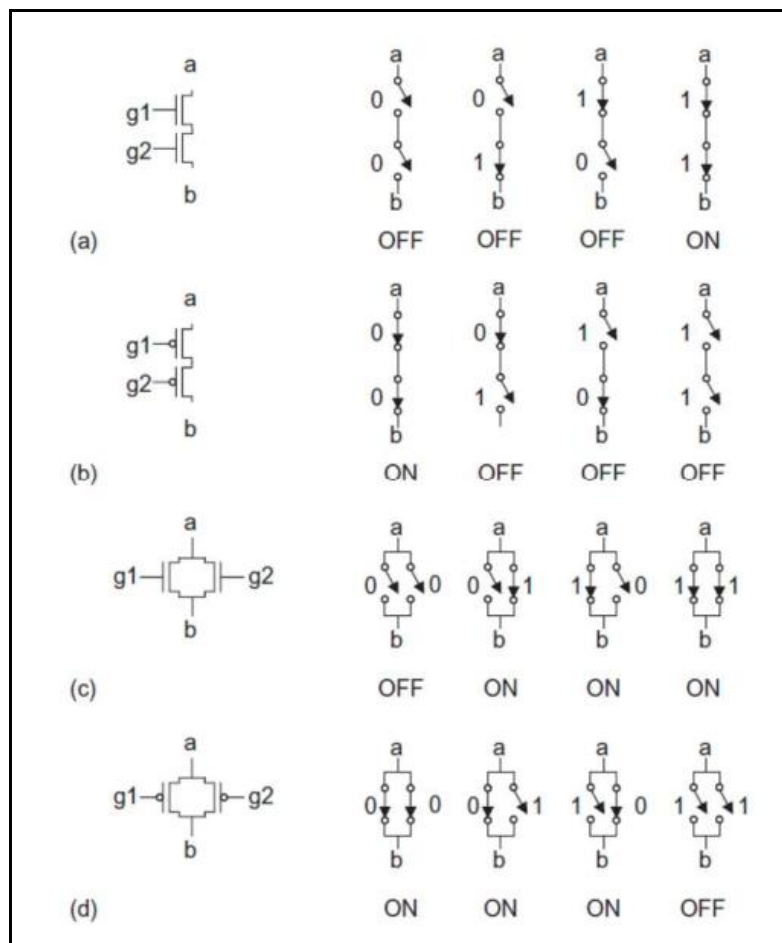


Figure 2.4 Combinations of CMOS logic

In general, when we join a pull-up network to a pull-down network to form a logic gate as shown in Figure, they both will attempt to exert a logic level at the output. The output of a CMOS logic gate can be in four states. The 1 and 0 levels have been encountered with the inverter and NAND gates, where either the pull-up or pull-down is OFF and the other structure is ON. When both pull-up and pull-down are OFF, the high impedance or floating Z output state results. This is of importance

in multiplexers, memory elements, and tri-state bus drivers. The crowbarred (or contention) X level exists when both pull-up and pull-down are simultaneously turned ON. Contention between the two networks results in an indeterminate output level and dissipates static power. It is usually an unwanted condition.

2.2.4 NAND Gate as an example

It consists of two series NMOS transistors between Y and GND and two parallel PMOS transistors between Y and VDD. If either input A or B is 0, at least one of the NMOS transistors will be OFF, breaking the path from Y to GND. But at least one of the PMOS transistors will be ON, creating a path from Y to VDD. Hence, the output Y will be 1. If both inputs are 1, both of the NMOS transistors will be ON and both of the PMOS transistors will be OFF. Hence, the output will be 0. The truth table is given in Table and the symbol is shown in Figure. Note that by DeMorgan's Law, the inversion bubble may be placed on either side of the gate.

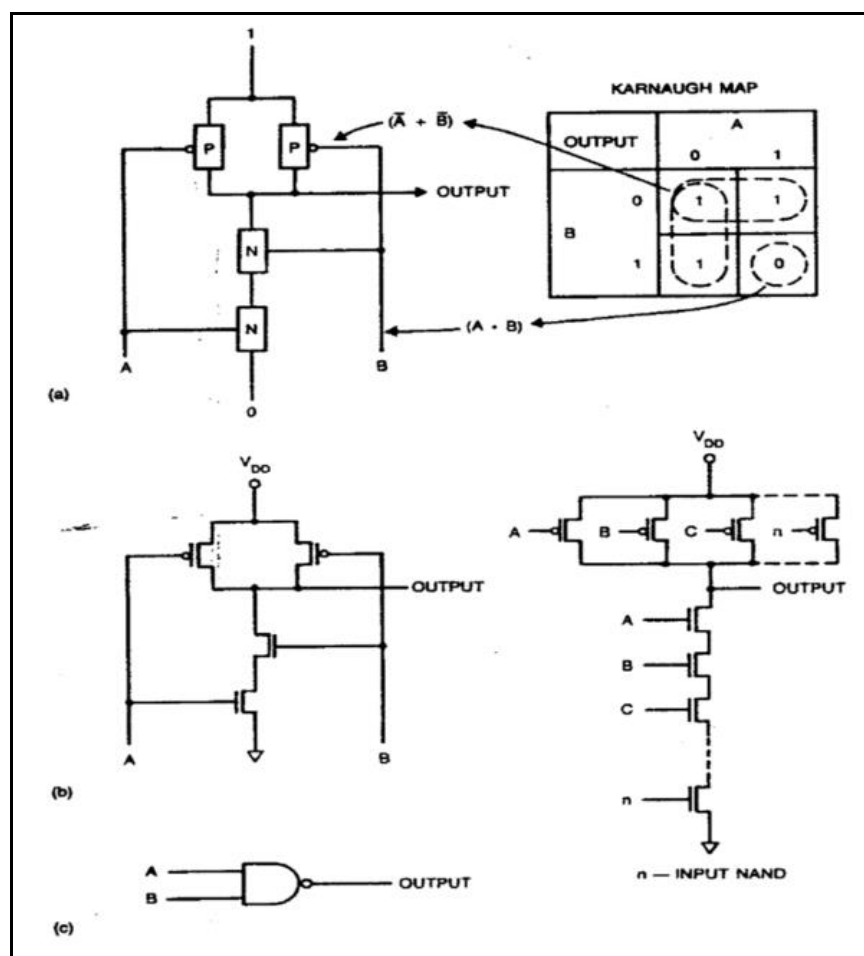


Figure 2.5 NAND Gate combinational logic

2.2.5 Compound Gates

A compound gate performing a more complex logic function in a single stage of logic is formed by using a combination of series and parallel switch structures. For example, the derivation of the circuit for the function $Y = (A \cdot B) + (C \cdot D)$. This function is sometimes called AND-OR-INVERT-22, or AOI22 because it performs the NOR of a pair of 2-input ANDs. For the NMOS pull-down network, take the uninverted expression $((A \cdot B) + (C \cdot D))'$ indicating when the output should be pulled to '0.' The AND expressions $(A \cdot B)$ and $(C \cdot D)$ may be implemented by series connections of switches. Now ORing the result requires the parallel connection of these two structures.

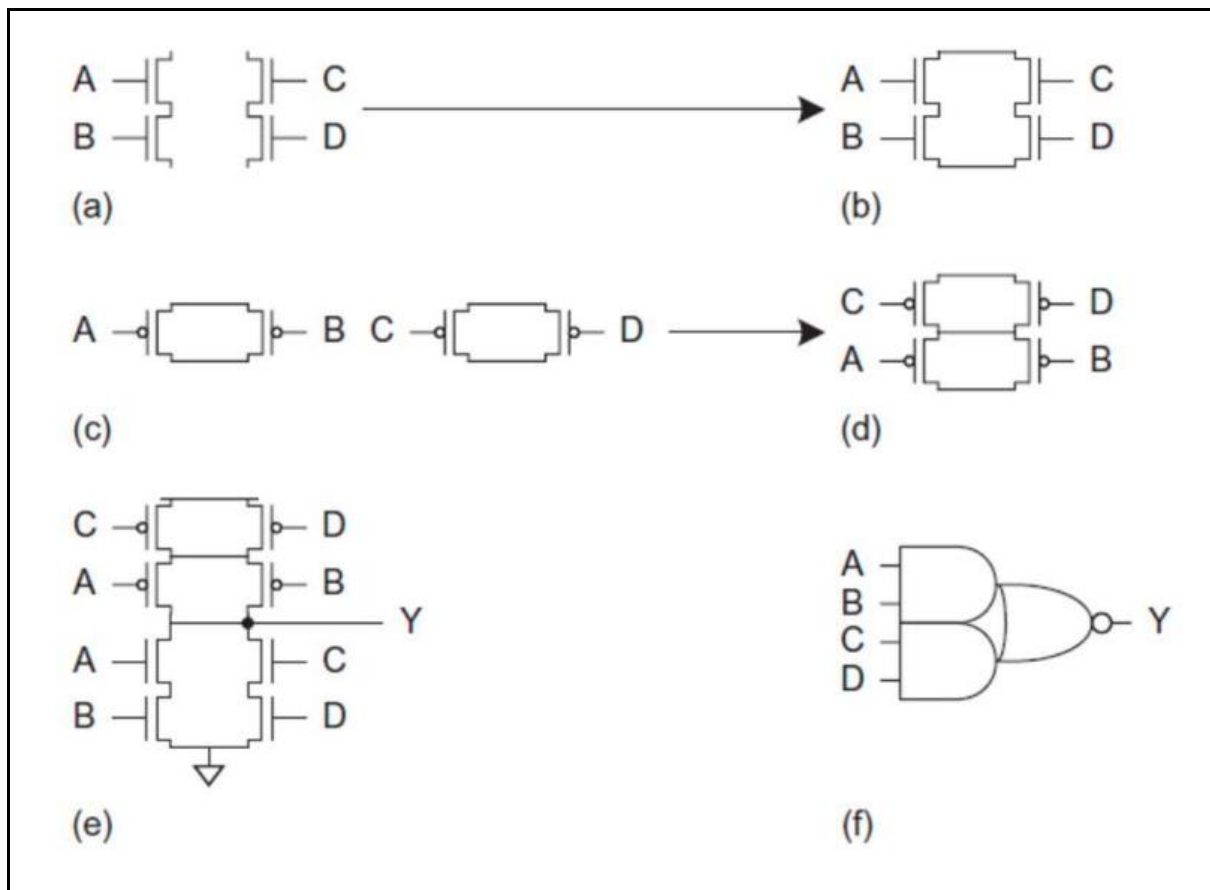


Figure 2.6 Compound gates logic

For the PMOS pull-up network, we must compute the complementary expression using switches that turn on with inverted polarity. By DeMorgan's Law, this is equivalent to interchanging AND OR operations.

Hence, transistors that appear in series in the pull-down network must appear in parallel in the pull-up network. Transistors that appear in parallel in the pulldown network must appear in series in the pull-up network. This principle is called conduction complements and has already been used in the design of the NAND and NOR gates. In the pull-up network, the parallel combination of A and B are placed in series with the parallel combination of C and D.

2.3 PRE-LAYOUT SIMULATION

Pre-layout simulations are done to get desired characteristic graphs like rise time, fall time, and delay by changing some of the states of inputs and also changing device parameters. Frequency of operation, VDD, input voltage, and the width of FET/ number of fins are some of the parameters that are altered. The pre-layout simulation excludes the parasitic components which will be obtained after implementing the layout.

Simulation and analysis experts tend to agree that most simulation work should be of the pre-layout variety. This is good advice because design changes tend to be costlier further into a design cycle. Specifically, any changes made after completing the layout can cost several times more than if they were avoided in the first place. The cost of changes made after prototyping can increase by another factor.

Even so, finding a problem early in the design cycle using post-layout simulation is still orders of magnitude less expensive than trying to fix a shipping product. Whether the preference is a pre-layout simulation, post-layout simulation, or a combination of both, it's clear that without either, the risk of design failure escalates dramatically.

2.4 LAYOUTS

Layouts are the core of making a cell as it instructs the foundry about the different positions of the layers of materials that are to be used. It works as a mask used in the manufacturing process.

Some basic layers in most of the Process nodes-

- SDT (Source-Drain Trench) – Connects raised SD (Source-Drain) to MOL (Metal Oxide Layer)– Self-aligned to gate spacers.
- LISD (Local Interconnect Source-Drain)– Connects SD to M1 thru V0.
- GATE CUT – used to discontinue gate fabrication for a particular area where it is used.
- LIG (Local interconnect Gate)– Connects Gate to M1 thru V0.

Process of doing Layout –

- Standard cell height selection is done which is application-specific – Related to fins/gate, i.e., drive strength. Our work is done in a 7.5-track ratio where there are 10 fins.
- Gear ratio: Fin-to metal pitch ratio – Cell height needs to be an integer number of fins and mostly an integer number of metals accessing the cell pins.
- Boundary is made within which the detection of the device takes place.
- Half of the area is covered with P select and the other half with n select. Fins and gates are placed which are perpendicular to each other.
- Active area is specified in which the devices are formed by LISD using SDT
- Gate cut is formed where the need is to separate two devices from shorting with a single gate.
- Contacts are placed and connections are made using metal tracks.
- Pins are placed on top of metal tracks as input or output.

2.5 DESIGN RULE CHECK (DRC)

DRC checks to see whether a design fulfills the limits given by the process technology that will be utilized to make it. It's an important aspect of such a physical design process since it assures that the design fits production standards and won't fail. Process engineers and fabrication facilities offer the process technology rules. There will be restrictions specific to each process technology. As manufacturing

technology reduces at advanced nodes, the number of DRC rules and their complexity grows. Minimum area, minimum width, minimum spacing, broad metal jog, misaligned through the wire, specific notch spacing, End of line spacing, and other design constraints may apply. DRC is a crucial stage in the design's physical verification process, which also includes LVS (layout versus schematic) checks, XOR checks, ERC (electrical rule check), and antenna checks. The relevance of design rules and DRC is highest for integrated circuits (ICs) with micro- or nano-scale geometries; for advanced processes, some fabs additionally insist on the usage of more restrictive rules to boost yield.

2.5.1 Layout Design Rules

The physical mask layout of any circuit to be manufactured using a particular process must conform to a set of geometric constraints or rules, which are generally called layout design rules. These rules usually specify the minimum allowable line widths for physical objects on-chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features. If a metal line width is made too small, for example, the line can break during the fabrication process or afterward, resulting in an open circuit. If two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process. The main objective of design rules is to achieve a high overall yield and reliability while using the smallest possible silicon area, for any circuit to be manufactured with a particular process.

Note that there is usually a trade-off between higher yield, which is obtained through conservative geometries, and better area efficiency, which is obtained through the aggressive, high-density placement of various features on the chip. The layout design rules which are specified for a particular fabrication process normally represent a reasonable optimum point in terms of yield and density. It must be emphasized, however, that the design rules do not represent strict boundaries that separate "correct" designs from "incorrect" ones. A layout that violates some of the specified design rules may still result in an operational circuit with a reasonable yield, whereas another layout observing all specified design rules may result in a circuit that is not functional and/or has a very low yield. To summarize, we can say, in

general, that observing the layout design rules significantly increases the probability of fabricating a successful product with a high yield.

The design rules are usually described in two ways:

- Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations, are stated in terms of absolute dimensions in micrometers.
- Lambda rules, specify the layout constraints in terms of a single parameter and, thus, allow linear, proportional scaling of all geometrical constraints.

Lambda-based layout design rules were originally devised to simplify the industry-standard micron-based design rules and to allow scaling capability for various processes. It must be emphasized, however, that most of the submicron CMOS process design rules do not lend themselves to straightforward linear scaling. The use of lambda-based design rules must therefore be handled with caution in sub-micron geometries.

2.6 LAYOUT VERSUS SCHEMATIC (LVS)

To determine if the design is functionally equivalent to the schematic, the LVS compares the layout of the design to the netlist/schematic. A collection of criteria that transforms the layout into connections is used to extract the connections from the design's layout. These connections are then compared to the netlist connections to see if they match. The LVS is deemed to be clean if the connections match. Unlike planar CMOS devices, the parasitic capacitance that exists between the wall surface of the gate, drain, and source connections is a significant contributor to the parasitic components of the FinFET-based gate hence increasing the rise time and fall time, on the other hand, also increases the stability of the device to some extent.

In ASIC physical implementation, once the layout is generated, it must follow all the design rules for successful manufacturing and must match the schematic of the required design. To ensure this in physical verification, a Design Rule Check (DRC) is carried out to check whether the layout follows the rules for fault-less manufacturing or not. These DRC checks provide good manufacturing yield and prevent faults during manufacturing; However, it does not ensure the correctness of

the layout. It needs to be ensured that the physical implementation of the design is the same as the schematics of the design. For this, the electrical circuit of the layout netlist is compared against the schematic netlist, which is known as Layout versus Schematic (LVS).

Common LVS issues-

- Open
- Shorts
- Missing components
- Missing global net connect

2.6.1 Open type LVS error

Shapes of the nets having the same layout text on them are not intersecting or touching, causing openings in design. Opens in the design are responsible for floating connections in the design. This floating connection will cause major defects in chips. So, it is very important to find openings in the design. Running open finding utility of the PnR tool before running LVS, is helpful in the early design phase.

This type of issue can be solved by connecting the layout shapes of a single net that is left open.

2.6.2 Short type LVS error

If layers in the layout having different layout text on them are overlapping or intersecting, it will result in a short in the design. The presence of the short in design will cause chip failure. It is important to find shorts present in design by running PnR shorts finding utility or by running LVS.

Shorts can be resolved by properly rerouting the net.

2.6.3 Missing components type LVS error

If some of the spice file or GDS file is missing while merging the database, it shows missing components error. For example: if you have cell ABC used in the design, but not defined in the GDS list or spice list to be used for LVS flow, it can

cause missing components error. Either the list needs to be modified or the ABC cell needs to be excluded from the LVS comparison (this depends on the functionality of the cell; only physical cells may be excluded in the comparison).

2.6.4 Missing global net connect type LVS error

If the Power/Ground pins of the cells are not connected to any power/ground net using `connect_pg_net` commands, it causes device mismatches and LVS errors for most of the design. For example, even if the standard cell PG pin name is VDD, the tool does not connect it to the VDD net of design.

CHAPTER 3

PROPOSED LIBRARY AND ITS CONSTRUCTION PROCESS

First of all, a circuit diagram is formulated that should work as per our desired scope, in our case basic gates like NOT, AND, OR, XOR, etc. As the circuit should work for both digital and analog signals, we have used a static CMOS logic with a pull-up and a pull-down network that complement each other. In Complementary logic, the pull-up network is formed by PMOS and the pull-down network by NMOS. Bodies of the FET device are shorted to VDD and VSS to remove any static voltage deposition on the device.

Schematics of all the devices proposed in the library are given in CMOS static logic-

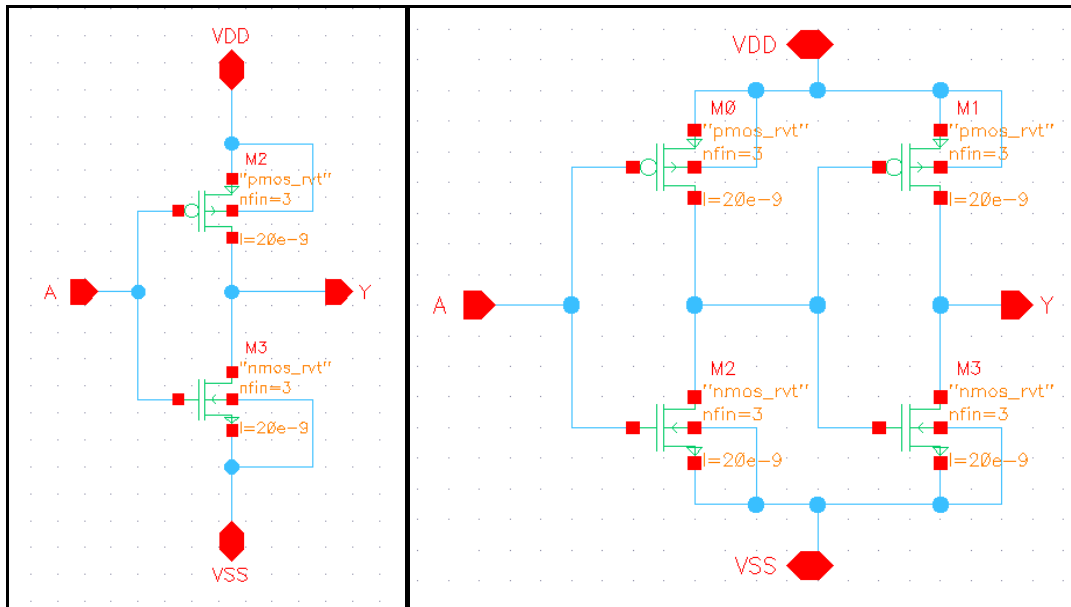


Figure 3.1 Schematic of Inverter and Buffer Gate

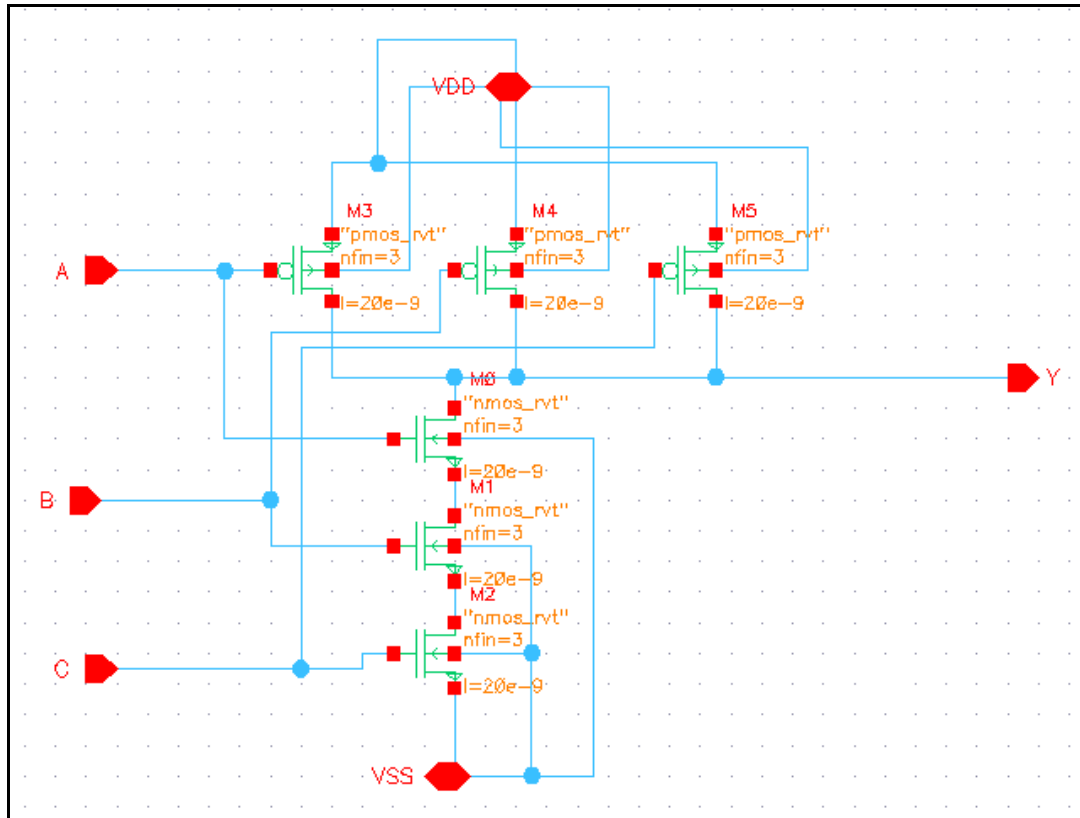


Figure 3.2 Schematic of 3 input NAND Gate

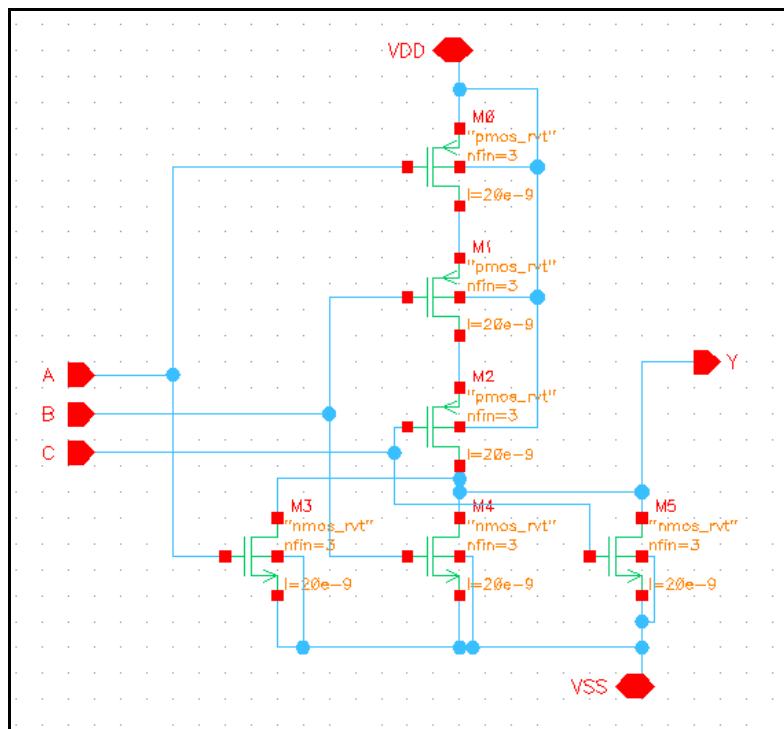


Figure 3.3 Schematic of 3 input NOR Gate

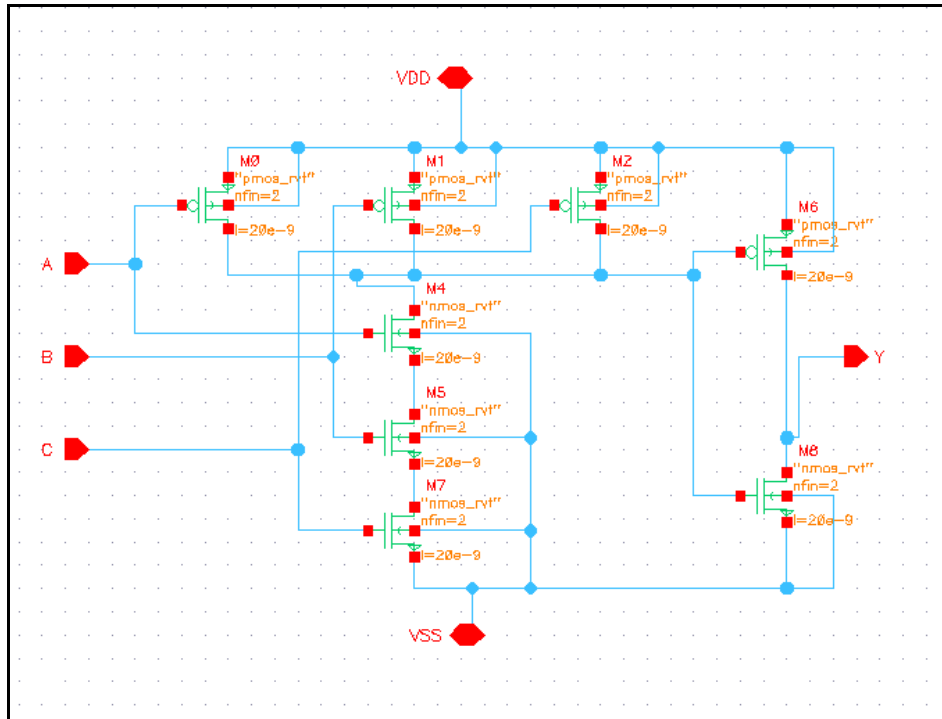


Figure 3.4 Schematic of 3 input AND Gate

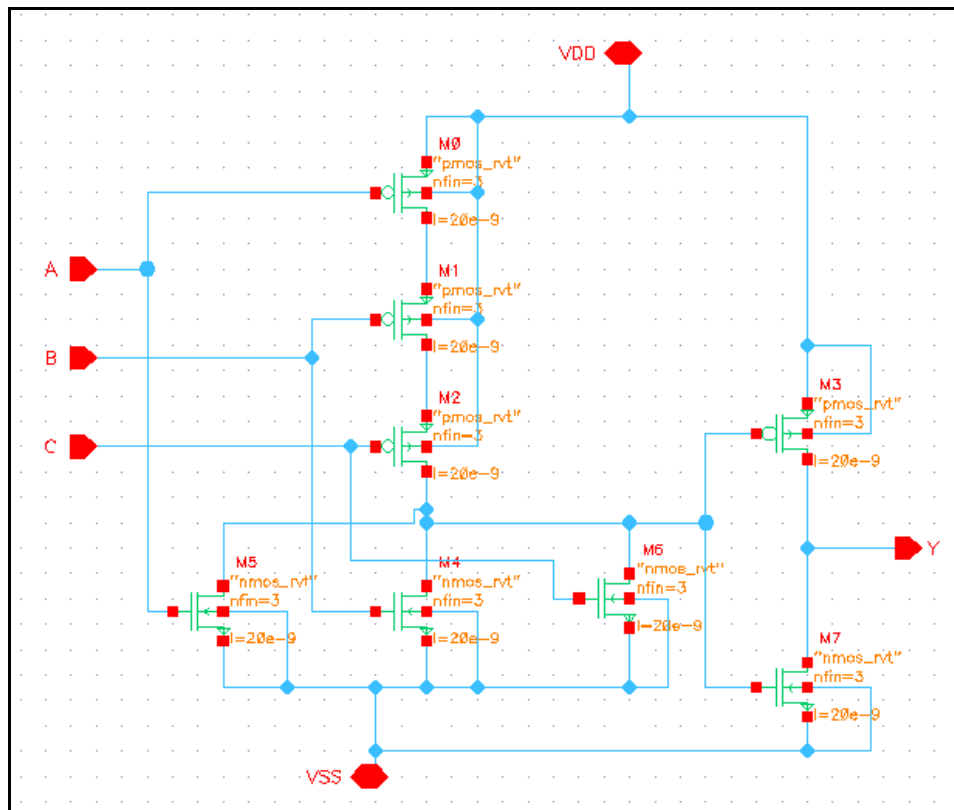


Figure 3.5 Schematic of 3 input OR

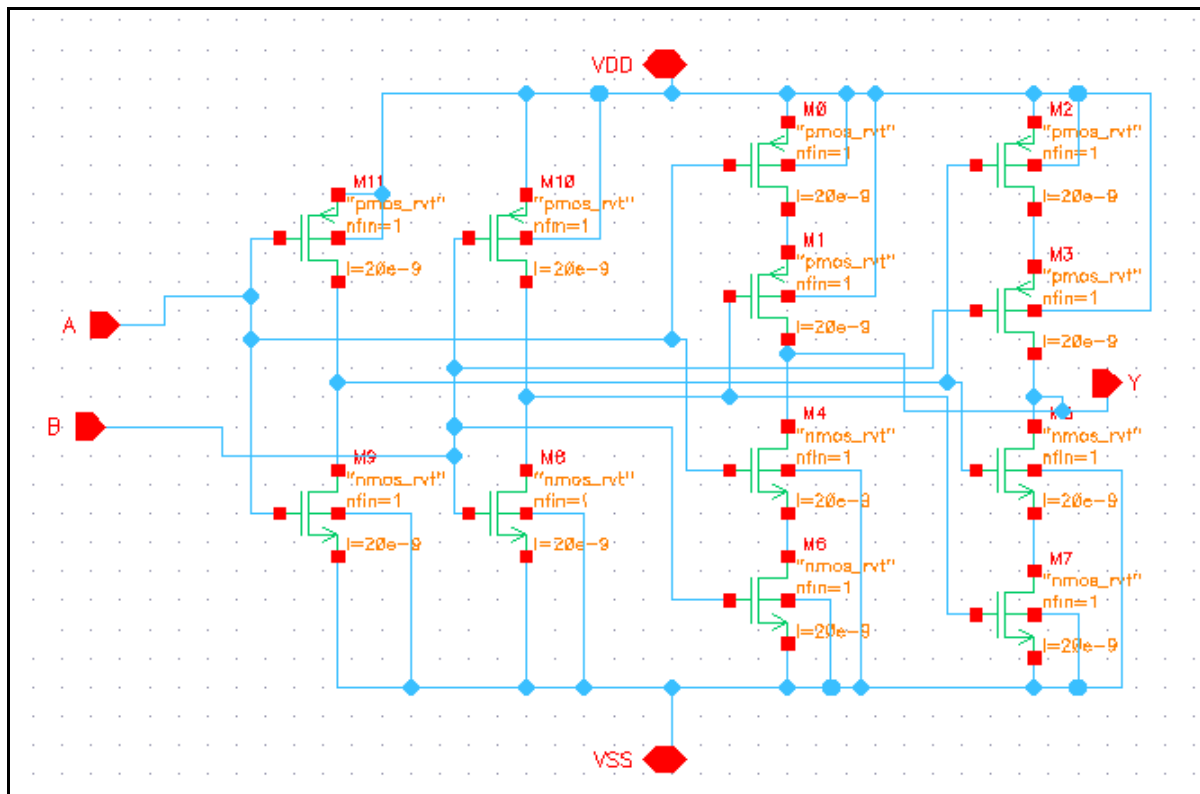


Figure 3.6 Schematic of 2 input XOR

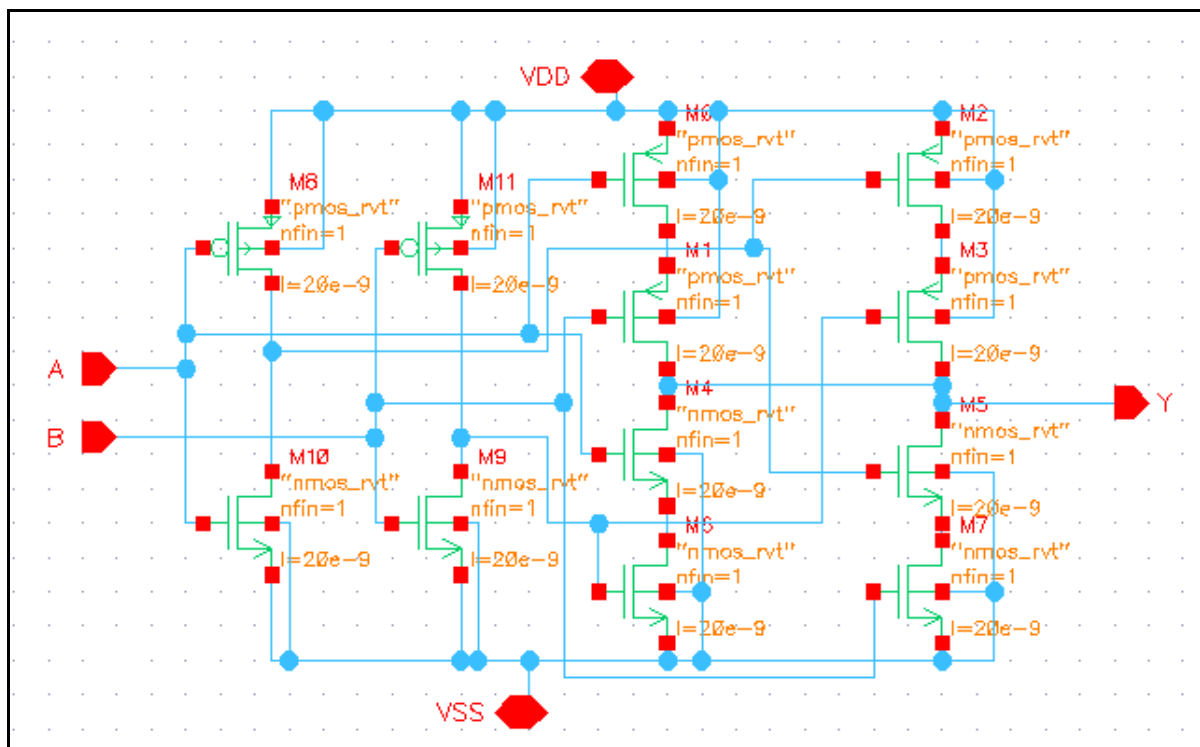


Figure 3.7 Schematic of 2 input XNOR

After schematics, the gates were simulated in a tool where the width of the FinFET device is determined as 1:1 for PMOS and NMOS respectively.

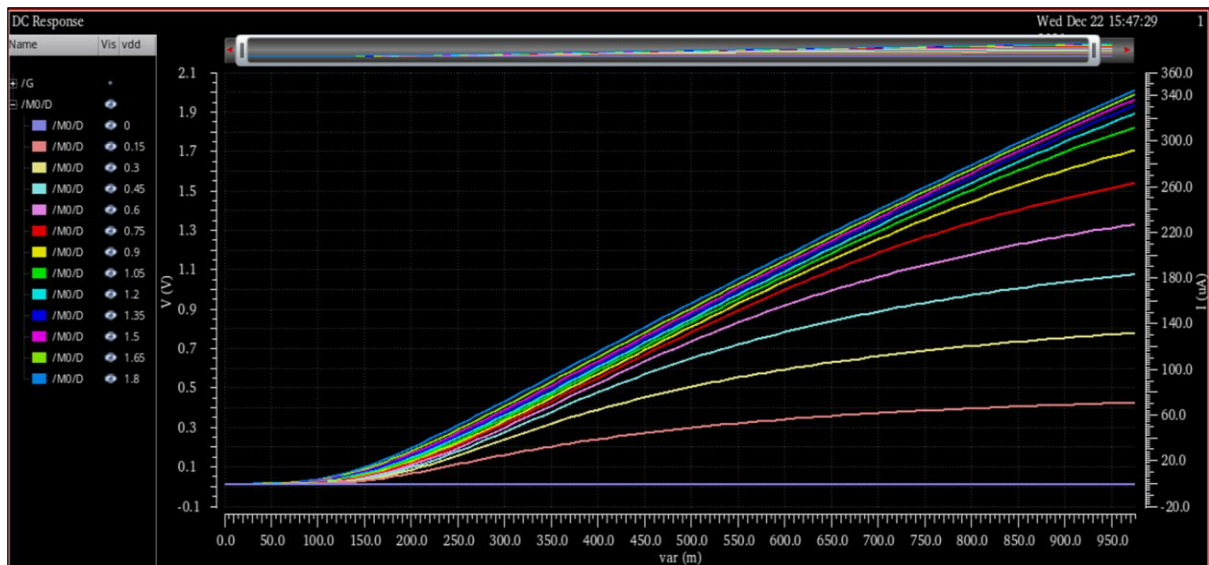


Figure 3.8 Output voltage variation for various widths of devices

This implies that as the width of PMOS and NMOS increases the output voltage increases.

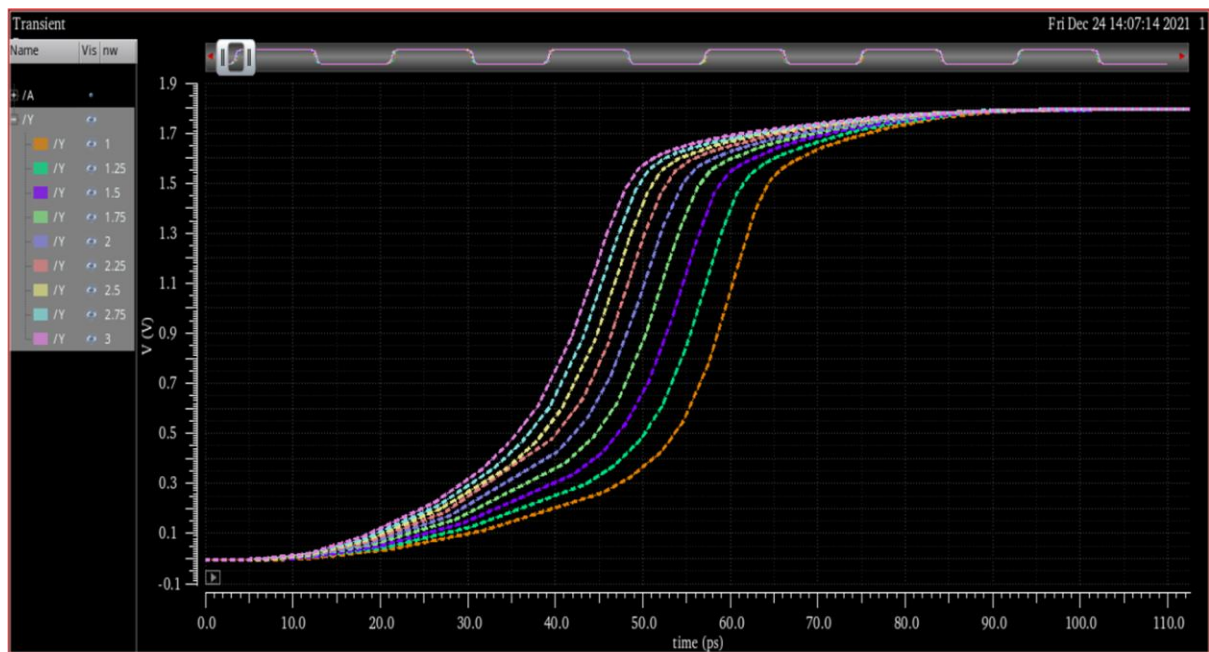


Figure 3.9 Effect of various widths of FinFET devices on the delay time of propagation

It is seen in the figure that as the ratio of NMOS: PMOS width increases the delay decreases exponentially, but contrary to that the rise time and fall time also increases with the decrease in delay. So, an intelligent tradeoff between these two factors is to be made.

We went with the ratio of 1:1 for the sake of simplicity, but this can be changed in the design to meet the desired value of delay and rise/fall time.

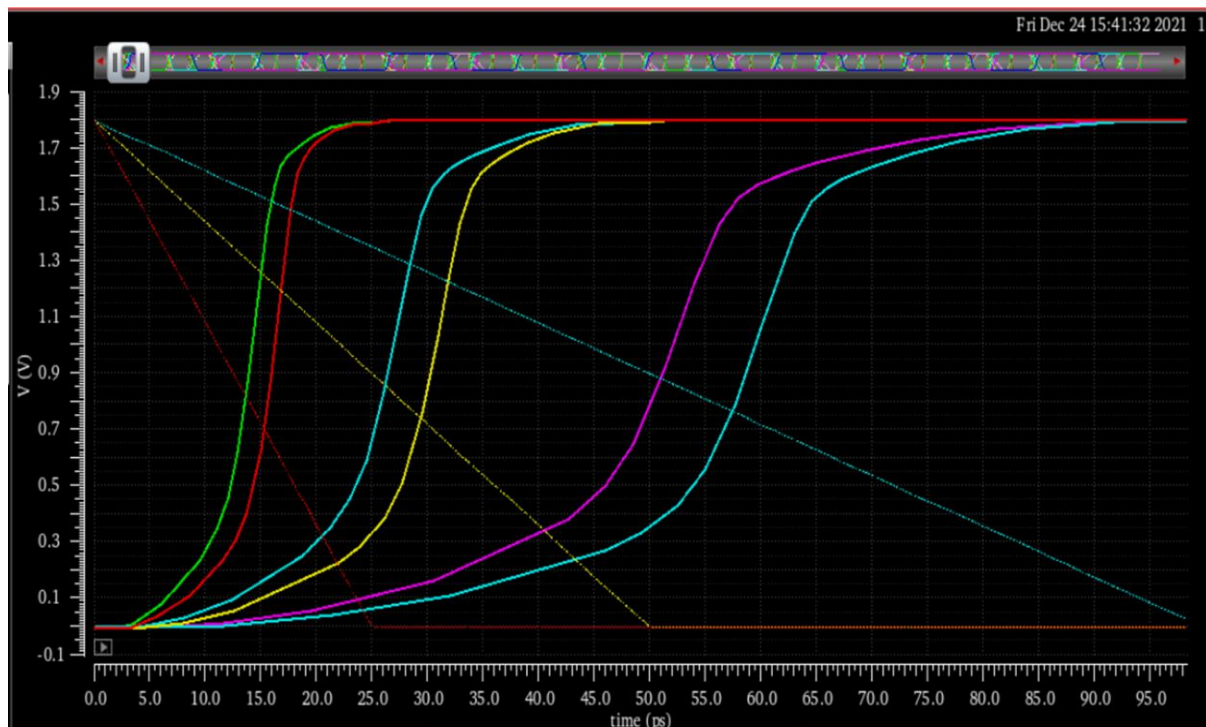


Figure 3.10 Effect of frequency on the output (from left to right is decreasing frequency)

As the input frequency decreases the delay and rise/fall time increases, which is why it is advised to operate any device at its frequency of operation, in the diagram the green line shows the 1GHz frequency response, which we have used in all our designs as a common input frequency.

The next set of figures shows the rise time and fall time variation depending on the width of NMOS and PMOS.

- If PMOS width increases the rise time decreases.
- If NMOS width increases the fall time decreases.

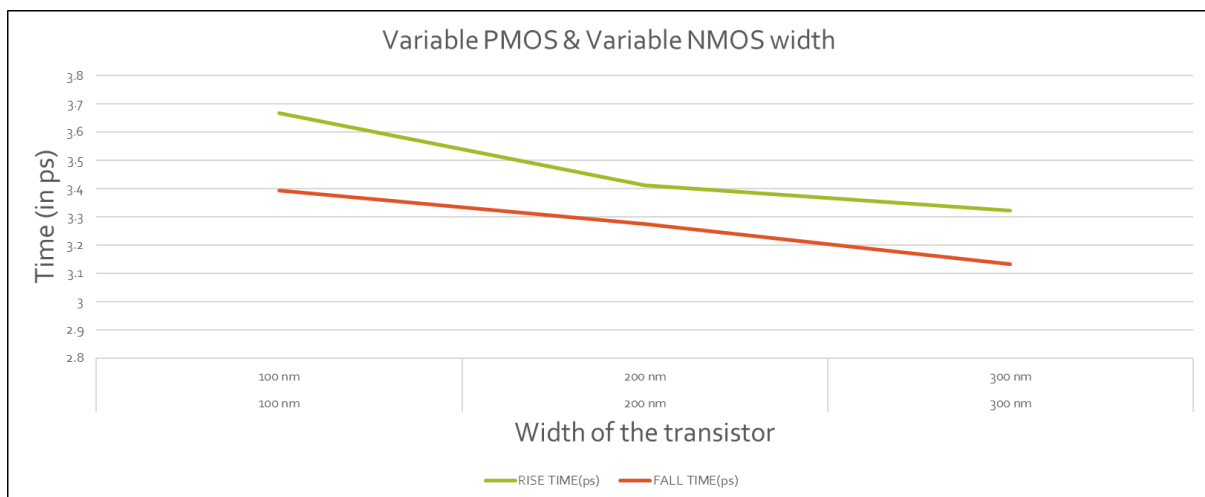
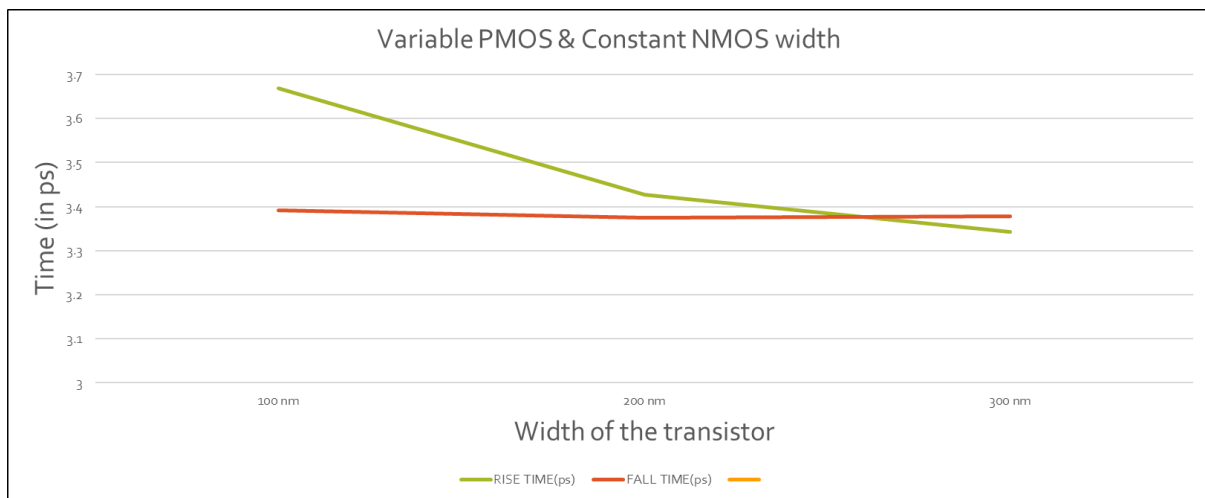
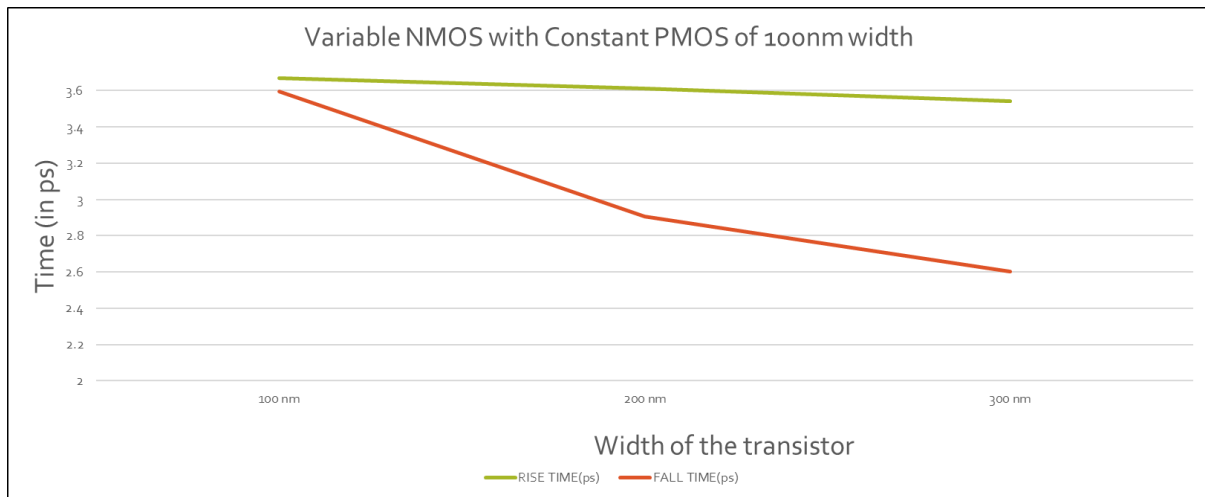


Figure 3.11 Effect of widths of PMOS and NMOS on rise/fall time (A) when nmos is varied (B) when pmos is varied (C) when both nmos and pmos are varied at the same time

The layout of the library is attached hereafter in this chapter, the nomenclature of the devices is like this-

DEVICE_NAME (Number of fins per device) X (Number of PMOS/NMOS devices)

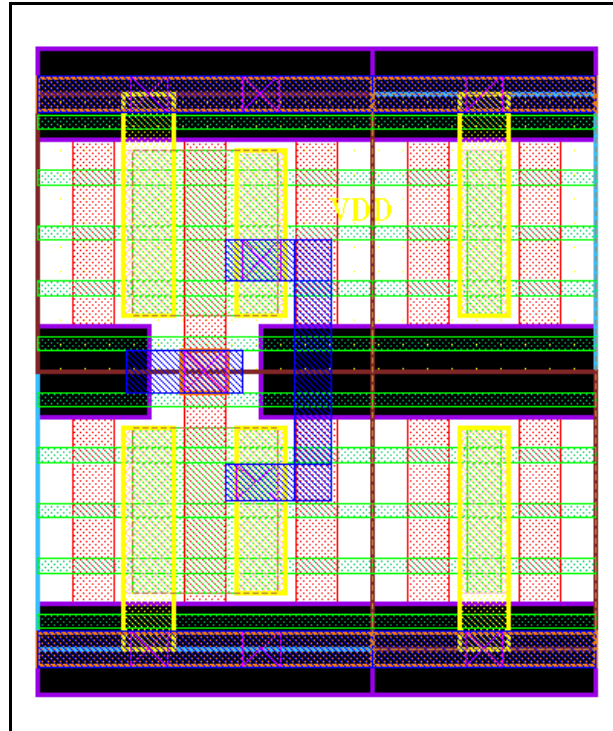


Figure 3.12 Inverter 3X1

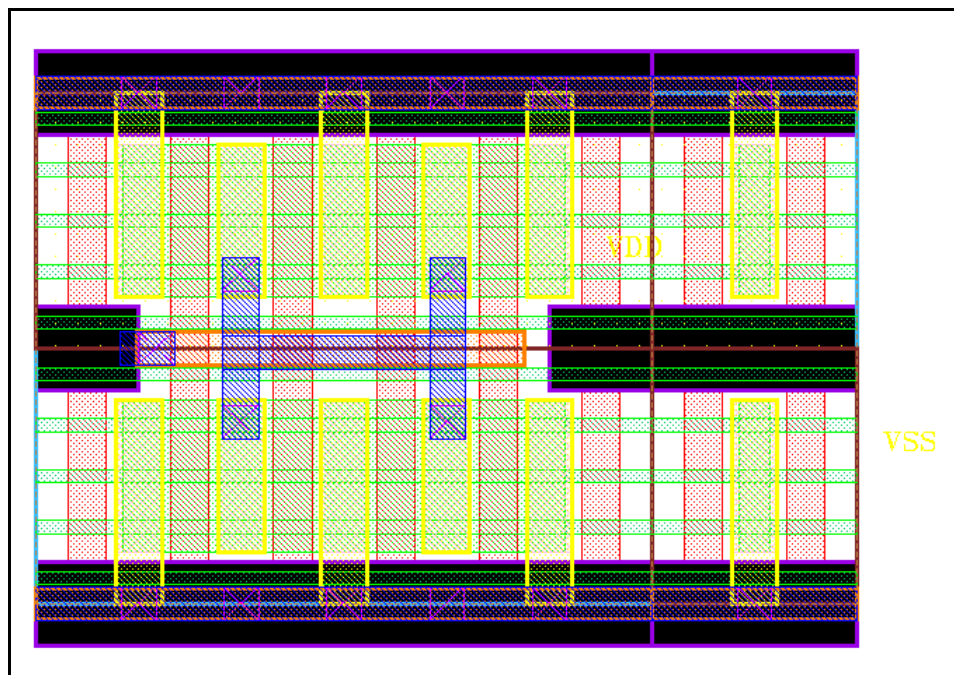


Figure 3.13 Inverter 3X4

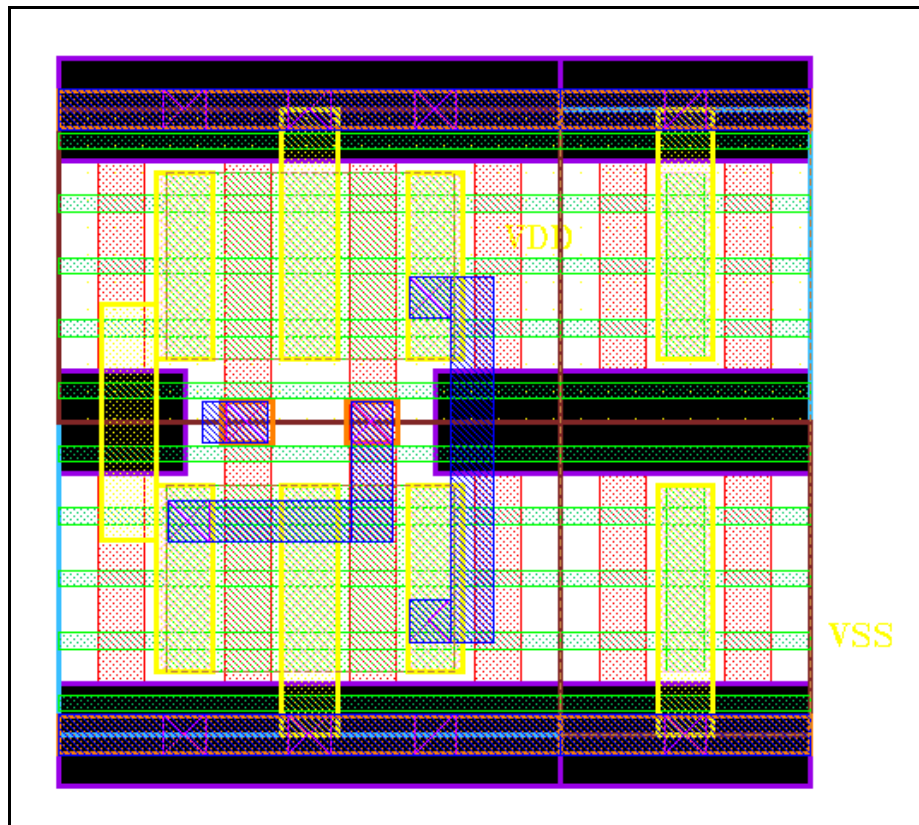


Figure 3.14 Buffer 3X1

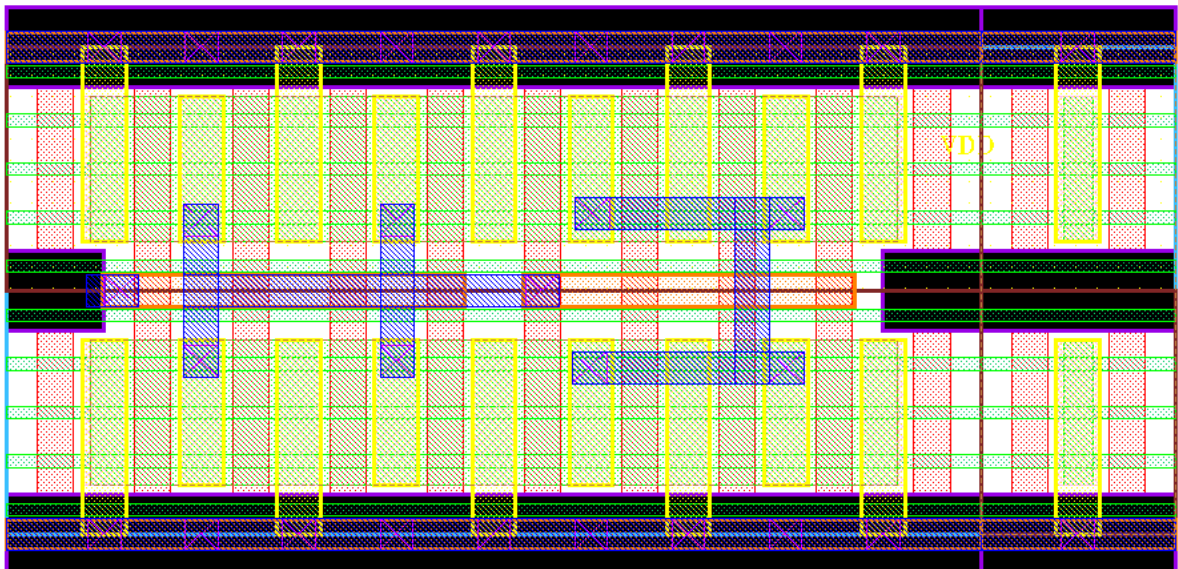


Figure 3.15 Buffer 3X4

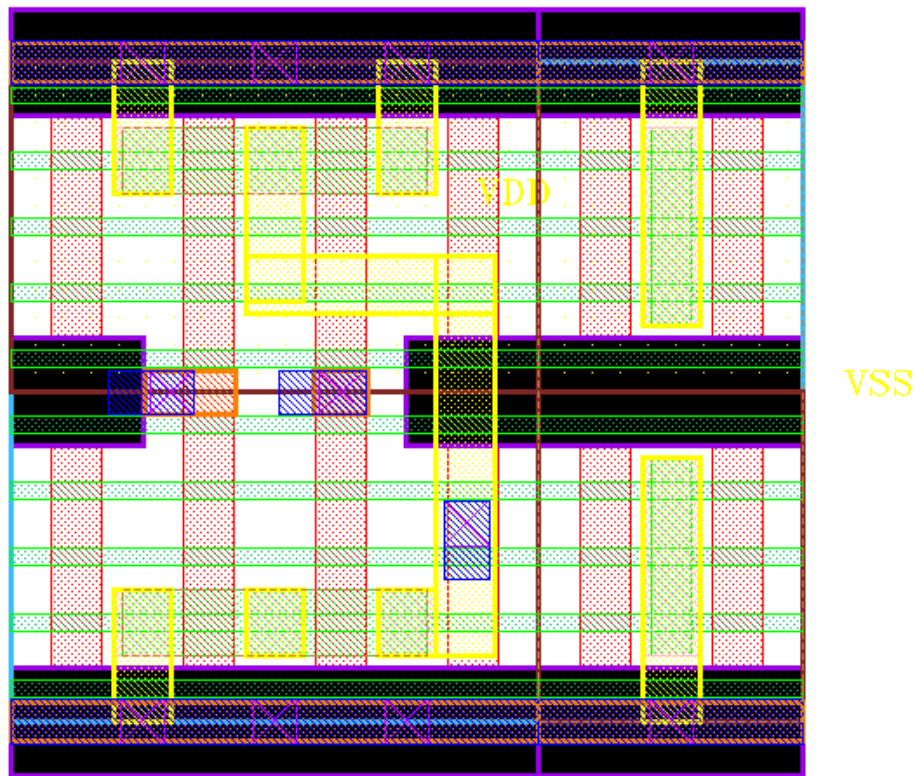


Figure 3.16 2 input NAND 1X1

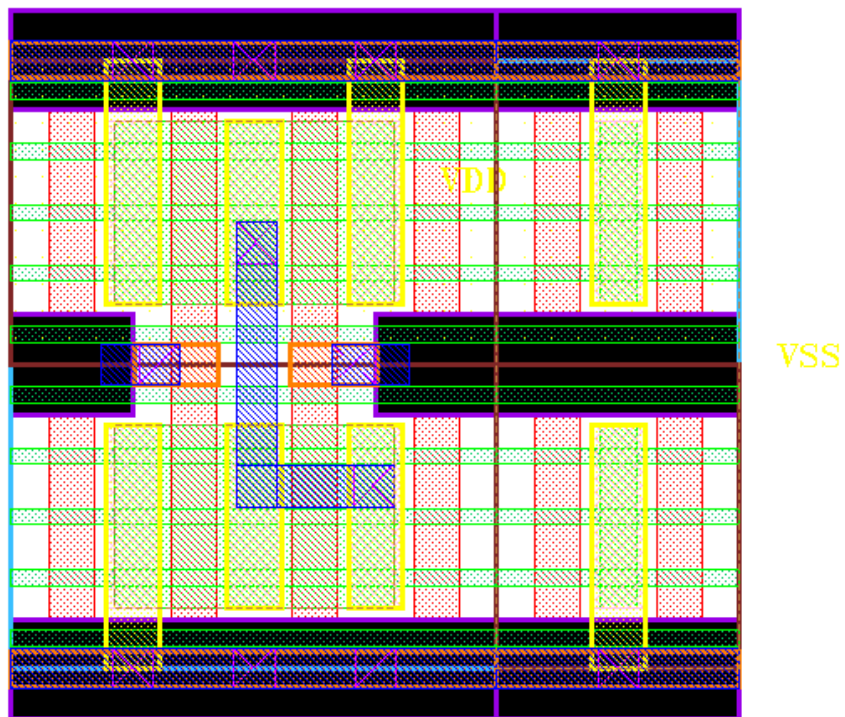


Figure 3.17 2 input NAND 3X1

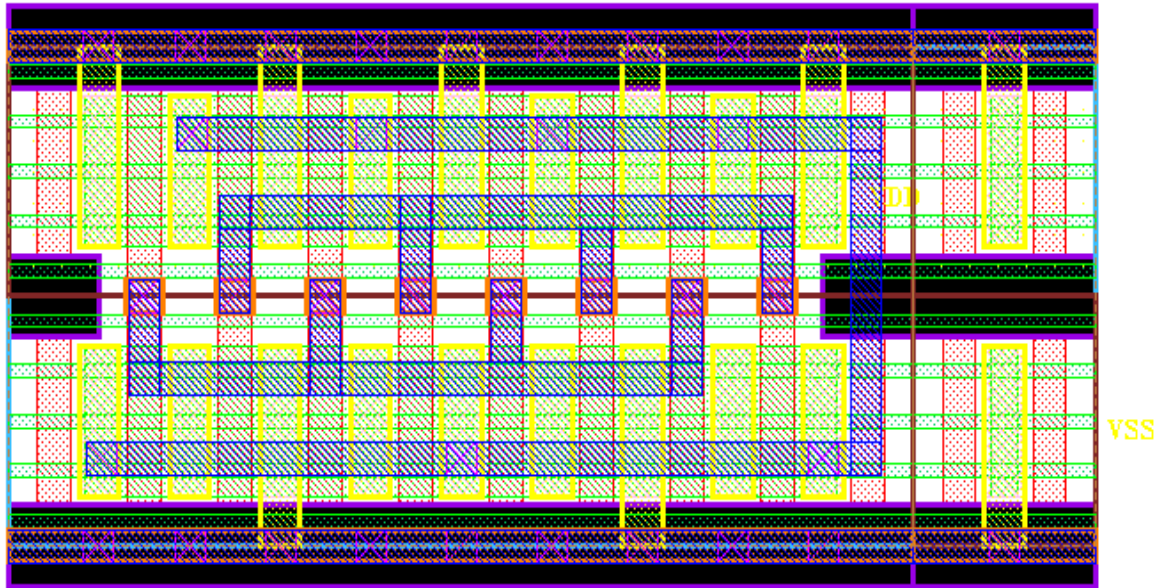


Figure 3.18 2 input NAND 3X4

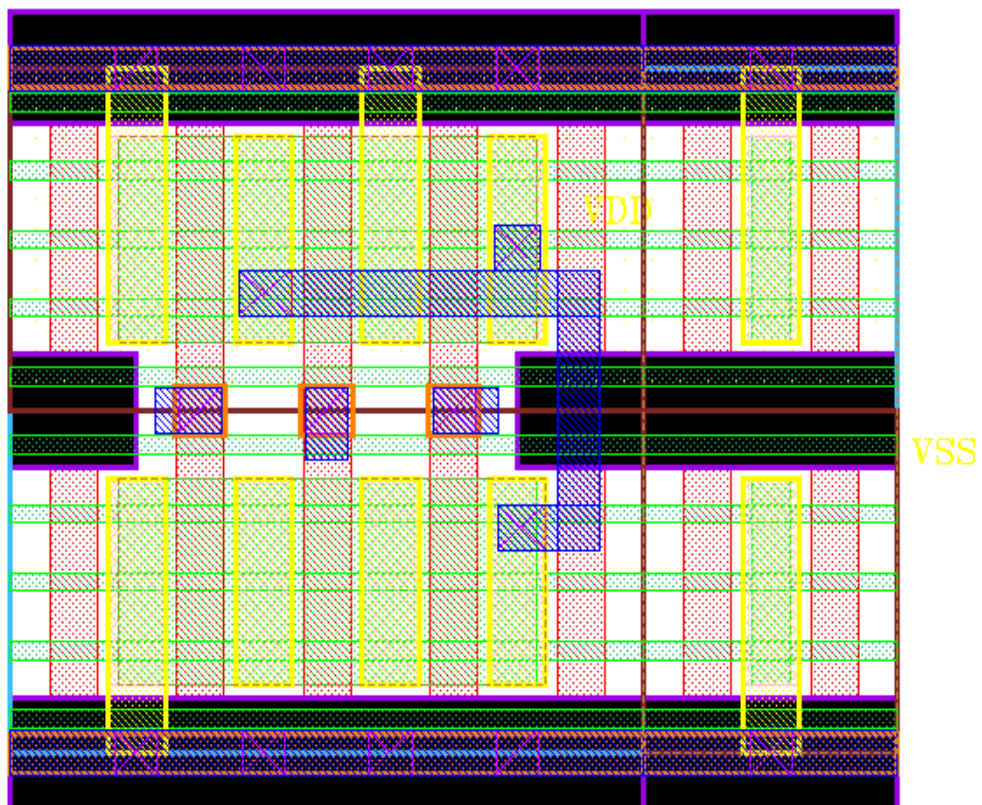


Figure 3.19 3 input NAND 3X1

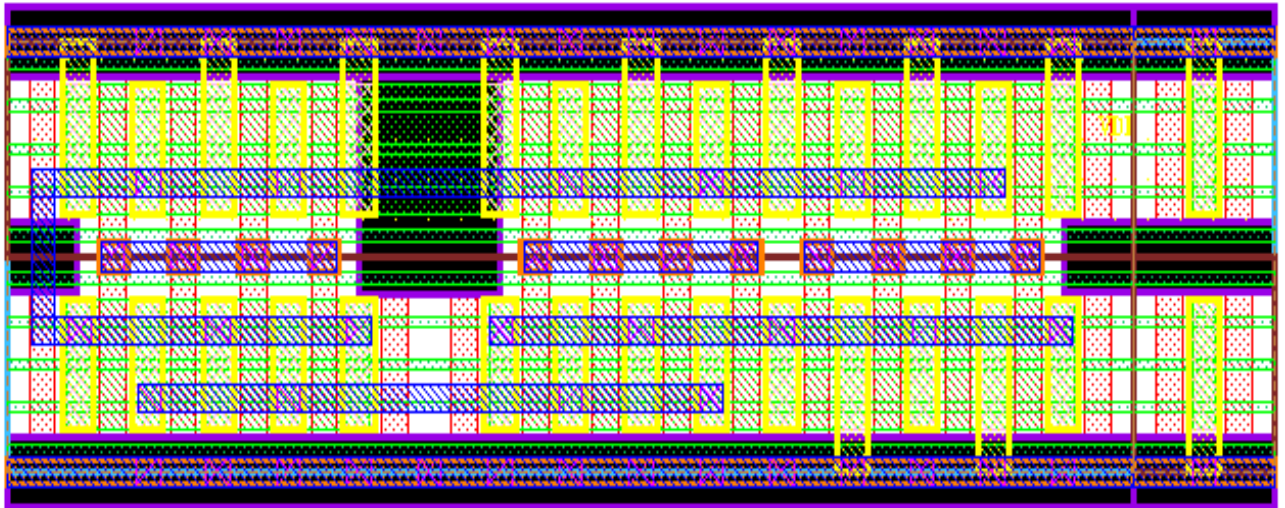


Figure 3.20 3 input NAND 3X4

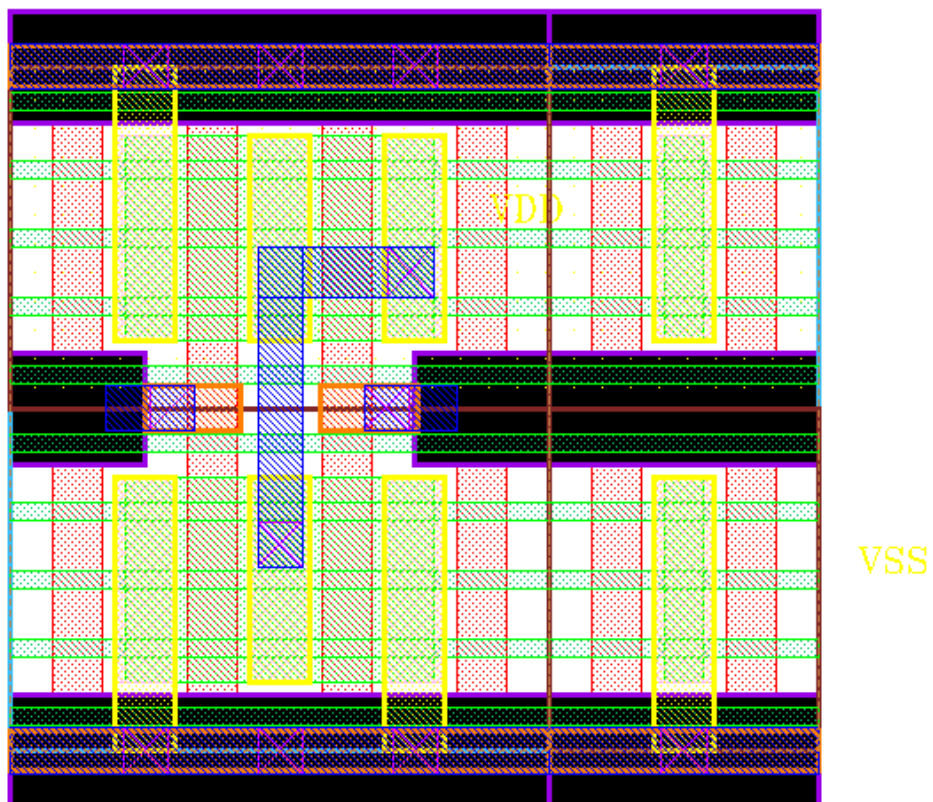


Figure 3.21 2 input NOR 3X1

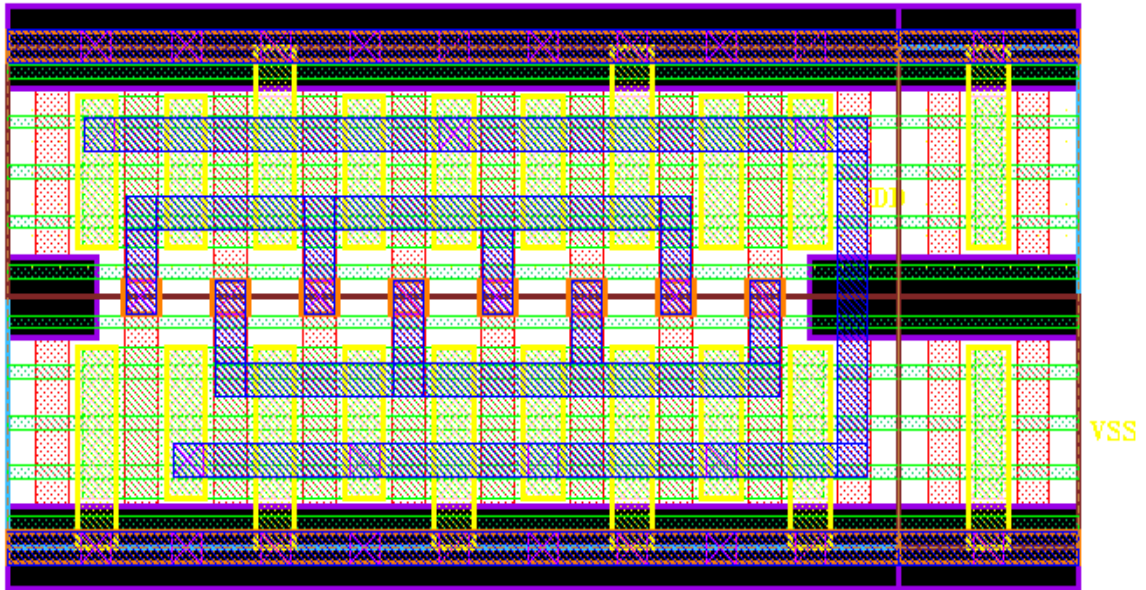


Figure 3.22 2 input NOR 3X4

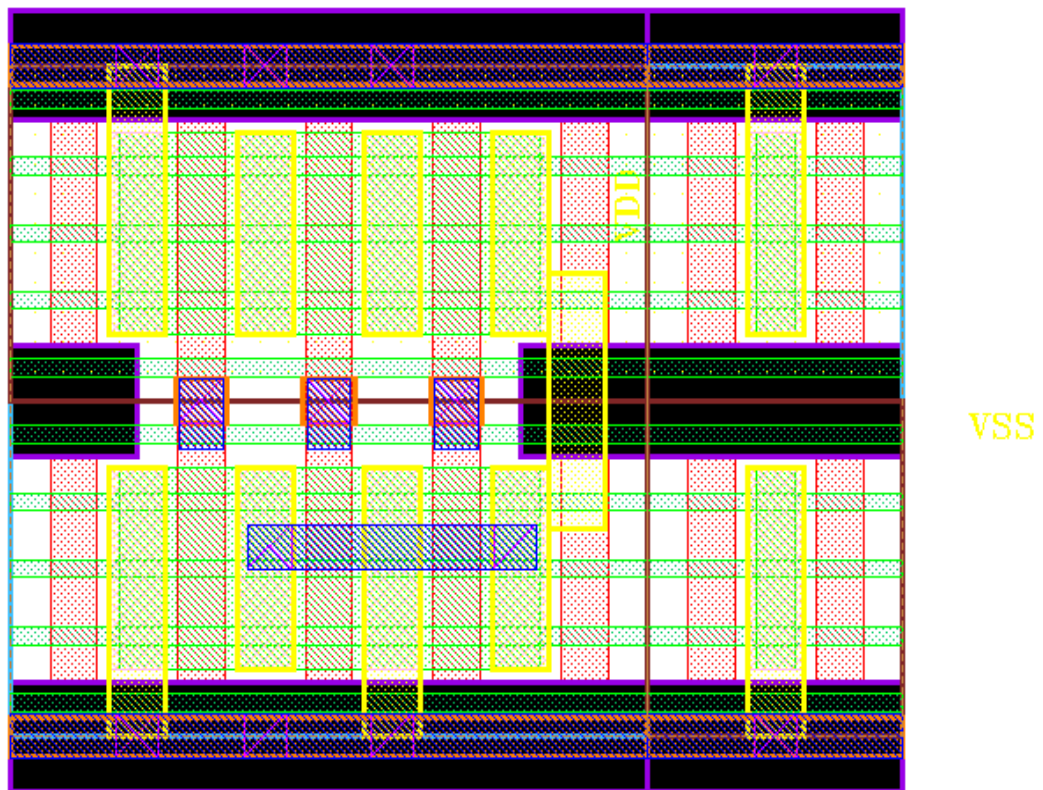


Figure 3.23 3 input NOR 3X1

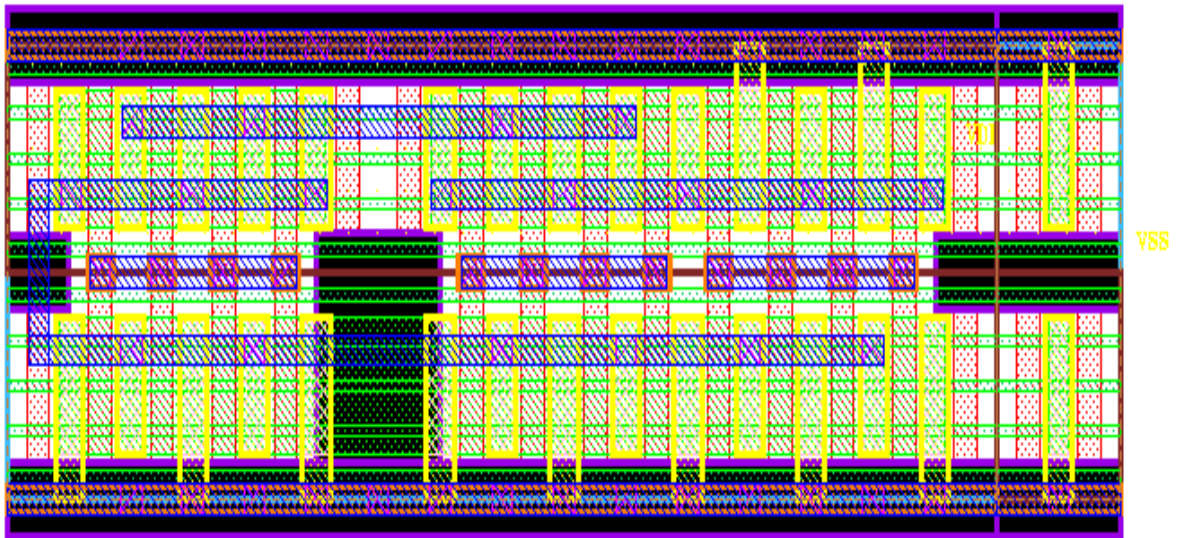


Figure 3.24 3 input NOR 3X4

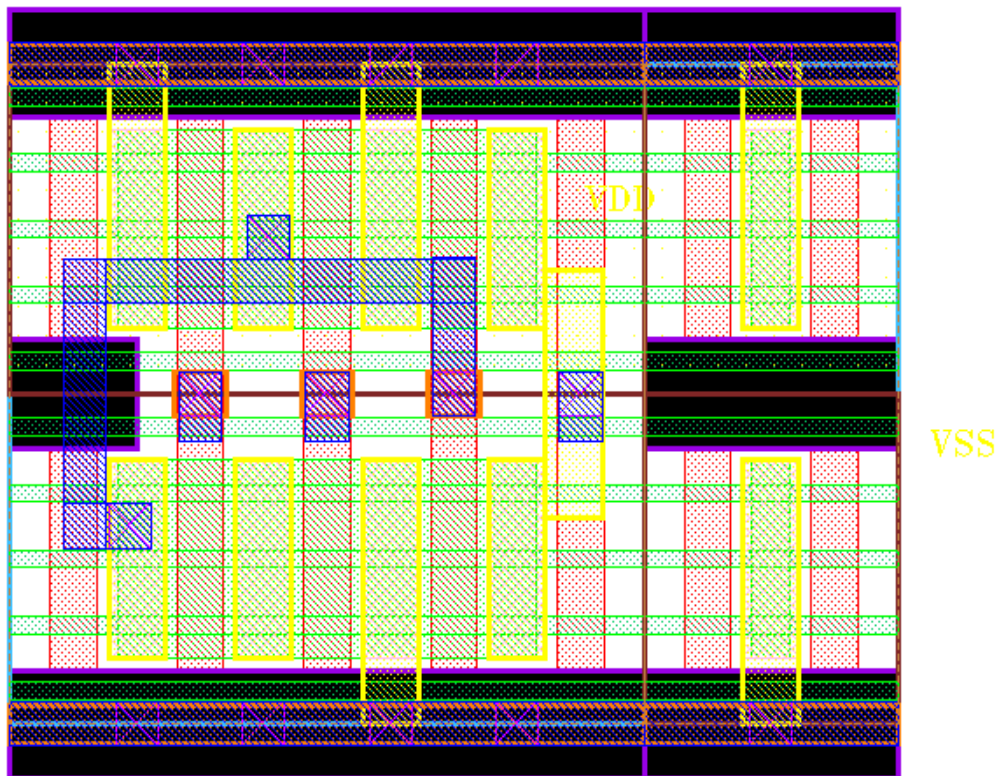


Figure 3.25 2 input AND 3X1

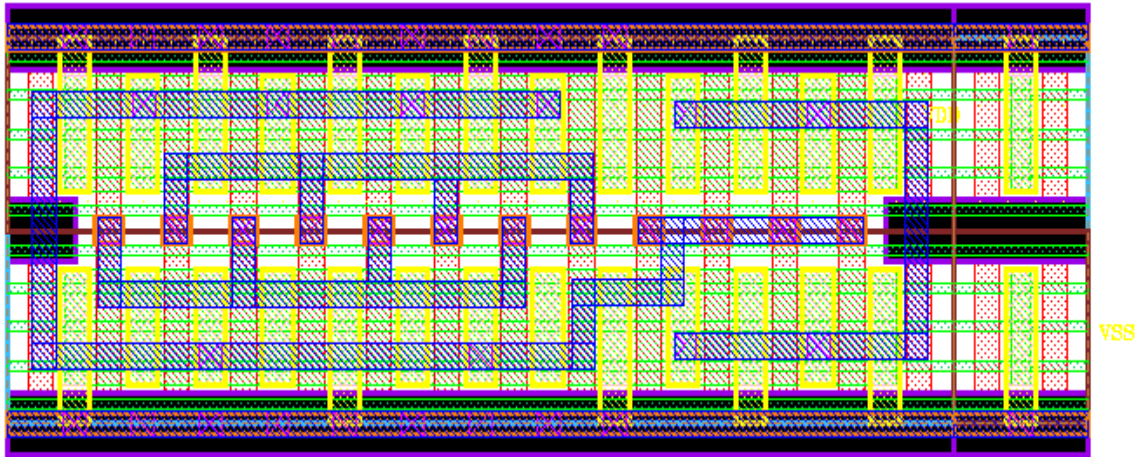


Figure 3.26 2 input AND 3X4

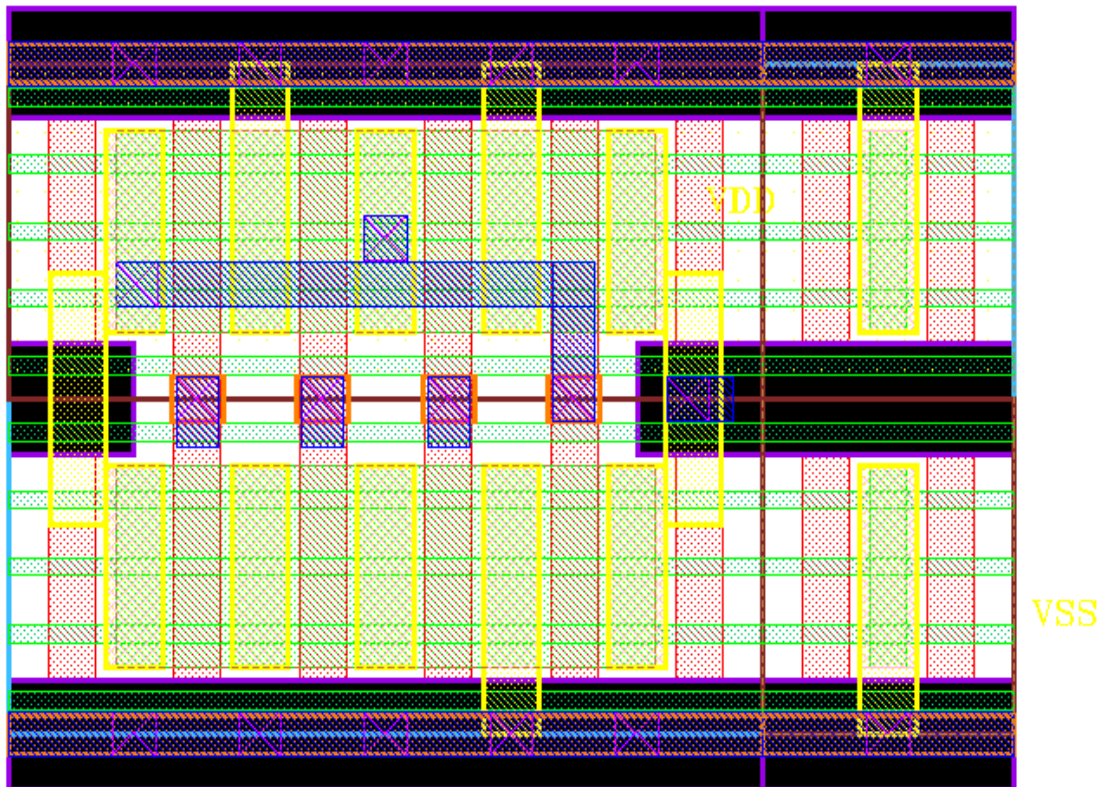


Figure 3.27 3 input AND 3X1

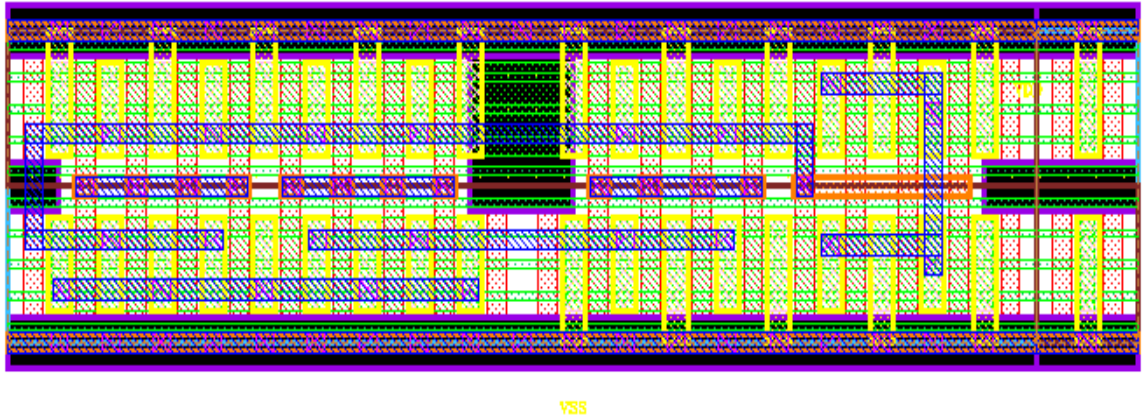


Figure 3.28 3 input AND 3X4

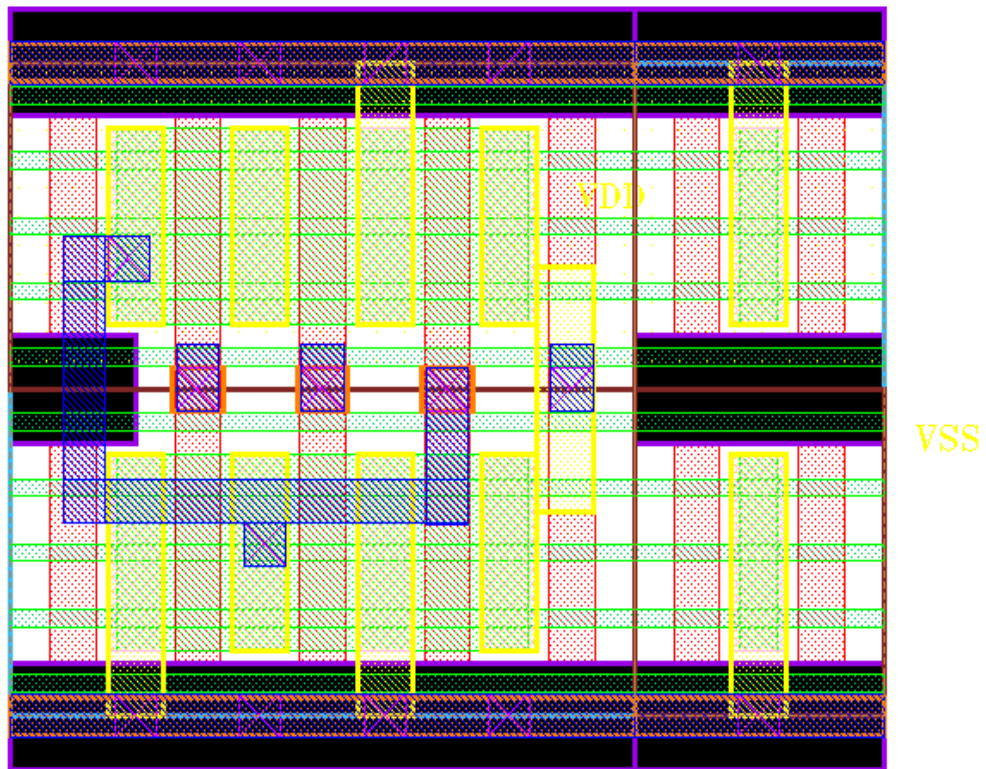


Figure 3.29 2 input OR 3X1

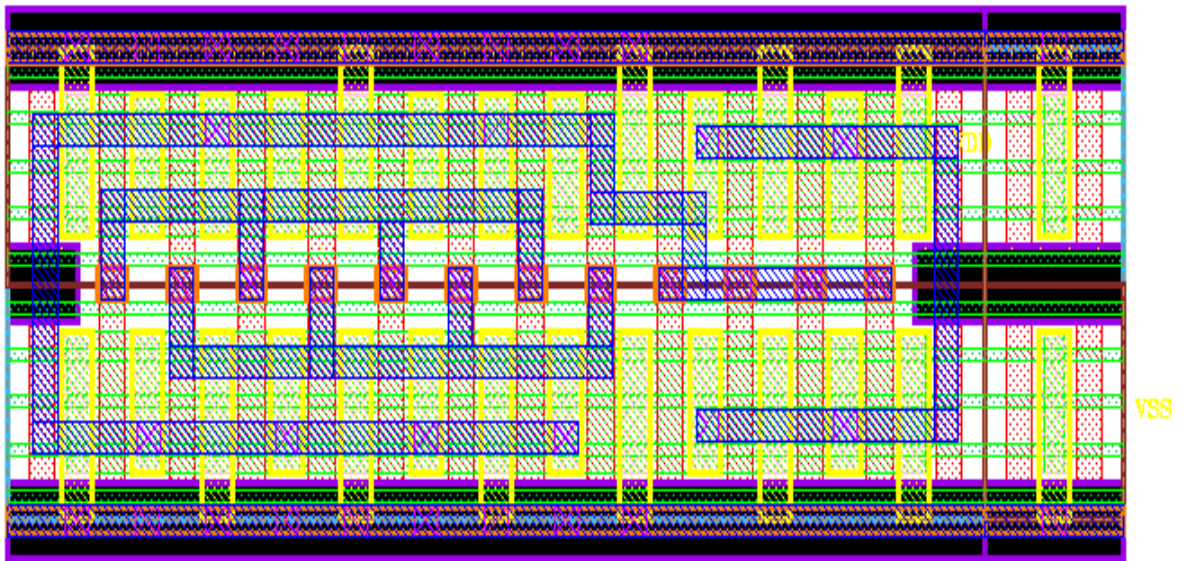


Figure 3.30 2 input OR 3X4

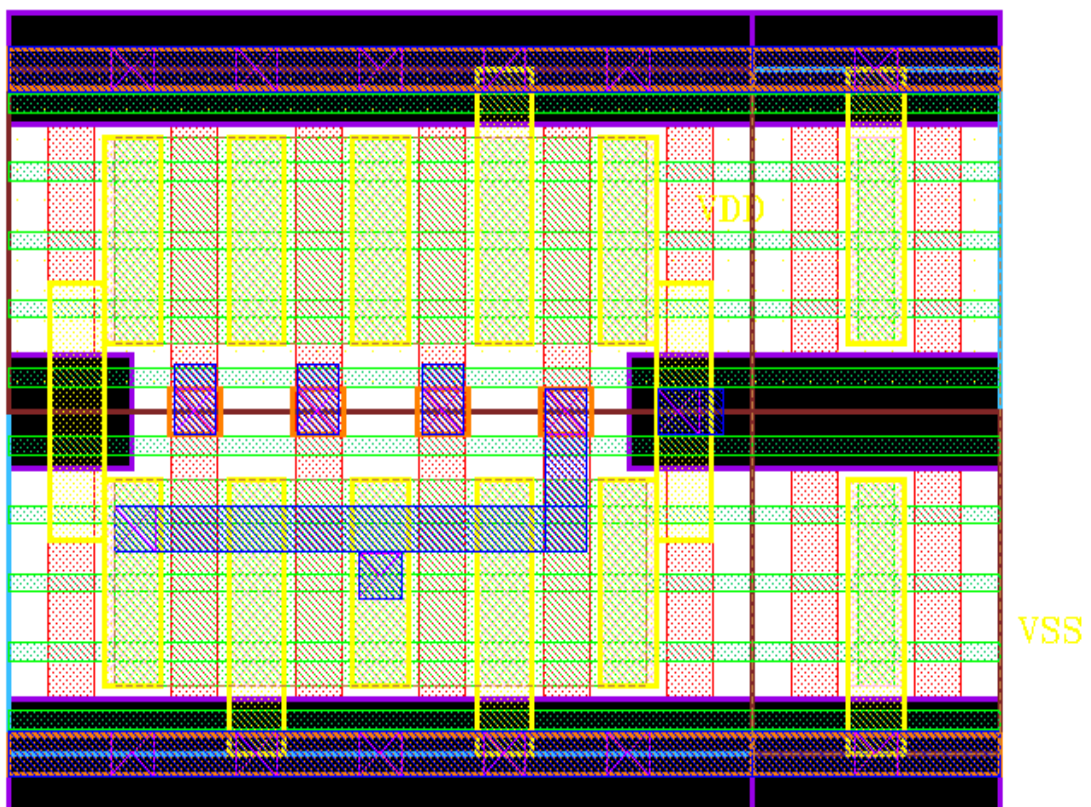


Figure 3.31 3 input OR 3X1

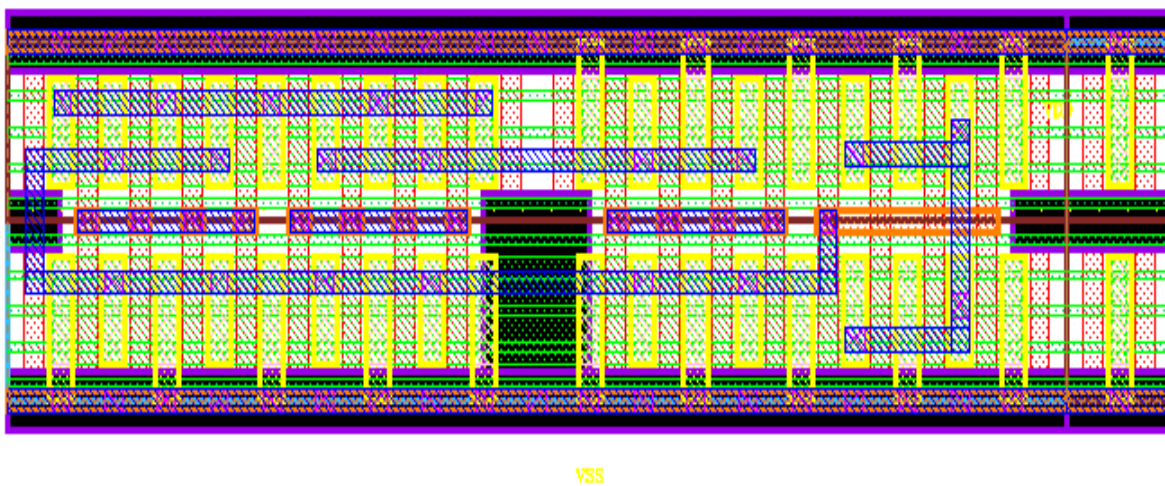


Figure 3.32 3 input OR 3X4

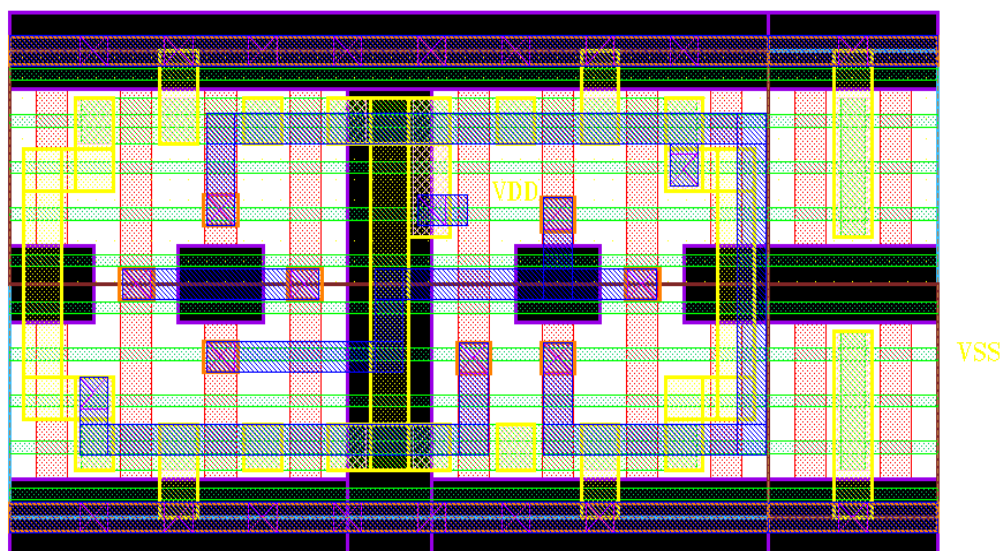


Figure 3.33 2 input XOR 1X1

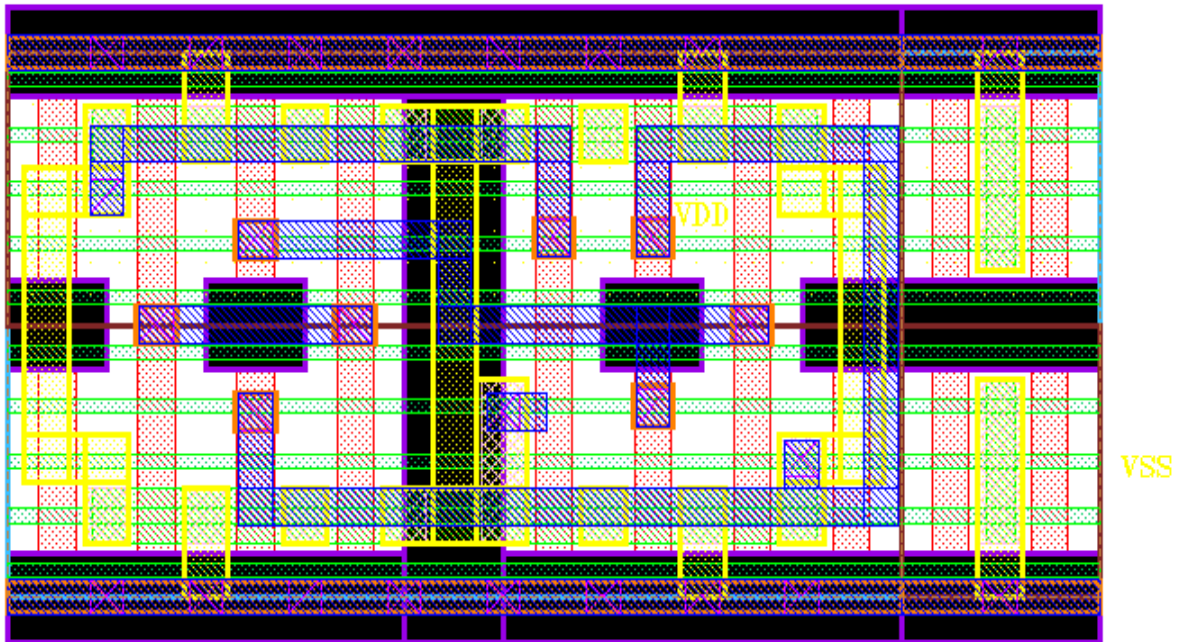


Figure 3.34 2 input XNOR 1X1

CHAPTER 4

RESULTS AND DISCUSSION

After completing the layout using minimum metal and optimizing the whole layout by placing routes and devices in compliance with the DRC we came to the following results-

- Metal tracks are the significant contributor of parasitic capacitance hence reducing the speed of operation of a particular device under test.
- LISD layer can also be used in complex designs instead of metal layers, where it is not possible to just use a metal track. But a tradeoff for higher resistance is seen in LISD as compared to metal.
- Increasing the number of fins or width increases the power of the device which could be used to operate on high loads and high currents.
- Designing a layout on lower fin pitches (8 fins) makes the design difficult for intra-cell routing and there is diminished library richness, Limited pin access. Whereas a higher pitch (12 fins) means that there is easy intra-cell routing, and a rich library but on the contrary wasteful for density. So, to make it even we have used an average of 10 fins pitches.
- Gate cut should be used in the gate which is not used in the design as a floating gate contributes as a virtual device, thereby deteriorating the performance of the device.

All the numbers tabulated here are for minimum strength	NOT GATE	3 input NAND GATE	2 input NOR GATE	Units
Capacitance load	10	10	10	aF
Max speed	2	1	1	GHz
Max power	142	124	80.5	pW
Area consumption	0.046494	0.07749	0.061992	μm^2
Supply Voltage	0.7	0.7	0.7	V

Table 4.1 Performance parameters

4.1 SCOPES AND LIMITATIONS

Complex architectures and designs can be constructed for any desired IC/ASICs using our standard cell library. The basic purpose of designing a standard cell library is to save the time of any designer, who can place and route the standard cells. The critical feature of these libraries is that they have a constant height, allowing them to be stacked in rows and enabling the automated digital designing process. The cells are usually enhanced full-custom layouts that reduce delays and maximize space. The time or price of designing or purchasing a standard-cell library, as well as the time required to construct all layers of the ASIC for each new design, is a significant limitation of designing a standard-cell library.

CHAPTER 5

CONCLUSION

Even though planar technology was substantially used for higher technological nodes, due to continuous downscaling of nodes, we are pushed to use some better technology like FinFET because of its own advantages when compared to planar technology. FinFET devices outperform traditional MOSFETs in terms of short-channel characteristics, switching times, and current density. FinFET, which is a low-power consuming device, can be made use of efficiently in wearable devices since they are expected to last long. Even storage devices can be made using FinFET which will drastically improve the data per area ratio. Short channel effects may be tuned using the geometry of a FinFET (e.g., triangular or curved fins). This could lead to future FinFET technology modifications in which the channel area is raised entirely off the substrate.

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