

# **A LOW POWER TECHNIQUE IN BIST TESTING SCAN CHAIN STITCHING FOR TEST-POWER REDUCTION**

Submitted in partial fulfillment of the requirements for the award of  
Bachelor of Engineering Degree in  
Electronics and Communication Engineering

by

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**DEPARTMENT OF ELECTRONICS & COMMUNICATION  
ENGINEERING**

**SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING**

**SATHYABAMA**

**INSTITUTE OF SCIENCE AND TECHNOLOGY  
(DEEMED TO BE UNIVERSITY)**

**Accredited with Grade "A" by NAAC**

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**MAY 2022**



**SATHYABAMA**

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ENGINEERING**

**BONAFIDE CERTIFICATE**

This is to certify that this Project Report is the bonafide work of **AISHWARYA.S** (Reg. No. 38130006) who carried out the project entitled "**A LOW POWER TECHNIQUE IN BIST USING SCAN CHAIN STITCHING FOR TEST POWER REDUCTION**" under our supervision from November 2021 to May 2022.

**Internal Guide**

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**Submitted for Viva voice Examination held on \_\_\_\_\_**

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Signature:

**Internal Examiner**

**External Examiner**



## DEPARTMENT OF ELECTRICAL AND COMMUNICATION ENGINEERING

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## DECLARATION

We **SHARON.G** (38130208) and **AISHWARYA.S** (38130006) hereby declare that the Project Report entitled “**A LOW POWER TECHNIQUE IN BIST USING SCAN CHAIN STITCHING FOR TEST POWER REDUCTION**” done by us under the guidance of **Dr.B.Rajasekar B.E,M.Tech,Ph.D**, at Sathyabama Institute of Science and Technology, Chennai- 600119 is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

1.

2.

**DATE:**

**PLACE:**

**SIGNATURE OF THE CANDIDATES**

## ACKNOWLEDGMENT

We are pleased to acknowledge our sincere thanks to the Board of Management of SATHYABAMA for their kind encouragement in doing this project and completing it successfully. We are grateful to them.

We convey our thanks to **Dr. N. M. NANDITHA, M.E., Ph.D., Dean, School of Electrical and Electronics Engineering**, and **Dr. T. RAVI, M.E., Ph.D., Head of the Department, Dept. of Electrical and Electronics Engineering** for providing us necessary support and details at the right time during the progressive reviews.

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We wish to express our thanks to all teaching and non-teaching staff members of the **Department of Electronics and Communication** who were helpful in many ways for the completion of the project.

## ABSTRACT

For the test of ICs, Two gold standard approaches are available for IC testing: external testing and built-in self-testing (BIST). After manufacturing an IC, it is essential to verify there are no manufacturing defects. For this purpose, the existing flipflops in the design can be made use of.

Flipflops are usually provided with two extra pins, Scan Input (SD) and Scan Enable (SE). A variety of hybrid testing strategies are achieved by resource partitioning testing (TRP). The ultimate goal is to provide a beneficial trade-off between test evaluation metrics such as test development and application cost, hardware overhead, fault coverage, etc.

However, most of these methods focus on power consumption during normal mode operation, while test mode operation was normally not a predominant concern. Indeed, most of the energy consumed comes from the switching activity in the nodes of the circuit under test (CUT), which is much higher in test mode than in normal mode operation.

The scan chain stitching is made power-aware by placing the flip-flops which have more test combination requirements at the beginning of scan chains, while flip-flops with lower test combination requirements are inserted towards the end of scan chains. This will give an output that lowers the quiescent power. Scan Input (SD) and Scan Enable (SE). We identify convenient chains of flipflops and stitch them together, and connect in the form of a shift register circuit with their SD, SE pins.

The proposed work also provides RTL schematic and Technology schematic for further implementation in FPGA for back-end development. In this proposed work hybrid model helps in further testing power reduction during the functional mode of circuit.

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## LIST OF ABBREVIATIONS

|           |   |                                    |
|-----------|---|------------------------------------|
| • DFT     | ⇒ | Design For Testability             |
| • BIST    | ⇒ | Built in Self Test                 |
| • CUT     | ⇒ | Circuit Under Test                 |
| • LFSR    | ⇒ | Linear Field Shift Register        |
| • BS-LFSR | ⇒ | Bit Swapping LFSR                  |
| • BCU     | ⇒ | BIST Control Unit                  |
| • FPGA    | ⇒ | Field Programmable Gate array      |
| • RTL     | ⇒ | Register Transistor Level          |
| • HDL     | ⇒ | Hardware Descriptive Language      |
| • VHDL    | ⇒ | Very High Speed Integrated Circuit |
| • ISE     | ⇒ | Integrated Synthesis Environment   |
| • TPG     | ⇒ | Test Pattern Generator             |
| • TRE     | ⇒ | Test Response Evaluator            |
| • FC      | ⇒ | Fault Coverage                     |
| • BIT     | ⇒ | Built In Test                      |
| • SFF     | ⇒ | Scan Flip Flops                    |

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# CHAPTER 1

## INTRODUCTION

### 1.1 SCAN CHAIN REORDERING

Although the proposed BS-LFSR can achieve good results in reducing the consumption of average power during the test and also minimizing the peak power that might result when digitizing a new test vector, it cannot reduce the overall peak power because there are some components that occur when scanning the captured response or when applying a test vector and capturing a response in the test cycle. To solve these problems, first, the proposed BS-LFSR was combined with a presented cell sorting algorithm to reduce the number of transitions in the scan chain during the BS-LFSR scan. This can be used to generate complete patterns for the tester latch. This will reduce the overall average power as well as the peak power that may occur when analyzing a captured response. The capture power problem (peak power in the test cycle) will be solved using a novel algorithm that will reorder some cells in the scan chain in such a way that minimizes the Hamming distance between them. In this scanchain ordering algorithm, some cells in the sorted scan chain that uses the algorithm will be reordered again in order to reduce the peak power which may result during the test cycle. This phase mainly depends on an important property of the BSLFSR. That reduces the number of transitions of an LFSR by 50%, the transition probability reduces.

The problem of the capture power (peak power in the test cycle) will be solved by using a novel algorithm that will reorder some cells in the scan chain in such a way that minimizes the Hamming distance between the applied test vector and the captured response in the test cycle, hence reducing the test cycle peak power (capture power). In this scan-chain-ordering algorithm, some cells of the ordered scan chain using the algorithm will be reordered again in order to reduce the peak power which may result during the test cycle. This phase mainly depends on an important property of the BS-LFSR.

That reduces the number of transition of an LFSR by 50%, the transition probability reduces.

## **1.2 SCAN CHAIN**

Scan chains are the elements or products in scan-based designs that are used to shift-in and shift-out test data. A scan chain consists of a number of back-to-back linked flops in a chain with one outgoing flop linked to another. The input of the first flop is connected to the chip's input pin (called scan-in) from which the scan data is fed. The output of the last flop is connected to the chip's output pin (called scan-out) which is used to extract the shifted data.

## **1.3 PURPOSE OF SCAN CHAIN**

Scan chains are inserted into designs to shift the test data into and out of the chip. This is done to make every point in the chip controllable and observable as discussed below. The proposed method is beneficial for reduction of both computation time and test power during testing with various test patterns. The method performs two processes to consider the shift-in and shift-out powers. The first process, logic topology-based scan partitioning, forms scan chains based on scan estimation value that estimates the shift-out data occurring in flip-flops. The second process, logic topology-based scan stitching, determines the order of the flip-flops by calculating the scan influence value, using which the proposed method can reduce the shift-in power by consolidating the care bit density in the test patterns.

The traditional architecture, which uses an LFSR to feed pseudo-random patterns into the scan route, is simple to construct and has a low impact on system performance. A variety of sophisticated strategies have been developed in the literature to tackle the problem of random pattern resistant defects.

## CHAPTER 2

### LITERATURE SURVEY

**S. Pathak, et.al [2017]** ; introduced a novel approach to scan cell stitching based on logic cluster controllability (LoCCo). By identifying flip-flops which would require more test combinations to test the logic and the creator called them as flip-flops of higher controllability. Further, these Flip Flops were then placed at the beginning of scan chains while flip-flops with lower required combinations or lower controllability flip flops are placed at the end of the circuit. It is, therefore, needed to have a solution that does not increase the hardware cost and keeps the software iterations to a minimum. Therefore, the creators intention was to provide the same by their new power-aware scan stitching method.

**S. Ukey, et.al [2016]**; S. Ukey, S. Rathkanthiwar, and S.Kakde, [April 2016], This paper proposes a novel scanning cell architecture for low power scanning technique that provides combined solution to reduce total average power in both combined part and scan cell during acquisition mode and move mode. Thus the novel method instigates implemented on the different combinational Tanner circuits and the experimental results were observed. It is inferred by the creators to save total average power in shift and capture mode to about 20%.

**S.A.Pathak, et.al [2016]**; designs verifications are growing in complexity, chip design cycle is desired to be shorter. Hence, methods has been implemented by the designers The scope of the work is also extended to reduce the cycle time of a derivative product from a base design. The author describes a technique which can modify the existing spare cells in the design for logic corrections or modifications during ECO.

**Sungyoul, et.al [2015]**; There are two main problems with low power testing. These two questions must therefore be treated differently. Thus the creator aimed blocking the malfunction during at-speed testing, the capture Power must be lowered not to generate excessive IR-drop and resulting . The major point is to capture power and shift delay in a nutshell the scan chain reordering (SR)-aware X-filling and the low power scan stitching, are specifically introduced to serve this purpose.

**Satyadev Ahlawat and Jaynaryan Tuduseri[2010];** scan design has become the de-facto design for testability technique. Ease of testing and high test coverage widely accepted by the industry Those scan-shift transitions can be further reduced by selectively using the inverse connections between scan cells. In addition, the trade-off between routing overhead and power consumption can also be controlled by the proposed scan-cell reordering techniques.

**Elif Alpaslan, et.al [2010];** in this novel the author, propose a DFT-based approach for reducing circuit switching activity during the scan shifting process. Instead of inserting additional logic at the gate level which leads to introducing extra delay on critical paths, this method modifies the design at the register transfer level (RTL) and uses the synthesis tools to automatically deal with timing analysis and optimization.

**Y.Z.Wu and M. C. T. Chao[2010];** A common practice to lower the power consumption during scan-based testing is to reduce the number of scan cell's signal transitions, which can be classified into the following three types: (1) capture transitions and (2) scan-out transitions. Hence, to reduce these critical problems the scan shift is combined with a pattern-filling technique. In addition, the trade-off between routing overhead and power consumption can also be controlled by the proposed scan-cell reordering techniques.

**M. Elm, et.al [2008];** The document focuses on power consumption during the test. An effective power-saving technique when analyzing testicles is to shut down unused analysis chains. It is not dependent on a test set and can improve the performance of any test power reduction technique as a result. The approach does not specify any sorting within strings and fits well with any standard scanning string integration tool. The approach produced but the proposed system does not imply any scan chain reordering but partitions the flip flop into sets.

**J.T.Zhang and Q. Zuo[2007];** The requirements for testing these portable products are so strict since the test power dissipation and reliability directly determine the quality of chips. In this paper, the MPC-SCAN (Multi-phase clock scan) technique has been proposed to reduce the average as well as the peak power of multiple scan circuits in a device. Unlike those previous methods proposed, MPC-SCAN technique has many unique advantages which maintains the fault coverage and dissipation limits.

**Swarup Bhunia, et.al [2005];** Power dissipation during test mode can be significantly higher. The author showed that the test power could be twice as high as the power consumed during the normal mode. Therefore the main concept is that test power is an important design concern to increase battery. Adding an extra transistor in only one logic level renders significant advantages with respect to area, delay, and power overhead compared to existing methods, which use gating logic at the output of scan flip-flops. Simulation results proposed by the author signifies ISCAS89 benchmarks show an average improvement of 62% in area overhead, 101% in power overhead (in normal mode), and 94% in delay overhead, compared to the lowest cost existing method.

**Min Hao Chiu and J.C.M.Li[2005];** This paper presents a Jump scan technique or also known as a J-scan technique for low power testing. The J-scan/Jump Scan shifts two bits of scan data per clock cycle so the scan clock frequency is reduced without evaluating the test time. Consecutively, the experimental data show that the proposed technique effectively reduces the test power by two thirds compared with the traditional MUX scan. The presented technique requires very few changes in the existing MUX-scan design for testability methodology and needs no extra computation. The penalties are area overhead and speed degradation.

**Kenneth M. Butler, et.al [2004];** In recent years structural (mostly scan-based) tests have come to be the predominant procedure for mass IC production. When adding speed structural tests to the standard production tests presents an series of new problems. In this paper, the author will begin by presenting pattern generation approaches to minimize power consumption that would be used if power-related problems were discovered after design completion. Hence investigates various heuristics for modifying test content to address power concerns.

**S. Ghosh and N. A. Toubia[2003];** Two of the main drawbacks of scan testing are the power dissipation and the area overhead. In CMOS circuits, power dissipation is proportional to the amount of switching activity that takes place. During scan testing, a much larger percentage of the scan cells will change value. In order to overcome this defect the paper focuses on technique for minimizing power dissipation that is also capable of reducing the circuit head area, relative to a random order of scan cells for

a given set of test vectors. The experiments show that with a proper choice of the parameter  $\lambda$ , the creators algorithm is quite effective in reducing the power in a circuit.

**P.Gupta, et.al [2003];** A scan chain is commonly used to implement the shift registers that store the input and output vectors during the testing phase of manufacturing. In this paper a routing-driven and timing-aware methodology for scan insertion with minimum wirelength is used. We take into account timing slacks at all sinks that are affected by scan insertion, to achieve a scan chain ordering that meets timing and has smallest wirelength. For the case where sink timing is not met, we also propose a buffer insertion methodology with minimum wirelength objective. The key contribution of this paper is a method to compute a timing-driven incremental connection suited to scan insertion.

**Patrick Girard [2002];** Production of current efforts by the creators are focused on leveraging the available on-chip scan design for-test (DFT) capability to afford effective and low cost structural timing tests based on the transition delay fault (TDF) gate delay and path delay fault models. He started with a discussion of power consumption which provides the reasons and consequences for the increase in power during the test. Thus concludes it with a discussion of the opportunity to use such techniques in varying situations.

**Y. Bonhomme, et.al [2002];** With ever decreasing geometry sizes and increasing clock speeds, ascertaining correct operation of digital circuits at the desired speed becomes a necessity rather than an option to maintain the quality level of the product. Detecting a delay fault normally requires the application of a pair of test patterns. Reductions of average and peak power consumption during scan testing are up to 58% and 24% respectively for experimented ISCAS benchmark circuits.

**Chein-Chung Tsai, et.al [2002];** this paper the author presents a methodology to insert scan paths in a functional Register Transfer Level also known as (RTL) which specifies a design that can damage existing functional paths between sequential elements in the original circuit for establishing scan chains. . This may prove to be very expensive cause of re optimization. Scan path insertion at Register Transistor Level is a step towards achieving RTL DFT.

**M. Bushnell and V. Agrawal [2000];** A client intercession based progressed method for the recognition of the effectiveness of the ILS architecture depends on the actual

configuration of individual scan chains. Consecutively, results on the ISCAS'89 benchmark circuits show that the proposed ILS configuration method can achieve on an average 5% more fault coverage in the Broadcast Mode and an average 15% more reduction in total test data volume and test application time than the existing methods.

**R.Sankaralingam and N. A. Toubia[2000];** has introduced a compaction procedure which can be used to find a minimal set of scan vectors that satisfies constraints on both average power and peak power. This proposed mechanism is simple yet effective and can be easily implemented and used in the conventional test vector generation flow which is increasingly used in industries today. And also controlled or minimized the amount of heat that can be safely dissipated without damaging the chip.

**S.Gerstendorfer and H.-J. Wunderlich[1999];**Power dissipation is a major concern for many designers. Power supply and packaging of a circuit are cost-intensive parts which must be sized corresponding to the peak power consumption and power dissipation during BIST limits the optimization potential of so-called "low power" designs. Secondly, It shorten the life of batteries. The authors use the switching activity of the circuit nodes as a metric for the energy consumption since in static CMOS circuits the switching energy contributes to over 90 % of the total energy consumption

**L. H. Goldstein and E. L. Thigpen [1980];** A method for analyzing the testability of digital circuits was described in detail. This paper describes the SCOAP program implementation of the testability analysis algorithms at Sandia Laboratories. First, related work in the area of design for testability is summarized. Next, the test-ability analysis method is reviewed. Two major approaches have emerged in recent years to facilitate the development of testable structured design for testability and testability measure analysis. Experience to date has indicated that SCOAP is a valuable tool for testability analysis of LSI complexity digital circuits throughout the design process.

## **CHAPTER 3**

### **AIM AND SCOPE OF THE PROJECT**

#### **3.1 OVERVIEW**

The main reason for Scan DFT(Testability) is to under the defects/faults imposed in a circuit during manufacturing. By applying various test patterns in the circuit leads to overdoing which in turn paves way for harming the circuit itself due to higher transition of the scan cells.

The motivation behind this process is to scan Flip-flop in the netlist and the flip-flops are stitched in alphabetical order by instance name into the scan chains.

After this process method determines the order of flip-flops to reduce the test power by using the circuit topology and can form low-power scan chains while maintaining the conventional DFT design flow.

#### **3.2 AIM OF THE PROJECT**

The main aim of the project is to aim in power reduction while testing a circuit in functional mode. We have collected schematics which can be implemented in an FPGA for further hardware productability.

From the literature studies the objective is confined to,

- Reduce in transition rate
- Reduction of energy consumption
- Improve the fault coverage area

The scan chain stitching is made power-aware by placing the flip-flops which have more test combination requirements at the beginning of scan chains, while flip-flops with lower test combination requirements are inserted towards the end of scan chains. This will give an output that lowers the quiescent power. Scan Input (SD) and Scan enable (SE). We identify convenient chains of flipflops and stitch them together, and connect in the form of a shift register circuit with their SD, SE pins.

The second process, logic topology-based scan stitching, determines the order of the flip-flops by calculating the scan influence value, using which the proposed method can reduce the shift-in power by consolidating the care bit density in the test patterns. The experiments conducted on ISCAS'89 and ITC'99 benchmark circuits demonstrate that on average, the proposed method reduces the shift power by 28.36% compared with a previous logic topology-based scan chain stitching method.

This technique can reduce the number of transitions by changing the order of scan cells that form the scan chains. However, most methods for scan chain stitching also known as scan chain reordering rely on specific test patterns, and reduction of test power is limited when additional test patterns are required. In addition, test patterns such as path delay and resistive bridge faults cannot be applied because they are generated after completion of the design process. Therefore, it is necessary to reduce the test power by considering the circuit testability rather than by relying on specific test patterns. This logic topology-based method as a low-power scan architecture has been implemented using clustering and logic cones.

Our new logic topology-based scan chain stitching method sets up the DFT after synthesis in a conventional front-end design flow

However, these methods rely on the reference test pattern to determine the order of flip-flops, which causes the occurrence of fewer transitions mathematically based on specific test patterns. If additional test patterns are required in the design established by these methods, the achieved reduction in test power is limited. Furthermore, test patterns generated after the complete design is established cannot be applied at all.

Therefore, a logic topology-based method is also necessary for reducing the test power in consideration of the circuit testability.

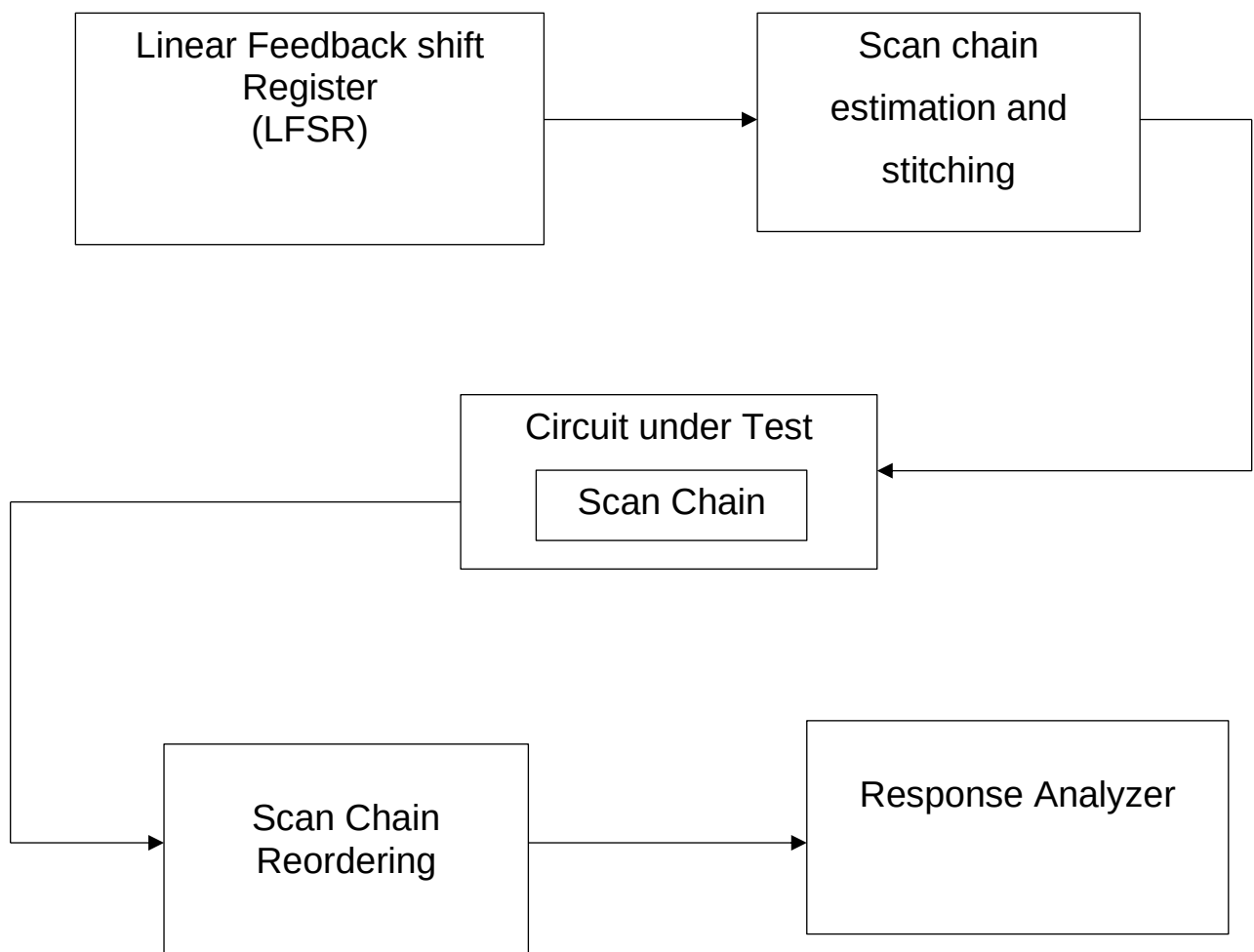
### **3.3 SCAN CHAIN TESTING**

Scan testing is carried out for various reasons, the two most prominent of them are:

- To test stuck-at faults in manufactured devices.
- To test paths in manufactured devices for the delay, i.e. to test whether each path is working at a functional frequency or not.

Scan chain stitching techniques have been studied as one of the low-power scan architectures for improving the reliability of scan-based testing. Scan-based testing is beneficial for obtaining high test coverage of system-on-chip designs.

When the circuit-under-test (CUT) is tested using the scan architecture, the test power is generated by switching activity through the scan chains.



**Fig 3.1 Block diagram of bit-swapping LFSR and Scan Chain Ordering**

The increase in the number of scan cells in recent times has led to an increase in the switching activity during scan shifting; consequently, the test-power consumption during scan-based testing has become higher than that in the functional mode

## CHAPTER 4

### EXPERIMENTAL SETUP AND IMPLEMENTATION OF PROJECT

#### 4.1 SCAN CHAIN

Scan chains are the elements or products in scan-based designs that are used to shift-in and shift-out test data. A scan chain consists of a number of back-to-back linked flops in a chain with one outgoing flop linked to another. The input of the first flop is connected to the chip's input pin (called scan-in) from which the scan data is fed. The output of the last flop is connected to the chip's output pin (called scan-out) which is used to extract the shifted data.

#### 4.2 PURPOSE OF SCAN CHAIN

Scan chains are inserted into designs to shift the test data into and out of the chip. This is done to make every point in the chip controllable and observable as discussed below.

#### 4.3 NORMAL TO SCAN FLIP FLOP

The flops in the design have to be modified or changed in order to be put in the scan chains. To do so, the normal input of the flip-flop has to be multiplexed with the scan-in. A signal called scan-enable is used to control which input will propagate to the output of the scan chain.

#### 4.4 PURPOSE OF TESTING

In VLSI designs millions of transistors are packed into a single chip. Therefore, this leads to manufacturing defects and all the chips need to be physically tested by giving input signals from a pattern generator and comparing all the responses using a logic analyzer; this process is called Testing of the circuit.

##### ***4.4.1 Objective of Testing***

- Exercise the system and analyze the response to ascertain whether it behaves correctly after manufacturing test objectives
- Ensure product quality

## **4.5 DESIGN FOR TESTABILITY(DFT)**

DFT in VLSI is an innovative design technique to make chip testing cost-effective by adding circuitry to the chip. They improve the observability and controllability of internal nodes to increase the testability of all logic in the chip.

## **4.6 DFT TECHNIQUE**

DFT techniques are broadly classified into two types:

### **4.6.1 Ad-Hoc TECHNIQUE**

These are a collection of techniques or rules (do's and don'ts) the chip design process learned from design experience to make design testability more comfortable. Typically, these are the rules that have been gathered over time after experiencing various errors.

## **4.7 STRUCTURED TECHNIQUES**

In contrast to Ad-hoc, structured DFT implies that the same design approach can In this technique, additional logic and signals are added to the circuit to allow testing according to a predefined procedure. This technique is the only solution to modern world DFT problems.

## **4.8 CLUSTERING**

Scan chain clustering has been employed as a logic topologybased technique for the realization of a low-power scan architecture.Each flip-flop corresponding to the output cone of a specific fault examines its fault-covering input cone, and the topology is modeled using a hypergraph. For reduction of the test-power consumption, scan chain partitioning is configured using the hypergraph. However, this method requires additional hardware to disable the scan chain partitioning. In the previous logic topology-based scan chain stitching method , termed logic cluster controllability (LoCCo), the design is parsed at the beginning to sort the flipflops according to their test combination, and higher test combination requirements are estimated through logic clustering.

## **4.9 XILINIX ISE**

Xilinx ISE 7.4i & Xilinx Platform Studio 7.4 are the programming tools for the system.

- This is used for generate RTL & FPGA schematic.

- This is used for create logic design like micro blaze design.

XPS includes a graphical user interface (GUI), along with a set of tools that aid in project design. From the XPS GUI, you can design a complete embedded processor system for implementation within a Xilinx FPGA device. The XPS main window is shown in the figure below.

#### ***4.9.1 Professionally built***

XILINX toolboxes are professionally developed, rigorously tested, and fully documented.

#### ***4.9.2 With interactive apps***

XILINX apps let you see how different algorithms work with your data. Iterate until you've got the results you want, then automatically generate a XILINX program to automate your work. Can work independently or in collaboration with Modelsim or Quatrus prime.

#### ***4.9.3 Ability to Scale***

Xilinx technology provides scalability, flexibility, and performance for packet networks so that you can support protocols ranging from legacy to cutting-edge.

#### ***4.9.4 Used For***

The Xilinx ISE is widely used for circuit synthesis and design. The ISE Project Navigator manages and processes your design through several steps in the ISE design flow.

### **4.10 MODELSIM**

ModelSim packs an unprecedented level of verification capabilities into a cost-effective HDL simulator and is ideally suited for the verification of small and medium-sized FPGA designs – especially designs with complex, mission-critical functionality. Fast time to coverage closure.

Languages that can be used:

Hardware descriptive languages as

- VHDL

- Verilog
- SystemC, and includes a built-in C debugger.

#### **4.10.1 Interactive apps**

ModelSim can be used independently, or in conjunction with Intel Quartus Prime, PSIM, Xilinx ISE or Xilinx Vivado.

#### **4.10.2 Used For**

ISIM or the ModelSim logic simulator is used for system-level testing. This document is for information and instruction purposes.

### **4.11 BASIC CONCEPT**

Built-in-self-test (BIST) is a technique in which additional circuitry is added to core under test (CUT) in order to make it able to test itself with minimum external help. The general structure of a self-testable circuit is composed of a test pattern generator (TPG) , a test response evaluator (TRE) and a BIST control unit (BCU) .This technique is especially preferable when it is difficult to access the CUT externally. It also helps to protect intellectual property (IP) and to reduce cost of the external test equipment (ATE) by minimizing the amount of test data that has to be stored off-chip.

Its implementation can lead to better test quality thanks to its improved speed test support, which is essential for detecting lagging faults. BIST supports in-field and on-line testing, which helps to reduce the cost of system maintenance. It also offers the opportunity to improve reliability by means of burn-in testing. BIST approaches can be divided into test-per-scan and test-per-clock schemes.

#### **4.11.1 BIST-Built In Self Test**

A built-in self-test (BIST) or built-in test (BIT) is a mechanism that permits a machine to test itself. Engineers design BISTs to meet requirements such as:

- high reliability
- lower repair cycle times

or constraints such as:

- limited technician accessibility
- cost of testing during manufacture

The main purpose of BIST is to reduce the complexity, and thereby decrease the cost and reduce reliance upon external (pattern-programmed) test equipment. BIST reduces cost.

## **4.12 TEST-PER-SCAN SCHEME**

Test-per-scan BIST schemes require scan-based design. In the case of sequential circuits, this means that all the storage cells can be configured as one or several scan paths (chains), which are used as serial shift registers in test mode. In this way, each storage device of the CUT becomes easily controllable and observable. The test stimuli/responses are shifted into/out of the scan paths. Scan-based design helps to reduce the problem of testing sequential circuits to the simpler problem of testing combinational circuits. The shift counter controls the bit stream which is generated and shifted into the scan path by a TPG.

### **4.12.1 TEST-PER-CLOCK Scheme**

In a test-per-clock scheme a test pattern is applied to the CUT every clock cycle. This scheme is best suited for register-based design. This type of scheme uses a specific BIST architecture that uses the Integrated Logic Block Observer (BILBO), which is a more sophisticated register that can function as a normal state register, scan register, PRPG or MISR. All functionality of the BILBO depends on the mode input signals.

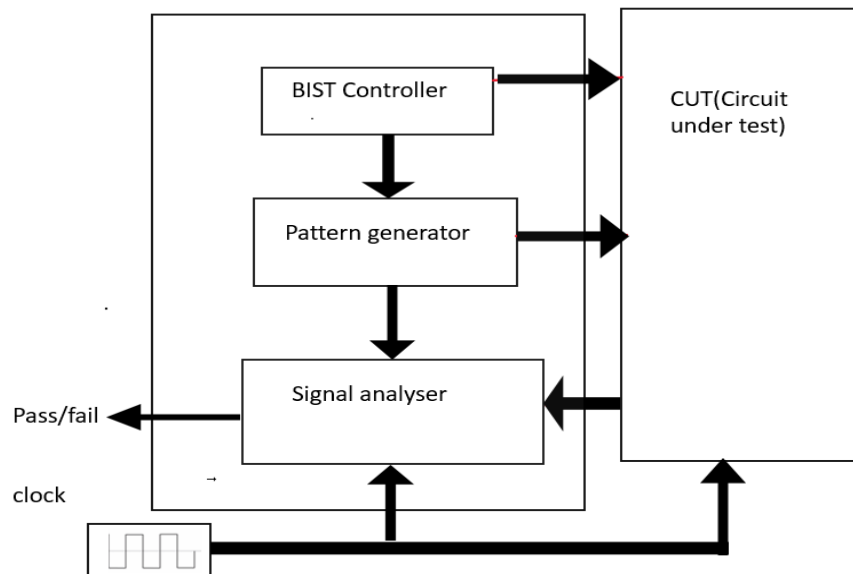
### **4.12.2 Test Pattern Generation**

Test pattern generation for both test-per-scan and test-per-clock BIST schemes can be classified into the following groups: pseudo-random, weighted, exhaustive, pseudo exhaustive, deterministic and mixed-mode schemes..

## **4.13 TEST RESPONSE ANALYSER**

Besides test pattern generation, BIST architectures should also be able to compress/evaluate test responses. As the number of test patterns applied to the CUT

is usually very large, it is infeasible to store all the expected values on-chip and compare them with the response values.



**Fig 4.1 BLOCK DIAGRAM of bit swapping LFSR n scan chain ordering**

It is much cheaper in terms of storage requirement and compacting circuitry to compress the test responses to short sequences, called signatures, which are delivered for analysis at the end of the test session. A signature is obtained as the final state of a finite state machine whose inputs are fed with test responses. This type of compression which addresses the length of the test response sequence is also known as time compression. Examples of time compressors are accumulator, LFSR- and counter-based compactors.

#### 4.14 ALGORITHM STEPS

- 1) Simulate the CUT for the test patterns generated by the BS-LFSR.
- 2) Identify the group of vectors and responses that violate the peak power.
- 3) In these vectors, identify the cells that mostly change their values in the test cycle and cause the peak-power shift.

## 4.15 CELL ORDERING

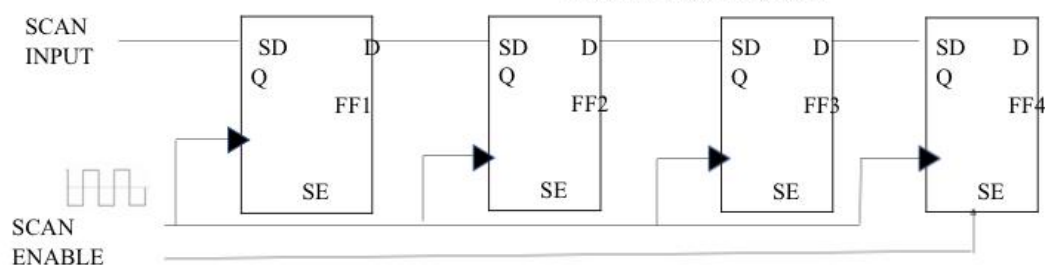
The proposed BSLFSR has been combined with a cell sorting algorithm, which reduces the number of transitions in the parse chain when parsing the captured response. The problem of capture power (peak power in the test cycle) will be solved using a new algorithm that will rearrange some cells in the scan chain so as to minimize the Hamming distance between the applied test vector and the captured response in the test cycle, hence reducing the test cycle peak power (capture. If you find that when two cells have a different value, the considered cell) will most probably have no transitions in the test cycle, then connect these cells together through an inverter.

### 4.15.1 Circuit under test

The BS-LFSR is evaluated regarding the length of the test sequence needed to achieve certain fault coverage. The scan-chain-ordering is performed in the circuit under test in order to reduce the capture power. The experiments were performed on full-scan ISCAS'89 benchmark circuits and the percentage of redundant faults in the CUT, and fault coverage is analyzed.

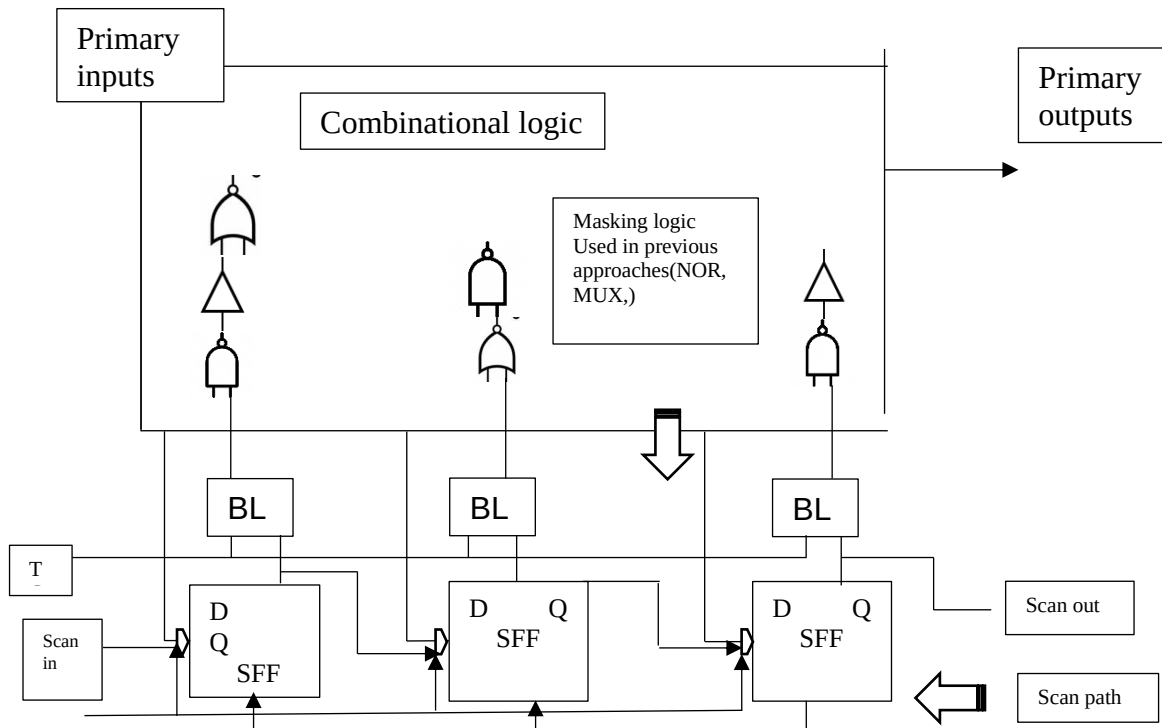
### 4.15.2 Low power design

Power dissipation during test mode can be significantly higher than that during functional mode, since the input vectors during functional mode are usually strongly correlated compared to statistically independent consecutive input vectors during testing.



**Fig 4.2 Scan ordering**

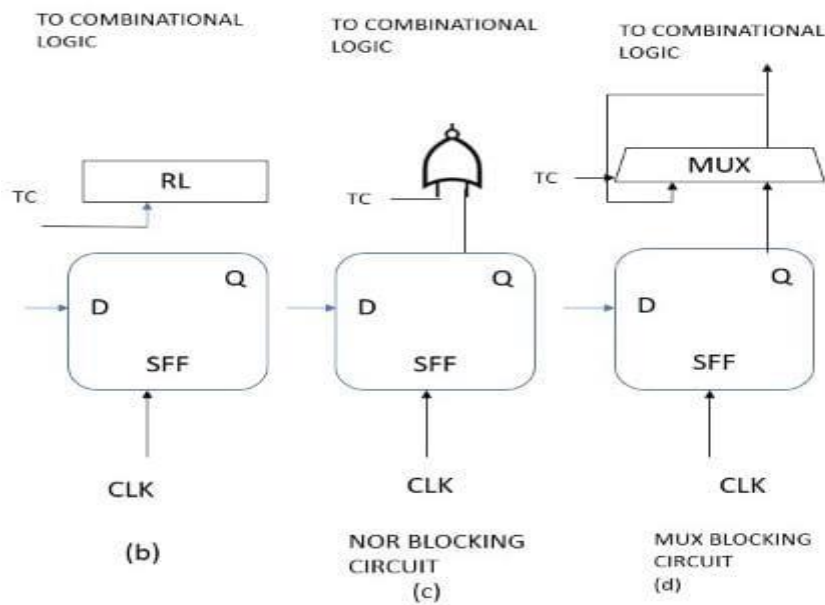
Increased peak power is likely to create noise problems in a chip by causing a drop in the supply voltage. Peak and average power reduction during test contributes to the enhanced reliability of the test and improvement of yield. It is,



## 4.16 INTERNAL ARCHITECTURE

automatic test pattern generation technique is proposed to redesign test vectors to reduce power dissipation during sweep test.

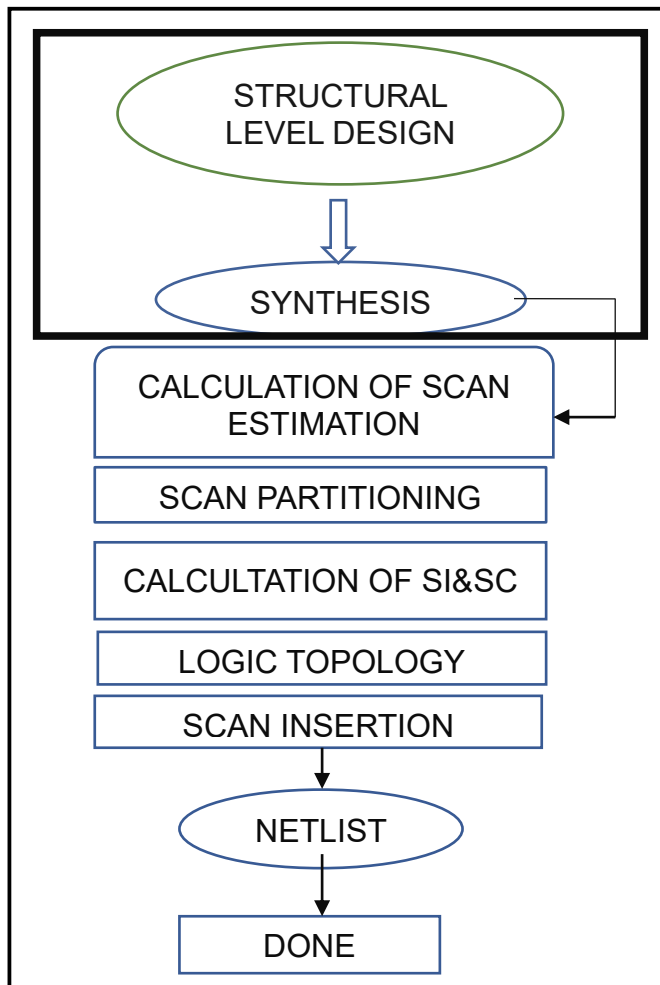
Thanks to their automatic test pattern on (ATPG), redundant transitions in combinatorial logic can be reduced but not completely eliminated. Additionally, the test application time can increase the power trade. Scan-latch reordering or input vector reordering techniques have been proposed for reduction in test power. However, these techniques target Reduction of transitions at the output of scan flip-flops and cannot eliminate redundant switching in combinatorial block .A solution is provided to reduce peak and average power dissipation by transforming the conventional sweep architecture into the desired number of selectable separate scan paths In this scheme, the test-set is generated and sorted so that only editable parts of consecutive tests are moved into the analysis .



**Fig 4.4 Combinational circuit**

There is the solution to prevent peak power violation during both shift and capture cycle using scan chain partitioning. However, the modification of the scan flip-flop in results in a substantial increase in area and degradation in performance. propagation ripple effect to logic gates offers a simple and effective solution to significantly reduce test power, independent of the test set. proposed the locking method based on NOR or NAND gate.

Blocking gates (of type NOR or NAND) are controlled by the test enable signal and the stimulus paths remain fixed at either logic “0” or logic “1” during the entire scan shift operation. Multiplexers at the output of the scan cells have been used, which hold the previous states of the scan register during shifting and total test power in a 45-nm.



**Fig 4.5 Low power BIST Technique**

There is the solution to prevent peak power violation during both shift and capture cycle using scan chain partitioning; degradation in performance. propagation ripple effect to logic gates offers a simple and effective solution to significantly reduce test power, independent of the test set. proposed the locking method based on NOR or NAND gate. Blocking gates (of type NOR or NAND) are controlled by the test enable signal and the stimulus paths remain fixed at either logic “0” or logic “1” during the entire scan shift operation. Multiplexers at the output of the scan cells have been used, which hold the previous states of the scan register during shifting and total test power in a 45-nm.

## CHAPTER 5

### RESULTS AND DISCUSSION

#### 5.1 EXPERIMENTAL RESULTS

A group of experiments was performed benchmark circuit In the first series of experiments, the BSLFSR is evaluated as a function of the length of the test sequence required to achieve some fault coverage with and without the scan chain ordering algorithm. Table 5.1 shows the results for a set of ten benchmark circuits. The columns labeled n, m and PI refer to the size of the LFSR, there respectively the number of flip-flops in the scanning chain and the number of primary inputs of the CUT.

**TABLE 5.1 Test Length Needed To Get Target Fault Coverage For LFSR And BSLFSR**

| Circuit | n  | m    | PI | RF%   | FC%  | Test length |        |                     |                    |
|---------|----|------|----|-------|------|-------------|--------|---------------------|--------------------|
|         |    |      |    |       |      | Det.        | LFER   | BS-LFSR no ordering | BS-LFSR with order |
| S641    | 32 | 19   | 35 | 0     | 98.0 | 53          | 5120   | 4910                | 4970               |
| S838    | 32 | 32   | 35 | 0     | 86.5 | 90          | 8160   | 8460                | 7910               |
| S1196   | 30 | 18   | 14 | 0     | 97.0 | 131         | 3750   | 3680                | 3370               |
| S1238   | 30 | 18   | 14 | 5.09  | 91.3 | 141         | 3890   | 3560                | 3610               |
| S5378   | 40 | 179  | 35 | .88   | 98.0 | 244         | 30110  | 33700               | 28900              |
| S9234   | 40 | 228  | 19 | 6.52  | 90.0 | 367         | 397800 | 401930              | 398170             |
| S13207  | 60 | 669  | 31 | 1.54  | 95.0 | 455         | 49660  | 47400               | 48110              |
| S35932  | 64 | 1728 | 35 | 10.19 | 89.8 | 63          | 18700  | 16640               | 16520              |
| S38417  | 64 | 1636 | 28 | .53   | 96.5 | 849         | 118580 | 125520              | 117080             |
| S38584  | 64 | 1452 | 12 | 4.15  | 94   | 632         | 43530  | 39660               | 40090              |

The column labeled RF indicates the percentage of redundant failures in the CUT, and fault coverage (FC) refers to the target fault coverage which includes redundant faults. The last four columns indicate the test duration required for a deterministic test (ex., the optimal set of test vectors is stored in a ROM), a conventional LFSR, a BSLFSR without scan chain sorting, and a BSLFSR with scan chain sorting, respectively. The results in Table show that the BS-LFSR needs a shorter test length than a conventional LFSR for many circuits even without using the scan chain-ordering

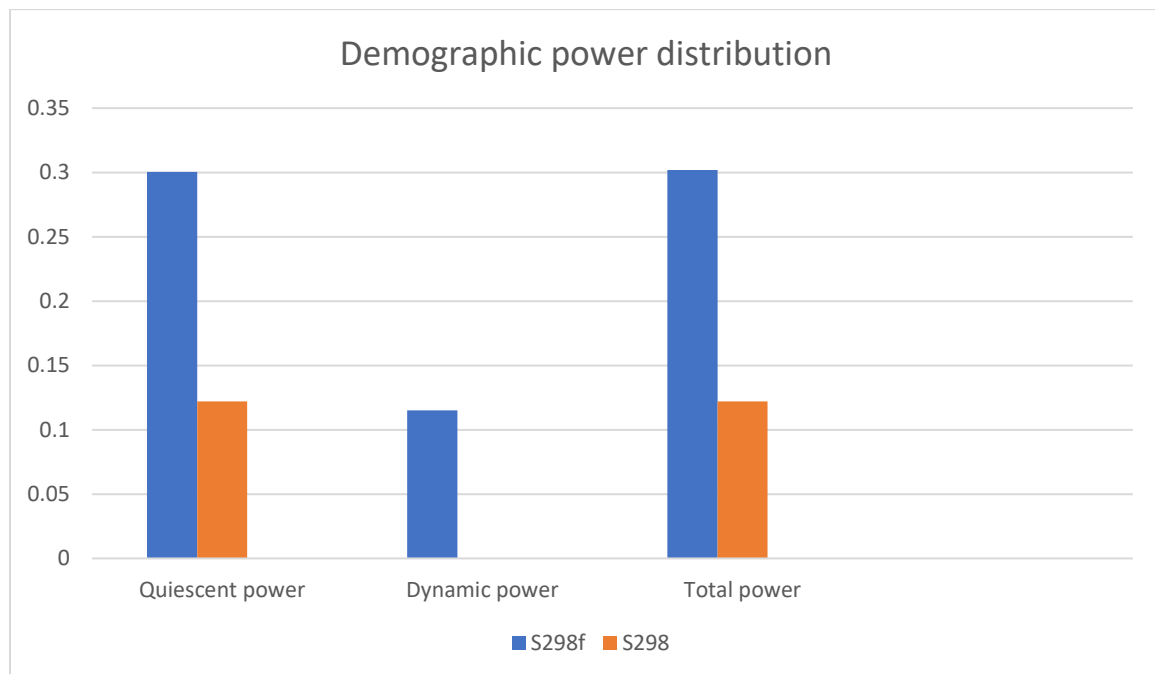
algorithm. It also shows that using the scan-chain ordering algorithm with BS-LFSR will shorten the required test length.

The second set of experiments is used to evaluate the BS-LFSR together with the proposed scan-chain-ordering algorithm in reduce the average and peak power. For each reference circuit, the same number of conventional LFSR and BSLFSR patterns are applied to the full scan configuration. The obtained results for the same benchmark circuits as in Table 5.1

Finally, the results obtained by the proposed technique for peak-power reduction as follows It is clear from the table that the proposed method has better results for most reference circuits.

## 5.2 RESPONSE ANALYSER

The response analyzer is used to compare the expected result with the response obtained from the circuit under test. And with this response the fault coverage of the circuit under test is analyzed.



***Fig 5.1 Xpower analysis of Fault and Proposed method***

Comparative response of different powers in S298 test model and s298 benchmark circuit.

| Name                  | Value                   | Used | Total Available | Utilization (%) |
|-----------------------|-------------------------|------|-----------------|-----------------|
| Clocks                | 0.00067 (w)             | 1    | ---             | ---             |
| Logic                 | 0.00014 (w)             | 72   | 19200           | 0.4             |
| Signals               | 0.00026 (w)             | 79   | ---             | ---             |
| IOs                   | 0.00044 (w)             | 50   | 222             | 22.5            |
|                       |                         |      |                 |                 |
| Total Quiescent Power | <b>0.30034 (w)</b>      |      |                 |                 |
| Total Dynamic Power   | <b>0.00150 (w)</b>      |      |                 |                 |
| Total Power           | <b>0.30184 (w)</b>      |      |                 |                 |
|                       |                         |      |                 |                 |
| Junction Temp         | <b>30.6 (degrees C)</b> |      |                 |                 |

**Fig 5.2 based power analysis**

Xilinx Power Estimator (XPE) can be used during the pre-design and pre-implementation phases of the power analysis design cycle.

XPE is also commonly used later in the design cycle during implementation and power closure to, for example, evaluate power implications of engineering change orders. The previous method has a Quiescent power of 0.30034W while the proposed method has a Total Quiescent power of 0.122W .There is a significant level drop of power that has been analyzed in the scan chain procedure.

| A                     | B                | C                  | D         | E             | F           | G               | H | I | J       | K       | L           | M           | N           |
|-----------------------|------------------|--------------------|-----------|---------------|-------------|-----------------|---|---|---------|---------|-------------|-------------|-------------|
| Device                |                  | On-Chip            | Power (W) | Used          | Available   | Utilization (%) |   |   | Supply  | Summary | Total       | Dynamic     | Quiescent   |
| Family                | Artix7           | Clocks             | 0.000     | 1             | ---         | ---             |   |   | Source  | Voltage | Current (A) | Current (A) | Current (A) |
| Part                  | xc7a100t         | Logic              | 0.000     | 122           | 63400       | 0               |   |   | Vccint  | 1.000   | 0.035       | 0.000       | 0.035       |
| Package               | csg324           | Signals            | 0.000     | 152           | ---         | ---             |   |   | Vccaux  | 1.800   | 0.021       | 0.000       | 0.021       |
| Temp Grade            | Industrial       | IOs                | 0.000     | 30            | 210         | 14              |   |   | Vcco18  | 1.800   | 0.003       | 0.000       | 0.003       |
| Process               | Maximum          | Leakage            | 0.122     |               |             |                 |   |   | Vccbram | 1.000   | 0.001       | 0.000       | 0.001       |
| Speed Grade           | -3               | Total              | 0.122     |               |             |                 |   |   | Vccadc  | 1.710   | 0.025       | 0.000       | 0.025       |
| Environment           |                  | Thermal Properties |           | Effective TJA | Max Ambient | Junction Temp   |   |   |         |         |             |             |             |
| Ambient Temp (C)      | 30.0             |                    |           | (C/W)         | (C)         | (C)             |   |   |         |         |             |             |             |
| Use custom TJA?       | No               |                    |           | 4.6           | 99.4        | 30.6            |   |   |         |         |             |             |             |
| Custom TJA (C/W)      | NA               |                    |           |               |             |                 |   |   |         |         |             |             |             |
| Airflow (LFM)         | 250              |                    |           |               |             |                 |   |   |         |         |             |             |             |
| Heat Sink             | Medium Profile   |                    |           |               |             |                 |   |   |         |         |             |             |             |
| Custom TSA (C/W)      | NA               |                    |           |               |             |                 |   |   |         |         |             |             |             |
| Board Selection       | Medium (10"x10") |                    |           |               |             |                 |   |   |         |         |             |             |             |
| # of Board Layers     | 12 to 15         |                    |           |               |             |                 |   |   |         |         |             |             |             |
| Custom TJB (C/W)      | NA               |                    |           |               |             |                 |   |   |         |         |             |             |             |
| Board Temperature (C) | NA               |                    |           |               |             |                 |   |   |         |         |             |             |             |

**Fig 5.3 Scan chain stitching method power analysis**

Timing constraints are instructions that the designer gives to the Xilinx tool about the speed at which the designer wants to run the design. The Xilinx tool uses these instructions to construct an implementation that meets the timing constraints.

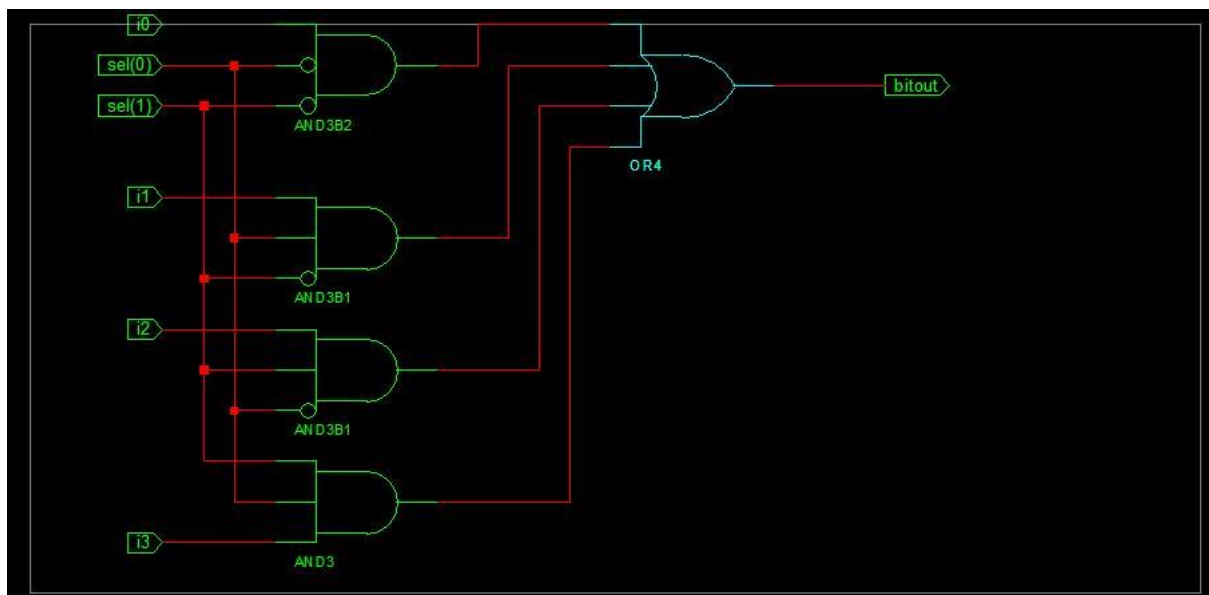
**Table 5.2 power estimation comparison**

| S.NO | CONTENT               | SCAN CHAIN<br>STITCHING<br>METHOD | EXISTING<br>METHOD |
|------|-----------------------|-----------------------------------|--------------------|
| 1    | TOTAL QUIESCENT POWER | 0.034W                            | 0.034W             |
| 2    | TOTAL DYNAMIC POWER   | 0.006W                            | 0.089W             |
| 3    | TOTAL POWER           | 0.039W                            | 0.124W             |
| 4    | TEMPERATURE(C)        | 25.0                              | 25.0               |

The previous method has a Quiescent power of 0.30034W while the proposed method has a Total Quiescent power of 0.122W .There is a significant level drop of power that has been analyzed in the scan chain procedure.

### 5.3 RTL SCHEMATIC

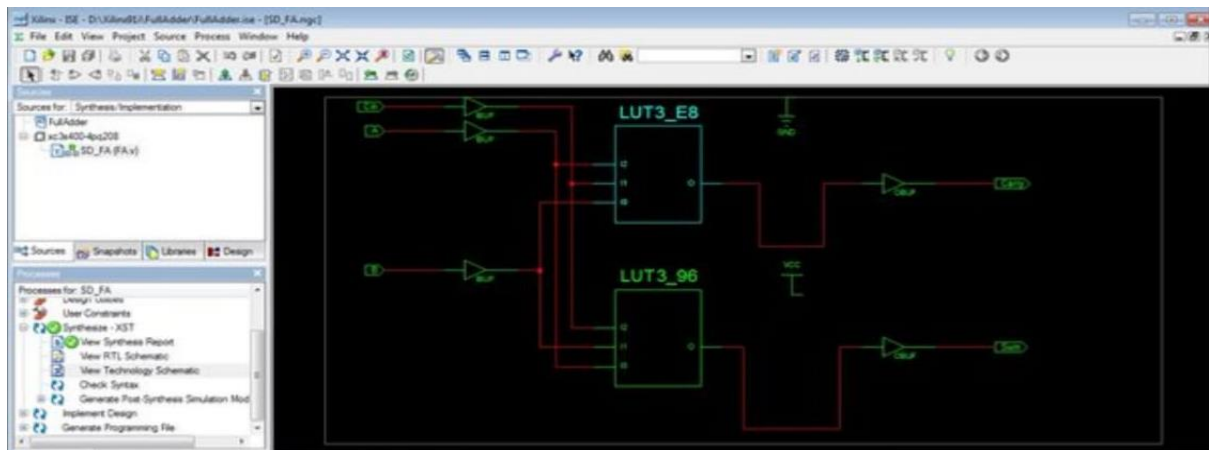
After XST synthesis is completed,hepls to view both RTL and technology schematic.I frequently observe discrepancies between these two schematics.RTL View shows you the representation of your design in terms of generic symbols means like AND Gates, OR Gates, adders, multipliers etc.



**Fig 5.4 RTL schematic of AND gate**

## 5.4 TECHNOLOGY SCHEMATIC

Technology View shows you the representation of your design in terms of logical elements means like LUTs, buffers, I/Os, and other technological components.



**Fig 5.5 Technology Schematic of full adder**

### 5.4.1 Difference between Schematic

Viewing an RTL schematic opens an NGR file that can be viewed as a gate-level schematic. This schematic is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

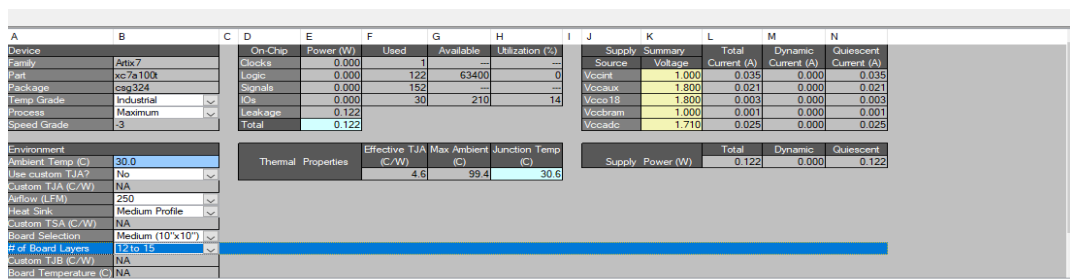
### 5.4.2 Technology View

Viewing a technology diagram opens an NGC file that can be viewed as an architecture-specific diagram. This diagram is generated after the optimization and technological targeting phase of the synthesis process. It shows a representation of the design in terms of logic elements optimized for the Xilinx target device or "technology"; for example, in terms of LUTs, transport logic, I/O buffers, and other technology-specific components. Viewing this diagram allows you to see a technology-level representation of your HDL optimized for specific Xilinx architecture, which might help you uncover design issues early in the design process.

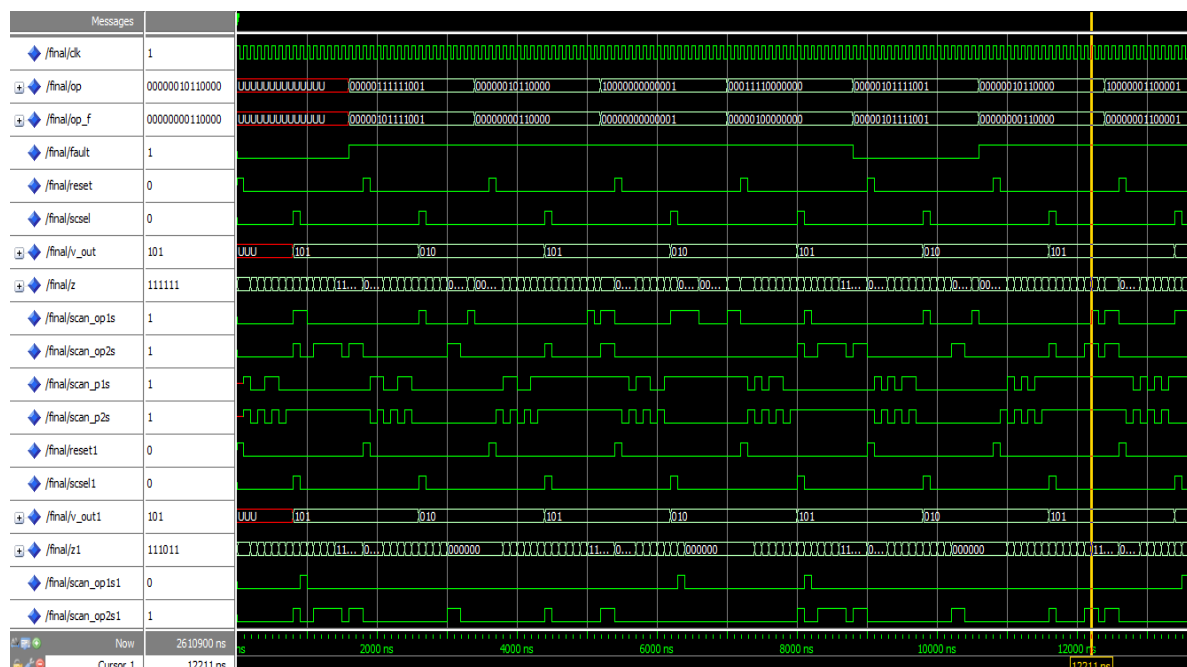
Xilinx Power Estimator (XPE) can be used during the pre-design and pre-implementation phases of the power analysis design cycle. With the increasing

complexity and computing power of modern programmable devices, the first analysis of electrical and thermal specifications is essential for successful product design.

XPE is also commonly used later in the design cycle when implementing and power closure to, for example, evaluate power implications of engineering change orders (ECO). For large designs implemented by multiple teams, the project leader can use XPE to import utilization and activity for each team's module, then monitor the total power and reallocate the power budget to ensure constraints.

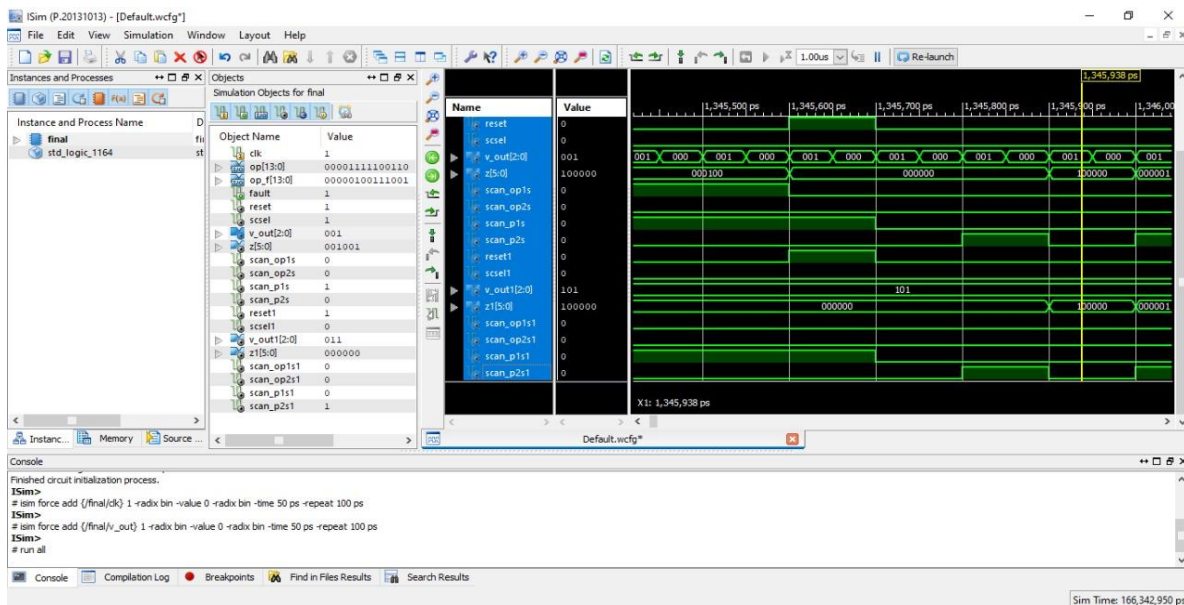


**Fig 5.6 Proposed method of power analysis**



**Fig 5.7 Output waveform in Modelsim**

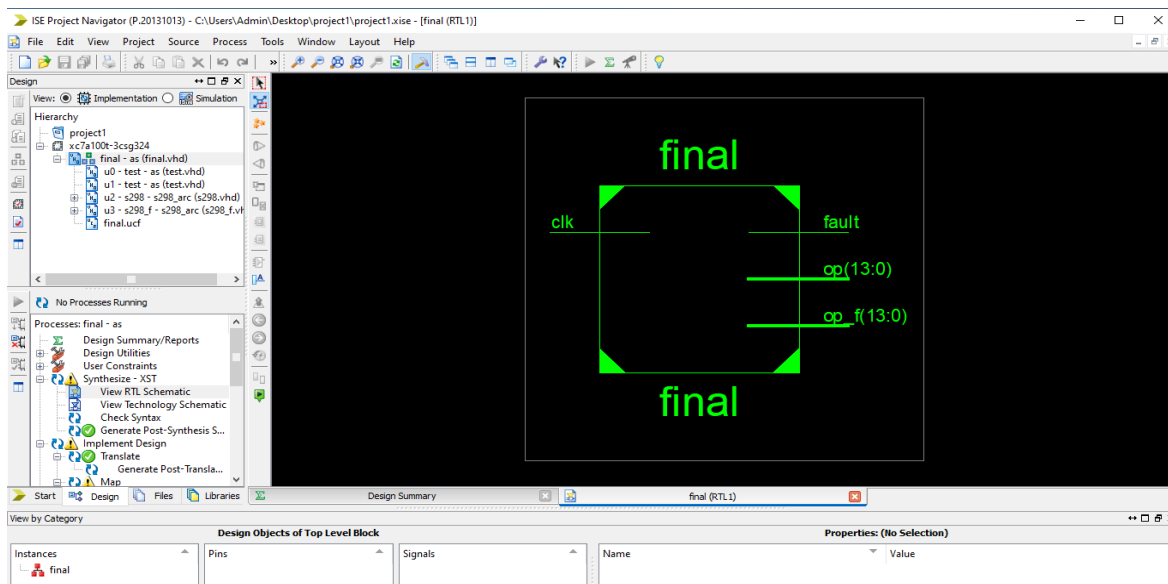
The waveform view contains waves (binary 0's and 1's, hexadecimal digits, binary digits, enumerated types, etc) for all of the signals in your design. It shows how your module reacts to different stimulus.



**Fig 5.8 Output waveform in the Project navigator**

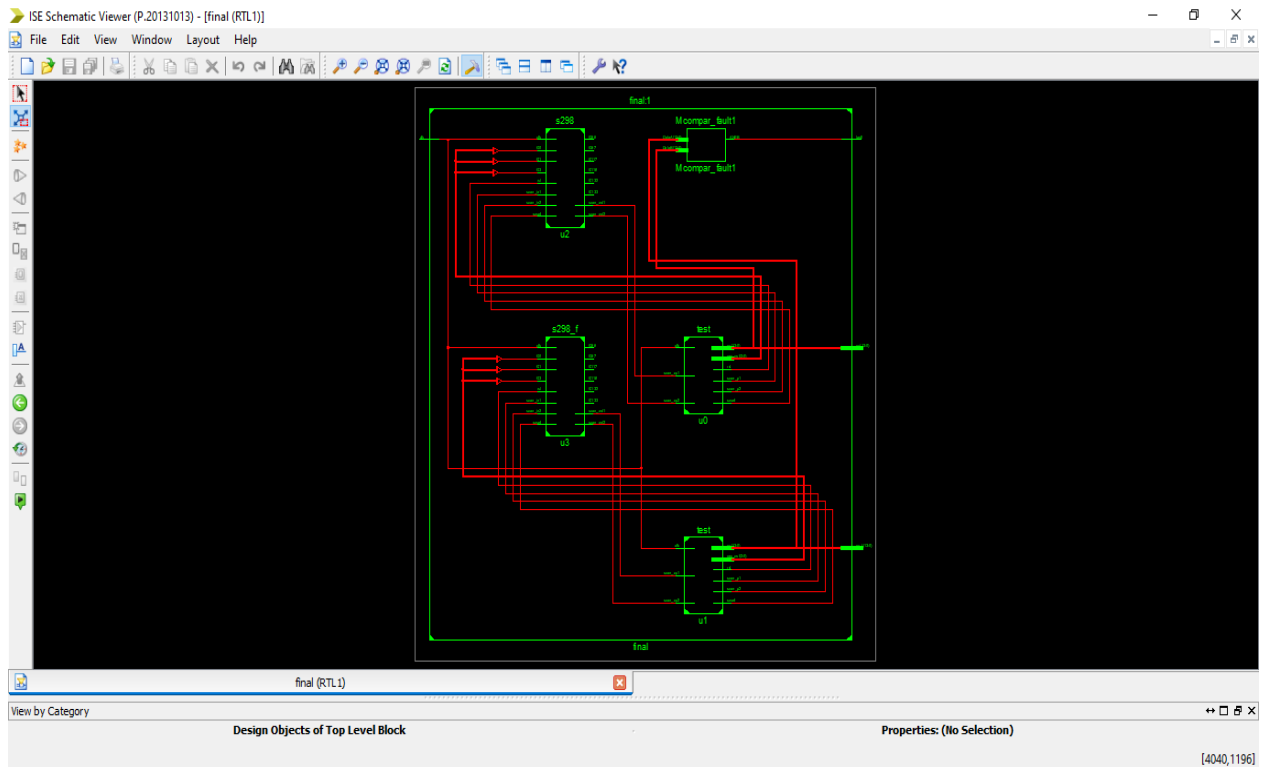
The Drawing Management environment within the Project Navigator helps you organize, create, and access all your project drawings in one unified interface. The output waveform is produced in Xilinx version 14.7.

After XST synthesis is completed, helps to view both RTL and technology schematic.



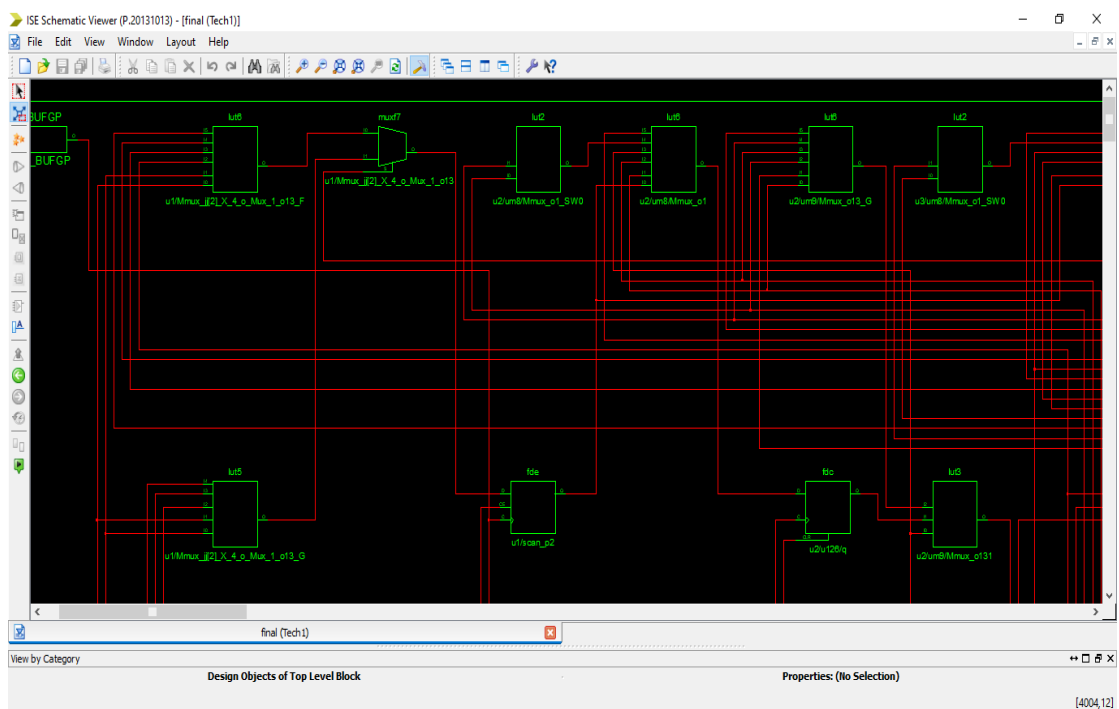
**Fig 5.9 RTL schematic**

It is frequently observed discrepancies between these two schematics. RTL View shows you the representation of your design in terms of generic symbols means like AND Gates, OR Gates, adders, multipliers, etc.

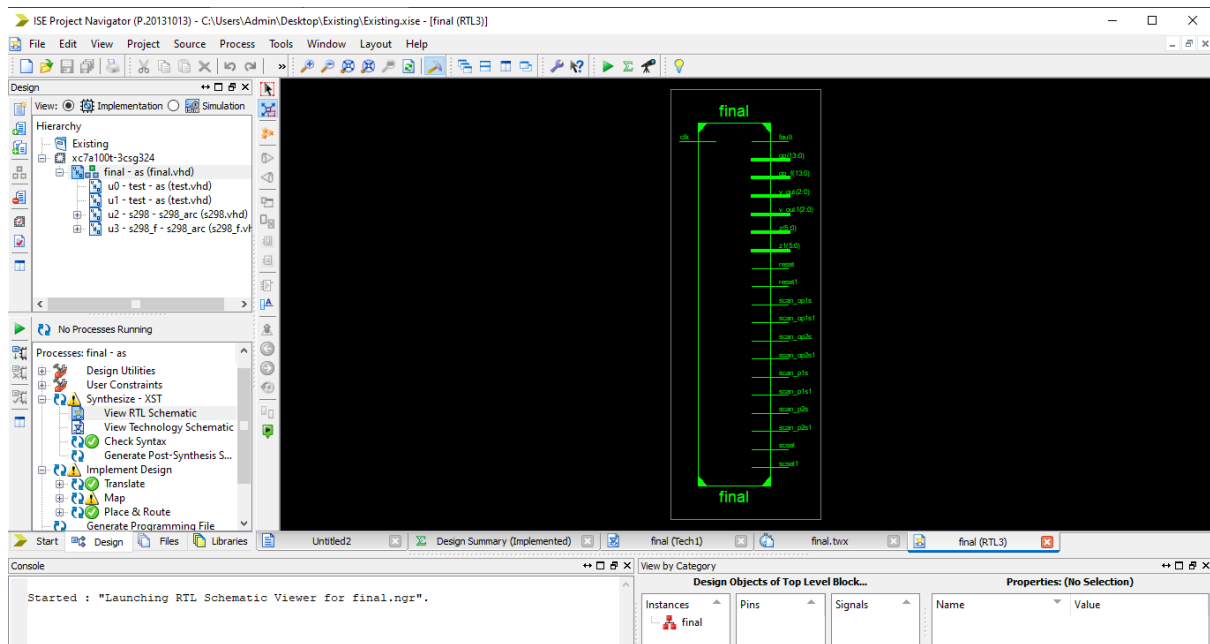


**Fig 5.10 RTL schematic final**

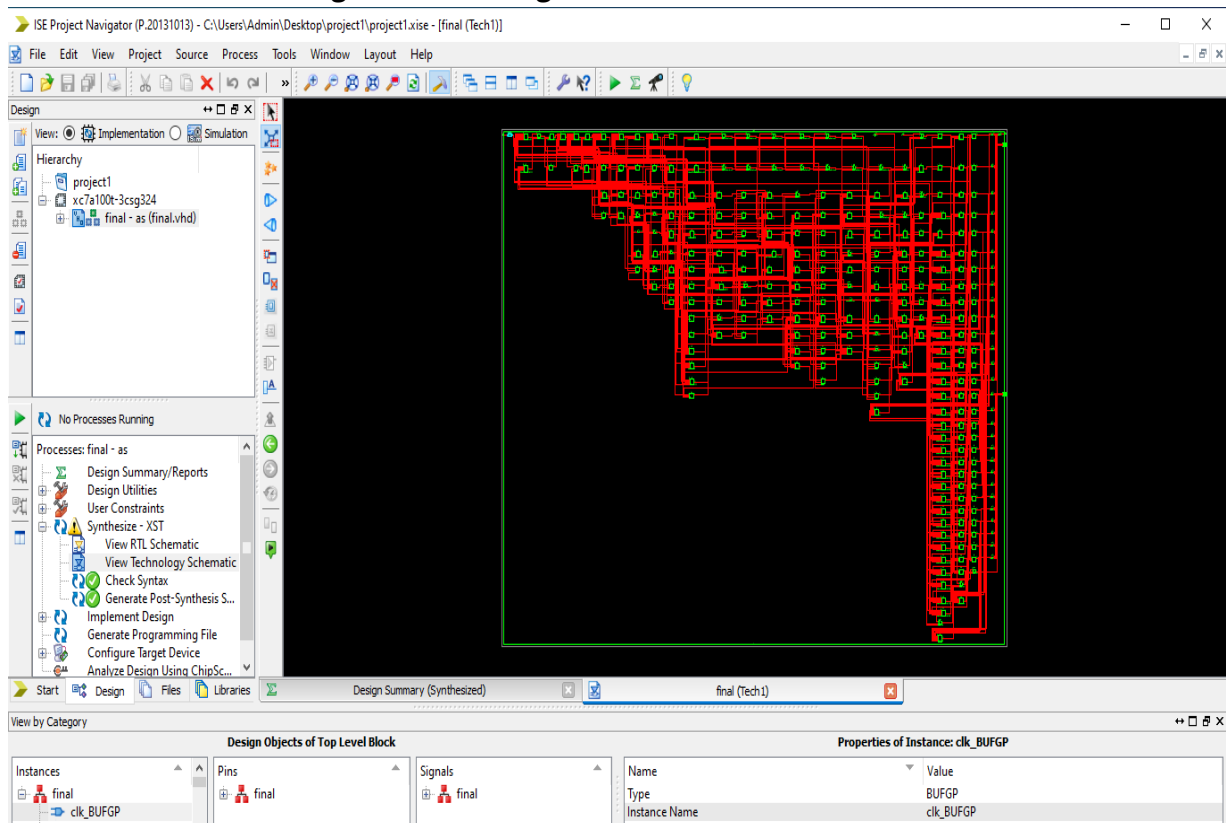
It views a Register Transfer Level graphical representation of your design. The RTL viewer shows the pre-synthesis schematic.



Closer view of technology schematic of ISAC 29 benchmark circuit has been displayed in the project navigator.

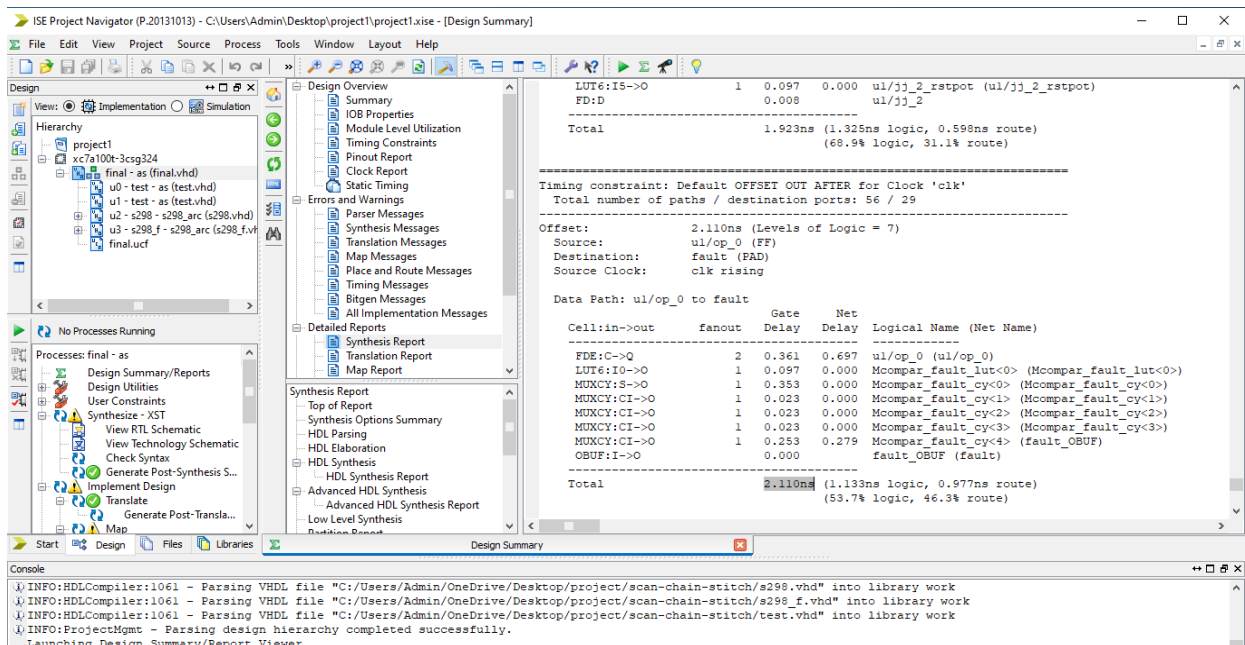


**Fig 5.12 Existing method RTL schematic**



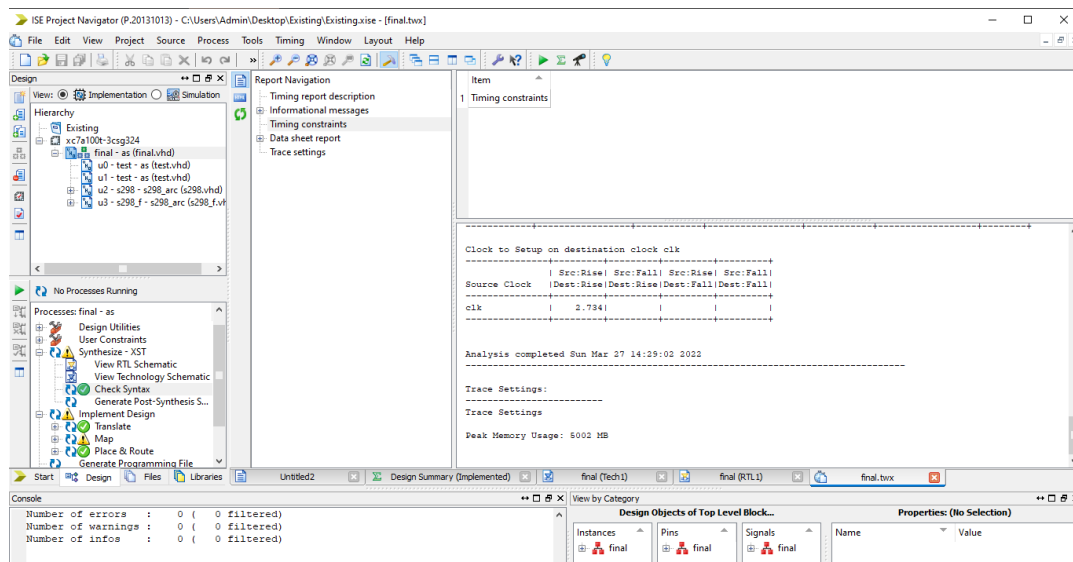
**Fig 5.13 Technology schematic**

Technology View shows you the representation of your design in terms of logical elements means like LUTs, buffers, I/Os, and other technological components.



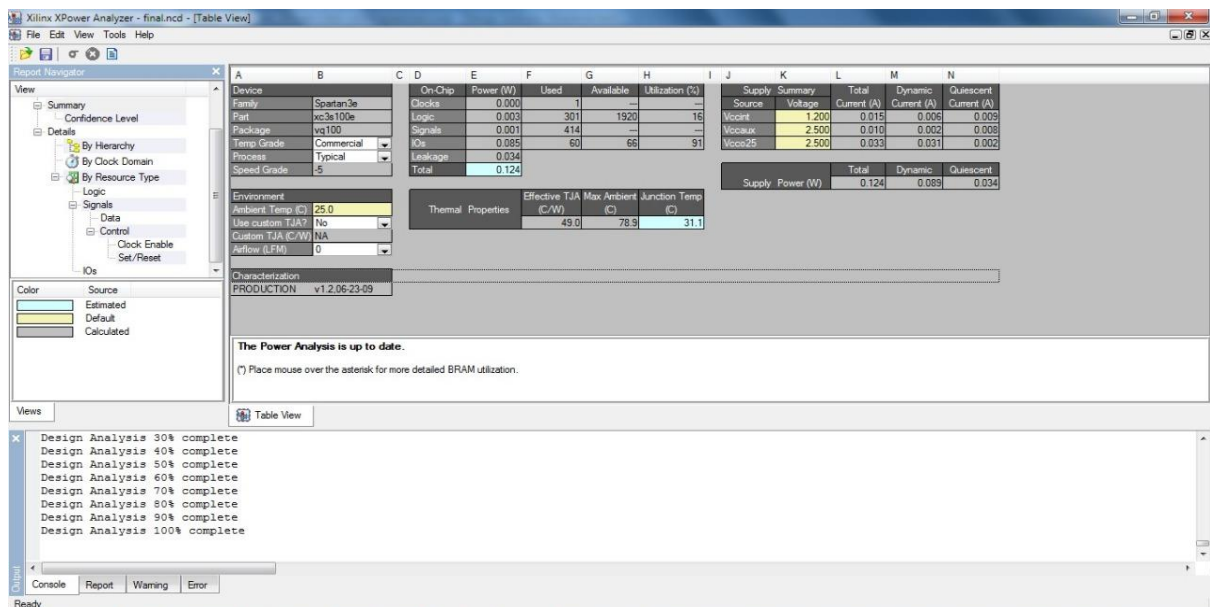
**Fig 5.14 Transition time of scan chain stitching**

Clock signal is used for controlling all the FFs in the chain during the shift phase and the capture phase. An arbitrary pattern can be entered into the chain of flip-flops, and the state of every flip-flop can be readout. Which has a transition time of 2.11ns.



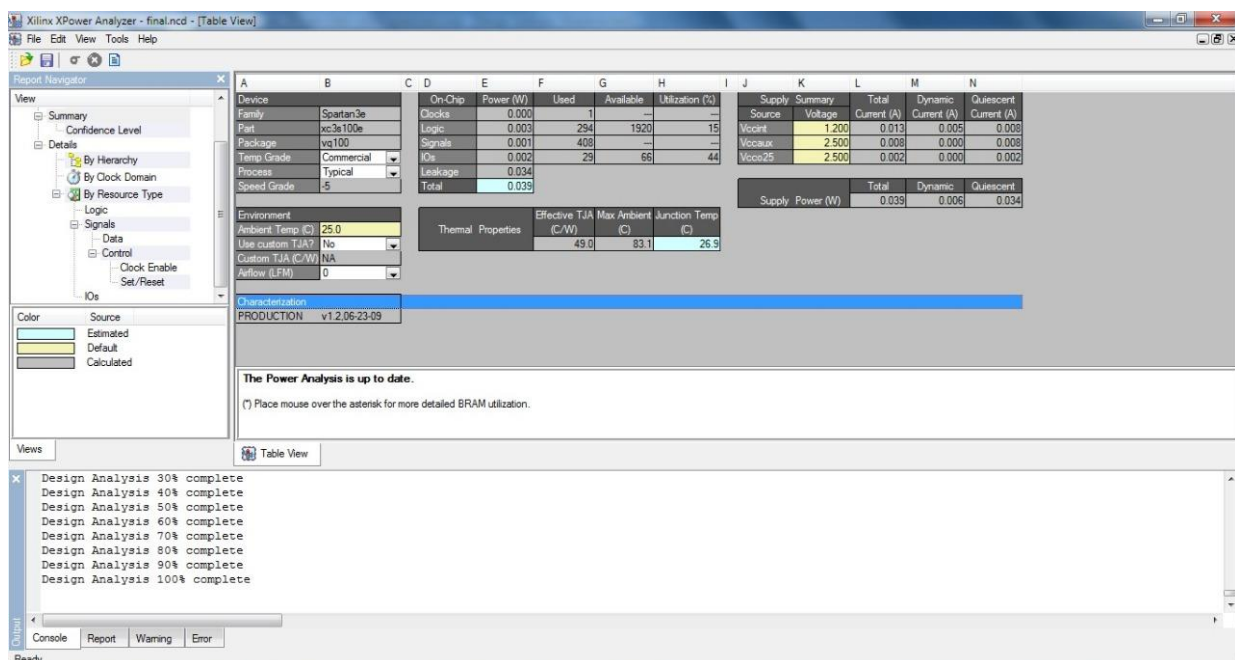
**Fig 5.15 Clock to setup on destination existing method**

A scan enables pin is a special signal that is added to a design. When this signal is asserted, every flip-flop in the design is connected into a long shift register.



**Fig 5.16 Power Analyser of the existing method**

It shows a significant total power of 0.124 with 49.0(C/W) Effective thermal resistance.  
At a junction temperature of 31.1 Centigrade.



**Fig 5.17 power analyzer of Scan chain stitched method**

There is an evident drop in power from a total of 0.124W to 0.039W respectively at different junction temperatures. There is a significant level drop of power that has been analyzed in the scan chain procedure.

## **CHAPTER 6**

### **SUMMARY AND CONCLUSION**

#### **6.1 SUMMARY**

POWER dissipation during test mode can be much higher with respect to that in functional mode since the input vectors in functional mode are generally strongly correlated with respect to the statistically independent consecutive input vectors during. Thus, the test power could be twice as high as the power consumed during the normal mode. Test power is a major design issue to increase battery life in portable electronic devices that incorporate self-test (BIST) circuitry for periodic self-testing. It is also important to improve test cost since reduced test power of a module allows parallel testing of multiple embedded cores.

Increasing peak power is likely to create noise problems in a chip, causing the supply voltage to drop. Reducing peak and average power during testing helps increase test reliability and improve yield.

Therefore, important to ensure a reduction in power dissipation during the test mode. Scan architectures represent the prevalent Design for Testability (DFT) approach to test digital circuits.

#### **6.2 CONCLUSION**

VLSI, which is part of the electronics industry, is also growing according to the developments in the electronics industry. Protocols like Bluetooth, Wifi, 5G, Zigbee, Thread, etc will evolve and therefore chip designers will create new IPs, Chips, and SoCs to support the new protocols.

ICs that are manufactured are not flawless in nature. They do inherit a certain extent of faults and implementing them in a hardware component leads to failure of the circuit. To check and rectify these faults is the job done by testability designers. Out of many profound methods, Scan chain stitching of the LFSR helped with maximum result coverage.

As an endeavor instead of stitching scan cells in alphabetical order, they are placed in a tested manner to reduce transition. In previous methods reduction of test power

during normal mode is mostly considered but functional mode power dissipation is also a major concern since the input vectors during functional mode are usually strongly correlated compared to statistically independent consecutive input vectors during testing.

An increase in logic gates these days inflicts an increment in the size of logic components. This ultimately leads to fault production in the circuit. The test power could be twice as high as the power consumed during the normal mode. Test power is an important design concern to increase battery life in hand-held electronic devices that incorporate built-in self-test (BIST) circuitry for periodic self-test. It is also important to improve test cost since reduced test power of a module allows parallel testing of multiple embedded cores. Not many methods focus on transition rate and fault coverage as a whole. Where they both are achieved using planned calculation.

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