

PERFORMANCE ANALYSIS OF AN EFFICIENT MAC UNIT FOR DIGITAL APPLICATIONS

Submitted in partial fulfillment of the requirements for the award of Bachelor of
Engineering Degree in Electronics and Communication Engineering

By

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(DEEMED TO BE UNIVERSITY)

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MAY - 2022



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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the Bonafide work of **M. ABINAYA** (38130003) and **M. SONALI** (38130211) who carried out the project entitled **"PERFORMANCE ANALYSIS OF AN EFFICIENT MAC UNIT FOR DIGITAL APPLICATIONS"** under my supervision from June 2021 to May 2022.

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DECLARATION

We, **M. ABINAYA (38130003)** and **M. SONALI (38130211)** hereby declare that the Project Report entitled “**PERFORMANCE ANALYSIS OF AN EFFICIENT MAC UNIT FOR DIGITAL APPLICATIONS**” done by us by the guidance of Ms.G.RAJALAKSHMI,M.E.,(Ph.D) is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering Degree in Electronics and Communication Engineering.

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1.

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ACKNOWLEDGEMENT

We are pleased to acknowledge our sincere thanks to Board of Management of **SATHYABAMA** for their kind encouragement in doing this project and for completing it successfully. We are grateful to them.

We convey our thanks to **Dr. N. M. NANDHITHA, M.E., Ph.D., Dean, School of Electrical and Electronics Engineering** and **Dr. T. RAVI, M.E., Ph.D., Head of the Department, Department of Electronics and Communication Engineering** for providing us necessary support and details at the right time during the progressive reviews.

We would like to express our sincere and deep sense of gratitude to our Project Guide **Ms. G. RAJALAKSHMI, M.E., (Ph.D), Assistant Professor, Department of Electronics and Instrumentation Engineering** for her valuable guidance, suggestions and constant encouragement paved way for the successful completion of the project work.

We wish to express our thanks to all teaching and Non-teaching staff members of the **Department of Electronics and Communication Engineering** who were helpful in many ways for the completion of the project

ABSTRACT

In this project, a low power and high speed MAC (multiply-accumulate) unit has been proposed. MAC unit performs a major role in DSP applications. Adder and multiplier are the two important blocks when it comes to MAC unit, therefore selecting the appropriate one is required to design an efficient MAC unit. Hence, in this project we have proposed a 16-bit MAC unit using 4-bit Ripple Carry Adder and 4x4-Vedic Multiplier. The MAC unit is simulated using HSPICE Synopsys. The delay of all the circuits in the MAC unit was found using COSMOSSCOPE. The MAC implementations of proposed and existing designs are compared with each other for the delay and power. Experimental results shows that the proposed MAC design using vedic multiplier and ripple carry adder significantly reduces the circuit delay and high power consumption thereby resulting in high speed and performance.

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LIST OF ABBREVIATIONS

VLSI	Very Large Scale Integration
IC	Integrated Circuit
HDL	Hardware Description Languages
TLM	Transaction Level Model
DUT	Design Under Test
RTL	Register Transfer Level
DFT	Design For Test
ULSI	Ultra Large Scale Integration
MAC	Multiply-Accumulate Unit
DSP	Digital Signal Processing

CHAPTER 1

INTRODUCTION

1.1 VLSI

Very Large Scale Integration (VLSI) is a process of creating an IC (Integrated Circuit) by combining millions and billions of transistors onto a single chip. VLSI is one of the reputed domain in semiconductor industry. VLSI lets IC designers to add electronics circuits like, RAM, ROM, CPU and other logics in a single chip. VLSI can be implemented using HDL (Hardware Description Language) like VHDL and Verilog. The base of VLSI to attain the Progression that it has today is Moore's Law. According to Gordon Moore, the Transistors in a chip doubles every two years, thereby increasing the performance and functionality of the devices.

VLSI mainly focuses on,

- Low power consumption
- Reduction in area
- High performance and speed.

1.2 VLSI DESIGN FLOW

1. **SPECIFICATION:** This specifies the complete information about the circuit that has to be built. Specifications are defined by architects. They interact with the marketing team and collect information from numerous consumers about the previous versions of the system. The specification should state the new features, requirements from consumers and also the key features to compete with the competitor.

2. **ARCHITECTURE:** Experienced architects design the architecture of the system to be made. It is basically a block diagram to represent the number of IP's and also the interconnection between them. The engineers will create the different components to be inserted and the technical lead will put them together and create a subsystem.
3. **BEHAVIORAL MODEL:** To verify the functionality and performance before the implementation, the design architect creates TLM(Transaction Level Model). It is non-synthesizeable. TLM is created to verify the performance of the chip during simulation and we even add the software to see how the chip will behave during simulation. During verification the TLM will be used as a reference model. The reference data will be collected from the TLM and the output will be collected from the DUT.
4. **RTL CODING:** RTL – Register Transfer Level. The data will be transferred from register to register, hence it is called as RTL. RTL Coding is for synthesizable model, when it comes to this, we look for the area and frequency in which the design is going to operate. HDL will be used to write a RTL code. Two things to keep in mind while writing RTL code,
 - Synthesizable Subset: We cannot use every constructs in the language when it comes to RTL as the language is pretty huge and not every construct is synthesizable.
 - Coding Style: Different logic expects different coding styles so we need to understand the difference.
5. **VERIFICATION:** This step is to prove whether the design is working as expected or not. To check the design we have to write another code called as the Test Bench. It generates Stimulus. The stimulus is fed into the DUT which in return will produce output, then we compare the output with the expected value. There are three types of verification,

- **White Box Verification:** White box testers dig into the internal structure and fix the source code of the Software.
- **Black Box Verification:** Black box testers make sure everything is fine with the interface and functionality. They check how the transformation is happening between the input and the output.
- **Grey Box Verification:** Grey box testers deal with both white and black box at the same time.

6. SYNTHESIS: Here, the RTL code will be converted into netlist (The entire design will be based on gates). Basically, a netlist consists of a list of electronic components and their interconnections. The chips are either based on nand or nor. Mostly Engineers chose it to be nand as it consumes less energy. Netlist describes the number of gates needed approximately, which will help in deciding the area and frequency.

7. GATE LEVEL SIMULATION: The gate level netlist and the RTL will be cross checked with the help of equivalent checkers as there might be some bugs. The test bench that we created for the RTL should be in such a way that it can be reused again. Here, instead of the RTL, the test bench and the gate level netlist will run the simulation and the output should be same for both.

8. DFT INSERTION: DFT – Design For Test. In DFT, we replace the flip flops in the RTL by scan flip flops to identify if we have any short or open circuit within the chip. Basically DFT runs in two modes,

- **Normal Mode** - In normal mode, the data transfers from one flip flop to combinational circuit and to other flip flop as a normal RTL would do.
- **Test Mode** – In test mode, it skips the combinational circuit and goes from flip flop to flip flop just like a shift register.

9. FLOOR PLANNING AND PLACEMENT: In Floor Planning we will decide the shape of the chip, either square or rectangle. Based on the shape we have to decide where the components has to be placed efficiently keeping the routing possibility in mind. We have to think how efficiently we can utilize the space. In Placement, we decide how the routing is going to be.

10.CLOCK TREE SYNTHESIS: In this, the clcok will be connected to varioud flip flops. When the clock reaches different flip flop at different timing then the issue is called as clock skew. So inorder to avoid the clock skew various methods will be followed. They are,

- H – Tree
- X – Tree
- I – Tree

The flip flops will be arranged neatly with same wire length and the clock will be reached at the same time, thereby avoiding the clock skew. In clock tree synthesis, we look for how to remove clock skew and how to insert clock buffer.

11.ROUTING: Here, components are interconnected and are placed well in the chip and the clock tree sysnthesis will also be done. We should make sure that there is no open or short circuit while making connections.

1.3 RECENT TRENDS AND FUTURE

Following of Moore's law has always been the biggest trend when it comes to VLSI. Bigshot companies and foundries still make sure that they follow the Moore's law inorder to compete with the ongoing technology and demands of the consumers.

Some of the trends in VLSI are,

Fabrication: The fabrication process is reaching new levels each day. The semiconductor industry reached its new milestone of designing 5nm chips which is a huge step towards the future.

Architecture: VLSI and ULSI will be taking a big turn in near future as all the semiconductor industries are planning on incorporating AI and Machine Learning in chips for high performance, cloud infrastructure and also to accelerate computing.

When it comes to the future of semiconductor industry or VLSI, we can deliberately state that as long as there is a need for IC's then the VLSI industry will withstand. We cannot even design cloud infrastructure without the help of chips. So the future of nm technology is going to reach new horizons.

1.4 ORIGIN OF IDEA

Our team has always been fond of VLSI. MAC Unit plays an important role in DSP Applications and we were intrigued by the idea of incorporating vedic multiplier along with ripple carry adder in order to design a low power and high speed MAC Unit.

CHAPTER 2

LITERATURE SURVEY

2.1 LITERATURE SURVEY

A reasonable amount of designs has been made for MAC. Although the techniques and algorithms used in the projects has been proven to reduce any one of the conflicting requirements like area, speed, power, etc., we have used an incorporation of ripple carry adder and vedic multiplier in order to reduce the power and delay.

Shraddha Lad and Varsha S. Bendre (2020) have proposed a paper for Design and Comparison of Multiplier using Vedic Sutras where they focused on enhancing the speed of multiplication. The sole purpose of this paper is to achieve best results for area, speed, and power parameters for each of the sutras. Design of four 16-bit sutras is carried out using Verilog language. Here, all the sutras are evaluated on basis of area, speed & power with existing research work.

Rakesh H. M and G. S. Sunitha (2020) have proposed a paper for Design and Implementation of Novel 32-bit MAC Unit for DSP Applications. This paper explains about the 32-bit MAC unit consisting of Vedic Multiplier using Urdhva Tiryakbhyam sutra and Efficient adder circuit using Modified Weinberger adder technique. From comparative analysis, the MAC unit designed was found to be proficient in terms of delay and energy consumed.

Akella Srinivasa Krishna Vamsi and S R Ramesh (2019) have proposed a paper for An Efficient Design of 16 Bit MAC Unit using Vedic Mathematics. This paper presents the need of designing an efficient multiplier in order to design the MAC Unit in an appropriate way as multiplier plays an important role when it comes to MAC Unit.

They concluded by comparing the existing and proposed work where they finally proved that the proposed design shows improvement in area and delay.

Aditi Chhabra and Jasdeep Dhanoa (2020) have proposed a Design Approach for MAC Unit using Vedic Multiplier. This paper elaborates about the different varieties of Vedic Multiplier and also the types of array multiplier. Here, the MAC Unit was designed using Artificial Neural Networks (ANN). The drawback of this is that MAC Unit composed of ANN algorithm tends to require additional adders and multipliers, so they focus on approaching a more suitable adder and multiplier to reduce the circuits required.

Ashish Bagwari and Isha Katna have proposed a paper on Low Power Ripple Carry Adder Using Hybrid 1-Bit Full Adder Circuit. This paper describes the role of Adder in most of the applications of electronics. They focused on designing a full adder circuit with low power consumption and high performance. Hence full adder with different topology than the existing one has been used to design such adder.

2.2 PROBLEM STATEMENTS FROM SURVEY

Many algorithms and works have been proposed to design an efficient MAC Unit. No matter what we do, at the end every proposed work will lack a few features. Even though the drawbacks of one project have been compensated by the other, there still are no work found to compromise all the conflicting requirements as a whole as it is impossible to do so when it comes to electronics.

Conflicting requirements such as area, speed, power and performance plays an important role when it comes to any type of circuit. Focusing on achieving all that at once have been proven faulty as it may increase the size of the circuit which is something developers avoid. Furthermore, the design can become complex. Hence focusing on designing selected requirement is appropriate.

2.3 OBJECTIVE

The objective of this project is to design a MAC Unit with low power and delay thereby increasing the speed and performance of the design. The procedure might be quite complicated as in order to select the desired adder and multiplier for the project, numerous survey's has to be conducted. In order to design the required adder, survey's of several full adders was needed and for multipliers, survey's on Vedic mathematics and sutras came in handy. Once the required adder and multiplier is selected, we decided the searching for the appropriate accumulator that can be incorporated with the selected adder and multiplier in order to design an efficient MAC Unit. Once the design is created, the comparison between the proposed and existing designs has to be taken thereby concluding the project.

- Ripple Carry Adder was designed using Hybrid Full Adder.
- Vedic Multiplier is designed on the basis of Urdhva Tiryagbhyam Sutra.
- Appropriate Accumulator is selected, thereby completing the design of MAC Unit.
- The final design was simulated using HSPICE Synopsys.
- The delay of all the circuits used in the MAC Unit was found by using COSMOSSCOPE.

CHAPTER 3

AIM AND SCOPE OF THE PRESENT INVESTIGATION

3.1 PROPOSED METHODOLOGIES

- Our proposed work integrates all the requirements to reduce the power and delay of our design.
- Ripple Carry Adder is used to achieve our desired goal.
- Vedic Multiplier when used with Ripple Carry Adder shows significant result in regards to delay and power.

3.2 ARRAY MULTIPLIER

An array multiplier is a digital combinational circuit that uses an array of full adders and half adders to multiply two binary values.

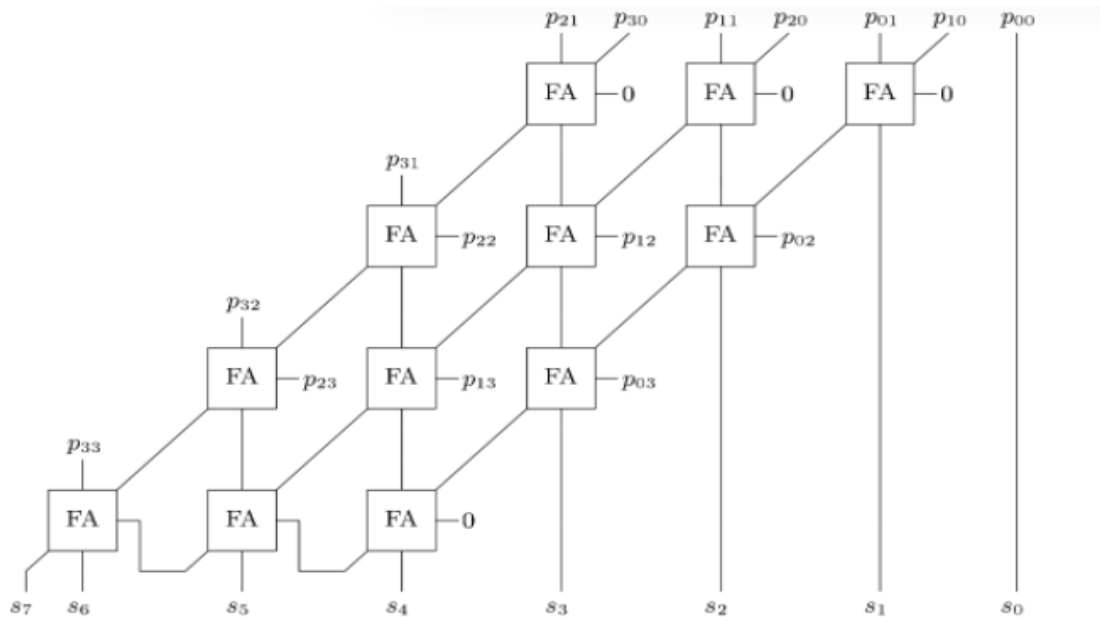


Fig: 3.1: Array Multiplier

This array is used to add the numerous product keywords involved in a near-simultaneous manner. Before the Adder array, an array of AND gates is utilised to produce the various product terms.

Because of its regular construction, the array multiplier is well-known. The add and shift algorithm is used in the multiplier circuit. The multiplicand is multiplied by one multiplier bit to obtain each partial product. The incomplete products are then added and shifted according to their bit ordering. A conventional carry propagate adder can be used to execute the addition. There are $N-1$ adders needed, where N is the multiplier length.

3.3 CARRY SAVE ADDER

Carry-save adder is a sort of digital adder that can quickly add three or more binary values together. It's unique from other digital adders in that it outputs two (or more) values, which can be added together to get the answer to the original summation.

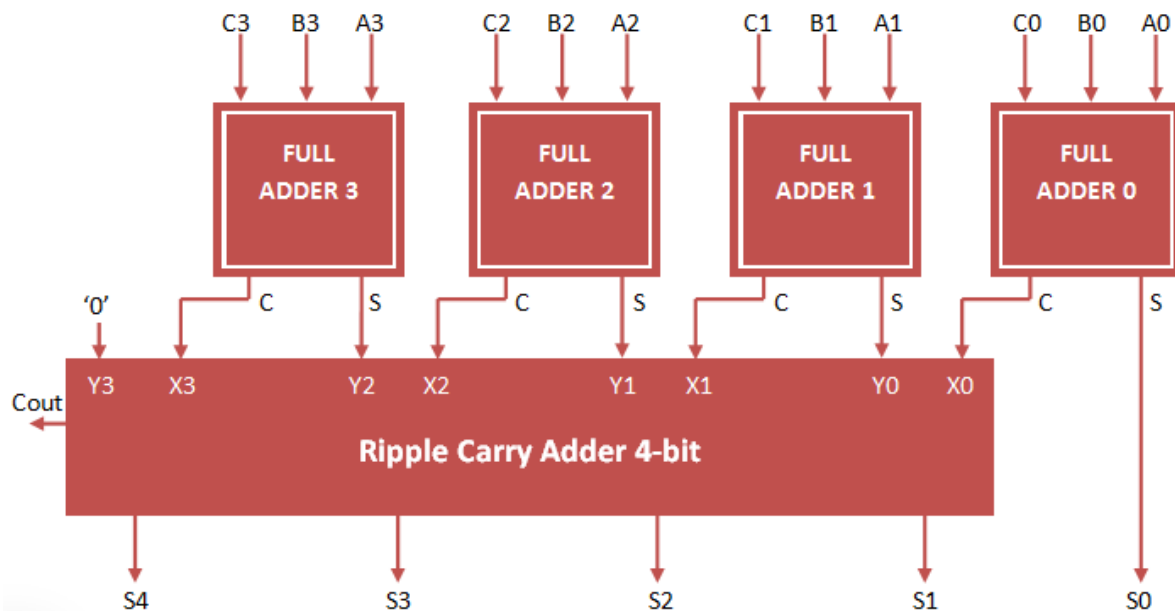


Fig: 3.2: Carry Save Adder

Because a binary multiplier includes the addition of two or more binary numbers after multiplication, a carry save adder is commonly utilised. A huge adder that uses this technique will actually be much faster than adding those numbers manually.

3.4 DSP APPLICATIONS

- DSP has a high level of precision. As a result, DSP-based filters have more control over output precision.
- Compared to an analog counterpart, it is less expensive.
- Reconfiguration is simple, requiring only the flashing of code or a DSP program after updates are needed.
- The digital circuits can be easily replicated in large quantities at a cheaper cost.
- There is no problem with cascading a digital system.
- Digital circuits are less affected by component value tolerances.
- Because digital signals can be processed offline, DSP is easily transportable.
- Allows signals to be sent over a long distance.
- Multi-directional transmission is a breeze with DSP.
- It's easier to convert human audio and video signals, as well as other messages, into machine language using DSP.

3.5 USE OF MAC IN DSP APPLICATIONS

- One of the capable processing units is digital signal processing (DSP). In DSP systems, the Multiply-Accumulate Unit (MAC) is the fundamental computational kernel.
- The MAC unit controls the whole system's power and speed, and it is always in the critical path.
- It is critical to develop high-speed, low-power MAC in order to leverage DSP in

the future.

- Signal processing is used in a wide range of situations. Object tracking, environmental monitoring, surveillance, and many more applications use infinite impulse response filtering (IIR), finite impulse response filtering (FIR), and Kalman Filter (KF).
- A low-power MAC unit would undoubtedly be the market leader. MAC architectures with great computational performance and low power consumption have been attempted by several researchers.

CHAPTER 4

MATERIALS AND METHODS USED

4.1 CIRCUITS USED FOR THE DESIGN

MAC unit is one of the fundamental blocks when it comes to DSP applications. MAC unit stands for multiply and accumulate unit. As the name suggests, it does multiplication and accumulation. Adder, multiplier and the accumulator are the main blocks when it comes to the MAC design. Apart from the three main blocks, the circuits which are used to design these three blocks are also considerable important.

4.1.1 AND GATE

A logic gate with two or more inputs and a single output is known as an AND gate. The logic multiplication rules are used to operate an AND gate. If any of the inputs is low (0), the output is also low in this gate. When all of the inputs are high (1), the output will be high as well. An AND gate can have any number of inputs, although the most common are two and three input AND gates.

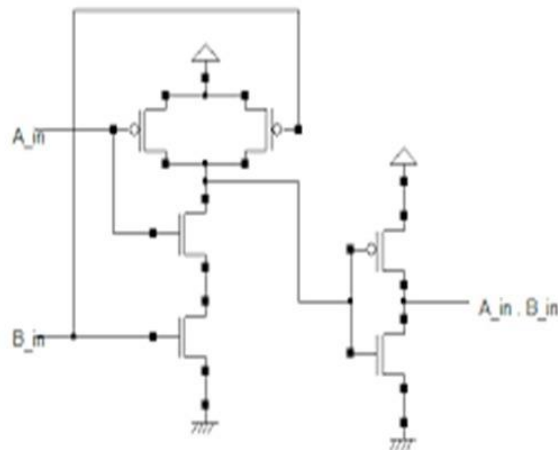


Fig: 4.1: CMOS Diagram of AND Gate

4.1.2 HALF ADDER

A half adder is a sort of adder, which is an electrical circuit that adds numbers. The half adder can add two single binary digits and output the result together with a carry value. It has two A and B inputs, as well as S (sum) and C (outputs) (carry). A XOR logic gate and an AND logic gate are used in the most frequent representation.

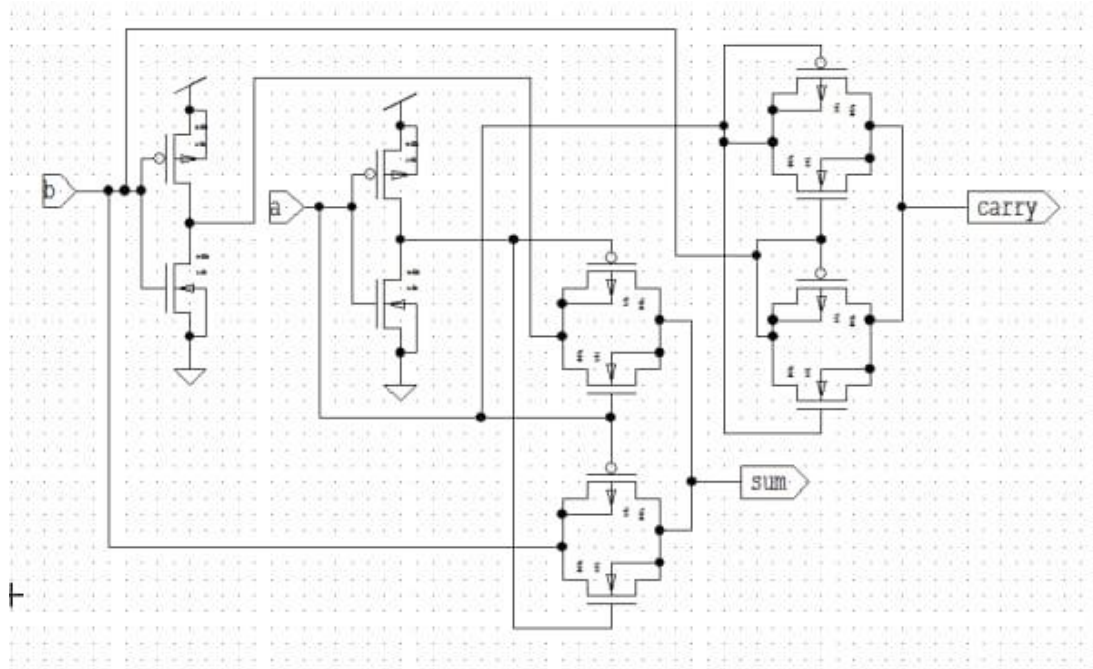


Fig: 4.2: CMOS Diagram of Half Adder

4.1.3 FULL ADDER

The adder is one of the main block in the MAC unit. We have used hybrid full adder for our design which is same as the normal full adder with 3 inputs A,B,C and 2 outputs SUM, Cout. Used exclusively in VLSI systems as the advanced circuits, including microprocessors, digital communication gadgets and DSP processors.

In our proposed work we have removed certain nodes in order to reduce area and power consumption. Our proposed hybrid full adder is deployed by both pass transistor logic(PTL), and CMOS logic.

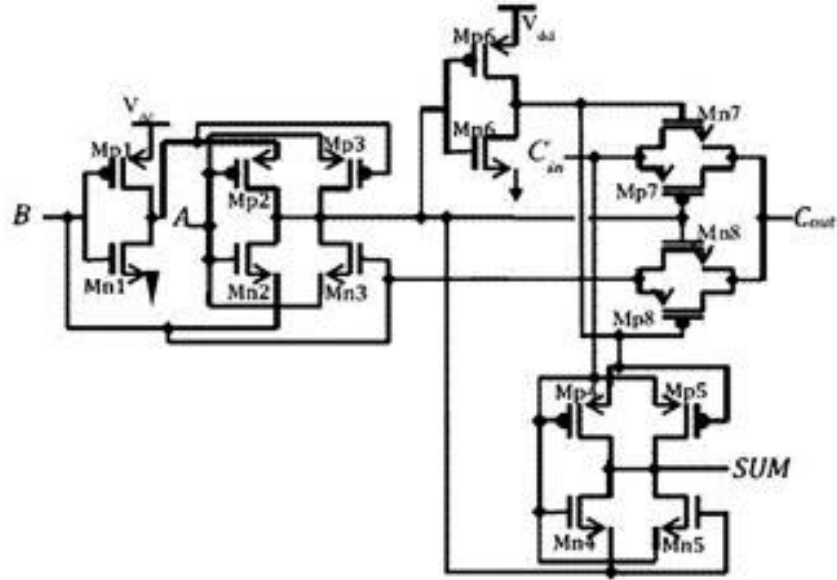


Fig: 4.3: CMOS Diagram of Hybrid Full Adder

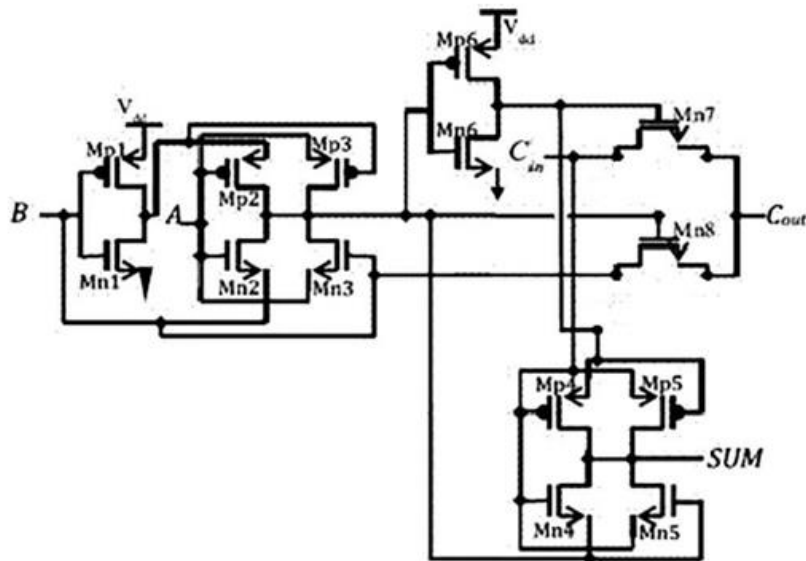


Fig: 4.4: CMOS Diagram of Proposed Hybrid Full Adder

4.1.4 FLIP FLOP

Flip-flop is an storage elements where data is stored in memory. It is a sequential circuit. We have preferred to use D flip flop for our design. It has single input, a clock and an output. The output of the flip flop truly depends on the clock pulse (rising or falling edge). Flip flop is one of the important blocks in the accumulator, in order to store accumulated values. The below diagram is our proposed flip flop.

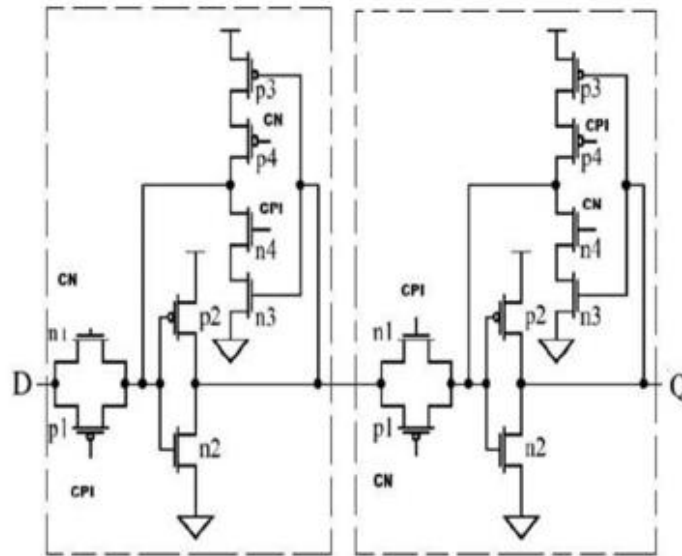


Fig: 4.5: CMOS Diagram of Flip Flop

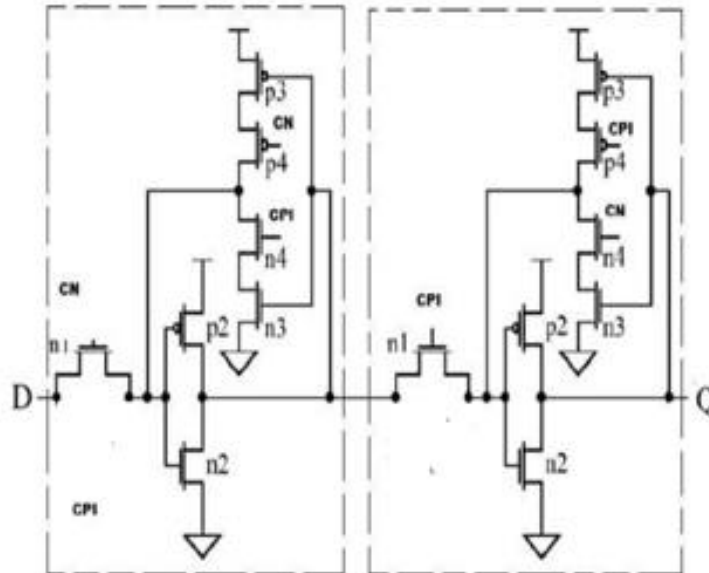


Fig: 4.6: CMOS Diagram of Proposed Flip Flop

4.1.5 RIPPLE CARRY ADDER

The purpose of Ripple Carry Adder is the addition of two n bit binary numbers. It is a combinational circuit. Ripple carry adder is designed by cascading n bit full adders in which each full adder has 3 inputs and two outputs. RCA is chosen because it is efficient in terms delay. Since our objective is to reduce power and delay after several surveys we have decided to use ripple carry adder for our MAC design. We have used 4 bit full adder four bit full adder for our design, where $A_0, B_0, A_1, B_1, A_2, B_2, A_3, B_3$ AND C_0 (carry in) are the inputs and S_0, S_1, S_2, S_3 and C_4 (carry out) are the outputs.

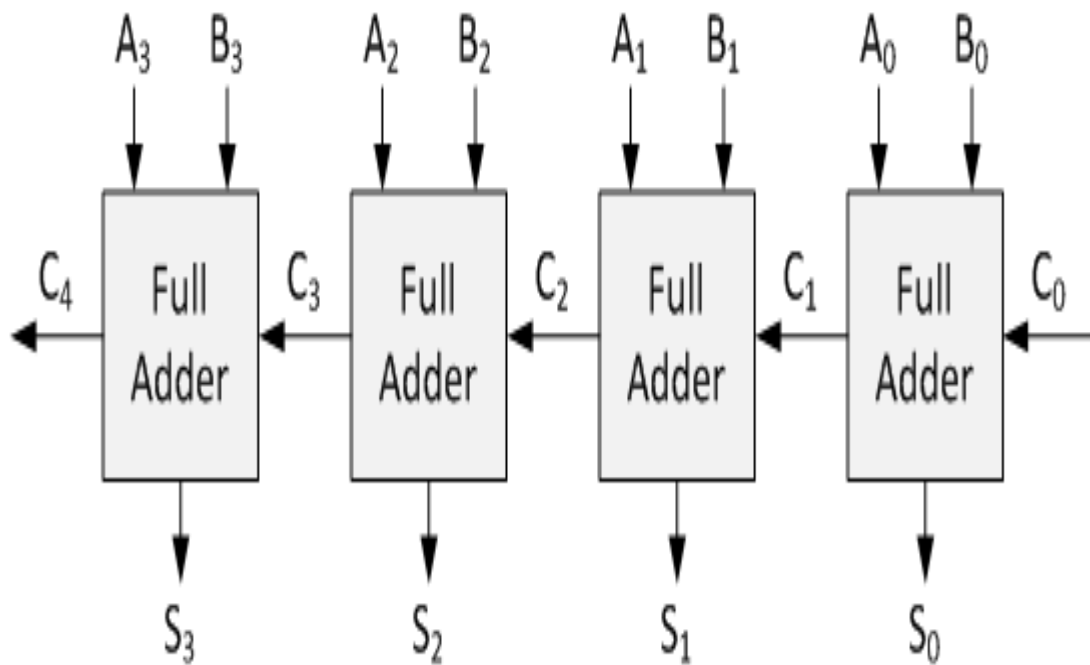


Fig: 4.7: Block Diagram of 4-Bit Ripple Carry Adder

4.1.6 VEDIC MULTIPLIER

Vedic Multiplier is an essential block in the MAC unit. It is a multiplier which based on vedic mathematics. Vedic mathematics is nothing but an algorithm or formulae which is based on sutras. There are 16 sutras in existence, out of which we have decided to use Urdhva Tiryakbhyam . Urdhva Tiryakbhyam literally means vertically and crosswise where the products are generated by the concurrent addition of partial products.

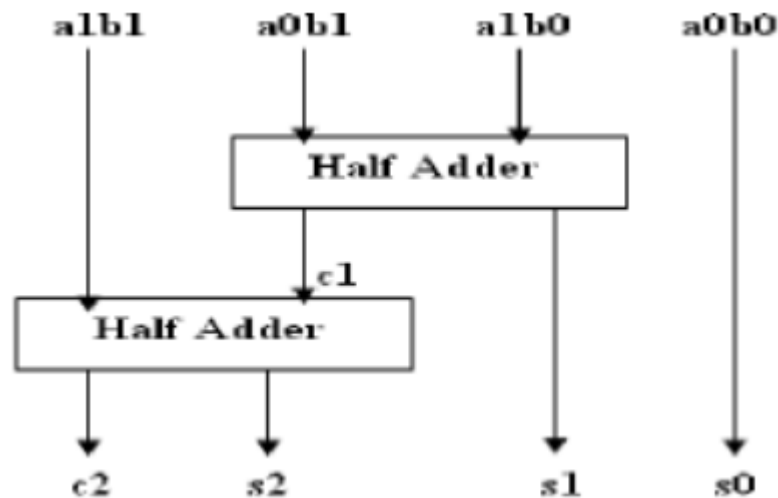


Fig: 4.8: Block Diagram of 2x2 Vedic Multiplier

We have chosen vedic multiplier over other multipliers in order to speed and performance of our MAC unit. When combined with ripple carry adder, the vedic multiplier which is based on Urdhva Tiryakbhyam works well in terms of reduction in delay and power.

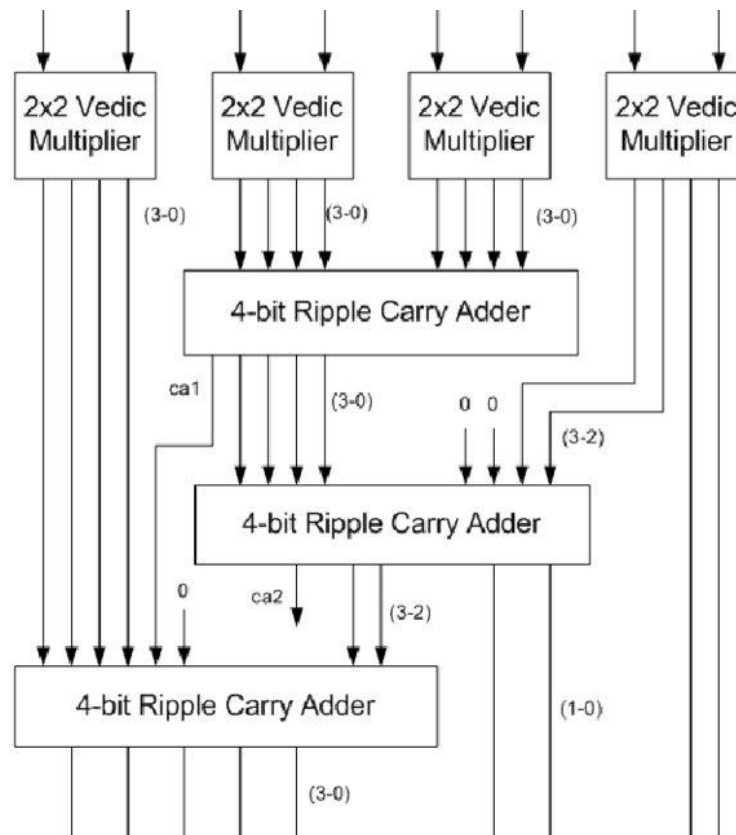


Fig: 4.9: Block Diagram of 4x4 Vedic Multiplier

4.1.7 ACCUMULATOR

The final block of the MAC unit is the accumulator. An accumulator is a register which acts as a storage element for arithmetic and logic datas. It is a sequential circuit. Accumulator is mainly used for adding a sequence of numbers. It consist of adder and flip flop where the output of flip flop is feedback as the one of the inputs of adder. The output accumulator is the output MAC design. The output of adder S (sum) acts as the input to the flip flop.

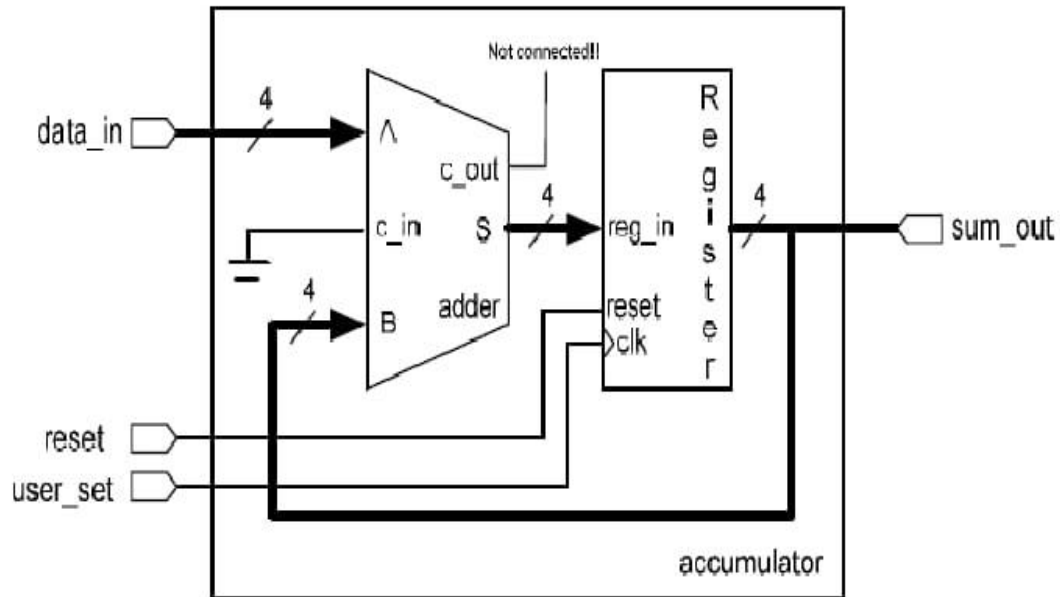


Fig: 4.10: Block Diagram of Accumulator

4.1.8 MAC UNIT

MAC unit plays an important role in DSP applications such as Fast Fourier Transform(FFT), FIR Filters, Multiplying and Accumulating as well as several DSP algorithms. MAC unit consists of three fundamental blocks which are namely multiplier, adder and accumulator. The elementary operations of the MAC unit is multiplication and accumulation.

Our MAC unit consists of Vedic multiplier, ripple carry adder and accumulator. The outputs of the vedic multiplier acts as the inputs to the ripple carry adder, the outputs of ripple carry adder acts as the inputs to the accumulator, and the output of accumulator is the final output of the MAC unit.

We have used ripple carry adder in order to reduce high power consumption and delay which is common in during the carry propagation of addition. Vedic multiplier proves to be the best choice when it comes to power and delay calculations.

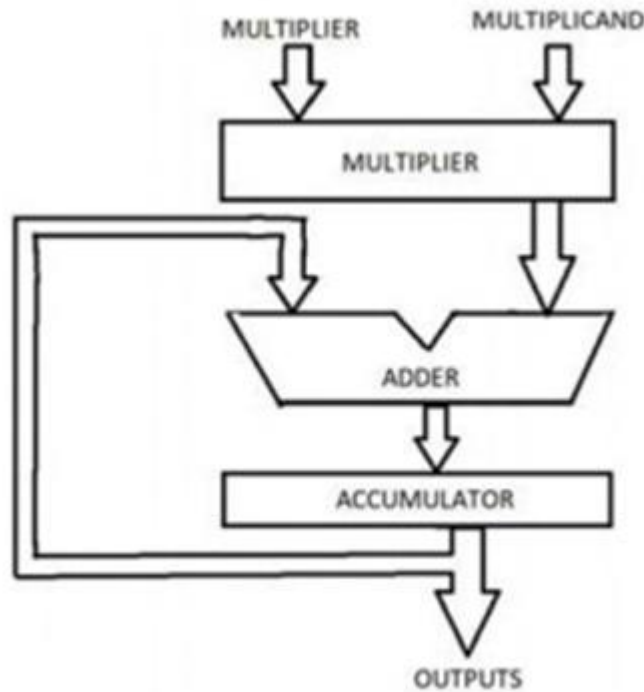


Fig: 4.11: Block Diagram of MAC Unit

4.2 SOFTWARE USED

The MAC unit was simulated using HSPICE Synopsys. The delay of all the circuits in MAC unit was found by using COSMOSSCOPE. The result derived from both the softwares has been used for calculating the PDP (Power-Delay Product) at the end.

4.2.1 HSPICE SYNOPSYS

HSPICE Synopsys is the most widely used, trustworthy, and comprehensive simulation software in the business. HSPICE is the software used for accurate circuit simulation in the industry and foundry for MOS device models and cutting-edge simulation and analysis techniques.

Cells and transistors are widely used in analog, RF, and mixed-signal IC design, characterization of memory and signal integrity of chips, packages, boards, and backplanes simulation of a circuit.



Fig: 4.12: HSPICE Simulation Tool

4.2.2 COSMOSSCOPE

CosmosScope is a graphical waveform analyzer application that lets you examine and evaluate simulation results as waveforms on graphs or numbers in lists.

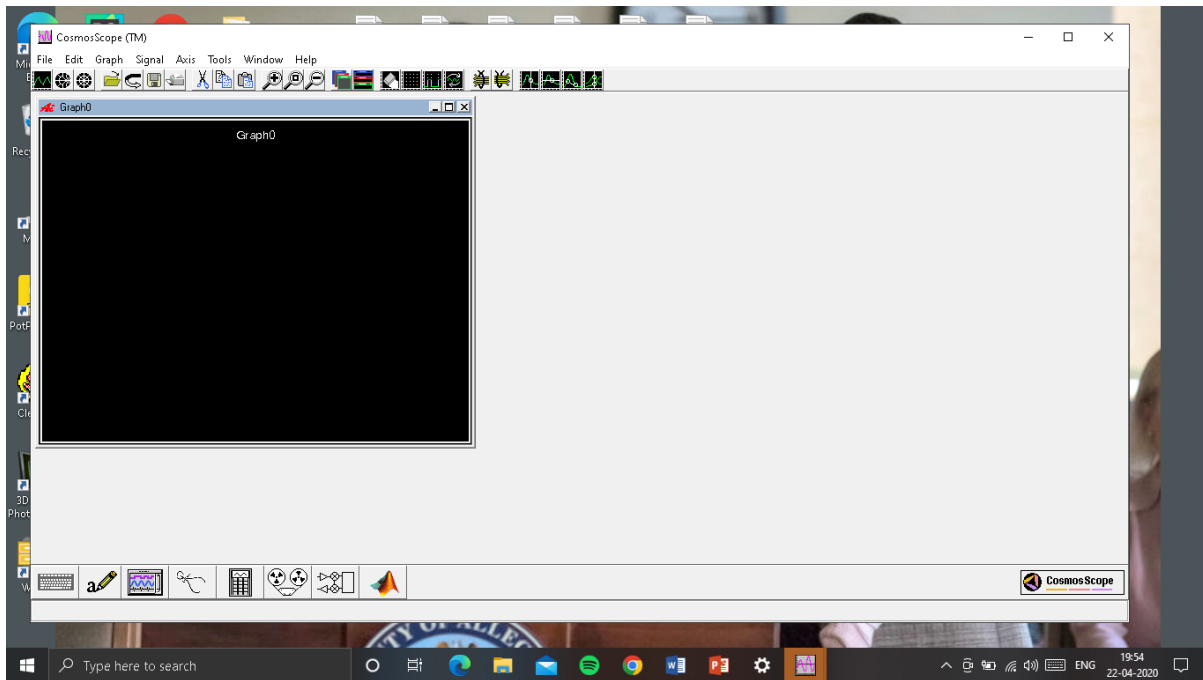


Fig: 4.13 Cosmosscope Window

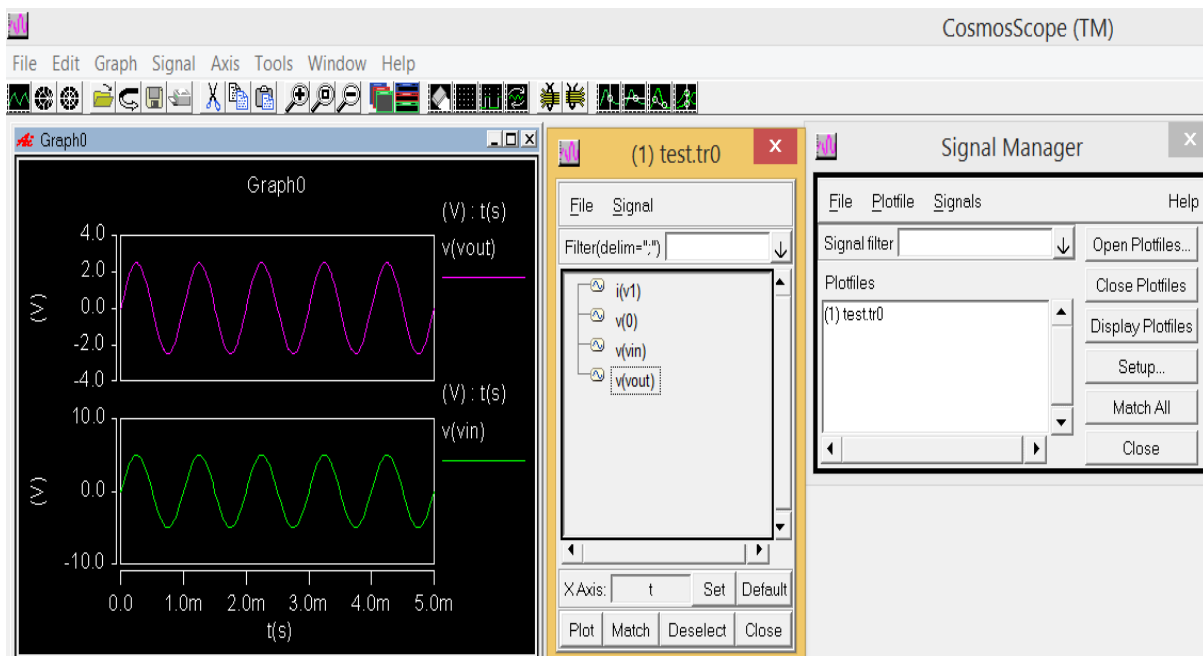


Fig: 4.14: Plotting Graph for Delay in Cosmosscope

4.3 ALGORITHM USED

- Vedic Mathematics is the most effective method for resolving numerical issues in the shortest amount of time. It benefits candidates prepare for competitive exams by assisting them in overcoming their mathematics fear.
- Vedic mathematics is an ancient system of Indian mathematics. It is a gift from India's ancient stages to the rest of the world. The Vedic mathematics were built utilising 16 sutras and 14 upa-sutras, or formulas. Vedic mathematics is set up in such a way that computations can be done mentally.

The following are some of the advantages of Vedic mathematics:

- Math fear is no longer a problem. Vedic Mathematics has the capacity to alleviate the psychological problem of mathematics - anxiety, due to its unique properties.
- It improves accuracy and speed. The Vedic mathematics offers one-line, mental, and super-fast procedures, as well as quick cross-checking tools.
- In comparison to the traditional method, it is more systematic, streamlined, unified, and speedier. Vedic Mathematics is focused on pattern recognition and offers a novel and completely distinct approach to the study of mathematics.
- It allows students to express their ideas on a regular basis and is easy to learn.
- It provides flexibility, enjoyment, and a great deal of happiness. Vedic Mathematics transforms a tiresome subject into a fun and enjoyable experience that everyone may enjoy while learning.

4.3.1 VEDIC SUTRAS

Sutra is nothing but a algorithm or formula which gives a very brief method for mentally performing tough mathematical computations in a very straightforward and simple manner.

S.NO	SUTRA
1	{Anurupye}Shunyamanyat
2	chalana-Kalanabyham
3	Ekadhikena Purvena
4	Ekanyunena Purvena
5	Gunakasamuccayah
6	Gunitasamuccayah
7	Nikhilam-Navatashcaramam Dashatah
8	Paraavartya-Yojayet
9	Puranapurabyham
10	Sankalana-vyavakalanabhyam
11	Shesanyankena-Charamena
12	Shunyam-Saamyasamuccaye
13	Sopantyadvayamantyam
14	Urdhva-Tiryakbhyam
15	Vyashtisamastih
16	Yavadunam

Fig: 4.15: Vedic Sutras

- Urdhva – tiryagbhyam is a universal multiplication formula that can also be used to divide two huge numbers by another large number. "Vertically and crosswise" is the literal meaning of Urdhva Tiryagbhyam.
- Urdhva Tiryagbhyam sutra is a QUICK GENERAL technique of multiplication in Vedic Mathematics.

$$\begin{array}{r} 12 \\ 13 \\ \hline 1:3 + 2:6 = 156 \end{array}$$

Fig: 4.16: Multiplication using Urdhva Tiryagbhyam

CHAPTER 5

Results and Discussion, Performance Analysis

5.1 RESULTS AND DISSCUSSION

Thus the proposed MAC Unit design with an intention of reduction in power and delay has been successfully completed. The final result shows a drastic improvement between the proposed and the existing design. The screenshots of the circuits used to build the MAC Unit is shown below,

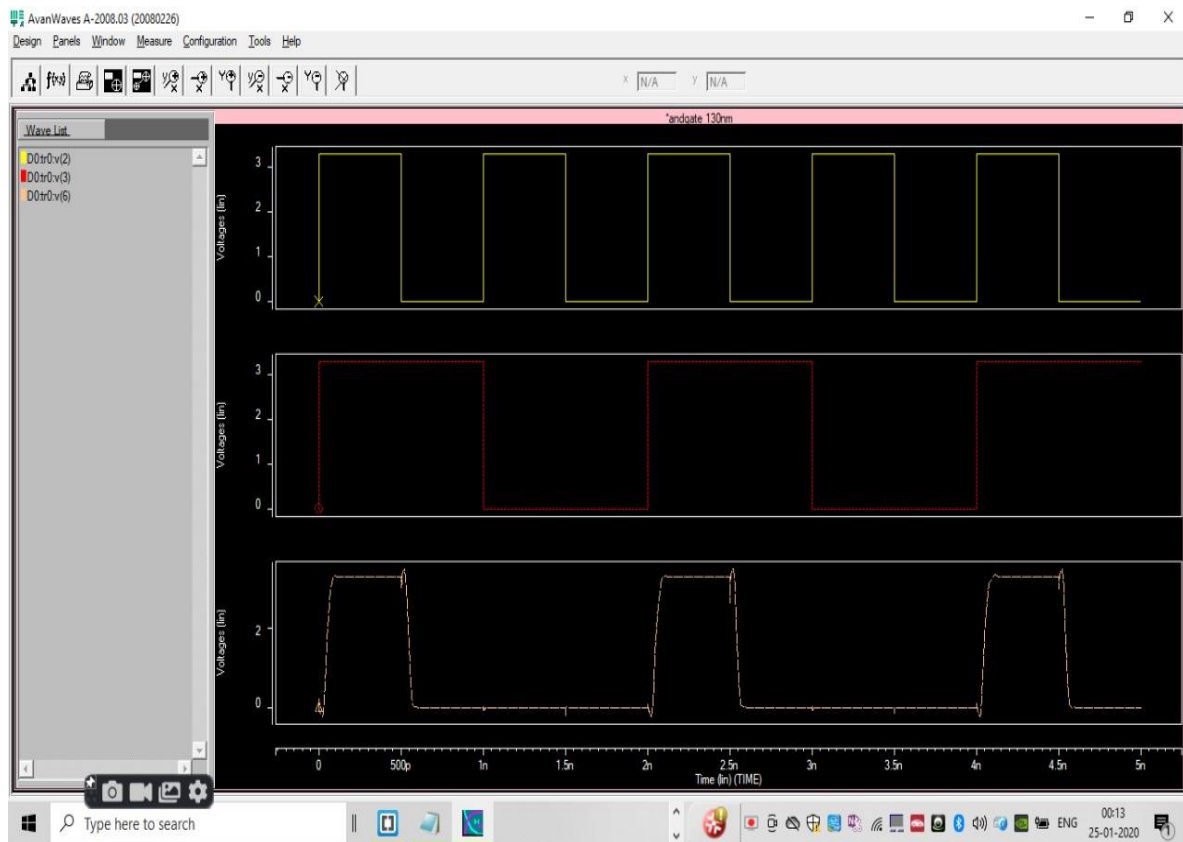


Fig: 5.1: Simulation result of AND Gate

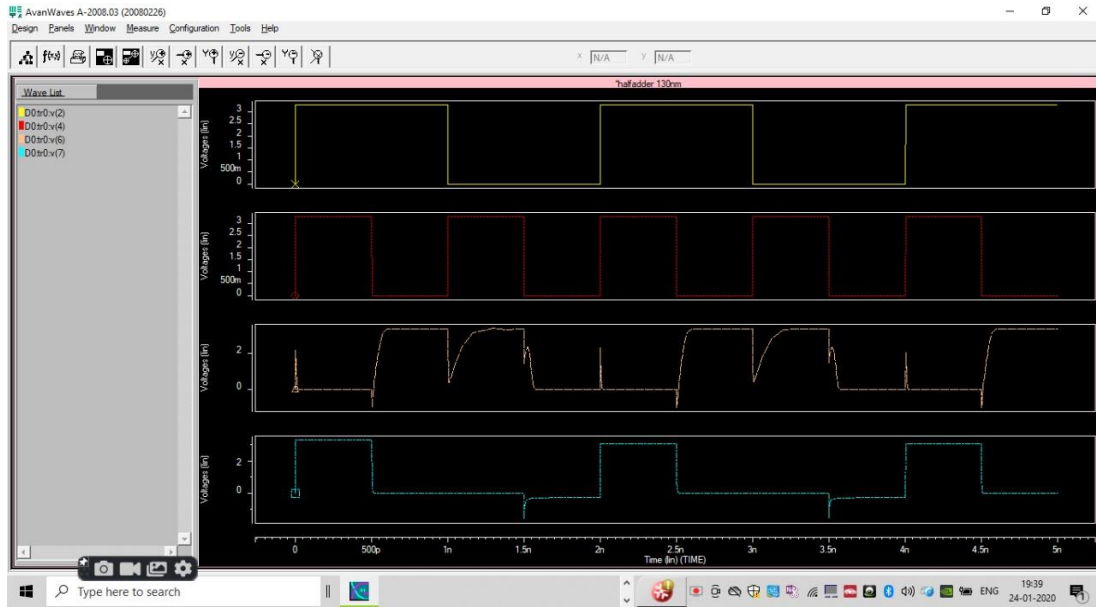


Fig: 5.2: Simulation Result of Half Adder

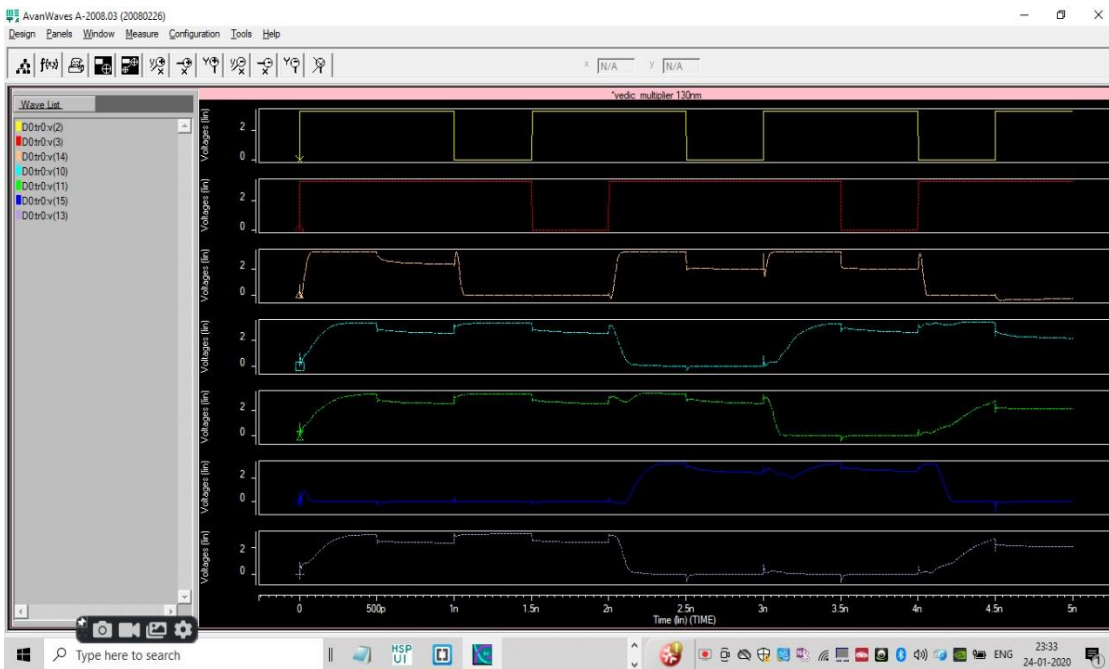


Fig: 5.3: Simulation Result of 2x2 Vedic Multiplier

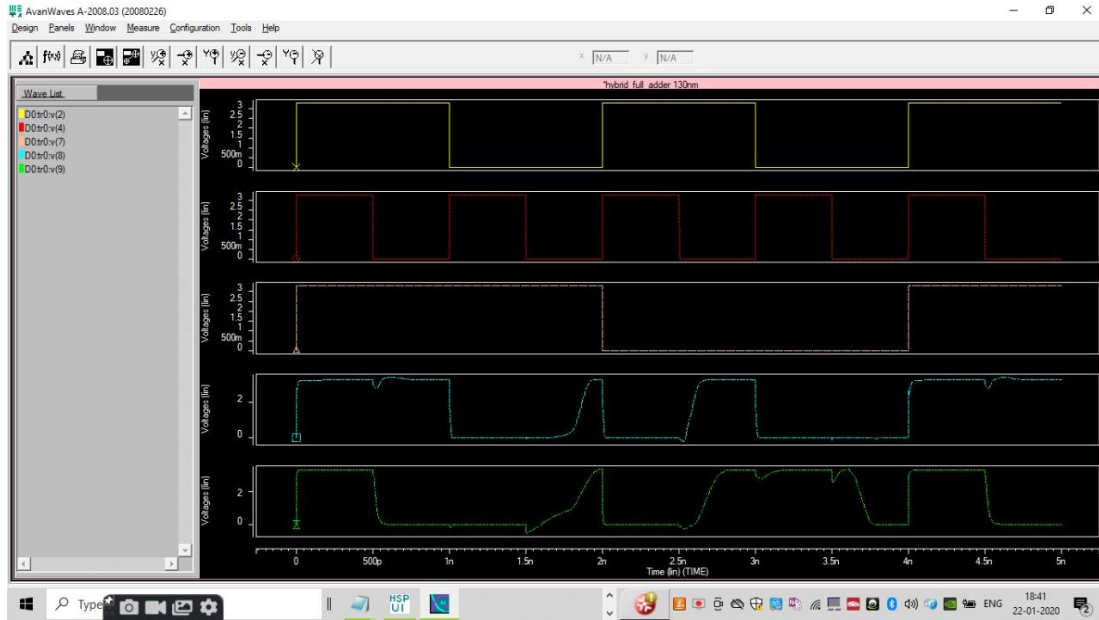


Fig: 5.4: Simulation Result of Existing Hybrid Full Adder

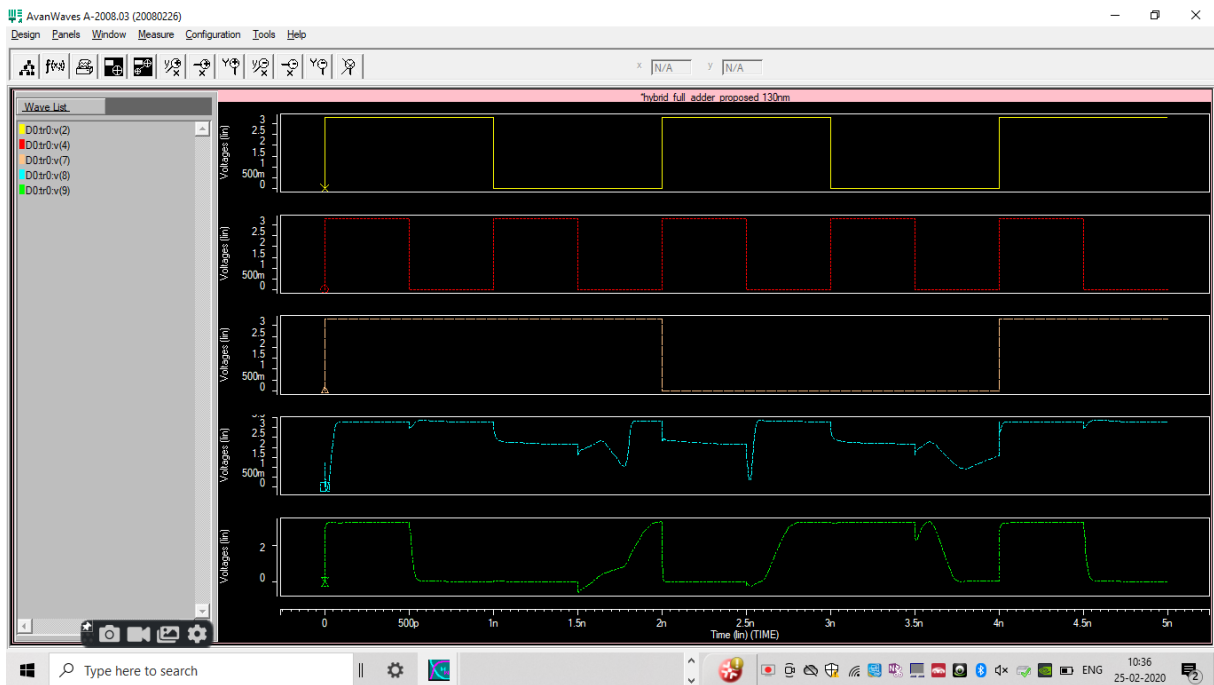


Fig: 5.5: Simulation Result of Proposed Hybrid Full Adder

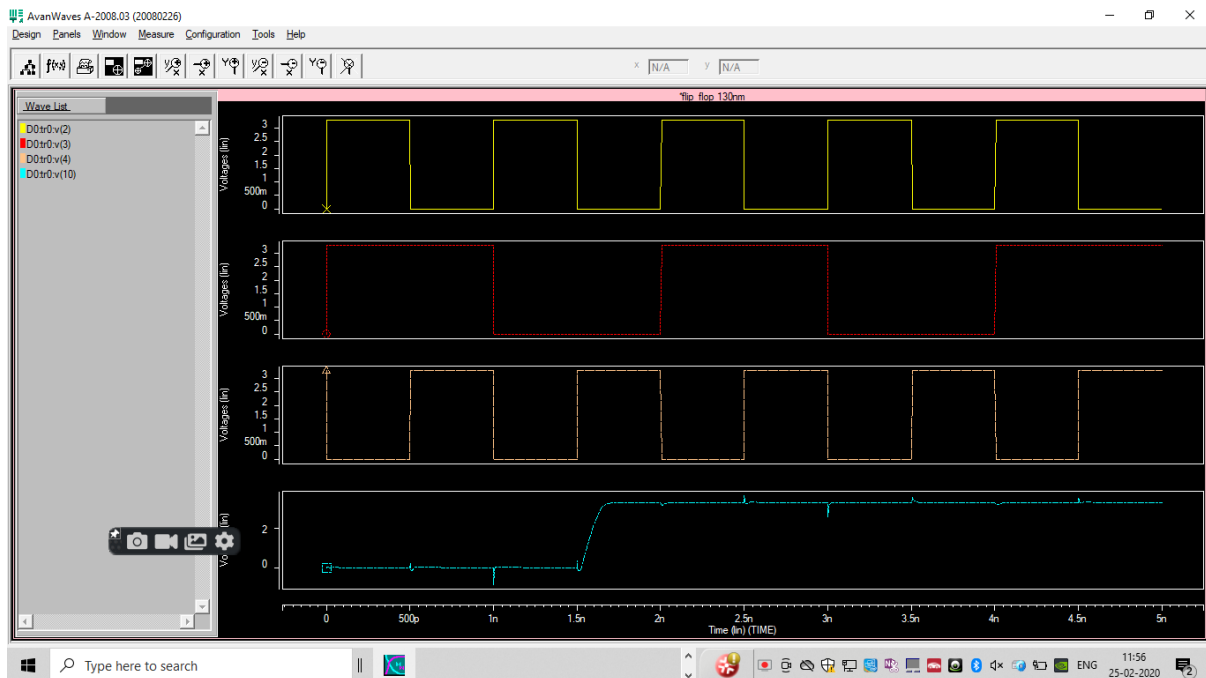


Fig: 5.6: Simulation Result of Existing Flip Flop

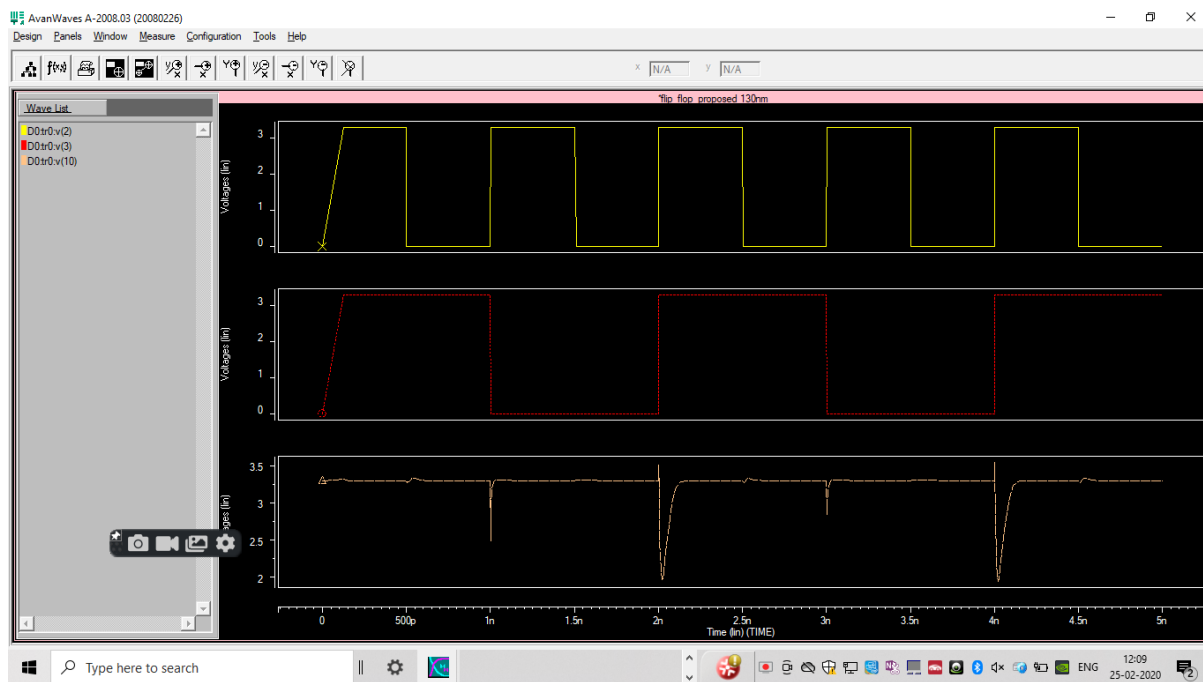


Fig: 5.7: Simulation Result of Proposed Flip Flop

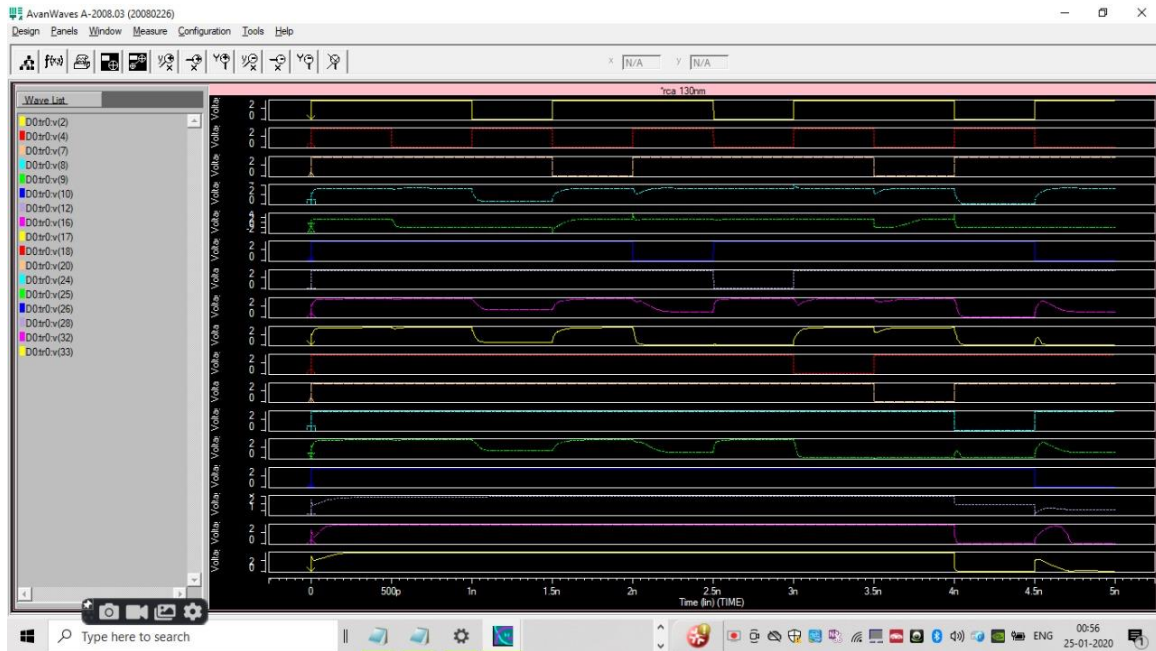


Fig: 5.8: Simulation Result of Existing 4-Bit RCA



Fig: 5.9: Simulation Result of Proposed 4-Bit RCA

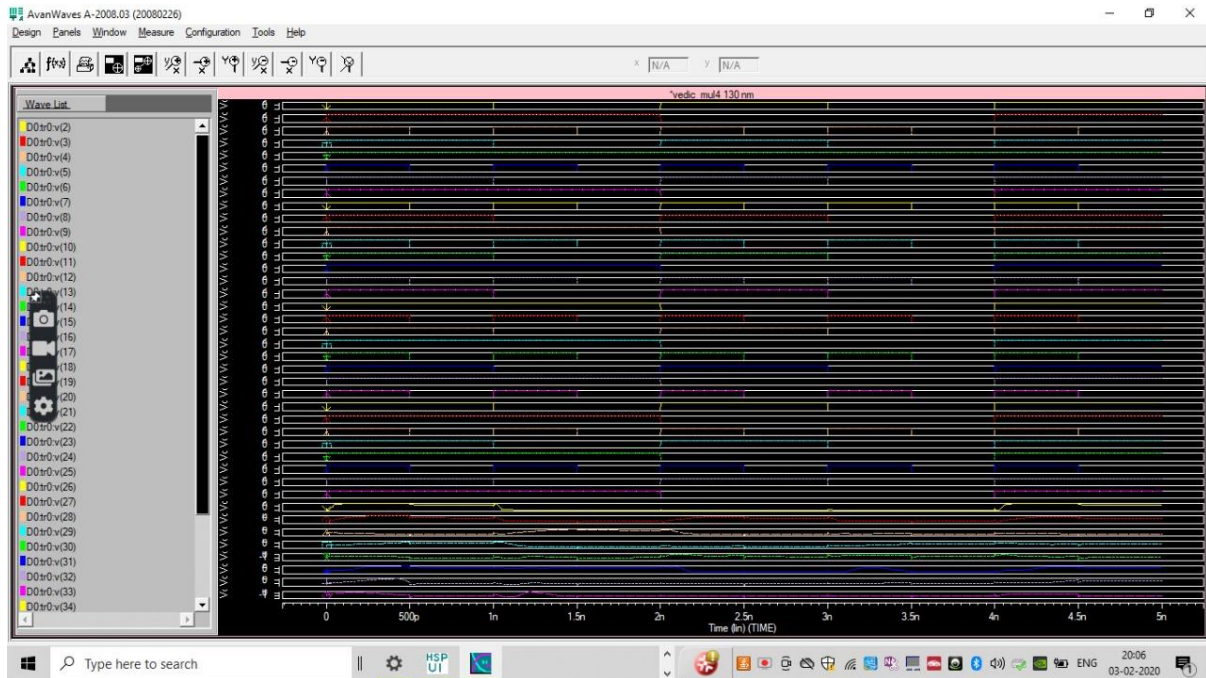


Fig. 5.10: Simulation Result of Existing 4x4 Vedic Multiplier

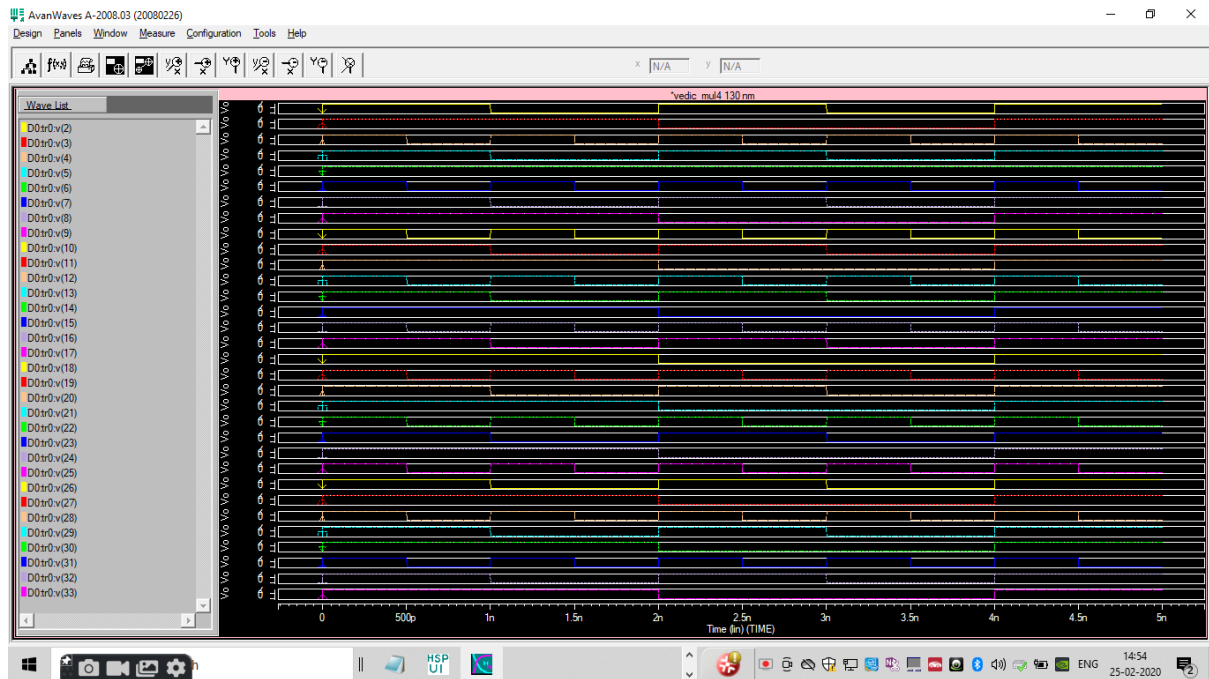


Fig. 5.11: Simulation Result of Proposed 4x4 Vedic Multiplier

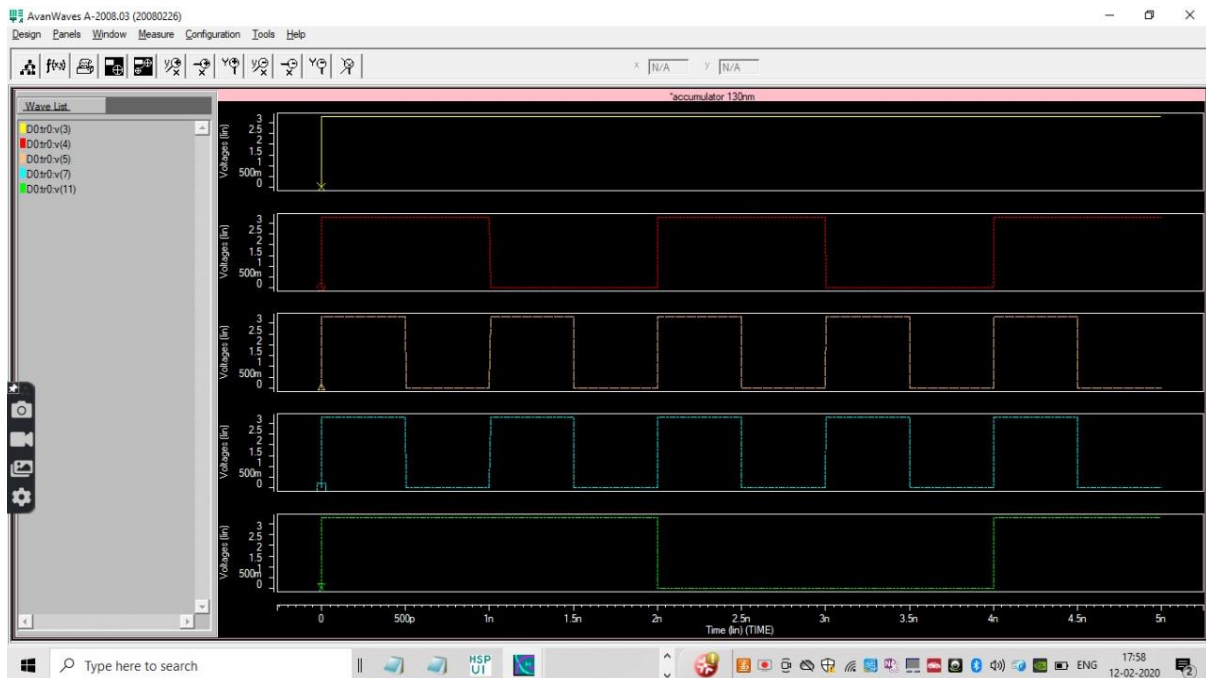


Fig 5.12: Simulation Result of Existing Accumulator

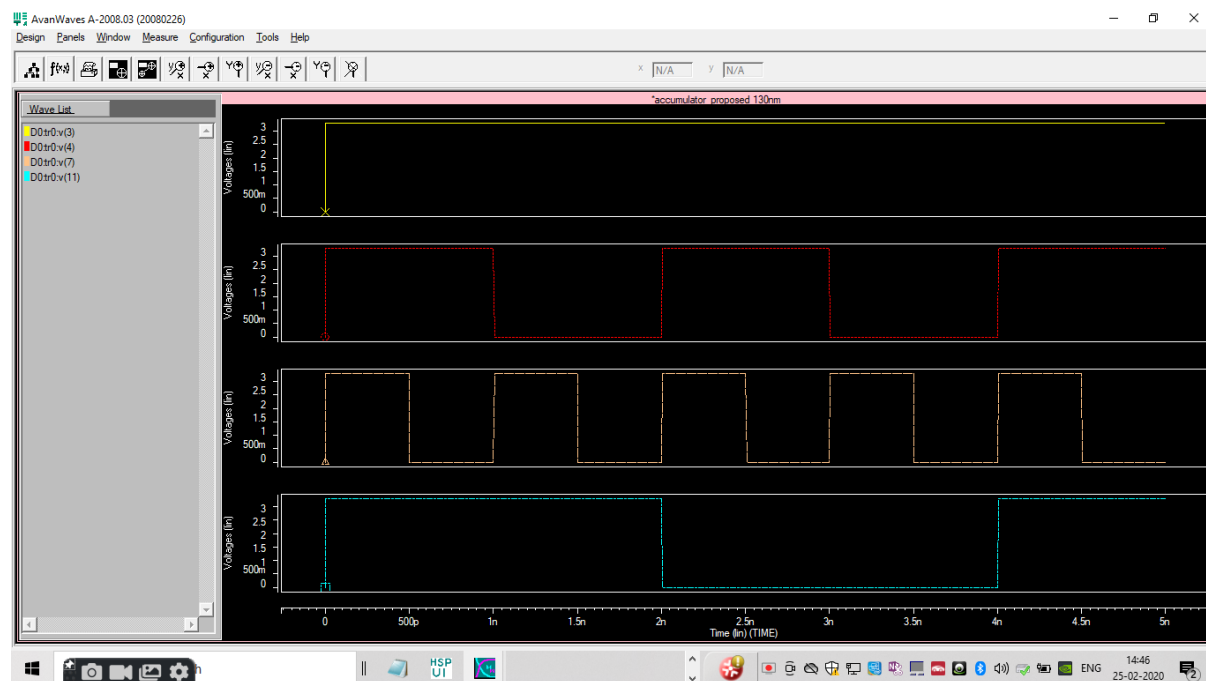


Fig 5.13: Simulation Result of Proposed Accumulator

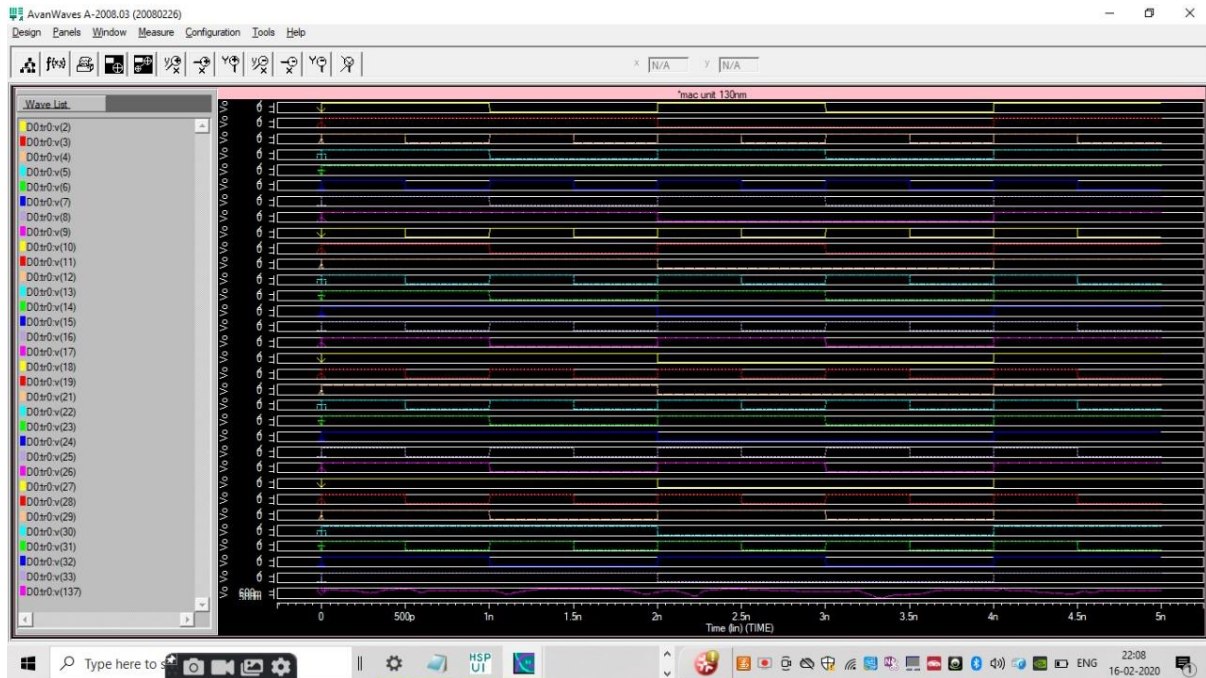


Fig. 5.14: Simulation Result of Existing 4-Bit MAC Unit

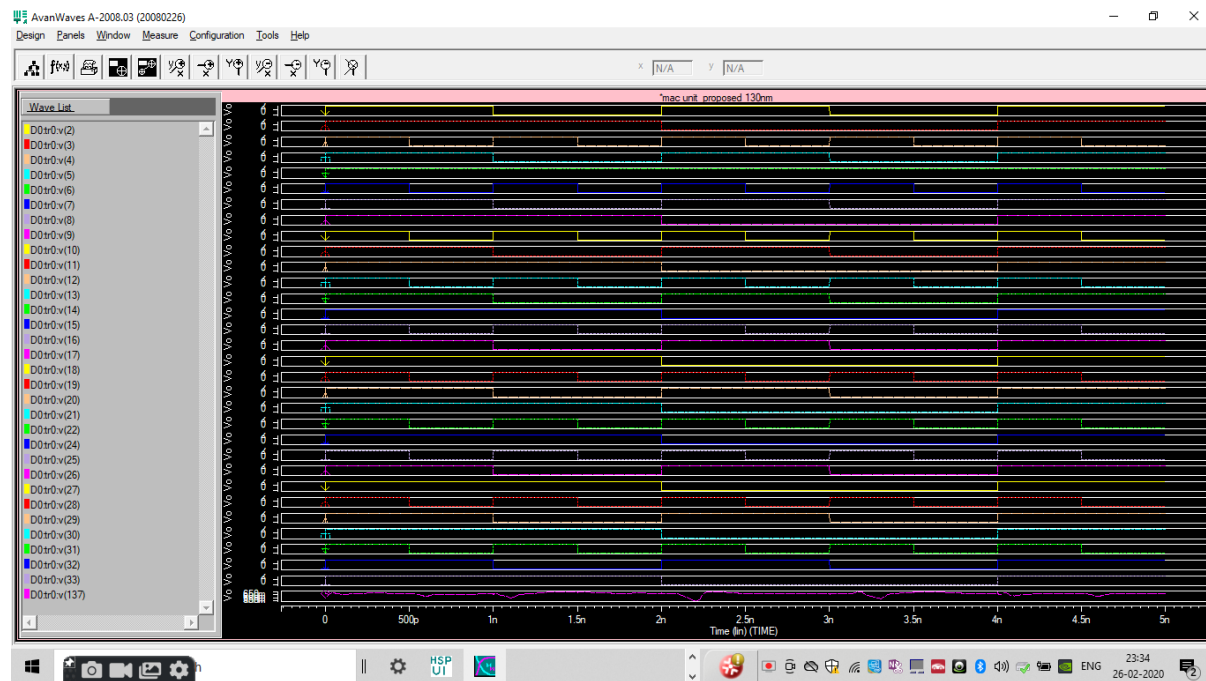


Fig. 5.15: Simulation Result of Proposed 4-Bit MAC Unit

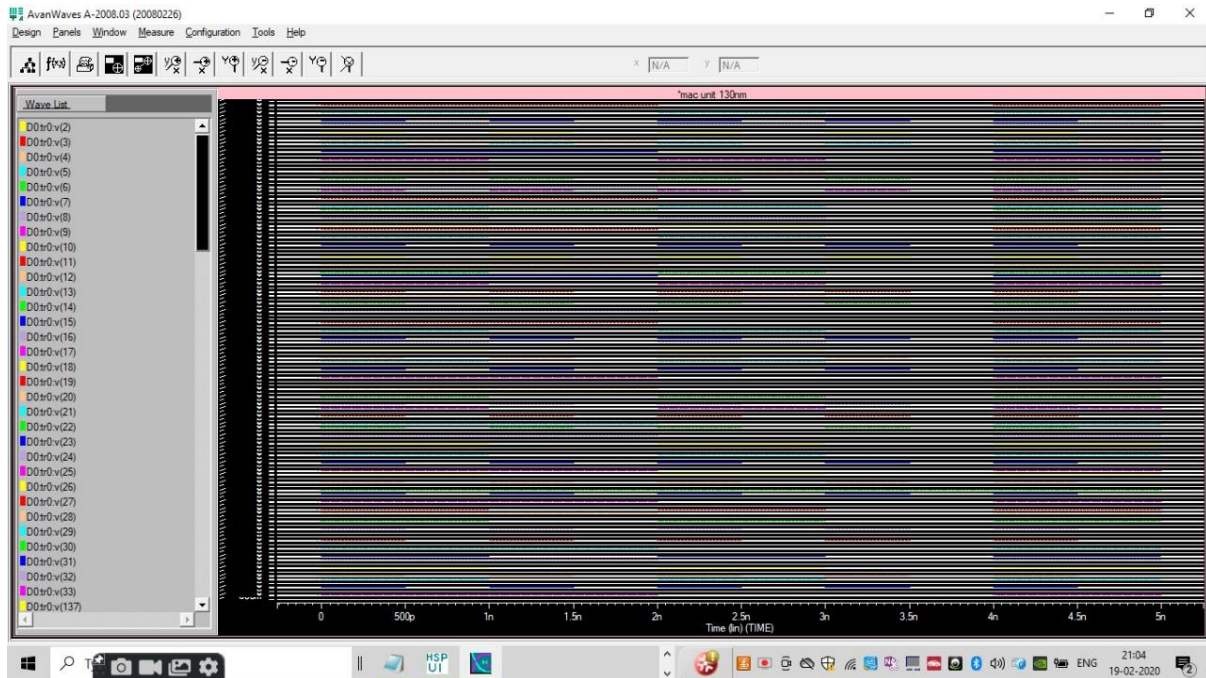


Fig: 5.16: Simulation Result of Existing 16-Bit MAC Unit

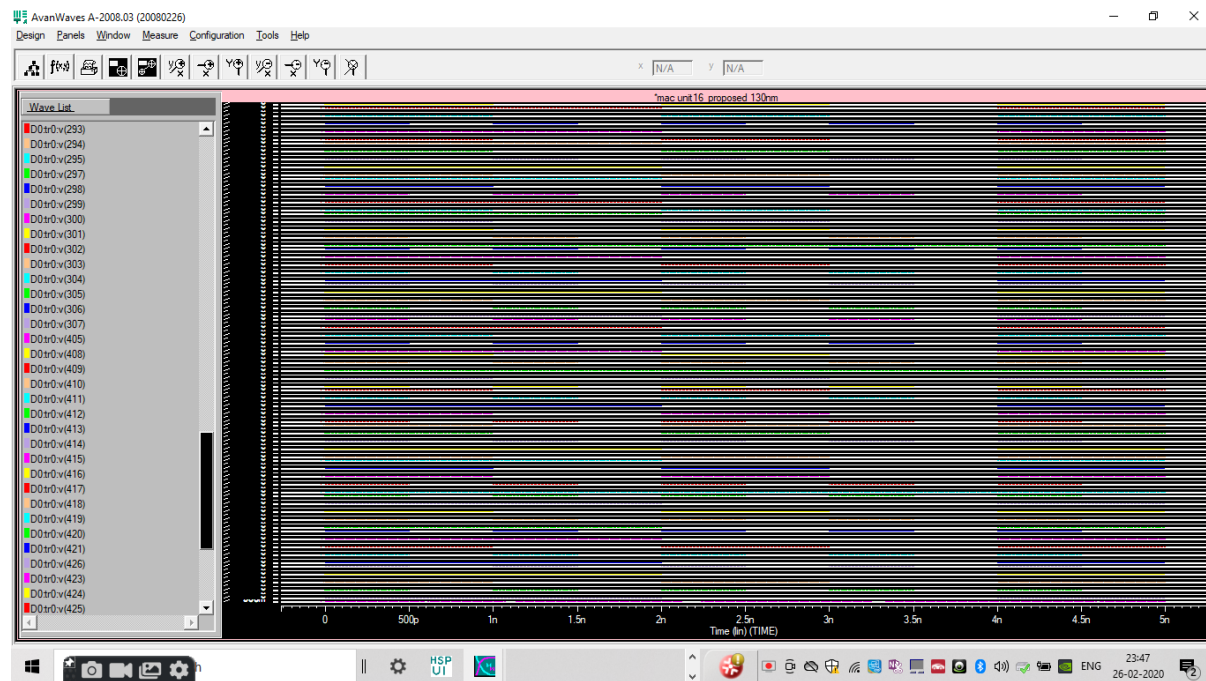


Fig: 5.17: Simulation Result of Proposed 16-Bit MAC Unit

5.2 PERFORMANCE ANALYSIS

We have simulated the MAC unit code in the HSPICE software.

TABLE 5.1: ANALYSIS OF EXISTING MAC UNIT

S.NO	DEVICE	POWER	DELAY	PDP
1	FULL ADDER	5.391×10^{-5} W	3.7718ps	20.33377aJ
2	FLIP FLOP	6.708×10^{-5} W	79.634ps	53.418487aJ
3	MULTIPLIER	5.551×10^{-4} W	35.961ps	199.61951aJ
4	ACCUMULATOR	5.547×10^{-4} W	253.16fs	0.14042785aJ
5	MAC UNIT	7.775×10^{-3} W	424.15ps	3297.7663aJ

Table 5.1 shows the power and delay values of the main components in the existing MAC unit under 130nm CMOS logic, where the Power is measured in Watts, Delay is measured in picosecond and PDP in attojoule.

TABLE 5.2: ANALYSIS OF PROPOSED MAC UNIT

S.NO	DEVICE	POWER	DELAY	PDP
1	FULL ADDER	$3.823 \times 10^{-5} \text{W}$	134.61fs	5.1461403aJ
2	FLIP FLOP	$7.936 \times 10^{-5} \text{W}$	5.5914ps	443.733504aJ
3	MULTIPLIER	$5.074 \times 10^{-4} \text{W}$	141.22ps	71655.028aJ
4	ACCUMULATOR	$1.731 \times 10^{-4} \text{W}$	$1.0547 \times 10^{-21} \text{s}$	0.00000018256857aJ
5	MAC UNIT	$6.663 \times 10^{-3} \text{W}$	152.04ps	1013042.52aJ

Table 5.2 shows the power and delay values of the main components in the proposed MAC unit under 130nm CMOS logic, where the Power is measured in Watta, Delay is measured in picosecond and PDP in attojoule.

The delay values were taken from COSMOSCOPE software for both the existing and proposed MAC unit. From the above tables Table 5.1 and Table 5.2, it is inferred that the power and delay of the circuits used in the MAC unit is efficiently reduced in the proposed MAC unit compared to that of the existing MAC unit.

5.3 OBSERVATION FROM THE RESULTS

The proposed design has highly efficient full adder and flip flop which is designed by using pass transistors and cmos gates. Using this full adder and flip flop the MAC unit is made which makes it efficient. Compared to the existing architecture, in our proposed architecture the average power, area, energy are reduced and speed is increased efficiently.

PDP of the MAC unit is significantly reduced when compared with existing MAC unit. We have used vedic multiplier which enhances the speed of operation of MAC unit by using Urdhva Tiryakbhyam. It can be concluded that the proposed MAC unit show significant improvement in their performance with good stability and reduced power consumption.

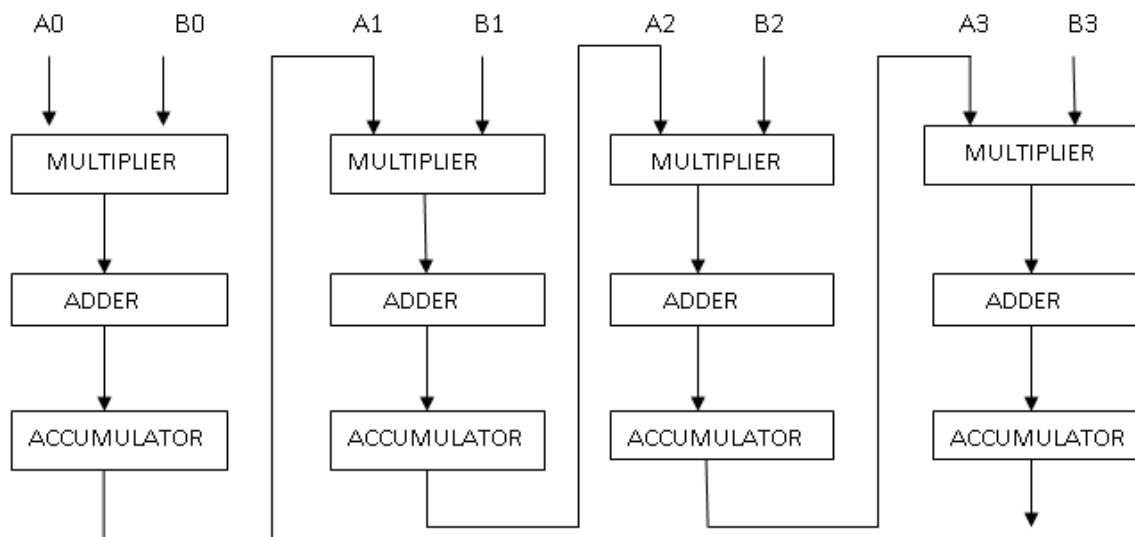


Fig: 5.18: The Final MAC Design

CHAPTER 6

SUMMARY AND CONCLUSIONS

6.1 SUMMARY

The above mentioned details summarize that the design of MAC Unit for high performance and speed has been successfully designed. Hence, our objective to create an MAC Unit to reduce the power and delay has been achieved.

6.2 CONCLUSION

- In conclusion, the design for the MAC (Multiply-Accumulate) Unit has been designed. The scope of application of this project is versatile, especially when it comes to DSP Applications.
- This project can be used for the designs where low power and delay is needed, thereby resulting in high speed and performance.
- We have used vedic multiplier which enhances the speed of operation of MAC unit by using Urdhva Triyakbhyam.
- It can be concluded that the proposed MAC unit shows significant improvement in their performance with good stability and reduced power consumption.

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