

| SECA7001 | SYSTEM ON CHIP DESIGN AND VERIFICATION<br>(For VLSI) | L | T | P | Credits | Total Marks |
|----------|------------------------------------------------------|---|---|---|---------|-------------|
|          |                                                      | 3 | 0 | 0 | 3       | 100         |

**COURSE OBJECTIVES**

- To study about the IP cores and application specific design that is becoming the order of the day.
- To learn System on chip fundamentals, their applications.
- To gain knowledge on NOC design.
- To learn the various computation models of SOC.

**UNIT 1 INTRODUCTION TO THE SOC APPROACH****9 Hrs.**

System Architecture, Processor Architectures, Memory and Addressing, Review of Moore's law and CMOS Scaling, Comparison on System-on-Board, System-on-Chip, and System-in-Package- benefits of system-on-chip integration in terms of cost, power, and performance - SOC Design, Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design, System Architecture and Complexity SoC Design.

**UNIT 2 PROCESSORS AND SYSTEM ON CHIP DESIGN PROCESS****9 Hrs.**

Processor Selection for SOC, Robust Processors- Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors-Acanonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up- Specification requirement, Types of Specification , System Design process and design issues, Soft IP Vs Hard IP, IP verification and integration, hardware-software co-design, Design for timing closure, Logic design issues Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in an SOC.

**UNIT 3 EMBEDDED MEMORIES****9 Hrs.**

Overview of SOC external memory, Internal Memory, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, memory interaction, Cache coherence, MESI protocol and Directory-based coherence.

**UNIT 4 NOC-BASED SOC****9 Hrs.**

Network on Chip (NOC), Architecture of NoC -Network on Chip topologies-Mesh-based NoC.- Routing in an NoC- Packet switching and wormhole routing- NoC Protocol Design, Low-Power Design for NoC, Low-Power Network on Chip Protocol, Low-Power Channel Coding, Low-Power Clocking, Low-Power Signaling, On-Chip Serialization.

**UNIT 5 NOC / MPSoCs****9 Hrs.**

Real Chip Implementation-BONE Series, Industrial Implementations-, Intel's Tera-FLOP 80-Core NoC, MPSoCs. Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design. Case study: A Low Power Open Multimedia Application Platform for 3G Wireless

**Max. 45 Hrs.****COURSE OUTCOMES**

On completion of the course, student will be able to

- CO1 - Remember the fundamentals of SoC design.
- CO2 - Understand the design of processors and SoC.
- CO3 - Analyze the design procedures of SoC memories.
- CO4 - Apply low-power design techniques onNoC.
- CO5 - Evaluate the design and performance of MPSoCs.
- CO6 - Create Low Power Application Platform for 3G wireless.

**TEXT / REFERENCE BOOKS**

1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiley India Pvt. Ltd., 2011.
2. Furber, "ARM System-on-Chip Architecture", Pearson Education India (2014).
3. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, "Low power NoC for high performance SoC Design", CRC Press, 2008.
4. Vijay Madisetti & Chonlameth Arpniakanondt, "A Platform-Centric Approach to System-on-Chip (SOC) Design", Springer, 2010.
5. Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
6. Ahmed Amine Jeraya, Wayne Wolf, "Multiprocessor System On chip", Morgan Kauffmann, 2010.
7. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition, 2009.

**END SEMESTER EXAMINATION QUESTION PAPER PATTERN****Max. Marks: 100****Exam Duration: 3 Hrs.****PART A:** 5 Questions of 6 Marks each – No choice**30 Marks****PART B:** 2 Questions from each unit of internal choice, each carrying 14 Marks**70 Marks**

| SECA7002 | VLSI FOR WIRELESS COMMUNICATIONS<br>(For VLSI) | L | T | P | Credits | Total Marks |
|----------|------------------------------------------------|---|---|---|---------|-------------|
|          |                                                | 3 | 0 | 0 | 3       | 100         |

**COURSE OBJECTIVES**

- To learn the concept of fading in Communication.
- To study the design concepts of low noise amplifiers.
- To study the concept of filter and learn about Design Parameters.
- To understand the various types of mixers designed for wireless communication.

**UNIT 1 INTRODUCTION****9 Hrs.**

Review of Modulation Schemes – BFSK - BPSK - QPSK - OQPSK - Classical Channel - Additive White Gaussian Noise - Finite Channel Bandwidth - Wireless Channel- Path Environment - Path Loss - Friis Equation - Multipath Fading - Channel Model - Envelope Fading - Frequency Selective Fading - Fast Fading - Comparison of different types of Fading.

**UNIT 2 RECEIVER ARCHITECTURES****9 Hrs.**

Receiver Front End - Motivations - General Design Philosophy - Heterodyne and Other architectures - Filter Design - Band Selection Filter - Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion - Intermodulation - Cascaded Nonlinear Stages - Gain Compression - Blocking - Noise - Noise Sources - Noise Figure - Design of Front end parameter for DECT.

**UNIT 3 LOW NOISE AMPLIFIER****9 Hrs.**

LNA: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Power matching - Salient features of LNA - Core Amplifier Design. Active Mixer - Balancing - Gilbert Mixer - Analysis - Noise - Complete Active mixer

**UNIT 4 ANALOG TO DIGITAL CONVERTERS****9 Hrs.**

Demodulators - Delta Modulators - Low Pass Sigma Delta Modulators - High Order Modulators - One Bit DAC and ADC - Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators - Comparison - PLL based Frequency Synthesizer - Loop Filter Design and Implementation.

**UNIT 5 SPREAD SPECTRUM****9 Hrs.**

Review of Spread Spectrum - DSSS - FHSS - Basic Principle of DSSS - Modulation – Demodulation - Performance in the presence of noise-narrowband and wideband interferences. Implementations: VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing.

**Max.45 Hrs.****COURSE OUTCOMES**

On completion of the course, student will be able to

- CO1 - Remember the fundamentals of Modulation Schemes.
- CO2 - Understand the design of Filters.
- CO3 - Analyze the design procedures of Low Noise Amplifier.
- CO4 - Apply modulators in applications.
- CO5 - Evaluate the design and performance of Spread Spectrum.
- CO6 - Create Application Platform for VLSI Architecture.

**TEXT / REFERENCE BOOKS**

1. Bosco Leung, "VLSI for Wireless Communication", Prentice Hall, 2002.
2. Andreas F.Molisch, "Wideband Wireless Digital Communication", Prentice Hall PTR, 2001.
3. George V. Tsoulous, "Adaptive Antennas for wireless Communication", IEEE Press, 2001.
4. Xiaodong Wang and H.Vincent, "Wireless Communication System, Advanced Reception", Pearson Education, 2004.

**END SEMESTER EXAMINATION QUESTION PAPER PATTERN****Max. Marks: 100****Exam Duration: 3 Hrs.****PART A:** 5 Questions of 6 Marks each – No choice**30 Marks****PART B:** 2 Questions from each unit of internal choice, each carrying 14 Marks**70 Marks**

|                 |                                                           |          |          |          |                |                    |
|-----------------|-----------------------------------------------------------|----------|----------|----------|----------------|--------------------|
| <b>SECA7016</b> | <b>NANO ELECTRONICS AND SENSORS<br/>(For VLSI And AE)</b> | <b>L</b> | <b>T</b> | <b>P</b> | <b>Credits</b> | <b>Total Marks</b> |
|                 |                                                           | <b>3</b> | <b>0</b> | <b>0</b> | <b>3</b>       | <b>100</b>         |

**COURSE OBJECTIVES**

- To understand the basic concepts of Nanoelectronics and Nanosensors.
- To acquire the knowledge of advancements in MOSFET Devices.
- To learn the basic concepts of Carbon Nanotubes.
- To be familiar with the Applications of Nanosensors.

**UNIT 1 FUNDAMENTALS OF NANOELECTRONICS****9 Hrs.**

Fundamentals of logic devices: Requirements - dynamic properties - threshold gates; physical limits to computations; concepts of logic devices: classifications - two terminal devices - field effect devices - coulomb blockade devices - spintronics - quantum cellular automata - quantum computing - DNA computer; performance of information processing systems- basic binary operations, measure of performance processing capability of biological neurons - performance estimation for the human brain. Ultimate computation: power dissipation limit - dissipation in reversible computation - the ultimate computer.

**UNIT 2 SILICON MOSFETS AND QUANTUM TRANSPORT DEVICES****9 Hrs.**

Silicon MOSFETS - Novel materials and alternate concepts:- fundamentals of MOSFET Devices - scaling rules - silicon-dioxide based gate dielectrics - metal gates - junctions & contacts - advanced MOSFET concepts - Quantum transport devices based on resonant tunneling: Electron tunneling - resonant tunneling diodes - resonant tunneling devices; Single electron devices for logic applications: Single electron devices - applications of single electron devices to logic circuits.

**UNIT 3 CARBON NANOTUBES****9 Hrs.**

Carbon Nanotube: Fullerenes - types of nanotubes - formation of nanotubes – assemblies - purification of carbon nanotubes - electronic properties - synthesis of carbon nanotubes - carbon nanotube interconnects - carbon nanotube FETs - Nanotube for memory applications - prospects of an all carbon nano tube nano electronics.

**UNIT 4 INTRODUCTION TO NANOSENSORS****9 Hrs.**

Fundamentals of Nano Sensors: Micro and nano-sensors, Fundamentals of sensors, biosensor, micro fluids, MEMS and NEMS, Packaging and characterization of sensors, Method of packaging at zero level, dye level and first level Sensors.

**UNIT 5 NANO SENSORS AND ITS APPLICATIONS****9 Hrs.**

Nanoparticles and Micro-organism - Biosensors - Bioreceptors and their properties – Biochips - Integrated nanosensor networks for detection and response - DNA based biosensors and diagnostics - Natural nanocomposite systems; spider silk, bones, shells - Nanomaterials in bone substitutes and dentistry - Implants and Prosthesis - Tissue Engineering - Neuroscience - Neuro-electronic Interfaces - Nanorobotics - Photodynamic Therapy - Protein Engineering - Nanosensors in Diagnosis - Drug delivery - Cancer therapy and Other therapeutic applications.

**Max. 45 Hrs.****COURSE OUTCOMES**

On completion of the course, student will be able to

- CO1 - Understand the fundamentals of nanoelectronics.
- CO2 - Analyse the material concepts for quantum devices.
- CO3 - Describe the carbon nanotubes.
- CO4 - Explain the method of packaging of nano sensors.
- CO5 - Apply the nano particles for designing bio sensors.
- CO6 - Design the nanosensor for bio application.

**TEXT / REFERENCE BOOKS**

1. Rainer Waser (Ed.), "Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices", Wiley VCH, 2003.
2. Meixner H., "Sensors: Micro & Nanosensors, Sensor Market trends", Wiley VCH, 1995.
3. Neelina H. Malsch (Ed.), "Biomedical Nanotechnology", CRC Press, 2005.
4. Raguse, "Nanotechnology: Basic Science and Emerging Technologies", Chapman & Hall/CRC, 2002.
5. T.Pradeep, "NANO: The Essentials – Understanding Nanoscience and Nanotechnology", TMH, 2007.

**END SEMESTER EXAMINATION QUESTION PAPER PATTERN****Max. Marks: 100****Exam Duration: 3 Hrs.****PART A:** 5 Questions of 6 Marks each – No choice**30 Marks****PART B:** 2 Questions from each unit of internal choice, each carrying 14 Marks**70 Marks**