

SEC5101	TRANSFORMS AND RANDOM PROCESS FOR ELECTRONICS ENGINEERING (For AE, EMB & VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- x To reinforce the mathematical foundation with advanced topics
- x To enable the student to appreciate the engineering aspect of mathematics
- x To equip the student with tools to confront continual mathematical challenges

UNIT 1 2D TRANSFORMS**12 Hrs.**

Need for transform – Review of 1D Transform – 2D DFT – IDFT – properties – Image transforms – 2D Orthogonal and Unitary transform and its properties – Separable transforms – Walsh, Hadamard, Haar, DST, DCT, Slant, SVD & KL transforms.

UNIT 2 WAVELET TRANSFORMS & ITS APPLICATIONS**12Hrs.**

Wavelet transforms – 1D & 2D Wavelet transform – basis and orthogonal basis – Time and frequency decompositions – STFT – CWT, DWT, Haar wavelet and Shannon wavelet – MRA – Orthonormal Wavelets – Fast Wavelet transform – Wavelet Packets – Biorthogonal Wavelet Bases – SPIHT Algorithm – Wavelet Denoising – Wavelet based Signal Processing – Signal & Image compression.

UNIT 3 PROBABILITY & RANDOM VARIABLES**12 Hrs**

Probability concepts – Random variable – moment generating function – discrete types, continuous types – Distributions – Binomial, Poisson, Geometric, Uniform, Normal and Exponential – Transformation of random variables – 2D random variables – marginal, conditional, joint probability – Correlation – Regression – Central Limit Theorem.

UNIT 4 RANDOMPROCESS**12 Hrs.**

Notion of Stochastic processes – Stationary and Independence; WSS & Ergodicity – Correlation Functions; Auto Correlation, Cross Correlation & its properties – expectations – variance, co variance – Power Spectral Density – properties – energy spectral density – Parseval's theorem – Wiener Khintchine relation – Linear systems with Random inputs – response of linear systems to white noise – simulation of white noise – Noise Bandwidth – low pass filtering of white noise.

UNIT 5 QUEUING THEORY**12 Hrs.**

Introduction to queuing theory – Characteristics of Queuing Systems – Little's Law – Markovian Queues – Single server models – Multiple server models – Non-Markovian Queues – Pollaczek-Khinchine formula – Machine interference model – steady state analysis – self service queue – Priority Queues – Open and Closed Networks – queuing applications.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Rafael C. Gonzalez & Richard E Woods, Digital Image Processing, Third Edition, Pearson Prentice Hall, 2009.
2. Peyton Z. Peebles, Probability, Random Variables and random signal principles, 4th edition, TMH publication, 2001.
3. Anil K Jain, Fundamentals of Digital Image Processing, Prentice Hall, 1989.
4. Raghuveer M Rao & Ajit S Bopardikar, Wavelet Transform: Introduction to Theory & Applications, Pearson Education, 1998.
5. Donald Gross, John F. Shortle, James M. Thompson, and Carl W. Harris, Fundamentals of Queuing Theory, 4th edition, Wiley 2008.

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each-No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5103	ADVANCED DIGITAL SYSTEM DESIGN (For AE)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- To explain how digital circuit of large complexity can be built in a methodological way
- To illustrate how the concepts presented in the lectures are applied in practice, and how the need to accommodate different practically-motivated trade-offs can lead to alternative implementations
- To expose students to the advanced design techniques and methodology

UNIT 1 INTRODUCTION TO COMBINATIONAL AND SEQUENTIAL LOGIC CIRCUITS 12 Hrs.

Combinational: Introduction; General Approach to Combinational Logic Design; Introduction to Digital Integrated Circuits; Decoders; Encoders; Digital Multiplexers; Binary Comparators; Array Multipliers; Tristate Buffers. Sequential: Latches; Flip-Flops; Counters - Ring counter and Johnson Counter; Counter Design; Sequential Circuit Design using State Graphs - Mealy and Moore Machines.

UNIT 2 SYNCHRONOUS SEQUENTIAL NETWORKS 12 Hrs.

Structure and Operation of Synchronous Sequential Networks; Analysis of Clocked Synchronous Sequential Networks (CSSN); Design of CSSN; State Table Reduction – Implication Chart method, Equivalence Classes method, Merger Graph method; State Assignment; Algorithmic state Machines – ASM Charts, ASM Tables, ASM Realizations.

UNIT 3 ASYNCHRONOUS SEQUENTIAL NETWORKS 12 Hrs.

Structure and Operation of Asynchronous Sequential Networks (Fundamental and Pulse Mode); Analysis of Asynchronous Sequential Networks (ASN); Design of ASN; Primitive Flow Table; Flow Table Reduction; State Assignment; Races in ASC –Static and Dynamic Hazards; Essential Hazards; Mixed Operating Mode Asynchronous Circuits.

UNIT 4 PROGRAMMABLE LOGIC DEVICES 12 Hrs.

Basic Concepts; Programming Technologies; Programmable Logic Element(PLE); ROM-Programmable Logic Array(PLA); Programmable Array Logic(PAL); Structure of standard PLD's; Complex PLD's(CPLD); System Design using PLD's; Design of Combinational and Sequential Circuits using PLD's; System Design Using the Concept of Controller.

UNIT 5 STUDY OF FPGA & XILINX 12 Hrs.

Introduction to Field Programmable Gate Arrays; Types of FPGA; Xilinx XC3000 series, Logic Cell Array(LCA); Configurable Logic Blocks(CLB); Input/Output Block(IOB); Programmable Interconnect Point(PIP); Introduction to ACT2 family and Xilinx XC4000 families; Design examples: Pseudo Random Generator, Traffic Light Controller, Vending Machine Controller.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Donald G. Givone, Digital principles and Design, Tata McGraw Hill, 2002.
2. John M Yarbrough, Digital Logic applications and Design, Thomson Learning, 2001.
3. William I. Fletcher, An Engineering Approach to Digital Design, Prentice Hall of India, 1996.
4. Charles H. Roth,Jr. and Larry L. Kinney, Fundamentals of Logic Design, 6th Edition, Cengage Learning, 2012.
5. Richard F. Tinder, Engineering Digital Design, 2nd Edition Revised, Academic Press, 2000.

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration: 3 Hrs.****PART A : 5 Questions of 6 Marks each-No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5110	DIGITAL CMOS VLSI DESIGN (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- x Basics of Semiconductor device, MOS transistors and device sizing, stick diagram and layout design of combinational and sequential circuits.
- x The challenges of digital VLSI design, Conceptual thinking and design methodology over detailed circuit analysis techniques

UNIT 1 INTRODUCTION TO MOSFET**12 Hrs.**

Introduction to MOSFET – MOS transistor switches - modes of operation – MOSFET I_{DS} versus V_{DS} relationship - Expression for Threshold voltage - Energy band structure - Secondary effects - MOSFET capacitance model – review of CMOS and Bi-CMOS technologies.

UNIT 2 CMOS LOGIC DESIGNS**12 Hrs.**

Basic inverter –CMOS inverter – CMOS inverter logic levels – combinational logic design - Static CMOS design - device sizing –CMOS design rules – stick diagram and layout – Static and Dynamic Power Dissipation - clocked CMOS structures - Dynamic CMOS Design – Domino logic- np CMOS logic - Pass transistor logic design.

UNIT 3 SEQUENTIAL CIRCUIT DESIGN**12 Hrs.**

CMOS Static latches and registers –Bistability principle - Dynamic sequential circuits – C²MOS register – True single phase clocked register –pulse registers - pipelining - NORA CMOS – nonbistable sequential circuits –CMOS Schmitt trigger – monostable sequential circuits.

UNIT 4 PROGRAMMABLE LOGIC DESIGN**12 Hrs.**

Programmable logic array designs – Folded PLA's – Multilevel minimization – Weinberger arrays – gate matrices – Capacitive Parasitics - Capacitance and performance in CMOS – driving large capacitance – Resistive parasitic – Resistance and performance in CMOS.

UNIT 5 COMBINATIONAL CIRCUIT DESIGN**12 Hrs.**

Design of adders: Static and Dynamic adder, Manchester carry chain adder, Carry bypass adder, CSA, Carry look ahead adder – Multipliers : Array multiplier, carry save multiplier, Booth Multiplier – Barrel shifter – NOR and NAND ROMs – operations in CMOS SRAM – Sense amplifiers.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Jan M . Rabaey "Digital Integrated Circuits", second edition, Prentice Hall of India Private Ltd-2003.
2. Eugene D. Fabricius "Introduction to VLSI Design", McGraw Hill 1990.
3. Douglas A. Pucknell "Basic VLSI Design", Prentice Hall of India, 1994.
4. Neil H.E. Weste and Kamran Eshraghian, Principles of CMOS VLSI Design, Pearson Education ASIA, 2nd edition, 2000.
5. Randall L, Geigar and Allence "VLSI Design for Analog and Digital circuits", McGraw Hill Co-1990
6. Abdellatif Bellaouar "Low-Power Digital VLSI Design: Circuits and Systems", Kluwer Academic Publishers-2000

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A :** 5 Questions of 6 Marks each – No choice**30 Marks****PART B :** 2 questions from each unit with internal choice, each carrying 10 Marks**70 Marks**

SEC5111	MODELING AND SIMULATION OF MOS DEVICES (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- x To understand the modeling and characteristics of MOSFET
- x To learn the SPICE programming that simulates the MOS Devices
- x To learn and understand the operation of advanced devices

UNIT 1 FUNDAMENTALS OF DEVICE DYNAMICS**12 Hrs.**

Characteristics of a MOS transistor- Small Signal model of MOSFET – High frequency Limitations - Mathematical model of

IV characteristics — Change in velocity with electric field-Secondary effects - Energy band diagram and band bending-Calculation of the threshold voltage (V_t) – Significance of threshold voltage - Non ideal effects- CV plots: importance –High frequency CV plots – low Frequency CV plots – Equations to CV plots

UNIT 2 RADIATION AND SHIFT IN THRESHOLD VOLTAGE**12 Hrs.**

Dose –Drain current due to photo generated carriers– Interface traps - C_{it} - Effect of AC signal on the interface states – Techniques to measure C_{it} – Sources of oxide trapped charge – radiation created oxide trapped charge and its annealing - Shifts in threshold voltage in P channel and N channel MOSFET – Shifts at dynamic bias – radiation hardening – Other alternative dielectrics

UNIT 3 DOPING, WEAK INVERSION AND SMALL GEOMETRY EFFECTS**12 Hrs.**

Weak inversion - I_d in the sub threshold region of operation- Doping Profiles - Non uniform doping and effect on threshold voltage - Short channel effect – Narrow width effect – Shrink and Scaling – NMOS versus PMOS Devices - MOS Device Layout

UNIT 4 SIMULATION USING PSPICE**12 Hrs.**

MOSFET Model Parameters: SPICE level1, level2, level 3, level 4, level 5, level 6, level 7 and BSIM– Types of Analysis: AC-DC-TF- Frequency – Noise -Transient – Parametric – Sensitivity –Temperature – Worst-case - Monte Carlo. Sub circuit.

UNIT 5 ADVANCED DEVICES**12 Hrs.**

Basics of Structure and Operation: DMOS, UMOS, VMOS, MESFET, MODFET, CNTFET and FinFET. MOS

Device application: Driver- Load–Resistor-Switch-Static protection. Device scaling and change in properties of the device.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Dewitt G. Ong "Modern MOS technology: processes, Devices and Design", Mcgraw Hill, 1984.
2. YannisTividis "Operation and Modeling of MOS Transistors", Mcgraw Hill, 1999
3. Shoji.M "CMOS Digital circuit Technology", Prentice Hall, 1988.
4. SorabK.Ghandhi "Semiconductor device principle", John wiley and sons, 1983.
5. S.M.Sze "VLSI Technology", Tata Mcgraw Hill, 2003.
6. PSpice Reference guide by Cadence Design Systems.

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each – No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5112	VLSI FABRICATION TECHNOLOGY (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- × To learn the integrated circuit design philosophy
- × To understand the methods in fabrication steps
- × To learn the assembling and packaging techniques

UNIT 1 CRYSTAL GROWTH, WAFER PREPARATION, EPITAXY AND OXIDATION 12 Hrs.

Electronic grade silicon – Basic steps in IC fabrication-crystal plane and orientation – Defects in the lattice– Czochralski crystal growing – silicon shaping – Processing consideration – Vapour phase epitaxy - Molecular beam epitaxy - Epitaxial Evaluation – Growth mechanism and kinetics – Thin oxides – Oxidation Techniques and systems – Oxide properties – Redistribution of dopants at interface – Oxidation of polysilicon – Oxidation induced effects.

UNIT 2 LITHOGRAPHY AND RELATIVE PLASMA ETCHING 12 Hrs.

Mask Making – Optical lithography – Electron lithography – X-ray lithography – Ion lithography – Plasma properties– Feature size control and Anisotropic Etch mechanism – Lift off Techniques – Plasma reactor – Relative plasma etching Techniques and Equipments.

UNIT 3 DEPOSITION, DIFFUSION, ION IMPLANTATION AND METALIZATION 12 Hrs.

Deposition process – polysilicon - plasma assisted deposition – models of diffusion in solids – Fick's one dimensional diffusion equation – Atomic diffusion mechanism – measurement techniques .

recovery due to annealing - Implantation equipment – Annealing Shallow junction – high energy implantation – Physical vapour deposition – patterning.

UNIT 4 METALLIZATION 12 Hrs.

Metallization applications – metallization choices – Patterning – Metallization problems – New role of metallization –metallization systems – sputtering – problems associated with Al – Cu interconnect – Comparison of RC delay of Polysilicon, Al.

UNIT 5 ANALYTICAL, ASSEMBLY TECHNIQUES & PACKAGING OF**VLSI DEVICES – NANOMETER TECHNIQUES 12 Hrs.**

Analytical beams – Beams specimen interaction – Chemical methods – package types – baking design considerations – VLSI assembly technology – Package Fabrication Technology. Fabrication challenges at nanometer technologies.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. S.M.Sze "VLSI Technology", Tata Mcgraw Hill, 2003.
2. Sorab. K. Gandhi "VLSI Fabrication and Principles", John Wiley and sons, 1983.
3. Amar Mukherjee "Introduction to NMOS & CMOS VLSI system Design", Prentice Hall, 1986.
4. Mccanny and J.C.White "VLSI Technology and design", Academic Press, 1987.
5. Dasgupta "VLSI Technology", Pearson Education Pvt Ltd 2001

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each – No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5114	DSP INTEGRATED CIRCUITS (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- To familiarize the concept of DSP and DSP algorithms.
- Introduction to Multirate systems and finite word length effects
- To know about the basic DSP processor architectures and the synthesis of the processing elements
- To gather an idea about the VLSI circuit layout design styles

UNIT 1 DIGITAL SIGNAL PROCESSING**12 Hrs.**

Digital signal processing, Sampling of analog signals, Selection of sample frequency, Signal-processing systems, Frequency response, Transfer functions, Adaptive DSP algorithms, DFT-The Discrete Fourier Transform, FFT-The Fast Fourier Transform Algorithm- Butterfly Diagram, DIT-FFT, DIF-FFT, Image coding, Discrete cosine transforms.

UNIT 2 DSP INTEGRATED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES**12 Hrs.**

Standard digital signal processors, Application specific IC's for DSP, DSP systems, DSP system design, Integrated circuit design, MOS transistors, MOS logic, VLSI process technologies, Trends in CMOS technologies

UNIT 3 DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS**12 Hrs.**

FIR filters, FIR filter structures, IIR filters, Specifications of IIR filters, Mapping of analog transfer functions, Mapping of analog filter structures, Multi rate systems, Interpolation with an integer factor L, Sampling rate change with a ratio L/M, Multirate filters. Finite word length effects - Parasitic oscillations, Scaling of signal levels, Round-off noise, Measuring round-off noise, Coefficient sensitivity.

UNIT 4 DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES**12 Hrs.**

DSP system architectures, Standard DSP architecture, Ideal DSP architectures, Multiprocessors and multicomputers, Systolic and Wave front arrays, Shared memory architectures. DSP Processor manufacturers, Types: Fixed and Floating-point processors. Features of DSP Processor: Single Cycle execution, Parallel operation / Multifunction, Zero overhead looping and pipe line concept. Mapping of DSP Algorithms onto hardware, Implementation based on complex PEs, Shared memory architecture with Bit – Serial PEs.

UNIT 5 ARITHMETIC UNITS AND INTEGRATED CIRCUIT DESIGN**12 Hrs.**

Conventional number system, Redundant Number system, Residue Number System. Bit-parallel and Bit-Serial arithmetic, Basic shift accumulator, Reducing the memory size, Complex multipliers, Improved shift-accumulator. Layout of VLSI circuits, FFT processor, DCT processor and Interpolator as case studies.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Lars Wanhammar, "DSP Integrated Circuits", Academic press, New York.,1999.
2. A.V.Oppenheim, etal, "Discrete-time Signal Processing" Pearson education, 3rd Edition, 2009.
3. Emmanuel C. Ifeakor, Barrie W. Jervis, "Digital signal processing – A practical approach", Pearson Edition, 2nd Edition,2009.
4. Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation", John Wiley & Sons, 2nd Edition, 1999.

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each – No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5115	MIXED SIGNAL INTEGRATED CIRCUIT DESIGN (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- To learn the Mixed circuit designing
- To understand the Data Acquisition System
- To get expertise Neural networks

UNIT 1 CURRENTMIRRORS**12 Hrs.**

Analog Octagon –Mixed Cell Layout - Simple CMOS current mirror - source degenerated current mirrors – high output impedance current mirrors – Bipolar current mirrors – Advanced current mirrors : Cascode stage Wilson current mirror- Bipolar current mirrors – Bipolar gain stages - Widlar current mirror - folded cascode and current mirror op amp- Frequency response.

UNIT 2 OP AMP DESIGN**12 Hrs.**

Performance Parameters - All NMOS enhancement mode Operational Amplifier Design - Two stage CMOS op amp – Gain Boosting - op amp as a comparator – Charge injection errors– Linear settling time revisited, fully differential op amp - Stability and Frequency Compensation – Phase margin - Latched Comparators - Basics of OTA Amplifiers Design

UNIT 3 SWITCHED CAPACITOR CIRCUITS**12 Hrs.**

Basic SC circuits: Parallel - Series -Series-Parallel – Bilinear. Operation and Analysis - Switched capacitor amplifier- Switched capacitor integrators – SC Transresistance circuits - Z Domain Model Representation of Switched Capacitor Circuits – Switched Capacitor filter Design - First order and Second order - Switched-Capacitor Common-Mode Feedback.

UNIT 4 DATA ACQUISITION SYSTEMS**12 Hrs.**

Sample and hold circuits – examples of CMOS S/H circuits – Bipolar and BiCMOS S/H circuits – translinear gain cell – Translinear multiplier - Band gap reference basics: Supply Independent Biasing, Temperature Independent References, PTAT Current Generation- High speed A/D and D/A converters - High resolution converters – Sigma delta A/D converter – Interpolative Modulators - Testing of converters

UNIT 5 PLL AND NEURAL INFORMATION PROCESSING**12 Hrs.**

Voltage-Controlled Oscillators - Mathematical Model of VCO - Phase-Locked Loops: Basic PLL Topology - Phase Detector- Loop Filter – Charge Pump PLL – Linearized PLL - Problem of Lock Acquisition - Nonideal Effects in PLLs - Jitter in PLLs - Frequency Synthesizer - Biologically Inspired Neural Networks – ANN Models –Genetic algorithm - Low Power Neural Networks

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. BehzadRazavi "Design of Analog CMOS Integrated circuits", Tata Mcgraw Hill India Pvt.Ltd, 2008.
2. David A Johns and Ken Martin "Analog Integrated circuit design", John wiley& Sons,2004.
3. Allen Holberg, CMOS Analog Circuit Design, Oxford Publications, 2002
4. Franco Maloberti "Analog Design for CMOS VLSI Systems", Kluwer Academic Publisher, 2001.
5. Roger T.Howe and Charles G.Sodini" Micro Electronics an Integrated Approach", Pearson Education Pvt Ltd 2004.
6. Baker, Li, Boyce, CMOS Mixed Circuit Design, Wiley Publications, 2002
7. Roubik Gregorian "Analog MOS Integrated Circuits for Signal Processing", John wiley and sons, 2004
8. Rudy Van de Plassche "CMOS Integrated A/D and D/A converters", Kluwer Academic Publisher, 2003.

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration: 3 Hrs.****PART A : 5 Questions of 6 Marks each – No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5116	MICROCONTROLLERS FOR EMBEDDED SYSTEM DESIGN (For AE & EMB)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- x To study the architecture of 8051 and 8 bit PIC Microcontrollers
- x To understand the concepts of Memory and Peripheral Interfacing with microcontrollers
- To learn assembly language programming for microcontrollers
- x To learn about software design tools used for programming microcontrollers

UNIT 1 REVIEW OF 8051 ARCHITECTURE**12 Hrs.**

Architecture – memory organization – addressing modes – instruction set –Timers - Interrupts -I/O ports, Interfacing I/O Devices – Serial Communication- Assembly language programming – Arithmetic Instructions – Logical Instructions –Single bit Instructions – Timer Counter Programming – Serial Communication Programming- Interrupt Programming

UNIT 2 8 BIT PIC MICROCONTROLLER**12 Hrs.**

Architecture – memory organization – addressing modes – instruction set – PIC programming in Assembly& C –I/O port, Data Conversion, RAM & ROM Allocation, Timer programming

UNIT 3 PERIPHERALS OF PIC MICROCONTROLLER**12 Hrs.**

Timers – Interrupts, I/O ports- A/D converter-UART- I2C bus –SPI- CCP modules -Flash and EEPROM memories- ADC, DAC and Sensor Interfacing

UNIT 4 DEVELOPMENT TOOLS**12 Hrs.**

Host and Target Machines- Linker/Locators for Embedded Software, Debugging Techniques- MPLAB overview: Using MPLAB, Toolbars, Select Development Mode and Device Type, Project, Text Editor-Assembler, MPLAB Operations – Emulators.

UNIT 5 SYSTEM DESIGN – CASE STUDY**12 Hrs.**

Interfacing LCD Display – Keypad Interfacing – Servo motor Control – Controlling DC/ AC appliances – Measurement of frequency – Stand alone Data Acquisition System- Interfacing Wireless Communication modules - RF, Zigbee and GSM modules with microcontrollers

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey ' PIC Microcontroller and Embedded Systems using Assembly and C for PIC18', Pearson Education 2008
2. John Iovine, 'PIC Microcontroller Project Book ', McGraw Hill 2000
3. MykePredko, "Programming and customizing the 8051 microcontroller", Tata McGraw Hill 2001.
4. Muhammad Ali Mazidi, Janice G. Mazidi and Rolin D. McKinlay, 'The 8051 Microcontroller and Embedded Systems' Prentice Hall, 2005.
5. Scott Mackenzie and Raphael C.W. Phan, "The Micro controller", Pearson, Fourth edition 2012

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each-No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5117	ADVANCED HDL PROGRAMMING (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- x To learn the programming in Verilog and System Verilog x
- To understand the RTL design
- x To get expertise in HDL programming

UNIT 1 VERILOG HDL**12 Hrs.**

Basic concepts – Module – Delays - Language elements – Compiler directives, Value set, Data types, Parameters

Expressions - Operands & Operators - Gate level modeling –User defined Primitives – Combination UDP, Sequential UDP.

UNIT 2 MODELING IN VERILOG**12 Hrs.**

Data flow modeling – Continuous Assignment, Net Declaration Assignment - Behavioral modeling - Procedural constructs, Timing Controls, Block Statement, Procedural Assignments – Conditional Statement – Case Statement – Loop Statement – Structural modeling – Module Instantiation, Generate Statement - Hardware modeling examples : Moore FSM, Mealy FSM.

UNIT 3 FEATURES IN VERILOG HDL**12 Hrs.**

Tasks, Functions - System Tasks and Functions – Attributes - Value Change Dump – Race condition - Verification – Modeling a Test Bench – Reading/Writing Vectors from/to a Text File – Switch level modeling

UNIT 4 SYSTEM VERILOG**12 Hrs.**

Introduction to System Verilog – Data types, Arrays, Operators & Expressions – Procedural Statements and Control flow – Tasks and Functions.

UNIT 5 FEATURES IN SYSTEM VERILOG**12 Hrs.**

Classes – Random constraints – Interprocess synchronization and Communication – Scheduling Semantics – Clocking Blocks – Program Block – Assertion – Hierarchy – Interfaces

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. J.Bhasker "Verilog HDL", Prentice Hall, 2000
2. Simon Davidmann, Stuart Sutherland & Peter Flake "System Verilog For Design", Springs Science Business Media, 2006.
3. Stephen Brown "Fundamental of Digital logic with Verilog Design", Tata McGraw Hill, 2008.
4. Mark Zwolinski "Digital System Design with System Verilog", Pearson Education, 2009.
5. Accellera – System Verilog Language Reference Manual, 2004
6. Chris Spear "System Verilog for Verification", Springer 2006

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each – No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC5203	TESTING OF VLSI CIRCUITS (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- x To understand the modeling and types of faults x
- To learn the various test procedures
- x To learn and understand the testing of memories

UNIT 1 INTRODUCTION**12 Hrs.**

Validation and testing of manufactured circuits – Test procedures – Issues in design for Testability – Observability and Controllability Adhoc Testing – Scan based Testing – Boundary scan Design – Design for Testability.

UNIT 2 FAILURES AND FAULTS**12 Hrs.**

Modeling of faults - Stuck at faults- Fault diagnosis of Digital circuits. Test generation techniques for combinational circuits – Boolean difference – D- Algorithm – Detection of multiple faults in combinational circuits.

UNIT 3 TESTING OF SEQUENTIAL CIRCUITS**12 Hrs.**

Test generation for sequential circuits – State table verification - functional fault model – Equivalence Checking- Level sensitive scan design – Clocked Hazard free latches – Arithmetic and Reed Muller Coefficients – Software and Hardware Fault Tolerance.

UNIT 4 BUILT-IN SELF-TEST (BIST)**12 Hrs.**

Test pattern generation for built in self test. Exhaustive pattern generation and deterministic testing – Output response Analysis – Transition count syndrome checking Signature Analysis – Circular BIST-IDDQ testing, scan synthesis.

UNIT 5 TESTABLE MEMORY DESIGN**12 Hrs.**

RAM fault model – Test algorithm for RAMs. GALPAT – March Test – Detection of pattern sensitive faults built in self test techniques for RAM chips. Self testable SRAM architecture. Test generation and BIST for Embedded RAMs.

Max. 60 Hours**TEXT / REFERENCE BOOKS**

1. Michael L.Bushnell & Vishwani. D.Agarwal Kulwer “Essentials of Electronic testing for digital, memory and mixed signal VLSI circuit”, Kluwer academic Publishers 2000.
2. Parag.K.lala “Digital circuit Testing and Testability”, Academic press-2007
3. Alfred L.Crouch “Design for test for Digital ICs and Embedded core systems”, Prentice Hall, 1999.
4. Giovanni De Michele “Synthesis and optimization of digital circuits”, Mcgraw Hill Higher Education, 1994.
5. Meloberti Franco “Analog design for CMOS VLSI systems”, Kluwer Academic Publishers-2001

END SEMESTER EXAM QUESTION PAPER PATTERN**Max. Marks : 100****Exam Duration : 3 Hrs.****PART A : 5 Questions of 6 Marks each – No choice****30 Marks****PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks****70 Marks**

SEC6532	CIRCUIT SIMULATION LAB (For VLSI)	L	T	P	Credits	Total Marks
		0	0	6	3	100

SUGGESTED LIST OF EXPERIMENTS

1. Series and Parallel resonant circuits
2. Constant K filters and Composite filters
3. Attenuators and Equalizers
4. Electrical circuit theorems
 - i) Superposition Theorem
 - ii) Maximum power transfer theorem
 - iii) Thevenin's Theorem
 - iv) Norton's Theorem
 - v) Reciprocity Theorem
5. Waveform Generation Circuits
 - i) Schmitt Trigger
 - ii) Square Wave Generator
 - iii) Switch mode power supply (SMPS)
6. Diode Experiments
 - i) Precision Rectifier
 - ii) Bridge Rectifier
7. Modulation Circuits
 - i) Analog modulation
 - ii) Frequency modulation
8. Internal circuit simulation
 - i) UA741
 - ii) 555 timer
 - iii) LM565
9. Low frequency and High frequency models of MOSFET
10. Instrumentation Amplifier and Operational transconductance amplifier

DIGITAL EXPERIMENTS

1. Full adder using CMOS logic
2. JK Master slave, D and T Flip Flops
3. Ripple counter
4. Barrel Shifter
5. Realization of SOP and POS forms

SEC6533	PROGRAMMING IN HDL LAB (For VLSI)	L	T	P	Credits	Total Marks
		0	0	6	3	100

SUGGESTED LIST OF EXPERIMENTS

VERILOG / SYSTEM VERILOG SIMULATION, SYNTHESIS AND FPGA IMPLEMENTATION OF VERIFICATION OF LOGIC GATES

1. Adders and Subtractors
2. 4 bit fast adders (RCA, CLA, CSA)
3. Design of FF (SR,D,T,JK, Master slave with delays)
4. Design of Code converters & Comparator
5. Design of 8 bit shift registers (SISO, SIPO, PISO, LFSR)
6. Design of Synchronous & Asynchronous Counters
7. Modeling of Moore & Mealy FSM
8. Static & Rolling Display
9. Frequency Multipliers & Dividers
10. Design of ALU
11. Barrel Shifters
12. Design of Memories
13. Design of MAC unit
14. UART model

SEC5605	WIRELESS SENSOR NETWORKS (For AE, EMB, VLSI & CS)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- × To understand the basic concepts about wireless sensor networks.
- × To study the communication protocols, Addressing and synchronization
- × To learn concepts of localization, data storage and tools used for simulation

UNIT 1 OVERVIEW OF WIRELESS SENSOR NETWORKS 12 Hrs.

Characteristics of WSN, Challenges for Wireless Sensor Networks, Enabling Technologies For Wireless Sensor Networks, Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture -Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts.

UNIT 2 COMMUNICATION PROTOCOLS 12 Hrs.

Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks contention-based protocols, schedule-based protocols- Link Layer protocols-Error control-ARQ techniques-FEC techniques-Framing-Link Management.

UNIT 3 ADDRESSING & SYNCHRONISATION 12 Hrs.

Naming and addressing: Address and Name Management, Assignment of MAC Addresses- content- based Addressing -Geographic Addressing; Time synchronization: Sender/ receiver synchronization-receiver/ receiver synchronization.

UNIT 4 INFRASTRUCTURE ESTABLISHMENT 12 Hrs.

Localization and Positioning- Localization -Ranging Techniques -Time of Arrival - Time Difference of Arrival - Angle of Arrival - Received Signal Strength - Range-Based Localization - Triangulation -Range-Free Localization - Ad Hoc Positioning System (APS). **Topology Control-Controlling topology in flat networks-Hierarchical networks; Routing: Geographic routing-Data centric routing-Qos Based protocols.**

UNIT 5 SENSOR NETWORK PLATFORMS AND TOOLS 12 Hrs.

Deployment & Configuration - Sensor deployment, scheduling and coverage issues, self configuration- **Congestion control- Security - Privacy issues - Attacks and countermeasures.**

Max. 60 Hours

TEXT / REFERENCE BOOKS

1. Holger Karl & Andreas Willig, Protocols and Architectures for Wireless Sensor Networks, John Wiley, 2005.
2. Kazem Sohraby, Daniel Minoli and Taieb Znati, Wireless Sensor Networks Technology- Protocols and Applications, John Wiley & Sons, 2007.
3. C.S.Raghavendra Krishna, M.Sivalingam and Tarib znati, Wireless Sensor Networks, Springer, 2006.
4. I.F. Akyildiz, W. Su, Sankarasubramaniam, E. Cayirci, Wireless sensor networks, Elsevier, 2010.
5. Feng Zhao & Leonidas J. Guibas, Wireless Sensor Networks- An Information Processing Approach, Elsevier, 2007.

END SEMESTER EXAM QUESTION PAPER PATTERN

Max Marks : 70

Exam Duration : 3 Hrs.

PART A : 5 Questions of 6 Marks each-No choice

30 Marks

PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks

70 Marks

SEC5622	HIGH SPEED VLSI DESIGN (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

× This course will focus on importance of Clock frequencies, high speed circuit design, clocking techniques and signaling standards.

UNIT 1 LOGIC STYLES IN CMOS VLSI 12 Hrs.

Clocked logic styles, single-Rail Domino logic styles, Dual-Rail Domino structures, Latched Domino structures, clocked pass gate logic- Non clocked logic styles, Static CMOS, DCVS logic, Non-clocked pass Gate Families.

UNIT 2 TECHNIQUES IN INDUCED VARIATIONS 12 Hrs.

Circuit design Margining, Design induced Variations, process induced Variations, Application induced Variations, Noise.

UNIT 3 LATCHES 12 Hrs.

Latching strategies, Basic Latch Design, Latching Differential logic, Hazards, Race Free Latches for Pre-charged logic, Asynchronous latch techniques.

UNIT 4 STANDARD NETWORK DESIGN 12 Hrs.

Signaling standards, chip-to-chip communication Networks, ESD Protection, Standards and Models with design - Skew Tolerant design.

UNIT 5 CLOCKING TECHNIQUES 12 Hrs.

Clocking styles, clock jitter, signal skew, clock skew, and data feed through clock generation, clock distribution, and asynchronous clocking techniques.

Max. 60 Hours

TEXT / REFERENCE BOOKS

1. Kerry Bernstein "High Speed CMOS Design styles", Kulwer Academic Publishers, 2002.
2. Ivan Sutherland, Bob sproull, David Harris "Logical Efforts: Designing Fast CMOS Circuits", Kluwer Academic Publishers, 1999.
3. David Harris, "Skew Tolerant domino Design", Prentice Hall of India Private Ltd, 2000.

END SEMESTER EXAM QUESTION PAPER PATTERN

Max. Marks : 100

Exam Duration : 3 Hrs

Part A : 5 Questions of 6 Marks each – No choice -

30 Marks

Part B : 2 Questions from each unit with internal choice, each carrying 14 Marks

70 Marks

SEC5625	LOW POWER VLSI DESIGN (For VLSI, AE & CS)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

x This course will focus on sources of power dissipation, types of analysis, Low power VLSI design Techniques and methodologies

UNIT 1 INTRODUCTION TO LOW POWER VLSI DESIGN 12 Hrs.

Introduction- Need for Low power VLSI design– Charging and Discharging Capacitance- Short circuit current in CMOS– CMOS leakage current- Static current- Principles of Low power design- Low power figure of Merits.

UNIT 2 POWER ANALYSIS METHODS 12 Hrs.

Simulation power analysis- SPICE circuit analysis- Discrete Transistor Modeling and analysis - Gate Level Logic simulation - Architecture level analysis - Data Correlation analysis in DSP systems - Monte Carlo Simulation – Random Logic signal- Probability Power analysis techniques- Signal entropy.

UNIT 3 GATING AND ENCODING TECHNIQUES 12 Hrs.

Transistor and gate sizing-Network Restructuring and Reorganization- special latches and Flip flops-Low power digital cell library - Gate Reorganization- Signal Gating –Logic Encoding -State Machine encoding-Precomputation Logic.

UNIT 4 SPECIAL TECHNIQUES 12 Hrs.

Special Techniques- Power reduction in clock networks- CMOS floating node -Low power Bus -Delay Balancing- Low power techniques for SRAM- Architecture and system- Power and performance management - Switching activity reduction -Parallel Architecture –Flow graph transformation.

UNIT 5 ADVANCED TECHNIQUES 12 Hrs.

Advanced techniques- Adiabatic Computation- Pass transistor Logic synthesis -Asynchronous circuits – Software Design for Low power- Sources of software power dissipation- Software power optimization.

Max. 60 Hours

TEXT / REFERENCE BOOKS

1. Gary Yeap "Practical Low Power Digital VLSI design", Kluwer Academic Publishers - 1998 Edition
2. Sharat Prasad and Koushik Roy "Low power CMOS VLSI Circuit design", John Wiley Publications", 2000 Edition
3. Kiat Seng Yeo & Kaushik Roy "Low voltage, Low power VLSI subsystems", McGraw-Hill 2009.
4. Meloberti Franco "Analog design for CMOS VLSI systems", Kluwer Academic Publishers-2001
5. Abdellatif Bellaouar "Low-Power Digital VLSI Design: Circuits and Systems", kluwer Academic Publishers - 1995
6. Saraju P. Mohanty- Nagarajan Ranganathan, Elias Kougianos, Priyadarsan Patra "Low-Power High-Level Synthesis for Nanoscale CMOS Circuits", Springer-2008.

END SEMESTER EXAM QUESTION PAPER PATTERN

Max. Marks : 100

Exam Duration : 3 Hrs.

PART A : 5 Questions of 6 Marks each-No choice

30 Marks

PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks

70 Marks

SEC5629	ASIC DESIGN (For VLSI & AE)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

× To understand the basic concepts of ASIC design flow

× To acquire the knowledge about memory architectures and back end of VLSI design × To

learn the fundamentals and recent advancements of SOC and NOC

UNIT 1 INTRODUCTION TO ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN 12 Hrs.

Types of ASICs - Design Flow - CMOS transistors, CMOS design rules - Combinational Logic Cell – Sequential logic cell - Data path logic cell - transistors as resistors - transistor parasitic capacitance - Logical effort - Library cell design - Library architecture.

UNIT 2 PROGRAMMABLE LOGIC CELLS AND I/O CELLS 12 Hrs.

Anti fuse – static RAM – EPROM and EEPROM technology – PREP bench marks – Actel ACT – Xilinx LCA – Altera FLEX – Altera MAX DC & AC inputs and outputs – Clock and power inputs – Xilinx I/O blocks-Actel ACT – Xilinx LCA – Xilinx EPLD – Altera MAX 5000 and 7000 – Altera MAX 9000 Altera FLEX.

UNIT 3 FLOOR PLANNING, PLACEMENT AND ROUTING 12 Hrs.

System partition - FPGA partitioning - partitioning methods - floor planning - placement - physical design flow - global routing - detailed routing - special routing - circuit extraction - DRC.

UNIT 4 SOC FUNDAMENTALS, SOFTWARE AND ENERGY MANAGEMENT 12 Hrs.

Essential issues of SoC design – A SoC for Digital still camera – **multimedia IP development: Image and video Codecs.** SoC embedded software – energy management techniques for SoC design.

UNIT 5 NOC DESIGN 12 Hrs.

Practical Design of NoC, NoC Topology-Analysis Methodology, Energy Exploration, NoC Protocol Design, **Low-Power Design for NoC: Low-Power Signaling, On-Chip Serialization, Low-Power Clocking, Low-Power Channel Coding, Low-Power Switch, Low-Power Network on Chip Protocol.**

Max. 60 Hours

TEXT / REFERENCE BOOKS

1. M.J.S. SMITH, “Application Specific Integrated Circuits”, Addison Wesley Longman Inc., 1997.
2. Youn-Long, Steve Lin, “Essential Issues of SoC Design: Designing Complex Systems - On- Chip”, Springer, 2006.
3. Wolf Wayne, “FPGA Based System Design”, Pearson Education India, 2004.
4. Axel Jantsch, Hannu Tenhunen, “Network on chips”, Kluwer Academic Publishers, 2003.
5. Hoi-jun yoo, Kangmin Lee, Jun Kyoung Kim, “Low power NoC for high performance SoC desing”, CRC press, 2008.
6. Vijay K. Madiseti Chonlameth Arpikanondt, “A Platform-Centric Approach to System- on- Chip (SOC) Design”, Springer, 2005.

END SEMESTER EXAM QUESTION PAPER PATTERN

Max. Marks : 100

Exam Duration: 3 Hrs.

PART A : 5 Questions of 6 Marks each-No choice

30 Marks

PART B : 2 Questions from each unit with internal choice, each carrying 14 Marks

70 Marks

SEC5631	DESIGN OF SEMICONDUCTOR MEMORIES (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

- × To learn the types of Semiconductor Memories with various design techniques.
- × To excel in Advanced Memory Technologies and Memory packaging technologies.
- × To analyze Memory faults and fault modeling

UNIT 1 RANDOM ACCESS MEMORY TECHNOLOGIES 12 Hrs.

Static Random Access Memory(SRAMs):SRAM cell structure-MOS SRAM architecture-MOS SRAM cell and peripheral circuit operation-bipolar SRAM technologies- Silicon on insulator(SOI) technology-advanced SRAM architectures and technologies, application specific SRAMs-CMOS CRAMs - DRAMs cell theory and advanced cell structures-BiCMOS DRAMs-soft error failure in DRAMs -Advanced DRAM designs and architecture-application specific DRAMs.

UNIT 2 NONVOLATILE MEMORIES 12 Hrs.

Masked Read-only memories (ROMs):High density ROMs-Programmable read only memories(PROMs) – Bipolar PROMs- CMOS PROMs-erasable (UV)- Programmable read only memories (EPROMs)-Floating Gate EPROM cell-one - time programmable (OTP) EPROMs-Electrically Erasable PROMs(EEPROMs)- EEPROM technology and architecture – non-volatile SRAM-Flash memories(EPROMs or EEPROM)-Advanced flash memory architecture –Phase Change Memory–Design Techniques of PCM–Magnetoresistive RAM– Resistive RAM.

UNIT 3 ADVANCED MEMORY TECHNOLOGIES AND HIGH –DENSITY MEMORY PACKAGING TECHNOLOGIES 12 Hrs.

Ferroelectric Random Access Memories (FRAMs)-Gallium Arsenide (GaAs) FRAMs-Analog memories magnetoresistive random access memories (MRAMs) – Experimental memory devices. Memory hybrids and MCMs (2D)-Memory stacks and MCMs (3D)-Memory MCM testing and reliability issues-memory cards-high density memory packaging future directions.

UNIT 4 SEMICONDUCTOR MEMORY RELIABILITY AND RADIATION EFFECTS 12 Hrs.

General Reliability issues-RAM failure modes and mechanism-nonvolatile memory reliability-reliability modelling and failure rate prediction- design for reliability-reliability test structures-reliability screening and qualification. Radiation effects-single event phenomenon (SEP)-radiation hardening techniques-radiation hardening process and design issues-radiation hardened memory characteristics-radiation hardness assurance and testing-radiation dosimetry – water level radiation testing and structures.

UNIT 5 MEMORY FAULT MODELING, TESTING AND MEMORY DESIGN FOR TESTABILITY & FAULT TOLERANCE 12 Hrs.

RAM fault modelling, electrical testing, Pseudo random testing-megabit DRAM-nonvolatile memory modelling and testing-IDDQ fault modelling and testing-application specific memory testing and the tools for fault modelling and testing.

Max. 60 Hours

TEXT / REFERENCE BOOKS

1. Ashok K.Sharma "Semiconductor Memories Technology, testing and reliability", IEEE Press, 1997.
2. Ivan Sutherland Bob sproull, David Harris, "Logical Efforts, Designing Fast CMOS Circuits", Kluwer Academic Press, 1999.
3. David Harris, "Skew Tolerant domino Design", Prentice Hall of India Private Ltd, 2000
4. Hai Li, "Nonvolatile Memory Design: Magnetic, Resistive, and Phase Change", CRC Press, December 19, 2011.

END SEMESTER EXAM QUESTION PAPER PATTERN

Max. Marks : 100

Exam Duration : 3 Hrs.

Part A : 5 Questions of 6 Marks each – No choice -

30 Marks

Part B : 2 Questions from each unit with internal choice, each carrying 14 Marks

70 Marks

SEC5646	NANO ELECTRONICS AND SENSORS (For VLSI)	L	T	P	Credits	Total Marks
		4	0	0	4	100

COURSE OBJECTIVES

× To understand the basic concepts of Nanoelectronics and Nanosensors. × To acquire the knowledge of advancements in MOSFET Devices. × To learn the basic concepts of Carbon Nanotubes.

× To be familiar with the Applications of Nanosensors.

UNIT 1 FUNDAMENTALS OF NANO ELECTRONICS 12 Hrs.

Fundamentals of logic devices:- Requirements – dynamic properties – threshold gates; physical limits to computations; concepts of logic devices:- classifications – two terminal devices – field effect devices – coulomb blockade devices – spintronics – quantum cellular automata – quantum computing – DNA computer; performance of information processing systems;- basic binary operations, measure of performance processing capability of biological neurons – performance estimation for the human brain. Ultimate computation: - power dissipation limit – dissipation in reversible computation – the ultimate computer.

UNIT 2 SILICON MOSFETS & QUANTUM TRANSPORT DEVICES 12 Hrs.

Silicon MOSFETS - Novel materials and alternate concepts:- fundamentals of MOSFET Devices- scaling rules – silicon-dioxide based gate dielectrics – metal gates – junctions & contacts–advanced MOSFET concepts-Quantum transport devices based on resonant tunneling:- Electron tunneling – resonant tunneling diodes – resonant tunneling devices; Single electron devices for logic applications:- Single electron devices – applications of single electron devices to logic circuits.

UNIT 3 CARBON NANOTUBES 12 Hrs.

Carbon Nanotube: Fullerenes – types of nanotubes – formation of nanotubes – assemblies – purification of carbon nanotubes – electronic properties – synthesis of carbon nanotubes – carbon nanotube interconnects – carbon nanotube FETs –Nanotube for memory applications – prospects of an all carbon nanotube nanoelectronics.

UNIT 4 INTRODUCTION TO NANO SENSORS 12 Hrs.

Fundamentals of Nano Sensors: Micro and nano-sensors, Fundamentals of sensors, biosensor, micro fluids, MEMS and NEMS, Packaging and characterization of sensors, Method of packaging at zero level, dye level and first level Sensors.

UNIT 5 NANO SENSORS AND ITS APPLICATIONS 12 Hrs.

Nanoparticles and Micro-organism- Biosensors- Bioreceptors and their properties - Biochips- Integrated nanosensor networks for detection and response- DNA based biosensors and diagnostics- Natural nanocomposite systems; spider silk, bones, shells - Nanomaterials in bone substitutes and dentistry – Implants and Prosthesis – Tissue Engineering – Neuroscience -Neuro-electronic Interfaces –Nanorobotics – Photodynamic Therapy – Protein Engineering – Nanosensors in Diagnosis–Drug delivery – Cancer therapy and Other therapeutic applications.

Max. 60 Hours

TEXT / REFERENCE BOOKS

1. Rainer Waser (Ed.), Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley-VCH, 2003
2. Meixner H., "Sensors: Micro & Nanosensors, Sensor Market trends" Wiley-VCH, 1995.
3. Neelina H. Malsch (Ed.), "Biomedical Nanotechnology", CRC Press 2005.
4. Raguse, Nanotechnology: Basic Science and Emerging Technologies, Chapman & Hall / CRC, 2002
5. T. Pradeep, NANO: The Essentials – Understanding Nanoscience and Nanotechnology, TMH, 2007

END SEMESTER EXAM QUESTION PAPER PATTERN

Max. Marks : 100

Exam Duration : 3 Hrs.

Part A : 5 Questions of 6 Marks each – No choice -

30 Marks

Part B : 2 Questions from each unit with internal choice, each carrying 14 Marks

70 Marks

SECA7001	SYSTEM ON CHIP DESIGN AND VERIFICATION (For VLSI)	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To study about the IP cores and application specific design that is becoming the order of the day.
- To learn System on chip fundamentals, their applications.
- To gain knowledge on NOC design.
- To learn the various computation models of SOC.

UNIT 1 INTRODUCTION TO THE SOC APPROACH**9 Hrs.**

System Architecture, Processor Architectures, Memory and Addressing, Review of Moore's law and CMOS Scaling, Comparison on System-on-Board, System-on-Chip, and System-in-Package- benefits of system-on-chip integration in terms of cost, power, and performance - SOC Design, Platform-Based SoC Design., Multiprocessor SoC and Network on Chip, Low-Power SoC Design, System Architecture and Complexity SoC Design.

UNIT 2 PROCESSORS AND SYSTEM ON CHIP DESIGN PROCESS**9 Hrs.**

Processor Selection for SOC, Robust Processors- Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors-Acanonical SoC Design, SoC Design flow waterfall vs spiral, top down vs Bottom up- Specification requirement, Types of Specification , System Design process and design issues, Soft IP Vs Hard IP, IP verification and integration, hardware-software co-design, Design for timing closure, Logic design issues Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in an SOC.

UNIT 3 EMBEDDED MEMORIES**9 Hrs.**

Overview of SOC external memory, Internal Memory, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, memory interaction, Cache coherence, MESI protocol and Directory-based coherence.

UNIT 4 NOC-BASED SOC**9 Hrs.**

Network on Chip (NOC), Architecture of NoC -Network on Chip topologies-Mesh-based NoC.- Routing in an NoC- Packet switching and wormhole routing- NoC Protocol Design, Low-Power Design for NoC, Low-Power Network on Chip Protocol, Low-Power Channel Coding, Low-Power Clocking, Low-Power Signaling, On-Chip Serialization.

UNIT 5 NOC / MPSoCs**9 Hrs.**

Real Chip Implementation-BONE Series, Industrial Implementations-, Intel's Tera-FLOP 80-Core NoC, MPSoCs. Techniques for designing MPSoCs, Performance and flexibility for MPSoCs design. Case study: A Low Power Open Multimedia Application Platform for 3G Wireless

Max. 45 Hrs.**COURSE OUTCOMES**

On completion of the course, student will be able to

- CO1 - Remember the fundamentals of SoC design.
- CO2 - Understand the design of processors and SoC.
- CO3 - Analyze the design procedures of SoC memories.
- CO4 - Apply low-power design techniques onNoC.
- CO5 - Evaluate the design and performance of MPSoCs.
- CO6 - Create Low Power Application Platform for 3G wireless.

TEXT / REFERENCE BOOKS

1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiley India Pvt. Ltd., 2011.
2. Furber, "ARM System-on-Chip Architecture", Pearson Education India (2014).
3. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, "Low power NoC for high performance SoC Design", CRC Press, 2008.
4. Vijay Madisetti & Chonlameth Arpniakanondt, "A Platform-Centric Approach to System-on-Chip (SOC) Design", Springer, 2010.
5. Sudeep Pasricha and NikilDutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers, 2008.
6. Ahmed Amine Jeraya, Wayne Wolf, "Multiprocessor System On chip", Morgan Kauffmann, 2010.
7. James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition, 2009.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN**Max. Marks: 100****Exam Duration: 3 Hrs.****PART A:** 5 Questions of 6 Marks each – No choice**30 Marks****PART B:** 2 Questions from each unit of internal choice, each carrying 14 Marks**70 Marks**

SECA7002	VLSI FOR WIRELESS COMMUNICATIONS (For VLSI)	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To learn the concept of fading in Communication.
- To study the design concepts of low noise amplifiers.
- To study the concept of filter and learn about Design Parameters.
- To understand the various types of mixers designed for wireless communication.

UNIT 1 INTRODUCTION**9 Hrs.**

Review of Modulation Schemes – BFSK - BPSK - QPSK - OQPSK - Classical Channel - Additive White Gaussian Noise - Finite Channel Bandwidth - Wireless Channel- Path Environment - Path Loss - Friis Equation - Multipath Fading - Channel Model - Envelope Fading - Frequency Selective Fading - Fast Fading - Comparison of different types of Fading.

UNIT 2 RECEIVER ARCHITECTURES**9 Hrs.**

Receiver Front End - Motivations - General Design Philosophy - Heterodyne and Other architectures - Filter Design - Band Selection Filter - Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion - Intermodulation - Cascaded Nonlinear Stages - Gain Compression - Blocking - Noise - Noise Sources - Noise Figure - Design of Front end parameter for DECT.

UNIT 3 LOW NOISE AMPLIFIER**9 Hrs.**

LNA: Low Noise Amplifier Design - Wideband LNA - Design Narrowband LNA - Impedance Matching - Power matching - Salient features of LNA - Core Amplifier Design. Active Mixer - Balancing - Gilbert Mixer - Analysis - Noise - Complete Active mixer

UNIT 4 ANALOG TO DIGITAL CONVERTERS**9 Hrs.**

Demodulators - Delta Modulators - Low Pass Sigma Delta Modulators - High Order Modulators - One Bit DAC and ADC - Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators - Comparison - PLL based Frequency Synthesizer - Loop Filter Design and Implementation.

UNIT 5 SPREAD SPECTRUM**9 Hrs.**

Review of Spread Spectrum - DSSS - FHSS - Basic Principle of DSSS - Modulation – Demodulation - Performance in the presence of noise-narrowband and wideband interferences. Implementations: VLSI architecture for Multitier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing.

Max.45 Hrs.**COURSE OUTCOMES**

On completion of the course, student will be able to

- CO1 - Remember the fundamentals of Modulation Schemes.
- CO2 - Understand the design of Filters.
- CO3 - Analyze the design procedures of Low Noise Amplifier.
- CO4 - Apply modulators in applications.
- CO5 - Evaluate the design and performance of Spread Spectrum.
- CO6 - Create Application Platform for VLSI Architecture.

TEXT / REFERENCE BOOKS

1. Bosco Leung, "VLSI for Wireless Communication", Prentice Hall, 2002.
2. Andreas F.Molisch, "Wideband Wireless Digital Communication", Prentice Hall PTR, 2001.
3. George V. Tsoulous, "Adaptive Antennas for wireless Communication", IEEE Press, 2001.
4. Xiaodong Wang and H.Vincent, "Wireless Communication System, Advanced Reception", Pearson Education, 2004.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN**Max. Marks: 100****Exam Duration: 3 Hrs.****PART A:** 5 Questions of 6 Marks each – No choice**30 Marks****PART B:** 2 Questions from each unit of internal choice, each carrying 14 Marks**70 Marks**

SECA7016	NANO ELECTRONICS AND SENSORS (For VLSI And AE)	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To understand the basic concepts of Nanoelectronics and Nanosensors.
- To acquire the knowledge of advancements in MOSFET Devices.
- To learn the basic concepts of Carbon Nanotubes.
- To be familiar with the Applications of Nanosensors.

UNIT 1 FUNDAMENTALS OF NANO ELECTRONICS**9 Hrs.**

Fundamentals of logic devices: Requirements - dynamic properties - threshold gates; physical limits to computations; concepts of logic devices: classifications - two terminal devices - field effect devices - coulomb blockade devices - spintronics - quantum cellular automata - quantum computing - DNA computer; performance of information processing systems- basic binary operations, measure of performance processing capability of biological neurons - performance estimation for the human brain. Ultimate computation: power dissipation limit - dissipation in reversible computation - the ultimate computer.

UNIT 2 SILICON MOSFETS AND QUANTUM TRANSPORT DEVICES**9 Hrs.**

Silicon MOSFETS - Novel materials and alternate concepts:- fundamentals of MOSFET Devices - scaling rules - silicon-dioxide based gate dielectrics - metal gates - junctions & contacts - advanced MOSFET concepts - Quantum transport devices based on resonant tunneling: Electron tunneling - resonant tunneling diodes - resonant tunneling devices; Single electron devices for logic applications: Single electron devices - applications of single electron devices to logic circuits.

UNIT 3 CARBON NANOTUBES**9 Hrs.**

Carbon Nanotube: Fullerenes - types of nanotubes - formation of nanotubes – assemblies - purification of carbon nanotubes - electronic properties - synthesis of carbon nanotubes - carbon nanotube interconnects - carbon nanotube FETs - Nanotube for memory applications - prospects of an all carbon nano tube nano electronics.

UNIT 4 INTRODUCTION TO NANOSENSORS**9 Hrs.**

Fundamentals of Nano Sensors: Micro and nano-sensors, Fundamentals of sensors, biosensor, micro fluids, MEMS and NEMS, Packaging and characterization of sensors, Method of packaging at zero level, dye level and first level Sensors.

UNIT 5 NANO SENSORS AND ITS APPLICATIONS**9 Hrs.**

Nanoparticles and Micro-organism - Biosensors - Bioreceptors and their properties – Biochips - Integrated nanosensor networks for detection and response - DNA based biosensors and diagnostics - Natural nanocomposite systems; spider silk, bones, shells - Nanomaterials in bone substitutes and dentistry - Implants and Prosthesis - Tissue Engineering - Neuroscience - Neuro-electronic Interfaces - Nanorobotics - Photodynamic Therapy - Protein Engineering - Nanosensors in Diagnosis - Drug delivery - Cancer therapy and Other therapeutic applications.

Max. 45 Hrs.**COURSE OUTCOMES**

On completion of the course, student will be able to

- CO1 - Understand the fundamentals of nanoelectronics.
- CO2 - Analyse the material concepts for quantum devices.
- CO3 - Describe the carbon nanotubes.
- CO4 - Explain the method of packaging of nano sensors.
- CO5 - Apply the nano particles for designing bio sensors.
- CO6 - Design the nanosensor for bio application.

TEXT / REFERENCE BOOKS

1. Rainer Waser (Ed.), "Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices", Wiley VCH, 2003.
2. Meixner H., "Sensors: Micro & Nanosensors, Sensor Market trends", Wiley VCH, 1995.
3. Neelina H. Malsch (Ed.), "Biomedical Nanotechnology", CRC Press, 2005.
4. Raguse, "Nanotechnology: Basic Science and Emerging Technologies", Chapman & Hall/CRC, 2002.
5. T.Pradeep, "NANO: The Essentials – Understanding Nanoscience and Nanotechnology", TMH, 2007.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN**Max. Marks: 100****Exam Duration: 3 Hrs.****PART A:** 5 Questions of 6 Marks each – No choice**30 Marks****PART B:** 2 Questions from each unit of internal choice, each carrying 14 Marks**70 Marks**