

ANALYSIS OF AN EFFICIENT SRAM ARRAY ARCHITECTURE FOR HIGH-SPEED APPLICATIONS

Submitted in partial fulfilment of the requirements for the award of Bachelor of
Engineering degree in Electronics and Communication Engineering

by

DEVA DHARSHINI S (40130043)

DENDUKURI NAGA HARSHITHA (40130041)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHOOL OF ELECTRICAL AND ELECTRONICS

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Categrory-1 UNIVERSITY BY UGC

**Accredited with Grade "A" by AAC | 12 B Status by UGC | Approved by AICTE
JEPPIAAR NAGAR, 100/101/102, GANDHI SALAI, CHENNAI - 600 119**

APRIL - 2024

ANALYSIS OF AN EFFICIENT SRAM ARRAY ARCHITECTURE FOR HIGH-SPEED APPLICATIONS

Submitted in partial fulfilment of the requirements for the award of Bachelor of
Engineering degree in Electronics and Communication Engineering

by

DEVA DHARSHINI S (40130043)

DENDUKURI NAGA HARSHITHA (40130041)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHOOL OF ELECTRICAL AND ELECTRONICS

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Category -1 UNIVERSITY BY UGC

**Accredited with Grade "A++" by NAAC | 12 B Status by UGC | Approved by AICTE
JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119**

APRIL - 2024



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

CATEGORY-I UNIVERSITY BY UGC

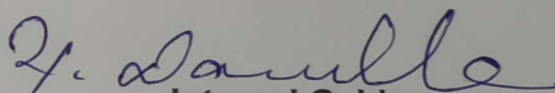
Accredited "A++" Grade by NAAC | 12B Status by UGC | Approved by AICTE

www.sathyabama.ac.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **Deva Dharshini S (40130043)** and **Dendukuri Naga Harshitha (40130041)** who carried out the Project entitled "**ANALYSIS OF AN EFFICIENT SRAM ARRAY ARCHITECTURE FOR HIGH-SPEED APPLICATIONS**" under my supervision from November 2023 to April 2024.


Internal Guide

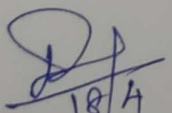
Dr. R. NARMADHA, M.E., Ph.D.,



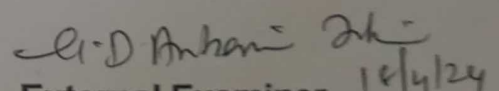
Head of the Department

Dr. T. RAVI, M.E., Ph.D.,

Submitted for Viva voce Examination held on 18-04-2024


18/4

Internal Examiner


18/4/24

External Examiner

DECLARATION

We Deva Dharshini S (40130043), Dendukuri Naga Harshitha (40130041) hereby declare that the Project Report entitled "Analysis of an efficient SRAM array architecture for high-speed applications" done by us under the guidance of Dr.R.Narmadha.,M.E., Ph.D is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

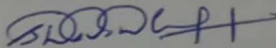
DATE: 18.04.2024

PLACE: CHENNAI

1.



2.



SIGNATURE OF THE CANDIDATES

ACKNOWLEDGEMENT

I am pleased to acknowledge our sincere thanks to **Board of Management of Satyabhama Institute of Science and Technology** for their kind encouragement in doing this project and for completing it successfully. We are grateful to them.

I convey our thanks to **Dr. N. M. NANDHITHA, M.E., Ph.D., Professor & Dean, School of Electrical and Electronics** and **Dr. T. RAVI, Ph.D., Professor & Head, Department of Electronics and Communication Engineering** for providing us necessary support and details at the right time during the progressive reviews.

I would like to express our sincere and deep sense of gratitude to our Project Guide **DR.R.NARMADHA.,M.E., PH.D**, for her valuable guidance, suggestions and constant encouragement which paved way for the successful completion of our project work.

I wish to express our thanks to all Teaching and Non-Teaching staff members of the **Department of Electronics and Communication Engineering** who were helpful in many ways for the completion of the project.

ABSTRACT

This project represents a significant endeavour, delving deep into the complexities of a newly devised SRAM (Static Random Access Memory) array architecture tailored explicitly to address the pressing needs of high-speed applications. In the contemporary landscape of computational systems, where the pace of operations is ever-accelerating, the optimization of SRAM arrays stands as a crucial pillar supporting the efficiency and performance of these systems. At its core, the project revolves around the meticulous examination of the proposed SRAM architecture, employing sophisticated simulation methodologies to assess its efficacy in enabling swift and seamless memory operations. The scrutiny extends across a spectrum of critical parameters, including access time, power consumption, area efficiency, and overall stability. Through this comprehensive analysis, the project aims to provide a holistic understanding of the architectural nuances and performance characteristics of the proposed SRAM array. A key aspect of the project involves conducting comparative evaluations against established SRAM architectures prevalent in the field. By juxtaposing the proposed design with existing solutions, the project endeavours to illuminate both its strengths and limitations. Such insights are invaluable in informing further refinements and optimizations, steering the evolution of SRAM architectures towards greater efficiency and efficacy. The findings derived from this exhaustive exploration offer more than mere theoretical insights; they serve as practical guidelines for crafting SRAM arrays that are not only adept at meeting the demands of modern computing paradigms but also excel in surpassing them. With applications spanning diverse domains such as advanced computing, artificial intelligence, and high-performance computing, the significance of this project reverberates across the technological landscape. In an era where rapid data access and processing are the cornerstones of technological advancement, the quest for robust and efficient SRAM architectures assumes paramount importance. By providing a roadmap for the development of such architectures, capable of powering high-speed applications with unparalleled efficiency, this project stands poised to leave a lasting impact on the trajectory of computational innovation.