

# **PERFORMANCE ANALYSIS OF AN EFFICIENT COMPRESSOR FOR MULTIPLIER DESIGN**

Submitted in partial fulfillment of the requirements for the award of Bachelor of  
Engineering Degree in Electronics and Communication Engineering

by

**ADEEBA FAIZ(40130001)**

**DAMINENI SHALINI(40130038)**



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING  
SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING**

## **SATHYABAMA**

**INSTITUTE OF SCIENCE AND TECHNOLOGY  
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**JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119**

**APRIL - 2024**



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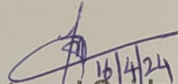
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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

## BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **ADEEBA FAIZ (40130001)** and **DAMINENI SHALINI (40130038)**, who carried out the project entitled "**PERFORMANCE ANALYSIS OF AN EFFICIENT COMPRESSOR FOR MULTIPLIER DESIGN**" under our supervision from NOVEMBER 2023 to APRIL 2024.

  
16/4/24  
Internal Guide

Dr.F.V.JAYASUDHA., M.E., PhD.,

  
Head of the Department  
Dr.T.RAVI.,M.E.,Ph.D.,

Submitted for Viva voce Examination held on \_\_\_\_\_

Internal Examiner

External Examiner

## DECLARATION

We ADEEBA FAIZ (40130001) and DAMINENI SHALINI(40130038), hereby declare that the Project Report entitled "PERFORMANCE ANALYSIS OF AN EFFICIENT COMPRESSOR FOR MULTIPLIER DESIGN" done by us under the guidance of Dr. F. V. JayaSudha., M.E., PhD, Associate Professor, Dept. of Electronics and Communication Engineering at SATHYABAMA INSTITUTE OF SCIENCE AND TECHNOLOGY, CHENNAI is submitted in partial fulfillment of the requirements for the award of the Bachelor of Engineering degree in Electronics and Communication Engineering.

DATE: 16.04.2024

PLACE: Chennai

SIGNATURE OF THE CANDIDATES

*Adeeba Faiz*

*Shalini*

## ACKNOWLEDGEMENT

I am pleased to acknowledge our sincere thanks to Board of Management of **SATHYABAMA** for their kind encouragement in doing this project and for completing it successfully. I am grateful to them.

I convey my thanks to **Dr. N.M. NANDHITHA, M.E., Ph.D., Dean, School of Electrical and Electronics** and **Dr. T. RAVI, M.E., Ph.D., Head of the Department, Department of Electronics and Communication Engineering** for providing me necessary support and details at the right time during the progressive reviews.

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# **CHAPTER 1**

## **INTRODUCTION**

VLSI is the technique of integrating lots of transistors right into a single chip. VLSI format is specifically used to limit the interconnecting material location. The principal factors which limit the development of smaller and more complex IC chip are the IC fabrication era, style designer productiveness and the fee. Depending on the utility, distinctive performance additives come to be critical. The Arithmetic Logic Unit (ALU) can be a simple building block of the Central Technique Unit (CPU) of a computer. Even one of the great microprocess or contains one ALU for functions along with keeping timers.

ALU is a middle factor of all most important processing unit inner in a laptop and is an critical a part of the execution unit. ALU is capable of calculating the results of a wide fashion of primary arithmetical and logical computations. The ALU takes as input the statistics to be operated on (called operands) and a code from the management unit indicating that operation to perform. The output is the end result of the computation. The ALU carried out will perform the subsequent operations: Arithmetic operations (addition, subtraction, increment, decrement, transfer). Logic operations (AND, NOT, OR, NAND, NOR, EX-OR, EX-NOR)

A combinational circuit that plays the addition of bits is called an Adder. Each laptop has an adder positioned in its CPU(ALU) that is liable for the method of addition. They also are used in different additives of the processor, wherein they may be used to calculate addresses, table indices, increment and decrement operators, and similar operations. The half of adder outputs a sum of the two inputs and a supply charge. A complete adder is a logical circuit that plays an addition operation on 3 one-bit binary numbers. The complete adder produces a sum of the 3 inputs and carry fee. Multipliers are very vital factor in Digital Signal Processing Systems and Embedded application. The performance of any multiplier will depend on strength, put off and place. Recent works in VLSI Design to reduce big quantity of Multiplier's energy intake. Multipliers carry out one of the maximum regularly arithmetic operations varying inputs. Multipliers are the principle resources of power intake in these gadgets. The area and velocity of the

multiplier is an essential difficulty, increment in pace consequences in massive area intake and vice versa

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### **1.1 MOTIVATIONS**

Energy efficiency has emerged jointly of the foremost crucial fashion parameters in updated computer gadget style. Approximate computing could be a brand new computing paradigm to obtain power efficiency by means of buying and selling- off energy/place/latency upgrades with accuracy for errors-resilient packages. There is a continual call for for strength-green yet compute- in depth designs for modern applications together with multimedia, virtual signal processing(DSP), and device learning-primarily based packages. To gain transformational power discounts the improvements in era nodes, voltage scaling, or designing parallel architectures are inadequate. There is an urgent want to sell opportunity computing strategies to deal with high power necessities for rising programs.

Out of 4 fundamental arithmetic operations, the division operation is carried out from time to time even as its electricity intake, latency, and complexity are more as compared to different mathematics operations. Approximate multiplier layout components like adders and compressor had been simplified to be used in approximate multiplier circuit. Division operation is used in some of the photograph/video processing tasks inclusive of compression, pixel division, foreground extraction, and so on. However, as using digital photo/video and signal processing techniques becomes greater customary, the significance of mathematics operation like division is gaining momentum.

There is a persistent demand for power-efficient yet compute intensive designs for modern packages together with multimedia, digital sign processing (DSP), and system getting to know-based programs. To achieve transformational power discounts the enhancements in generation nodes, voltage scaling, or designing parallel architectures are insufficient.

One magnificence of strategies which may be applied in such scenario is based on this. However, the use of approximate computing techniques results in a trade-off between circuit parameters (vicinity, delay, and power) with the output accuracy. The computational satisfactory in addition to the available power necessities of an application varies at runtime.

## **1.2 LOGIC GATES**

A properly judgment gate is an idealized version of computation or bodily virtual tool imposing a Boolean characteristic, a logical operation accomplished on one or greater binary inputs that produces a unmarried binary output. The bits stored in such registers may be made to transport in the registers and in/out of the registers through making use of clock pulses. An n-bit shift check in may be shaped thru connecting n flip-flops wherein every flip flop shops a single little bit of data. A sign on can be defined as at the same time as a hard and fast of FFs may be related within the series, the definition of the shift test in is even as the stored records may be moved within the registers. It is a sequential circuit, specially used to hold embody such gadgets as multiplexers, registers, arithmetic logic gadgets (ALUs), and laptop memory, all of the manner up through whole microprocessors, which can also contain greater than a hundred million gates. In present day-day exercising, maximum gates are made from MOSFETs (steel–oxide–semiconductor concern effect transistors).

### **A. Types of Logic Gates**

Logic gates are of many sorts majorly by their mode of operation. NAND and NOR gates are referred to as usual gates, because using the ones we

can design another logic circuits. There are six (6) basic types of common sense gates that are listed below NAND gate – (not AND)

- AND gate
- NOR gate – (not OR)
- OR gate
- XOR gate
- NOT gate

### **1.2.1 NAND GATE**

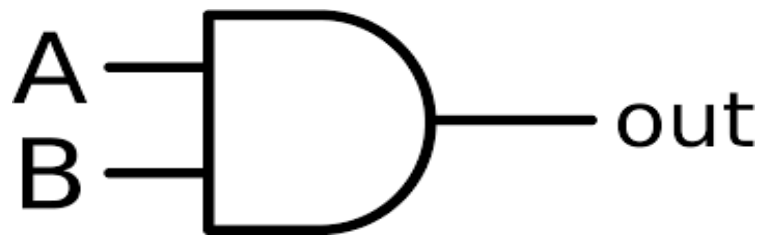


**Fig:1.1: NAND gate**

There are two inputs and one output basically, it is also one of the universal gates. It is simply an opposite to AND gate and the function is also the opposite to the AND. Hence, this the brief explanation about NAND gate.

### **1.2.2 AND GATE**

The second form of good judgment gate we may be considering is the Serial in – Parallel out shift test in. The AND gate is a primary virtual logic gate that implements logical conjunction. The output is HIGH (1) first-rate if all of the inputs to the AND gate is HIGH (1). If none or not all inputs to the AND gate is HIGH, LOW output outcomes. An AND gate can be designed using handiest N-channel(pictured) or P- channel MOSFETs, however is usually done with every (CMOS).The virtual inputs a and b reason the output to have the identical result due to the fact the AND function. The feature may be prolonged to any kind of inputs. It is really a contrary to NAND gate and the characteristic is likewise the alternative to the nand.



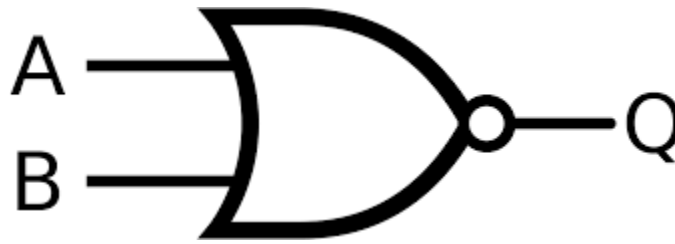
***Fig:1.2: AND gate***

The feature may be prolonged to any number of inputs. It is in reality an contrary to NAND gate and the function is likewise the other to the NAND. Hence, this the brief clarification approximately AND gate.

### **1.2.3 NOR GATE**

The NOR gate might be a virtual circuit that implements logical NOR it behaves according to the reality table to the proper. A HIGH output (1) consequences if each the inputs to the gate vicinity unit LOW (0); if one or each input is HIGH (1), a output (0) result. Nor is the consequences of the negation of the OR operator. It can also in a few senses be visible because the inverse of AN AND circuit. Neither is a operationally complete operation—NOR gates might be mixed to get the alternative logical characteristic. This property is shared with NAND gate. In opposition to this, the OR operator is monotonic because it will solely amendment LOW to HIGH but not contrariwise

In maximum, however no longer all, circuit implementations, the negation comes free of charge—which includes CMOS and TTL. In such good judgment families, OR is the more complicated operation; it may use a NOR observed by way of a NOT. NOR Gates are basic common sense gates, and as such they are known in TTL and CMOS IC'S. Hence, this the brief explanation approximately AND gate



**Fig:1.3: NOR gate**

#### **1.2.4 OR GATE**

The OR gate is a digital logic gate that implements logical disjunction – it acts in step with the reality desk of it. The output is HIGH if one or each of the inputs are HIGH. If neither enter is high, a LOW output. In another feel, the function of OR successfully unearths the maximum among binary digits, just because the complementary AND function unearths the minimal. OR gates are primary logic gates, and are to be had in TTL and CMOS ICs good judgment households. The preferred 4000 collection CMOS IC is the 4071, which incorporates 4 unbiased two-input OR gates. The TTL device is the 7432. In addition to the standard 2-input OR gate, 3- and 4-input OR gates also are available. The good judgment circuit given below in figure 1. Four [12] suggests the OR gate.

With energetic low open collector common sense outputs, as used for manipulate alerts in lots of circuits, an OR characteristic may be produced by means of wiring collectively numerous outputs. This association is called a stressed out OR. This implementation of an OR feature usually is also determined in included circuits of N or P-kind most effective transistor strategies. Hence, this is the quick clarification approximately OR gate.



**Fig:1.4: OR gate(Source [12])**

### **1.2.5 NOT gate & XNOR gate**

XOR gate is a virtual common sense gate that offers a true (1 or HIGH) output when the number of genuine inputs is atypical. An XOR gate implements an exceptional or; that is, a real output comes if one, and handiest one, of the inputs to the gate is real. If both inputs are fake (zero/LOW) or both are true, a fake output result. XOR represents the inequality feature, i.e., the output is genuine if the inputs aren't alike in any other case the output is fake. Whereas, an inverter circuit outputs a voltage representing the opposite good judgment-level to its input. Its important characteristic is to invert the enter signal applied. If the applied input is low then the output turns into excessive and vice versa. Inverters can be built the usage of a unmarried NMOS transistor or a single PMOS transistor coupled with a resistor. Since this 'resistive-drain' technique makes use of simplest a unmarried type of transistor, it could be fabricated at a low value.

#### ***B. Applications of Logic gates:***

Logic gates are used to increase digital circuits like

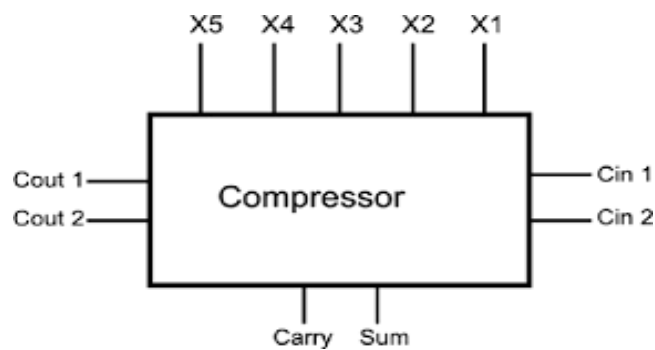
- Microprocessor
- Microcontroller
- Embedded structures
- And additionally, in numerous electronic and electrical circuits.

A good judgment gate is an idealized version of computation or bodily digital tool imposing a Boolean characteristic, a logical operation accomplished on one or more binary inputs that produces a unmarried binary output. The bits saved in such registers can be made to move within the registers and in/out of the registers via making use of clock pulses. An n-bit shift sign in can be fashioned by using connecting n flip-flops where each turn flop stores a unmarried little bit of statistics. A sign up may be described as whilst a hard and fast of FFs may be related inside the collection, the definition of the shift register is while the stored facts can be moved in the registers. It is a sequential circuit, particularly used to keep consist of such gadgets as multiplexers, registers, mathematics common sense devices (ALUs), and pc reminiscence, all of the way up via complete microprocessors, which may additionally include more than a hundred million

gates. In modern practice, most gates are crafted from MOSFETs (metallic–oxide–semiconductor subject effect transistors).

### 1.3 ADDER

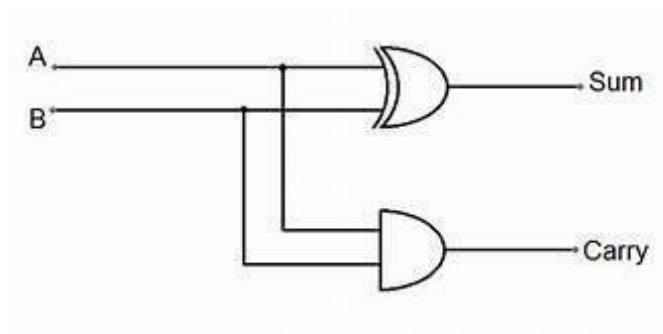
In digital systems, numerous statistics processing obligations may be finished. Arithmetic circuits are derived from the combinational logic circuit in which mathematics operations such as addition. An adder is a digital circuit that performs addition of numbers. In many computers and other sorts of processors adders are used inside the mathematics good judgment devices (ALUs). They are also utilized in other elements of the processor. Adder is a combinational circuit that plays the addition of bits. Each computer has an adder placed in its CPU (ALU) that is chargeable for the manner of addition.



***Fig:1.5: Symbolic representation of compressor***

#### 1.3.1 Half Adder

The half adder is a combinational circuit used to carry out the addition of binary inputs and produces the 2 binary outputs as sum (S) and the carry(C) bits. The time period half-adder ends in the conclusion that one full-adder can be configured using two half-adders.



**Fig:1.6: Logic diagram of Half Adder**

**Table 1.1: Truth table of Half adder**

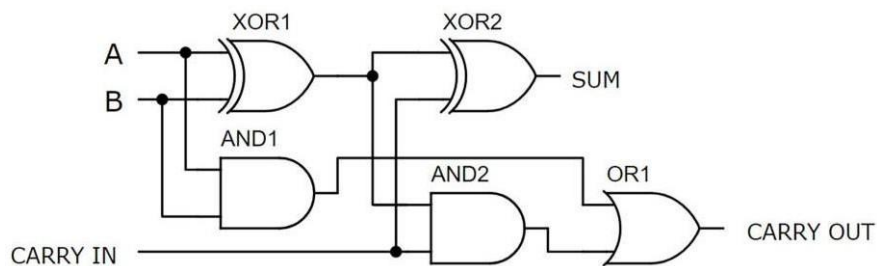
| Input |   | Output |       |
|-------|---|--------|-------|
| A     | B | Sum    | Carry |
| 0     | 0 | 0      | 0     |
| 0     | 1 | 1      | 0     |
| 1     | 0 | 1      | 0     |
| 1     | 1 | 0      | 1     |

### **1.3.2 Full adder**

The half adder is used to feature most effective numbers. To overcome this problem, the total adder changed into evolved. The full adder is used to add 3 1-bit binary numbers A, B, and deliver C. The complete adder has 3 input states and output states i.e., sum and carry. Full Adder can be designed the usage of Half Adder circuit or Single-bit Full Adder circuit and Multi-bit addition using Full Adder

Full adder reduces circuit complexity. It may be used to assemble a ripple carry counter to feature an n-bit variety. Thus it's miles used within the ALU also. It is used in Processor chip like Snapdragon, Exynos or Intel Pentium for CPU element. Which consists of ALU (Arithmetic Block unit). This Block is used to make operations like Add, subtract, multiply and many others. Complete adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, regularly written as A, B, and Cin; A and B

are the operands, and Cin is a chunk carried in from the preceding less considerable degree. The full adder is often a component in a cascade of adders, which upload eight, sixteen, 32, and so forth. Bit binary numbers.



**Fig:1.7: Logic Diagram of Full Adder**

The above figure 1.7[13] illustrates the block diagram of a full adder

**Table 1.2: Truth table for full adder**

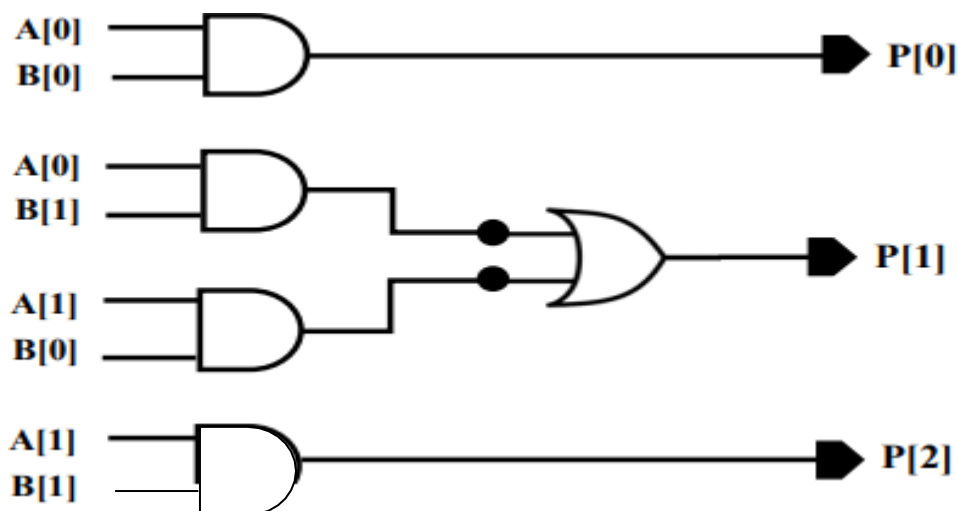
| A | B | C | Sum | Carry |
|---|---|---|-----|-------|
| 0 | 0 | 0 | 0   | 0     |
| 0 | 0 | 1 | 1   | 0     |
| 0 | 1 | 0 | 1   | 0     |
| 0 | 1 | 1 | 0   | 1     |
| 1 | 0 | 0 | 1   | 0     |
| 1 | 0 | 1 | 0   | 1     |
| 1 | 1 | 0 | 0   | 1     |
| 1 | 1 | 1 | 1   | 1     |

## 1.4 MULTIPLIER

### 1.4.1 APPROXIMATE MULTIPLIER

Approximate computing is a rising fashion in digital layout that trades off the requirement of actual computation for stepped forward velocity and strength performance these are broadly being recommended for power-green computing in packages that show off an inherent tolerance to inaccuracy. However, the inclusion of accuracy as a key design parameter, except the performance, region and electricity, makes the identification of the most appropriate approximate multiplier quite tough.

This 2\*2 approximate multiplier is designed by the usage of AND gate and HALF adders as shown underneath The partial products are generated the use of 2-bit multipliers and the primary adders are used to derive the output



**Fig: 1.8: Logic diagram of approx 2\*2 multiplier**

## CHAPTER 2

### LITERATURE SURVEY AND OBJECTIVES

This chapter discusses the approximately the literature survey and precis. It also offers a detailed concept on the prevailing compressor circuits and the way their structures are synthesized.

#### 2.1 LITERATURE SURVEY

**Dr. Karthick Dr. kamalanathan et al. (2018)** An implementation of the proposed compressor in the processing element of systolic array based digital filter is done to evaluate its performance An 8- bit Wallace tree multiplier is designed using proposed compressor and other state-of-the-art designs. From this we have seen that the multiplier design using proposed compressor architecture achieves better performance in terms of PDP compared to other state-of-the- art designs

**Noor Mahammad S , Chinthalgiri Jyothi et al. (2020)** In multiplication the design has two approach for approximate multiplier In the first approach, all partial products are reduced using full adders& half adders and at the last stage of calculation the proposed adder used. In the second approach, all partial products are reduced by proposed 4-2 compressor and at the last stage propose dadder New approximate compressor by eliminating the Cin and Cout of the compressor. The functionality of the proposed compressor is  $S_{prop} = Sum + Carry$

$$Carry = A+B, Sum = B+D$$

**T. Roshini, R. Sai Krishna et al. (2020).** The proposed design uses a tree compressor which contains an XOR-MUX adder. IN order to design a more efficient multiplier, MATC can be used instead of ATC, the presence of XOR-MUX

adder simultaneously lessens the quantity of logic gates used and the number of inputs processed. In the first two stages, PPG and PPR are performed. The Novel Carry Maskable Adder(CMA) is used in the last phase of this approximate multiplier instead of the Carry Propagation Adder.

**Lavanya Maddisetti, JVR Ravindra et al. (2018)** Approximate multiplier has been demonstrated in this paper, employing inexact 5:2 compressors for partial product reduction stage of multiplication operation. In the exact 5:2 compressor using XOR-XNORs and 2X1 multiplexers, the XNOR terminal of the second XOR-XNOR gate has been pruned such that one of the input terminal of the related multiplexer is grounded. The proposed multiplier used a pass transistor based XOR and Inverter based XOR in place of second XOR-XNOR circuit.

**Che-Wei Tung, Shih-Hsu Huang et al. (2019)** The design complexity of a multiplier is primarily related to the PPM reduction circuitry (i.e., the multiplier is primarily related to the PPM reduction circuitry (i.e., the second part). The proposed design has two main features. First, according to the significance, different weights utilize different compressors (in different levels of accuracy) to accumulate their product terms in Stage 1, OR tree is used for Lower Significance weight and high-order approximate compressor is used for Middle Significance Weight. In Stage 2, Accurate Compressor is used for Higher Significance weight.

## 2.2 LITERATURE SUMMARY

Instead of the usage of conventional multipliers, proposed multiplier may be used to do the favored paintings. Thus, the paper presents multiplier. The

performance analysis of conventional circuit has been shown using exceptional strategies

## **2.3 PROBLEM DEFINITION**

To analyze an Efficient Compressor for Multiplier Design and analyze the performance using Synopsis Hspice tool. Therefore, the performance of the circuits has become the bottle neck for the overall system performance.

## **2.4 OBJECTIVE OF THE PROJECT**

- To increase the efficiency of the Compressor for High Speed applications
- In order to improve Efficiency, Low Power Techniques will be applied in all Circuits.
- To compare, the characteristics of MOSFET Technology in terms of Power, Delay and Power Delay Product.
- To identify the Feasibility of Compressor for VLSI Applications.
- To analyse the performance of proposed Multiplier circuits using Hspice tool.

## **CHAPTER 3**

### **AIM AND SCOPE OF PRESENT INVESTIGATION**

#### **3.1 EXISTING METHODOLOGY**

- The present multiplier presents a power and vicinity optimized architecture for blunders-tolerant multiplier.
- To provide a strength green answer, the fashion designer reduced the electricity consumption and the computing time through lowering logic blocks so the static energy can be reduced.
- The proposed approximate structure is likewise discovered to be even better within the chip location. The silicon place is stored up to 25.7%

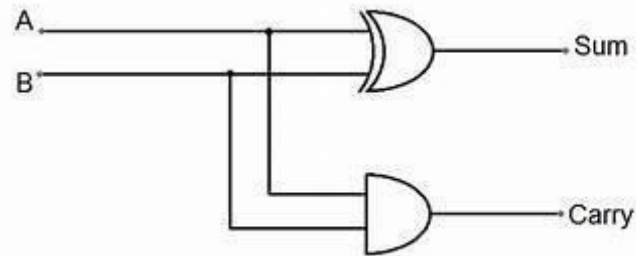
#### **3.2 AREA OF THE PRESENT WORK AND APPLICATION**

Multipliers with low latency and minimum power dissipation are preferred to layout an optimized circuit in order that maximum in the course of may be done in minimal response time. Hence approximate computing has extended for DSP applications. This leads to similarly optimization in terms of power and location with amazing enhancement in computational velocity within an appropriate errors range. So, the performance and the error function are considered with equal importance. The proposed approximate architecture is also located to be even better in the chip area.

#### **3.3 HALF ADDER**

The half adder is one among the combinational circuits, which is used for performing addition of two input bits; the two inputs are A, B. The output of adder is bits: the sum S and carry Cout. This is similar to the addition algorithm in

decimal. The inputs which are A, B represent the inputs and the output sum is generated by or gate i.e., A or B and carry is generated by and gate i.e., A and B.



**Fig:3.1: Block diagram of half adder**

**Table 1.1: Truth table of Half Adder**

| Input |   | Output |       |
|-------|---|--------|-------|
| A     | B | Sum    | Carry |
| 0     | 0 | 0      | 0     |
| 0     | 1 | 1      | 0     |
| 1     | 0 | 1      | 0     |
| 1     | 1 | 0      | 1     |

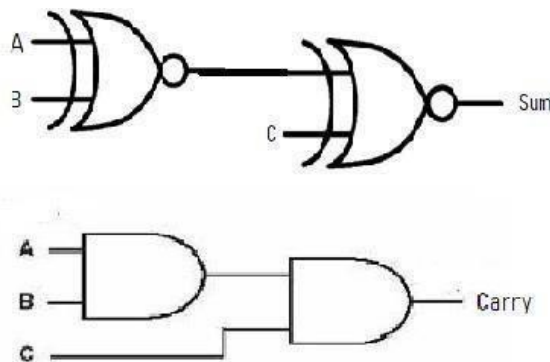
### 3.4 FULL ADDER

The full adder is one some of the combinational circuits, that's used for addition of three enter bits; the two inputs A, B, and bring in Cin . The output of adder is bits: the sum S and bring Cout. This is similar to the addition algorithm in decimal.

The inputs which are A, B and Cin, represent the inputs and the output of first xnor gate is given to the second xnor as input, for full adder to generate carry we have used two and gates and inputs are A, B the output of A and B is given to the next

and gate with Cin as other inputs. The two outputs, Sum and Carry represent the sum and output carry respectively.

Here they have used xnor gates instead of xor gates to reduce the power consumption. Hence the approximate full adder is designed and it's also one among the combinational circuits, which is used for performing addition of three input bits; the inputs A, B, and Cin. The output of adder is two bits: the sum S and carry Cout. This is similar to the addition algorithm in decimal.



**Fig:3.2: Block Diagram of compressor**

**Table 1.2: Truth Table of Full adder**

| A | B | C | Sum | Carry |
|---|---|---|-----|-------|
| 0 | 0 | 0 | 0   | 0     |
| 0 | 0 | 1 | 1   | 0     |
| 0 | 1 | 0 | 1   | 0     |
| 0 | 1 | 1 | 0   | 1     |
| 1 | 0 | 0 | 1   | 0     |
| 1 | 0 | 1 | 0   | 1     |
| 1 | 1 | 0 | 0   | 1     |
| 1 | 1 | 1 | 1   | 1     |

Hence, this is the truth table of full adder and it explains the good judgment and functioning of the circuit.

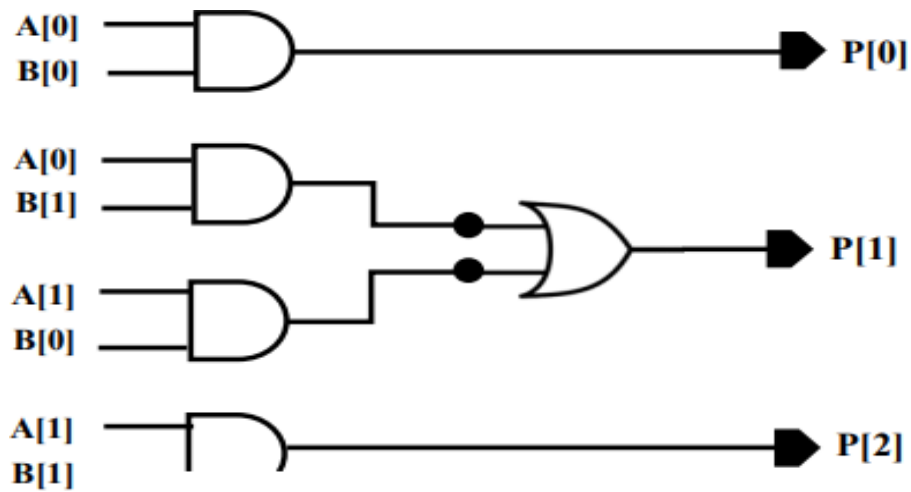
### 3.5. APPROXIMATE (2\*2) MULTIPLIER

Approximate multipliers are widely being endorsed for strength-green computing in applications that show off an inherent tolerance to inaccuracy. However, the inclusion of accuracy as a key layout parameter, except the performance, place and energy, makes the identification of the maximum appropriate approximate multiplier quite difficult. The concept of techniques of approximation followed in earlier works is hard. When bit length goes higher and higher, the accurate element i.e. The multipliers turn out to be extra complex to generate the partial merchandise. Hence, for blunders tolerant packages the approximation may be taken into consideration at multiplication degree and adders may be reconfigured. This will lessen the circuit complexity to reduce the static energy and dynamic energy as nicely because of the decreased dynamic nature of the indicators.

The existing 2\*2 multiplier is designed with two 2 bit numbers. In which the inputs are (A0A1), (B0B1) and the output bits p0, p1, p2. To generate partial product p0 the and gate is used Where the inputs are provided by LSB's of two 2 bit numbers ,p1 is generated by using 2 and gates and 1 or gate, the output of first and gate is produced by using LSB and MSB of first and second numbers respectively , the output of second and gate is produced by using MSB and LSB of first and second numbers respectively the partial product p1 is generated by using an or gate in which inputs are the outputs of first and second and gates, and the final partial product p2 is generated by the MSB's of the two 2 bit numbers.

Therefore the partial product of two 2 digit numbers are generated, Here the error rate is major issue so that we should minimize the use of approximate 2\*2

multiplier in 4\*4 multiplier to generate the first of partial products



**Fig:3.3: Logic diagram of existing approximate multiplier**

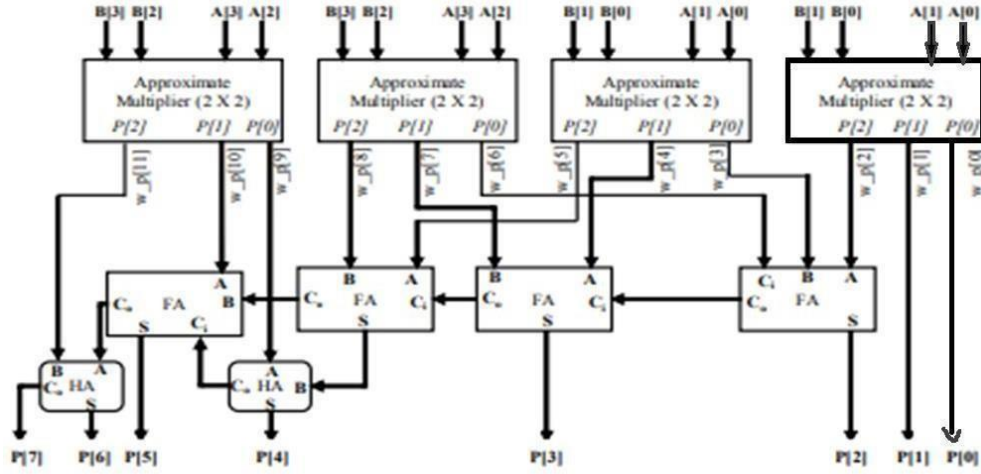
**Table 3.1: Truth table approximate 2\*2 multiplier**

| <i>Inputs</i> |          | <i>output</i> |
|---------------|----------|---------------|
| $A[1:0]$      | $B[1:0]$ | $P[2:0]$      |
| 00            | 00       | 000           |
| 00            | 01       | 000           |
| 00            | 10       | 000           |
| 01            | 11       | 011           |
| 01            | 00       | 000           |
| 01            | 01       | 001           |
| 10            | 10       | 100           |
| 10            | 11       | 110           |
| 10            | 00       | 000           |
| 11            | 01       | 011           |
| 11            | 10       | 110           |
| 11            | 11       | 111           |

### 3.6: Existing 4\*4 multiplier

Multipliers are utilized in a extensive range of virtual signal processing and different packages. Due to advancements in present day technologies, many researchers have specially targeting the layout factors, for better performance. Some of the layout objectives are – excessive velocity, accuracy, low power intake, the regularity of layout, much less place. DSP processor has diverse computational blocks, like multiplexers, adders, MAC. The pace of operation and execution of those blocks have advanced whilst as compared to preceding variations. The execution pace of multipliers depends on two factors, semiconductor technology, and multiplier architecture. Adders are the fundamental building block of virtual multiplexers, in which we carry out a series of repeated additions, to speed up the multiplier operation, the adder's operation speed needs to be accelerated. Digital signal processing programs, wherein essential delay course and the overall performance of the processor lies inside the multiplier.

This multiplier is also one some of the combinational circuits, that's used for acting multiplication of enter four bit numbers, the operation of 4-bit multiplier can be defined in stages. In first stage operands are grouped and multiplication is performed the use of 2-bit multipliers. The outputs of the first degree are brought as much as derive the end result. The partial merchandise is generated the use of 2-bit multipliers and the simple adders are used to derive the output. Because of decreased partial product the adder length is decreased all through 4-bit and 8-bit multiplier layout. The Reduced Partial Product Multiplier (RPPM) gives low-energy and area green solution for approximate computing and error tolerant applications



**Fig.3.3: Logic diagram of existing 4\*4 multiplier**

### 3.7. PROPOSED CIRCUITS

Energy potency has emerged in concert of the foremost essential style parameters in modern computer system style. Approximate computing could be a new computing paradigm to realize energy potency by trading- off energy/area/latency enhancements with accuracy for error-resilient applications. The paper conjointly introduces the look of overflow detector victimisation lowest hardware resources. A comprehensive accuracy and hardware analysis on PASS Transistor 130-nm technology node area unit performed for the planned dividers furthermore as different state-of-the- art reconfigurable circuit styles. Compared to the correct circuit styles, the planned circuits show an improvement of forty ninth in terms of energy potency and is 1.26x faster, whereas introducing lowest errors. The planned style is in contestable for its potency in ALU's and shows nominal result on the output.

## **CHAPTER 4**

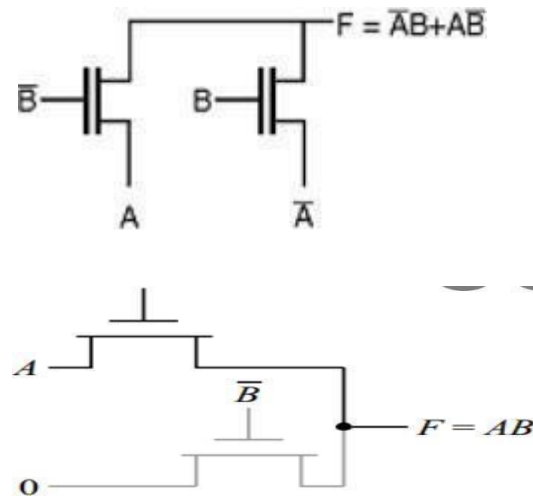
### **PROPOSED METHOD**

In the existing work Full adder, Half adder and 2\*2 Approximate Multipliers with OR and AND gates are implemented in CMOS technology. In the proposed work All the circuits like full adder, half adder and 2\*2 Multipliers are designed in PASS Transistor logic using a Hspice Tool and the proposed design have less delay compared to the existing circuits and also with conventional circuits and also the existing method has the probability error. It was reduced in the proposed work.

#### **4.1 PROPOSED HALF ADDER**

The redundant transitions and the long-stacked transistor paths in the previous or general Half adder can significantly increase the power dissipation. To overcome the aforementioned challenges, a Half adder is proposed to effectively reduce the power consumption without degrading the speed performance. The schematic of the proposed Half adder is illustrated in Figure 4.1. It is made up of two and gates and one or gate. The Carry is generated using the And gate. The half adder is implemented in Pass transistor logic thereby the transistor count had decreased.

Half adder circuits use 2-bit operands to supply an 1-bit result and a carry is generated. Half adder circuits are hardly ever encountered in virtual structures (for motives as a way to be explained later), but they though offer an interesting design opportunity. Like existing adders, the handiest proposed half of adder circuits carry out addition bit-through-bit from the LSB to the MSB, and they're maximum without problems designed the use of the bit-slice method. The design manner closely follows existing adder design, in that sample addition issues may be studied to benefit insight into adder requirements, a fact table may be organized primarily based at the observations, and then a circuit may be designed from the reality desk.



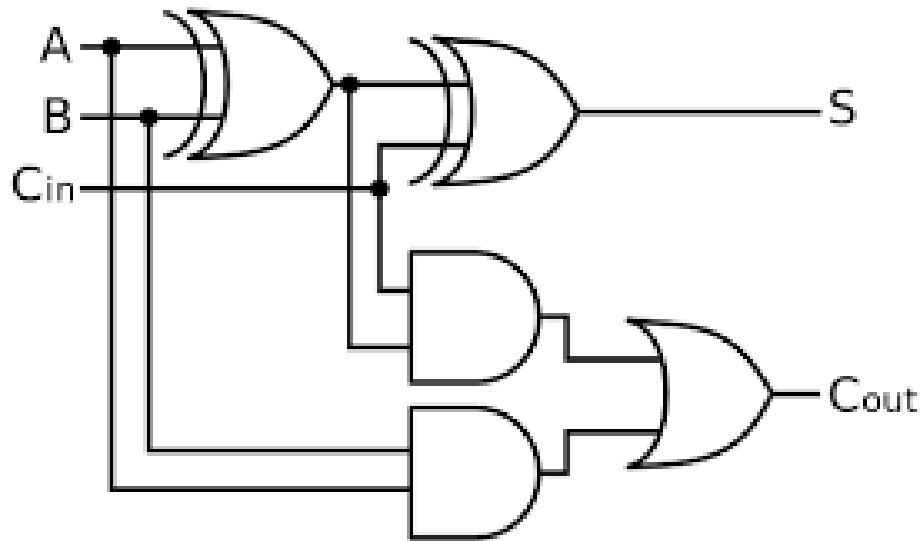
**Fig:4.1: Proposed Half adder**

## 4.2 PROPOSED FULL ADDER

The redundant transitions and the long-stacked transistor paths in the previous or general full adder circuit can significantly increase the power dissipation. To overcome the aforementioned challenges, a full adder is proposed to effectively reduce the power consumption without degrading the speed performance. The schematic of the proposed full adder is illustrated in Figure

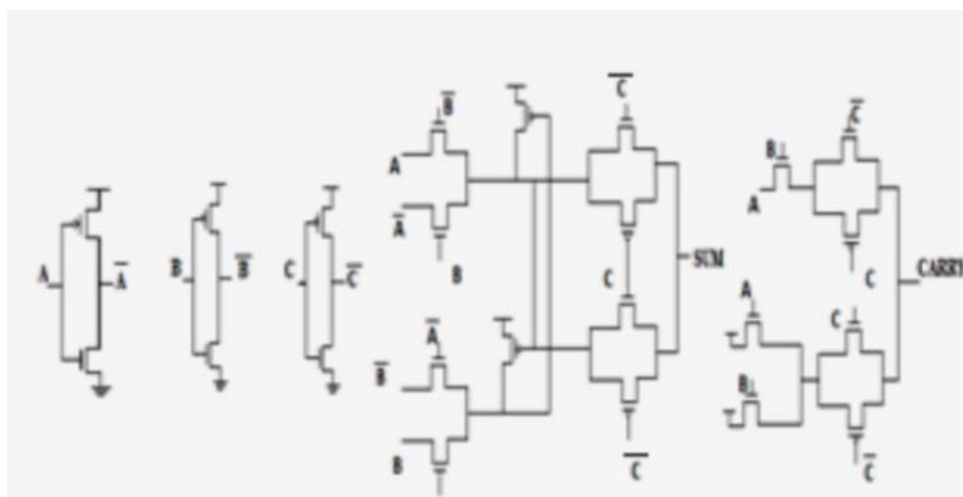
It is made up of logic gates and approximate signal.

Full Adder is that the adder that provides three inputs and produces two outputs. The primary inputs region unit A associated with B and consequently the third input is an input bring as C-IN. The output bring is chosen as C-OUT and consequently the conventional output is selected as S that is total. A full adder common sense is supposed in any such manner which could take eight inputs alongside to form a byte-huge adder and cascade the bring bit from one adder to the any other. The circuit is represented in fig.4.2.



**Fig:4.2: Existing full adder circuit**

The proposed circuit has many modifications as compared to the present one. The good judgment gates used are almost comparable but here an additional OR, AND gates are used. The power intake and put off values are way better than the previous ones. This technique permits us in discount of power intake, put off and area of digital circuits, along with maintaining low complexity of good judgment layout.

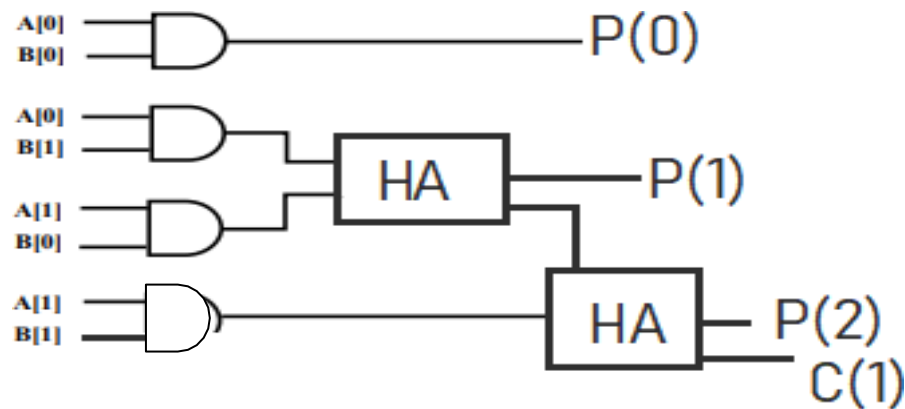


**Fig:4.2.1: Proposed full adder**

The existing full adder will be modified, such that the proposed architecture will be more efficient in terms of average power, speed and energy consumption. Proposed Reconfigurable full adder has designed using Hspice tool. The existing conventional full adder has designed and analyzed.

### 4.3 Proposed 2\*2 Multiplier

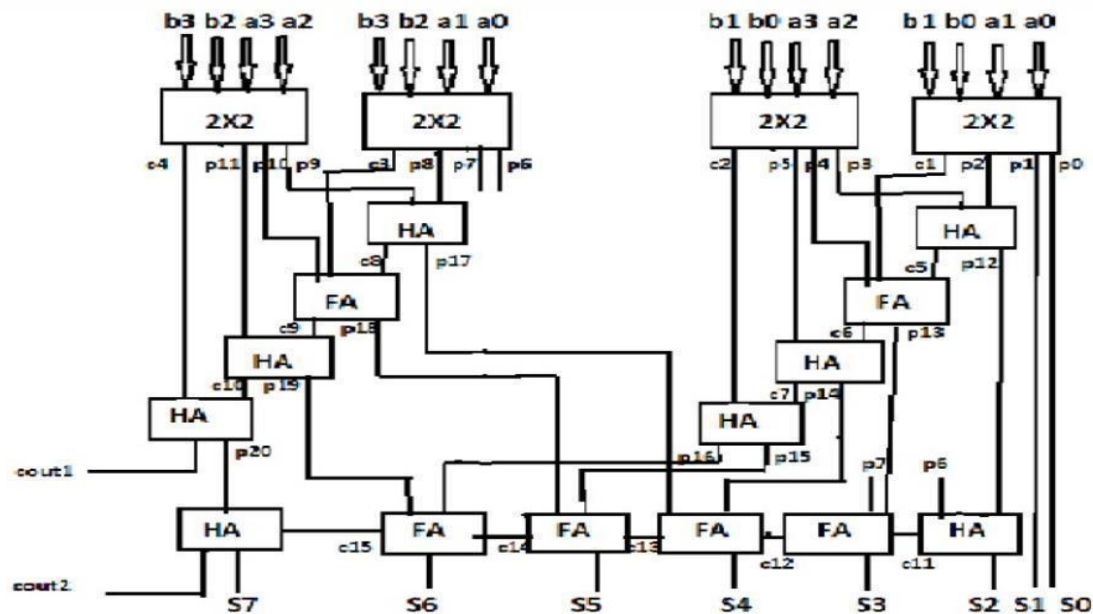
The redundant transitions and the long-stacked transistor paths in the previous or general full adder circuit can significantly increase the power dissipation. To overcome the aforementioned challenges, a 2\*2 multiplier is proposed to effectively reduce the power consumption without degrading the speed performance. The schematic of the proposed 2\*2 multiplier is illustrated in Figure 4.3. It is designed using logic gates and approximate signal. The existing multiplier has been designed and analyzed using conventional method only.



**Fig:4.2.2: 2\*2 Approximate Multiplier**

The existing approximate multiplier will be modified, such that the proposed architecture will be more efficient in terms of average power, speed and energy consumption. Proposed multiplier has been designed using Hspice tool. The existing full adder has been designed and analysed using conventional method only but everything is designed in Pass Transistor logic which reduces the transistors count to half of it.

#### 4.4 PROPOSED 4\*4 MULTIPLIER - FINAL CIRCUIT



**Fig:4.2.3: Proposed 4\*4 Multiplier**

The proposed multiplier is better than existing multiplier in some parameters. In the Existing 4\*4 multiplier they have used approximate multiplier to generate partial products hence we can find error when inputs are above (110) so to rectify the error we have used half adder so that we can add carry and probability error is almost rectified. Efficiency is rectified to maximum Hence the existing multiplier has 50% probability error hence its rectified and error rate is very minimal. By using more half and full adders the chip area will be increased. So for the improvement in chip area we have used Pass Transistor Logic (PTL) instead of Complementary Metal Oxide Semiconductor (CMOS) Logic. So the chip area reduces Because in PTL we use only pmos transistors whereas in CMOS logic we use both pmos and nmos transistors. With the proposed multiplier power consumption and delay is also reduced. Hence the difference between the power values is  $9.130 \times 10^{-4}W$ . Hence the delay is decreased by 113.7ns. The proposed 4\*4 multiplier is more efficient in terms of number of transistors used, Power consumption, Delay and Accuracy.

## **4.5 INCLUDES**

Performance analysis of an efficient compressor for multiplier design is a critical aspect of optimizing arithmetic operations in digital circuits. The compressor, a fundamental building block in multiplier circuits, plays a pivotal role in reducing the complexity and improving the efficiency of multiplication operations. By examining the performance metrics of the compressor, such as speed, area, and power consumption, researchers can evaluate its effectiveness in enhancing the overall performance of multiplier designs. Efficiency in compressor design is achieved through various techniques, including the optimization of transistor sizing, topology selection, and logic synthesis methodologies. These optimizations aim to minimize critical path delays, reduce transistor count, and mitigate power dissipation while maintaining reliable operation across different process technologies.

## **4.6 STANDARDS**

The performance analysis of an efficient compressor for multiplier design should adhere to rigorous standards to ensure the reliability and validity of the proposed work. This entails comprehensive benchmarking against existing state-of-the-art compression techniques to demonstrate superiority in terms of speed, area efficiency, and power consumption. Methodologically, the analysis should employ accurate simulation tools, such as Verilog HDL or System Verilog, validated against industry-standard benchmarks to ensure fidelity to real-world conditions. Additionally, thorough sensitivity analysis should be conducted to assess the compressor's robustness across various design parameters and operating conditions. Moreover, the proposed compressor's scalability and compatibility with different multiplier architectures should be evaluated, alongside its potential integration into larger digital systems. Finally, the analysis should be accompanied by clear and quantitative performance metrics, such as delay, power dissipation, and area overhead, to facilitate fair comparison with existing solutions and enable informed decision-making by designers.

## **4.7 CONSTRAINTS**

The performance analysis of an efficient compressor for multiplier design involves several key constraints to consider. Firstly, the compressor's efficiency must be evaluated within the context of the multiplier's overall performance requirements, such as speed and accuracy, ensuring that the compressor does not introduce significant delays or errors. Additionally, the design must adhere to specified power consumption limits, as excessive power usage can lead to inefficiencies and increased costs. Furthermore, compatibility with the target technology node and integration into the overall multiplier architecture must be ensured, requiring careful consideration of area constraints and design complexity. Finally, the proposed work must address trade-offs between performance metrics, such as throughput versus area overhead, to achieve optimal overall system performance.

## **4.8 TRADE OFFS**

The proposed design of an efficient compressor for multiplier applications offers several trade-offs to consider. While aiming for improved performance in terms of speed and power efficiency, the design may face challenges in terms of area overhead and complexity. Achieving higher efficiency typically involves employing more intricate circuitry or utilizing advanced fabrication processes, which could result in increased silicon area and manufacturing costs. Moreover, optimizing for efficiency may introduce additional latency or pipeline stages, potentially impacting the overall speed of the multiplier. Balancing these trade-offs requires careful consideration of the specific application requirements and performance metrics, ensuring that the benefits of improved efficiency outweigh any drawbacks in terms of area, complexity, or speed.

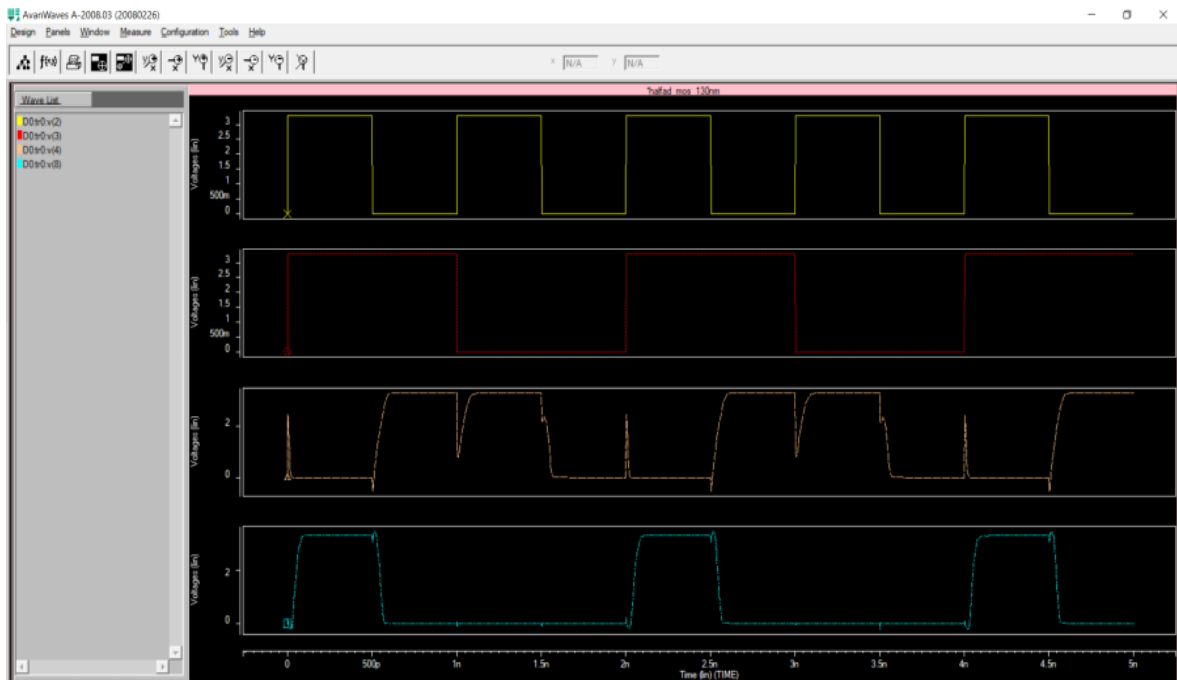
## CHAPTER 5

### RESULTS AND DISCUSSION

The existing architectures are analyzed using H-spice tool. And the proposed Architectures are designed and analyzed in H-spice environment. Output of the proposed full adder, half adder, 2\*2 approximate multiplier and proposed 4\*4 multiplier are analyzed through the analysis done in Hspice environment and it is focuses that the proposed architecture reduces the delay compared with the existing architectures

The design has been evaluated in 130 nano meter technology. The spice code of the schematic design can be viewed in edit NL in H-spice tool. It is simulated. The avan waves in H-spice tool shows the transient analysis of the corresponding design with the specified time values.

#### 5.1 PROPOSED HALF ADDER SIMULATION OUTPUT

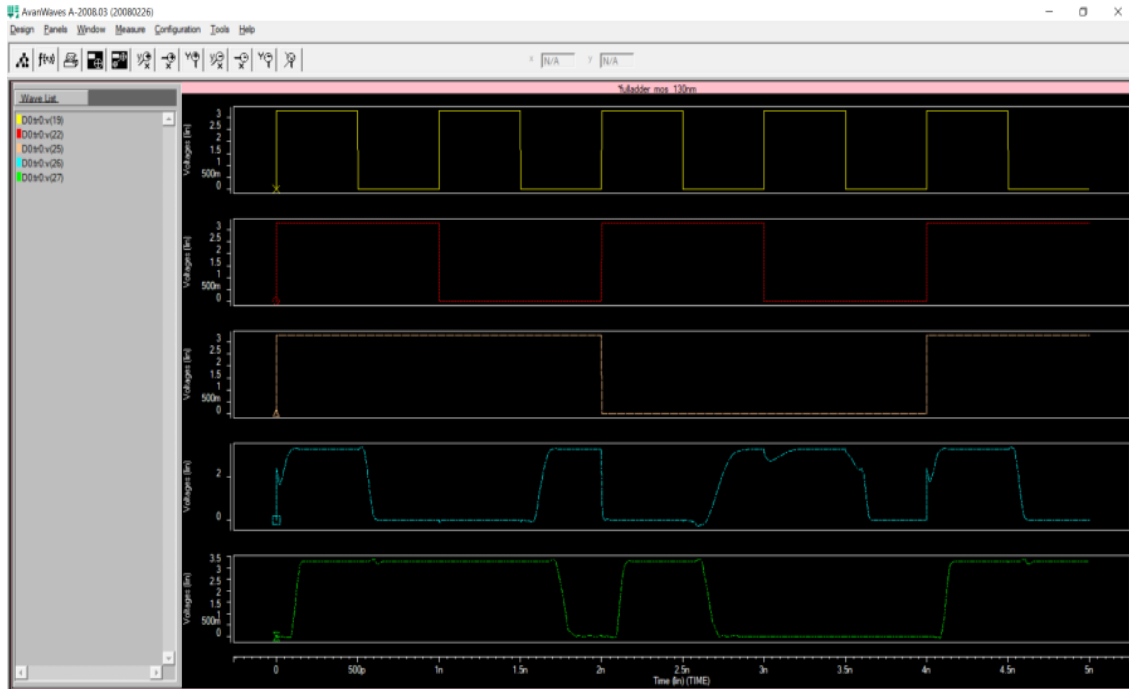


**Fig:5.1: Output Waveform for Half Adder**

Figure 5.1 shows the simulation output of proposed half adder. The input and output are given as: v (2)-input, v (3)-input, v (4)-output, v (5)-output.

The output waveform for a half adder illustrates the behavior of its sum (S) and carry (C) outputs in response to different input combinations.

## 5.2 PROPOSED FULL ADDER SIMULATION OUTPUT



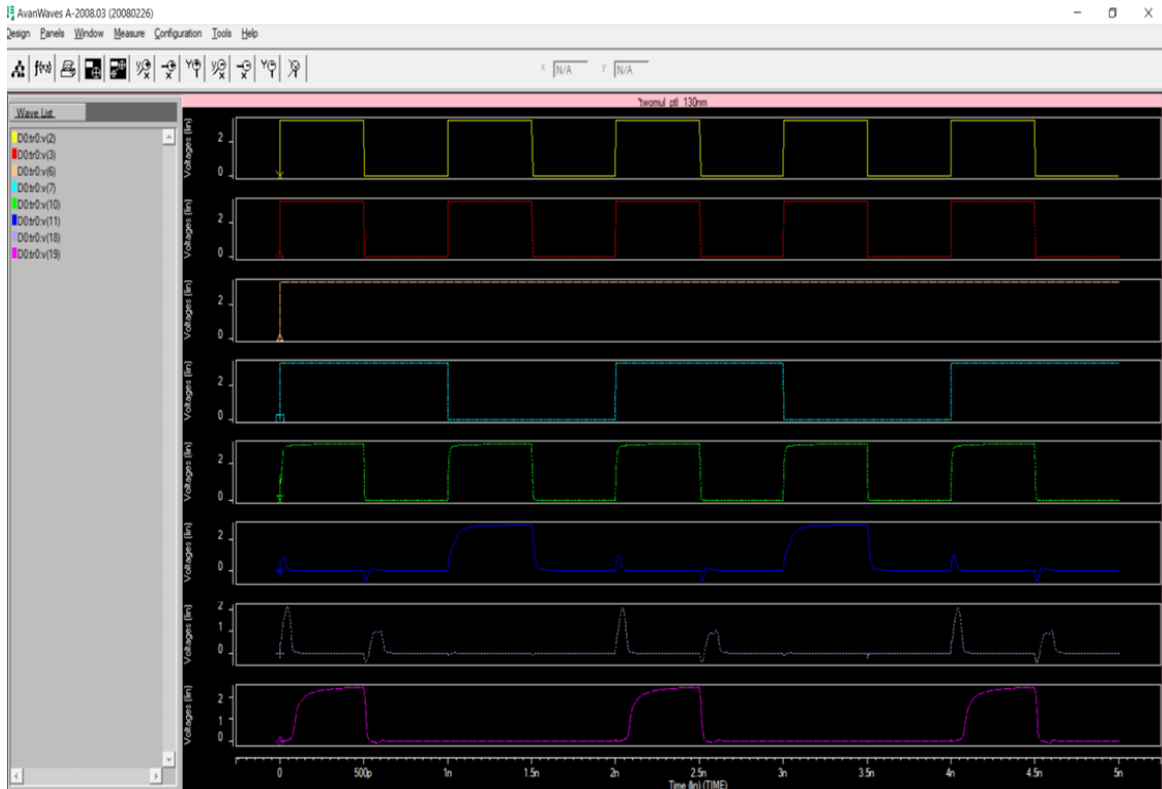
**Fig:5.2: Output Waveform for proposed Full Adder.**

The Figure 5.2 shows the simulation output for the proposed full adder. The inputs are given as: v (19), v (22), v (25) whereas the outputs are v (26) and v (27).

The waveform for the sum output (S) will show transitions between logic levels (0 and 1) as the inputs change, reflecting the binary addition operation performed by the full adder. Similarly, the waveform for the carry output (C) will depict transitions indicating when a carry is generated during addition.

Depending on the input values (A, B, Cin), the output waveform may vary. For instance, if both A and B are high, and there's no carry input (Cin), the sum output (S) will be high, indicating a binary '1', and Cout will be low, indicating no carry.

### 5.3 PROPOSED 2\*2 MULTIPLIER SIMULATION OUTPUT



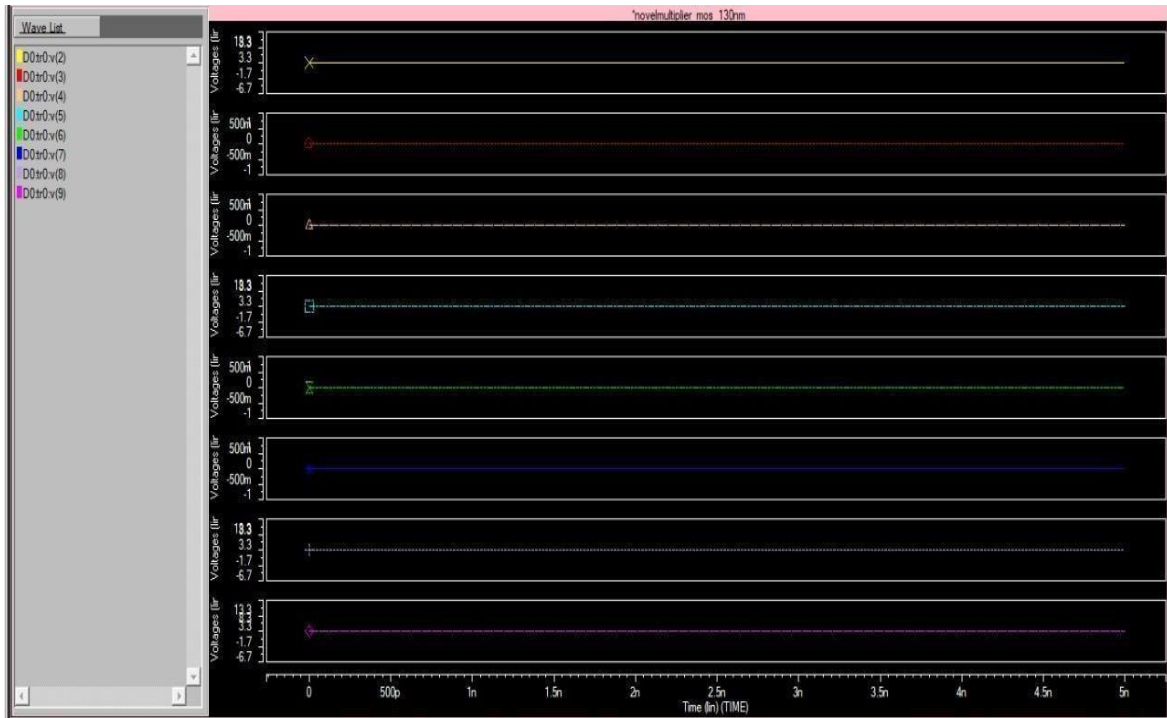
**Fig:5.3: Output Waveform for 2\*2 Multiplier**

Figure 5.3 shows the simulation results for the proposed 2\*2 Multiplier. The inputs are given as v (2), v (3), v (6) and v (7) and the outputs are v (10), v (11), v (12) and v (13).

A 2x2 multiplier is a basic digital circuit used in various applications such as signal processing, arithmetic operations, and digital filtering. It takes two inputs, each consisting of two bits, and produces a single output representing the result of multiplying these two binary numbers.

The output waveform of a 2x2 multiplier typically depends on the logic design used. In a basic implementation using AND gates and a partial product approach, the output waveform will consist of multiple stages of addition, carrying, and final result generation.

## 5.4 PROPOSED 4\*4 MULTIPLIER



**Fig:5.4: Output Waveform for 4\*4 MULTIPLIER**

Figure 5.4 shows the simulation output for proposed reconfigurable ripple carry adder. The inputs are given as v (2), v (3), v (4) and v (5) and the outputs are v (6), v (7), v (8) and v(9).

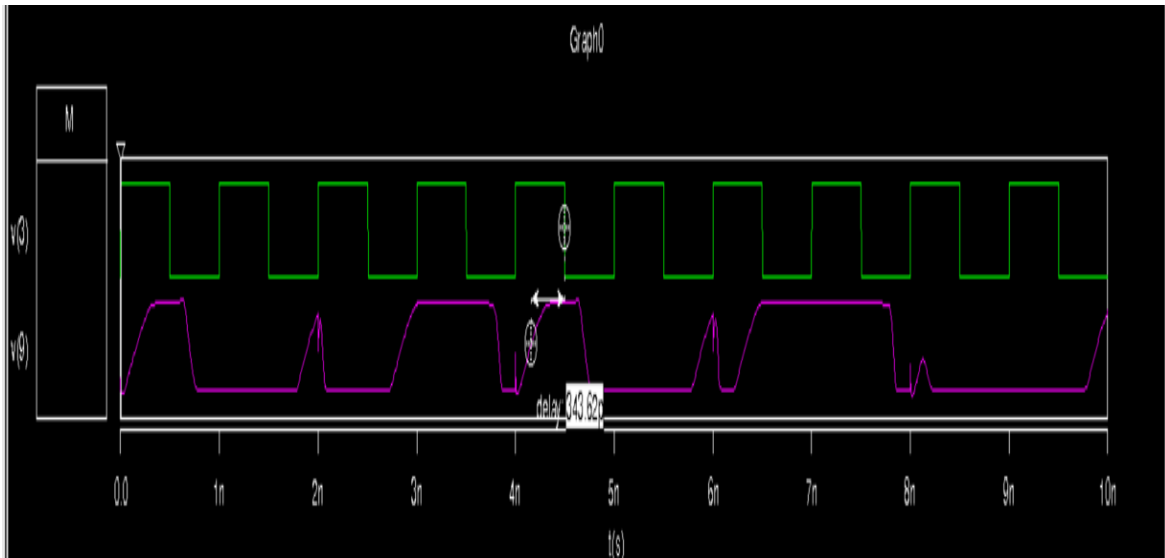
For a 4x4 multiplier, the output waveform would generally consist of 8 bits, representing the possible range of values resulting from multiplying two 4-bit numbers together. Each bit in the output waveform corresponds to a specific power of 2, with the least significant bit (LSB) representing  $2^0$  and the most significant bit (MSB) representing  $2^7$ .

The waveform would vary depending on the input values being multiplied. For example, if the input values were 3 (0011 in binary) and 5 (0101 in binary), the result would be 15 (1111 in binary), and the output waveform would reflect this binary representation.

## 5.5 PERFORMANCE ANALYSIS

The performance of Half adder, full adder, 2\*2 multiplier and final 4\*4 multiplier are analyzed in terms of power and delay and energy consumption.

### 5.5.1 Power and Delay Analysis of Existing circuits



**Fig:5.5: Delay analysis of existing 4\*4 multiplier**

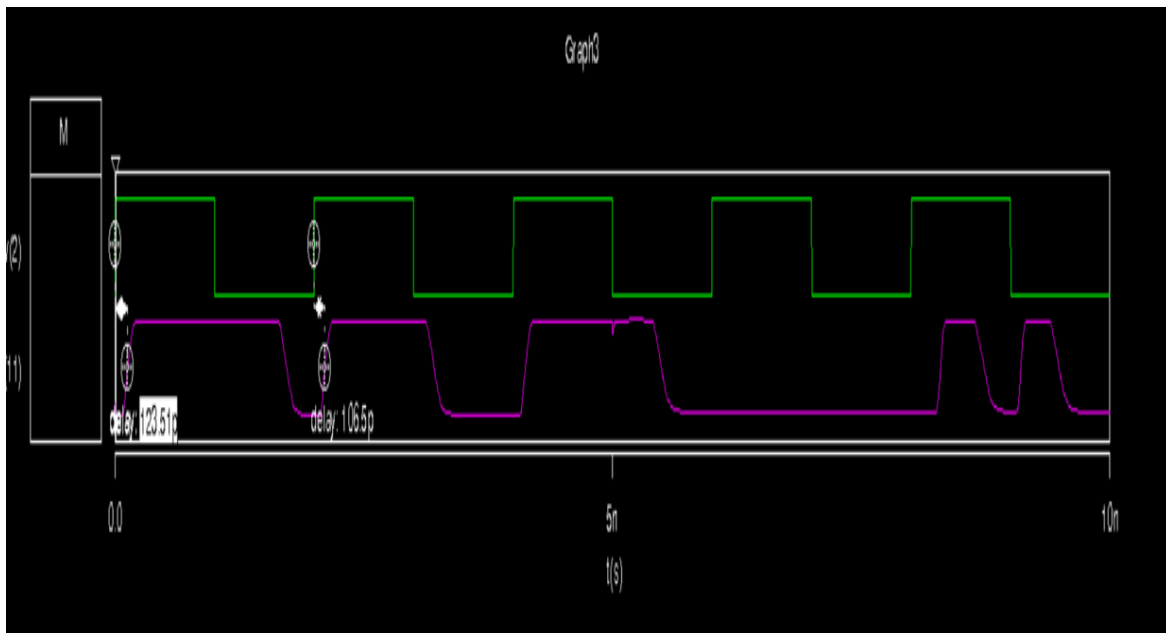
From the Table 5.1 the power and delay of existing work has been shown.

Delay analysis of an existing 4x4 multiplier involves assessing the time it takes for the multiplier to produce an output given certain inputs. This analysis is crucial for understanding the performance of the multiplier and identifying potential bottlenecks in its design. Factors affecting delay include the architecture of the multiplier, the technology used for implementation, and the propagation delays of individual components.

**Table 5.1: Performance analysis of existing 4\*4 Multiplier**

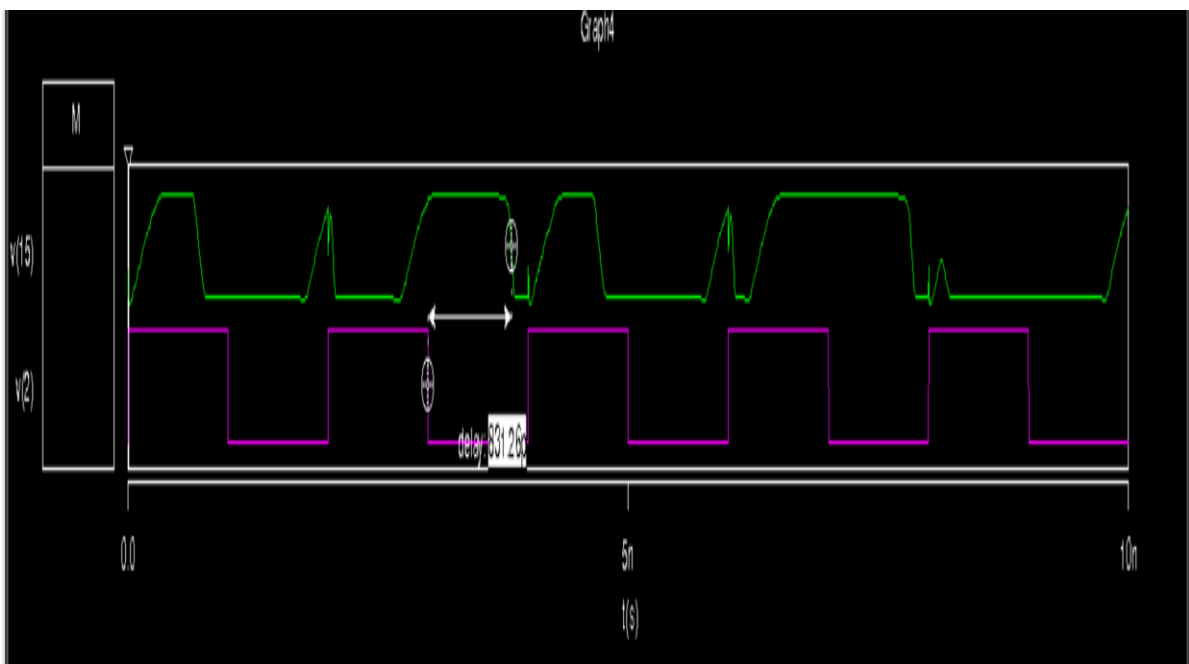
| EXISTING<br>CIRCUIT | AVERAGE<br>POWER (W)            | DELAY (S) |
|---------------------|---------------------------------|-----------|
| 4*4 multiplier      | $9.171 \times 10^{-4} \text{W}$ | 1.137ps   |

### 5.5.2 Power and Delay Analysis of proposed circuits



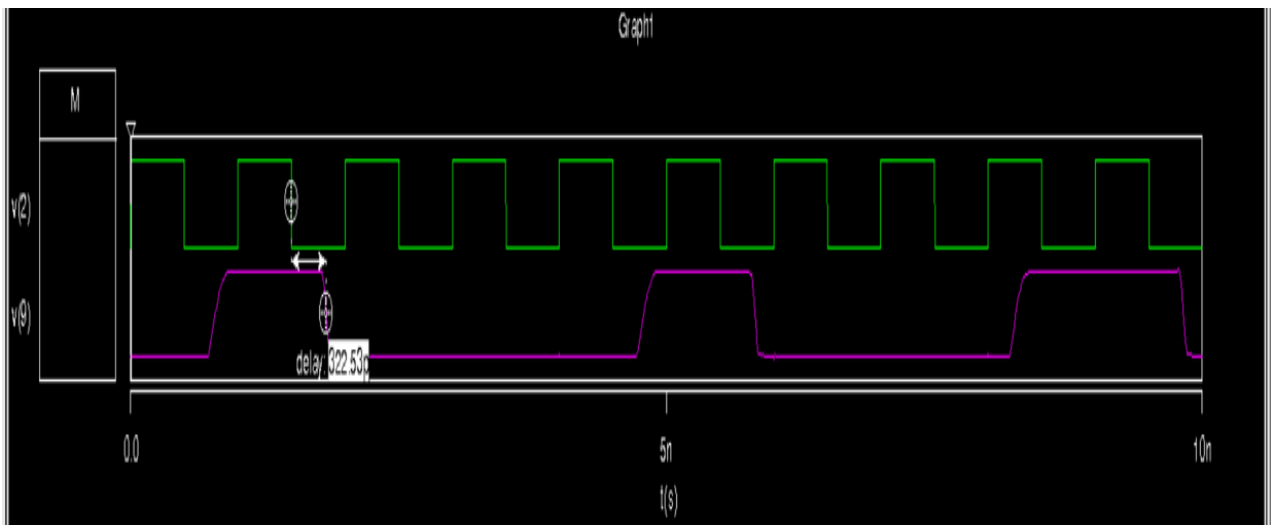
**Fig:5.6: Delay analysis of Half adder**

In the analysis of a half adder's delay, several factors are typically considered. These include gate delays, propagation delays, and interconnect delays within the circuit.



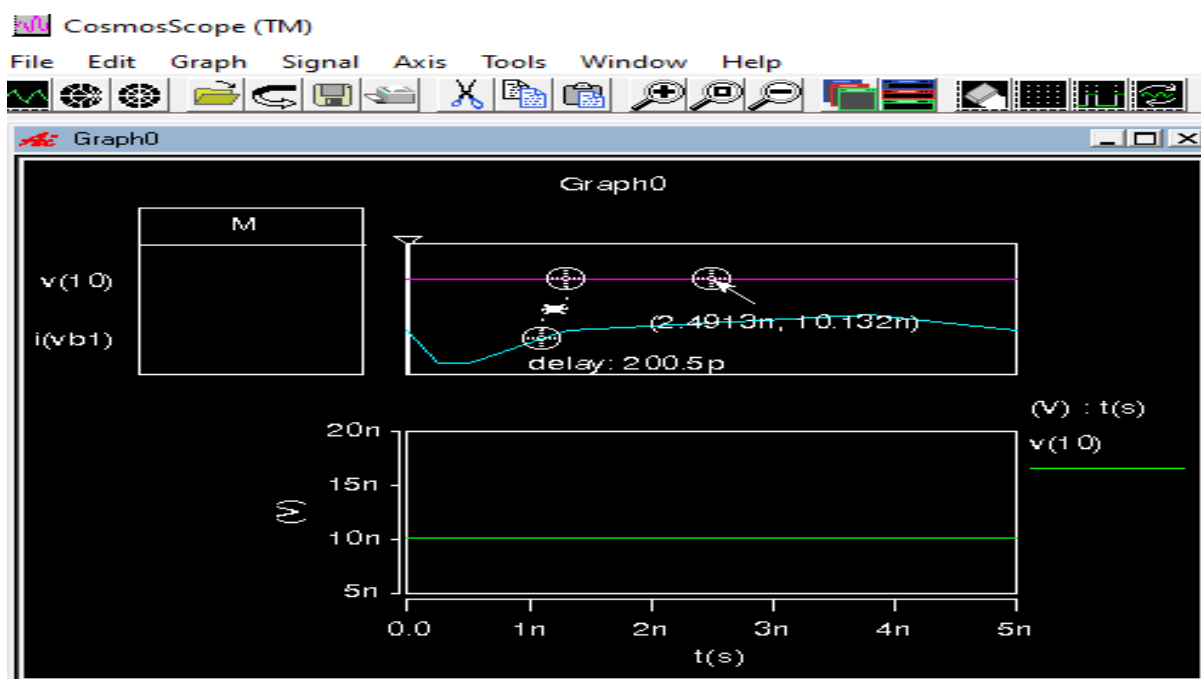
**Fig:5.7: Delay analysis of Full adder**

The delay analysis of a full adder involves evaluating propagation and contamination delays to understand its speed performance.



**Fig:5.8: Delay analysis of 2\*2 multiplier**

The delay primarily depends on the critical path within the multiplier circuit, which is the longest path from input to output. In a 2x2 multiplier, this critical path typically involves the multiplication of the highest-order bits of the two input numbers.



**Fig:5.9: Delay analysis of 4\*4 multiplier**

A delay analysis of a 4x4 multiplier involves examining the time it takes for the multiplier to produce its output after receiving its inputs. In the case of a 4x4 multiplier, it multiplies two 4-bit numbers to produce an 8-bit result.

### 5.5.3 Performance analysis of Proposed 4\*4 Multiplier

From the Table 5.3 the power and delay of proposed work of the half adder, full adder, 2\*2 multiplier and 4\*4 multiplier have been shown.

**Table 5.2: Performance analysis of proposed circuits**

| PROPOSED CIRCUIT | AVERAGE POWER (W)               | DELAY (S) |
|------------------|---------------------------------|-----------|
| Half adder       | $4.074 \times 10^{-5} \text{W}$ | 46.632pS  |
| Full adder       | $1.231 \times 10^{-4} \text{W}$ | 120.11pS  |
| 2*2 multiplier   | $6.417 \times 10^{-4} \text{w}$ | 76.58pS   |
| 4*4 multiplier   | $2.876 \times 10^{-4} \text{W}$ | 200.5pS   |

During performance analysis, engineers may use simulation tools, hardware prototypes, or FPGA implementations to evaluate the proposed 4x4 multiplier under different scenarios and input conditions. They aim to identify trade-offs and optimizations that improve overall performance while meeting design constraints and specifications. Additionally, comparative analysis with existing multipliers or alternative designs can provide valuable insights into the proposed multiplier's strengths and weaknesses.

Overall, a comprehensive performance analysis of the proposed 4x4 multiplier involves evaluating its speed, resource utilization, power consumption, functionality, correctness, scalability, and flexibility. This analysis enables designers to identify strengths and weaknesses in the design and make informed decisions to enhance its overall performance and suitability for specific applications

## **CHAPTER 6**

### **CONCLUSION AND FUTURE SCOPE**

#### **A. CONCLUSION**

The proposed design of Half adder, full adder,  $2 \times 2$  multiplier and  $4 \times 4$  multiplier gives more output functions as compared to the conventional circuits. The proposed architectures are designed and the timing response are analyzed through transient analysis and the performance analysis are analyzed through power, delay and energy consumption analysis. So the proposed computational blocks are more suitable for real time architectures.

#### **B. FUTURE SCOPE**

Energy efficient approximate arithmetic logic units can be designed using these proposed computational blocks. In future multipliers can be designed using computational blocks such as ALU and Memory and so on.

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