

MIPS Processor Using CISC Architecture

Submitted in partial fulfillment of the requirements for the award of

Bachelor of Engineering degree in Electronics and
Communication Engineering

by

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION
ENGINEERING**

SCHOOL OF ELECTRICAL AND ELECTRONICS

SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

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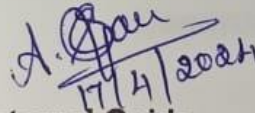
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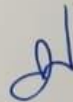
BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **HARA GOPALA KRISHNA (40130288), NARESH P(40130705)** who have done the project work as a team who carried out the project entitled "**MIPS PROCESSOR USING CISC ARCHITECTURE**" under our supervision from November 2023 to April 2024.


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Internal Guide

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ACKNOWLEDGEMENT

DECLARATION

I am pleased to acknowledge my sincere thanks to the Head of I, **NARESH P (40130705)**, hereby declare that the Project Report entitled "**MIPS Processor using CISC Architecture**" done by me under the guidance of **Dr. A. SAHAYA ANSELIN NISHA M.E., Ph.D.**, is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in **DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**.

DATE : 17/04/2024

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SIGNATURE OF THE CANDIDATE

DECLARATION

I, HARA GOPALA KRISHNA (40130288), hereby declare that the Project Report entitled "MIPS Processor using CISC Architecture" done by me under the guidance of Dr. A. SAHAYA ANSELIN NISHA M.E., Ph.D., is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING.

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I convey our thanks to **Dr. N. M. NANDHITHA, M.E., Ph.D., Professor & Dean, School of Electrical and Electronics** and **Dr.T. RAVI, Ph.D., Professor & Head, Department of Electronics and Communication Engineering** for providing us necessary support and details at the right time during the progressive review

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ABSTRACT

This project aims to design and implement a MIPS (Microprocessor without Interlocked Pipeline Stages) processor based on the CISC (Complex Instruction Set Computing) architecture with a focus on the pipeline design. The MIPS processor is a widely used RISC (Reduced Instruction Set Computing) architecture, but in this project, the concept of implementing a CISC application on processors. The project will begin with a comprehensive review of the MIPS architecture and its RISC characteristics. The CISC architecture, known for its complex and multi-step instructions, will then be adapted and integrated into the original MIPS design. The modification will involve creating new instruction sets, adding microcode support, and designing a pipeline to handle the decoding and execution of complex instructions. The processor will be designed and simulated using a hardware description language (HDL) like Verilog or VHDL. Several pipeline stages will be considered, such as instruction fetch, decode, execute, memory access, and write-back.

The pipeline design will be optimized for performance and efficiency, taking into account factors like instruction latency, data hazards, and control hazards. Once implemented, the MIPS processor's pipeline will undergo extensive testing and verification to ensure its correctness and functionality. Testbench programs will be developed to validate the execution of both RISC and CISC instructions, and corner cases will be examined to assess the processor's stability and reliability. This project presents the design and implementation of a MIPS (Microprocessor without Interlocked Pipeline Stages) processor in Verilog HDL, focusing on its pipeline architecture, register memory, and latches. The MIPS processor is a RISC (Reduced Instruction Set Computing) architecture known for its simplicity and efficiency. The design includes key components such as an instruction fetch unit, instruction decode unit, ALU (Arithmetic Logic Unit), register file, and data memory. The pipeline architecture consists of stages including instruction fetch, instruction decode, execute, memory access, and write back. Latches are used between pipeline stages to store intermediate results and control signals.

TABLE OF CONTENT

Chapter	Topic	Page no
	ABSTRACT	V
	LIST OF ABBEREVIATIONS	VIII
	LIST OF FIGURES	IX
1	INTRODUCTION	1
	1.1 GENERAL INTRODUCTION	1
	1.2 BACKGROUND	2
	1.3 DESCRIPTION	2
	1.4 PROBLEM STATEMENT	3
	1.5 OBJECTIVE OF PROJECT	4
	1.6 PROJECT SCOPE	4
2	LITERATURE SURVEY	5
	2.1 LITERATURE REVIEW	5
	2.2 LITERATURE SUMMARY	8
3	AIM AND SCOPE OF PROJECT	9
	3.1 AIM	9
	3.2 SCOPE OF ARCHITECTURE	10
	3.3 PROPOSED BLOCK DIAGRAM	11
	3.4 RTL DESIGN	12
	3.5 ALGORITHM FOR MIPS DEVELOPMENT	13
4	PROPOSED SYSTEM	15
	4.1 KEY FEATURES OF MIPS	15
	4.2 OVERVIEW OF MIPS ARCHITECTURE	16

4.3	HARDWARE MODELLING OF MIPS	18
4.4	MODELLING OF MEMORY	19
4.5	INITIALIZE MEMORY	20
4.6	MODELLING REGISTER BANK	22
4.7	PIPELINE IMPLEMENTATION	26
4.8	MIPS INSTRUCTION ENCODING	28
4.8.1	R-TYPE INSTRUCTION	29
4.8.2	I- TYPE INSTRUCTION	30
4.8.3	J- TYPE INSTRUCTION	31
4.9	MICRO-OPERATION IN PIPELINED MIPS32	31
4.10	STANDARDS	33
4.11	CONSTRAINTS	34
4.12	TRADE OFFS	34
5	RESULT AND DISCUSSION, PERFORMANCE ANALYSIS	36
5.1	SIMULATION RESULTS	36
5.2	PIPELINE RTL SIMULATION	37
5.2.1	MEMORY DESIGN	38
5.2.2	MIPS RTL DESIGN	38
5.5	PERFORMANCE ANALYSIS	40
6	SUMMARY AND CONCLUSION	41
6.1	SUMMARY	41
6.2	FUTURE SCOPE	41
6.3	CONCLUSION	42
	REFERENCES	43

LIST OF ABBREVIATIONS

1.	MIPS	Microprocessor Interlocked Pipeline Stages
2.	RISC	Reduced Instruction Set Computer
3.	CISC	Complex Instruction Set Computer
4.	ISA	Instruction Set Architecture
5.	IF	Instruction Fetching
6.	ID	Instruction Decoding
7.	EX	Executing
8.	MEM	Memory Access
9.	WB	Write Back
10.	R-type	Register-Type
11.	I-type	Immediate-Type
12.	J-type	Jump- Type
13.	ALU	Arithmetic Logic Unit
14.	CPU	Controlled Processing Unit
15.	RTL	Register Transfer Level
16.	FPGA	Field Programmable Logic Array
17.	SIMD	Single Instruction Multiple Data

LIST OF FIGURES

Figure No	TITLE	Page no
3.1	Block Diagram	11
3.2	RTL Design	12
4.1	Memory Initialization	21
4.2	Register Bank	22
4.3	3-Stage Pipeline	25
4.4	R-type Instruction	29
4.5	I-type Instruction	30
4.6	J-type Instruction	31
4.7	MIPS32 Datapath	32
4.8	Syn- Clock Shifting	33
5.1	MIPS Simulation	36
5.2	ALU Simulation	37
5.3	4-Stage Pipeline RTL	37
5.4	Memory Design	38
5.5	MIPS RTL outlook	39
5.6	MIPS RTL Inter blocks	39
5.7	RTL of MIPS	40

CHAPTER – I

INTRODUCTION

1.1 GENERAL INTRODUCTION

The MIPS (Microprocessor without Interlocked Pipeline Stages) processor is a renowned example of a RISC (Reduced Instruction Set Computing) architecture, widely recognized for its efficiency and simplicity in handling mathematical applications. This project focuses on designing and implementing a MIPS processor tailored for mathematical computations using Verilog. The CISC (Complex Instruction Set Computing) architecture of the MIPS processor allows for intricate and multi-step instructions, making it ill-suited for efficient handling of various mathematical operations. Implementing this CISC architecture in Verilog enables a detailed exploration of instruction decoding, execution, and data management in mathematical contexts.

The project's core objective involves designing the MIPS processor's instruction set for mathematical operations, including addition, subtraction, multiplication, and division. Each mathematical operation will be implemented as a module in Verilog, accompanied by the necessary control logic to orchestrate these operations effectively. Furthermore, the project will delve into optimizing the MIPS processor specifically for mathematical applications. This optimization process may encompass techniques such as pipelining and parallel processing to enhance performance and efficiency in executing mathematical computations.

In essence, this project aims to provide a thorough understanding of the MIPS processor's CISC architecture and its Verilog implementation for mathematical applications. It serves as a practical demonstration of designing and optimizing processors for specialized tasks, showcasing the versatility and effectiveness of the MIPS architecture in mathematical computing.

1.2 BACKGROUND

Overview of the MIPS architecture, including its key components like registers, ALU, control unit, and memory. Explanation of the MIPS instruction set architecture (ISA). MIPS Pipeline Description of the MIPS pipeline stages (IF, ID, EX, MEM, WB). Discussion of pipeline hazards and their solutions in MIPS. Instruction Set Overview of the MIPS instruction formats (R, I, J). Explanation of key instructions and their functions (e.g., arithmetic, logical, branch, and memory instructions). MIPS Applications Common uses of MIPS processors in industry and academia. Comparison with other architectures in terms of performance, port efficiency, and application domains.

1.3 DESCRIPTION

The heart of this project lies in the development of a custom instruction set that seamlessly integrates the core principles of MIPS and CISC. This instruction set will embody variable-length instructions, complex addressing modes, and an extensive range of operations, offering the versatility required for modern computing demands. The processor's core will be meticulously crafted, encompassing components such as the Arithmetic Logic Unit (ALU), control unit, registers, and data paths. These elements will be optimized to facilitate the efficient execution of instructions from our hybrid instruction set. To develop a novel MIPS developed under CISC hybrid processor that seamlessly combines the efficiency of the MIPS architecture with the versatility of a CISC instruction set, catering to both simple and complex computing tasks.

The MIPS (Microprocessor without Interlocked Pipeline Stages) architecture, developed by MIPS Computer Systems in the early 1980s, stands as a hallmark of RISC (Reduced Instruction Set Computing) designs. Known for its efficiency and simplicity, MIPS processors have been widely adopted in various computing domains, including embedded systems, consumer electronics, and high-performance computing. The architecture's strength lies in its streamlined instruction set, featuring a fixed-length, 32-bit format and a reduced number of instructions, which enables fast decoding and execution. MIPS processors employ a load-store architecture, restricting memory access to load and store operations while performing all other

computations within registers. With 32 general-purpose registers, MIPS processors minimize memory access, enhancing performance. Additionally, the architecture's five-stage pipeline, consisting of instruction fetch, decode, execute, memory access, and write back stages, allows for high clock frequencies and instruction throughput.

1.4 PROBLEM STATEMENT

The MIPS (Microprocessor without Interlocked Pipeline Stages) architecture, while renowned for its efficiency and simplicity, faces several challenges that impact its performance and usability in modern computing environments. One significant issue is the limited number of general-purpose registers in MIPS processors. With only 32 registers available, programmers often face constraints when attempting to optimize code for performance. This limitation can lead to frequent data transfers betide registers and memory, which can degrade performance.

The project aims to address a critical challenge in computer architecture by attempting to reconcile the distinctive design philosophies of RISC and CISC within a single CPU. The primary problem lies in the divergence of these two paradigms, while RISC architectures like MIPS emphasize simplicity and efficiency through a reduced set of instructions, CISC architectures such as x86 offer a broad array of complex instructions to accommodate diverse computing tasks.

Another challenge is the handling of complex data types and operations in MIPS. While the architecture is it'll-suited for basic arithmetic and logical operations, more complex operations, such as those involving floating-point numbers or multimedia data, require additional instructions and processing steps. This can result in inefficient code execution and reduced performance for applications that rely heavily on these operations.

Furthermore, the MIPS architecture's branch delay slot, a feature that allows an instruction to be executed after a branch instruction, can be challenging to optimize. Programmers must carefully select instructions to fill the delay slot, which can be a non-trivial task and may not always result in performance improvements.

This disparity poses a dilemma for CPU designers: should they prioritize the streamlined execution of simple instructions or the versatility needed to handle complex workloads efficiently. Overall, these challenges highlight the need for further enhancements and optimizations in the MIPS architecture to address the evolving demands of modern computing applications.

1.5 OBJECTIVE OF THE PROJECT

In this project, the MIPS processor's architecture and functionality. It will examine its key components, including the instruction set, registers, and memory organization. By understanding how the MIPS processor processes instructions and data, it can write more efficient programs tailored to its architecture, it will study how the MIPS processor handles interrupts and exceptions, which are crucial for building reliable and robust systems. Overall, this project will provide a comprehensive overview of the MIPS processor and its applications in real-world scenarios.

1.6 PROJECT SCOPE

The scope of this project includes gaining a deep understanding of the MIPS processor architecture, its instruction set, and its applications. It will explore how the MIPS processor executes instructions, manages memory, and handles various types of data. Additionally, it will study the MIPS pipeline and its stages to understand how instructions are processed.

In the future, this project can be expanded to include advanced topics such as optimizing code for the MIPS architecture, implementing complex algorithms, and exploring the use of the MIPS processor in embedded systems and real-time applications.

CHAPTER -2

LITERATURE SURVEY

2.1 LITERATURE REVIEW

Agarwal and Hsu (1992) [1] discusses architectural support for address translation on CISC/RISC processors, presented at the International Symposium on Computer Architecture (ISCA). The paper likely explores how complex instruction set computing (CISC) and reduced instruction set computing (RISC) processors handle address translation, which is the process of converting virtual addresses to physical addresses. Additionally, the paper might discuss the implications of these differences on system performance, complexity, and compatibility with existing software. Understanding the architectural support for address translation in CISC and RISC processors is important for computer architects, system designer.

Bhandarkar, D., & Gupta, R. (1991).[2] Reducing RISC Instruction Cache Misses by Preloading Instruction Caches with Instructions Issued by the CISC Architecture. In ACM/IEEE Conference on Supercomputing. The approach may involve analysing the behavior of CISC instructions and using this information to optimize the instruction cache content for RISC processors. It could also discuss the impact of this technique on the overall performance of RISC processors, such as reduction in cache miss rates and improvement in instruction fetch latency. By leveraging instructions from CISC architectures, which typically have more complex instruction sets, RISC processors may be able to achieve better performance without sacrificing their architectural principles.

Clark, D. W., & Terman, L. M. (1988). [3]. The Design and Implementation of a CISC/RISC Microprocessor. In International Symposium on Microarchitecture. This paper likely describes a microprocessor that combines elements of both complex instructions set computing (CISC) and reduced instruction set computing (RISC) architectures. It may also discuss the design challenges and trade-offs involved in creating such a hybrid architecture. This work is significant as it explores a hybrid approach to

microprocessor design, which was a relatively new concept at the time. By combining the strengths of CISC and RISC architectures, the CISC/RISC microprocessor may offer improved performance and flexibility compared to traditional designs.

Borch, J. V., & Flynn, M. J. (1980). [4]. Some Trade-offs in Instruction Set Architecture Design. In International Symposium on Computer Architecture (ISCA). This paper likely describes a microprocessor that combines elements of both complex instructions set computing (CISC) and reduced instruction set computing (RISC) architectures. It may also discuss the design challenges and trade-offs involved in creating such a hybrid architecture. This work is significant as it explores a hybrid approach to microprocessor design, which was a relatively new concept at the time. By combining the strengths of CISC and RISC architectures, the CISC/RISC microprocessor may offer improved performance and flexibility compared to traditional designs.

Dubois, M., Annavaram, M., & Stenström, P. (2008). [5]. Towards Energy-Efficient CISC-RISC Architectures. IEEE Computer Architecture Letters, 7(1), 25-28. The goal is to achieve higher performance with lower energy consumption. Simulation-based evaluation of their proposed architecture using a set of benchmarks. They compare the energy efficiency of their hybrid architecture with traditional CISC and RISC architectures, demonstrating the potential benefits of their approach. The authors conclude that a hybrid CISC-RISC architecture has the potential to improve energy efficiency in computing systems and suggest further research directions in this area.

Horowitz, M. A. (1990). [6] Computational Structures for RISC and CISC Processors. ACM Computing Surveys, 22(4), 277-313. This paper probably discusses the underlying computational structures that differentiate RISC and CISC processors. It likely explores the architectural features and design principles that define each type of processor, including instruction formats, operand addressing modes, pipeline organization, and control unit complexity. Impact processor performance, power efficiency, and

design complexity. Additionally, it may analyse the trade-offs involved in selecting between RISC and CISC architectures for specific applications. This knowledge can help in designing more efficient processors, optimizing software for different architectures, and making informed decisions about processor selection for various computing tasks.

Smith, J. E., & Pleszkun, A. R. (1981). [7] Implementation of Precise Interrupts in Pipelined Processors. In International Symposium on Computer Architecture (ISCA). This paper probably discusses the design considerations and methods for handling interrupts in pipelined processors to ensure precise interrupt behavior ensuring that the system state is correctly saved and restored such as the need to track the state of instructions in the pipeline, handle instruction reordering, and manage the interruption of in-progress instructions. It may also present specific techniques or mechanisms used to achieve precise interrupts in pipelined processors.

Dreslinski, R., Mudge, T., & Scott, M. (2010). [8]. A Comparison of CISC and RISC Architectures for Embedded Applications. IEEE Micro, 30(6), 69-79. Focusing on performance metrics such as instruction count, CPI (Cycles Per Instruction), and execution time. The authors analyse the results, discussing the reasons behind the performance differences between CISC and RISC architectures. They also consider the implications of their findings for embedded system designers. The paper concludes with a summary of the key findings and recommendations for designers of embedded systems, based on the performance comparison between CISC and RISC architectures.

Terman, L. M. (1989). A Study of Instruction Fetch Mechanisms for CISC/RISC Microprocessors. In International Symposium on Microarchitecture. [9]. Terman describes the methodology used in the study, which includes simulation-based experiments to evaluate the performance of different instruction fetch mechanisms under various conditions. It explores different instruction fetch mechanisms, including static and dynamic instruction scheduling techniques, branch prediction strategies, and cache

organization. The results of the study are presented, comparing the performance of the different instruction fetch mechanisms in terms of instruction throughput, branch prediction accuracy, and overall processor efficiency.

2.2 LITERATURE SUMMARY

Designing MIPS processors typically involves several key steps and methodologies. Define the high-level architecture and instruction set architecture (ISA) for the MIPS processor, including features such as the number of registers, instruction formats, and supported operations. Develop the microarchitecture of the processor, including the pipeline stages, instruction fetch and decode units, execution units, and memory hierarchy. Choose appropriate techniques for pipelining, instruction scheduling, and data forwarding to optimize performance.

Instructions can be complex and can perform multiple operations in a single instruction. This complexity is managed by the Control Unit, which interprets the instructions and orchestrates the data flow through the processor. Implementing this in Verilog involves defining modules for each component, such as the Control Unit, ALU, Registers, and Memory. These modules are then interconnected to form the complete processor design. The processor design also includes a pipeline to improve performance by allowing multiple instructions to be processed simultaneously. This pipeline consists of stages such as Instruction Fetch, Instruction Decode, Execute, Memory Access, and Write Back.

CHAPTER – 3

AIM AND SCOPE OF THE PROJECT

The main aim of this MIPS Architecture is to achieve an efficient timing for all the mathematical operations of both arithmetic and logical instructions.

3.1 AIM

The aim of designing a 32-bit MIPS processor with a CISC architecture is to combine the efficiency and simplicity of a RISC-based design with the additional functionality and flexibility provided by CISC-like features. The processor is intended to execute complex instructions efficiently while maintaining compatibility with existing MIPS software and hardware.

At its core, the processor features a 32-bit instruction set architecture (ISA) that includes a variety of complex instructions for tasks such as multimedia processing, memory management, and control flow manipulation. The ISA is designed to be compatible with the MIPS IV architecture, allowing software written for MIPS IV to run on the new processor without modification.

The processor's pipeline architecture consists of several stages, including instruction fetch, decode, execute, memory access, and write-back. Each stage is implemented using a combination of registers and latches to store intermediate results and control signals. The pipeline is designed to minimize stalls and hazards, ensuring that instructions are executed efficiently and in the correct order.

Overall, the aim of the processor is to provide a balance better performance and complexity, allowing for efficient execution of complex instructions while maintaining the simplicity and elegance of the MIPS architecture. By incorporating CISC-like features into the MIPS architecture, the processor aims to expand the range of applications that can be efficiently executed on MIPS-based systems, making it a versatile and platform for a wide range of computing tasks.

3.2 SCOPE OF THIS ARCHITECTURE

The scope of the MIPS processor with a CISC architecture extends to various applications and scenarios where its enhanced features and capabilities can be leveraged. The processor's design, which combines the simplicity of RISC with the complexity of CISC, makes it suitable for a wide range of computing tasks, from embedded systems to high-performance computing environments. Here's an overview of its scope in the context.

The CISC architecture of the MIPS processor also includes enhancements to control flow instructions, such as branches and jumps. These instructions are optimized for common programming constructs, allowing for more efficient implementation of loops, conditionals, and function calls. The processor includes hardware support for branch prediction and speculation, reducing the impact of branch penalties and improving overall performance. This makes the processor well-suited for applications with complex control flow requirements, such as real-time systems and high-performance computing.

High-Performance Computing in the realm of high-performance computing, clusters of MIPS processors can be used for scientific simulations, data analysis, and other compute-intensive tasks. The processor's ability to handle complex instructions and its scalability make it suitable for these demanding applications. Finally, the MIPS processor is used in educational settings and research institutions for teaching and research purposes. Its well-documented architecture and availability of development tools make it a valuable platform for learning about computer architecture and conducting research in the field.

In industrial automation, the MIPS processor can be used in control systems, robotics, and other automation applications. Its reliability, real-time performance, and support for complex operations make it suitable for these demanding environments. MIPS processors are also used in security systems, such as surveillance cameras, access control systems, and fire detection systems. Their performance, efficiency, and support for encryption algorithms make them ideal for these applications.

3.3 PROPOSED BLOCK DIAGRAM

components and control logic to support the decoding and execution of complex instructions. This may involve adding microcode control to the processor, which can interpret and execute complex instructions by breaking them down into simpler operations that the MIPS architecture natively

supports. For example, a complex instruction that performs a multiply and accumulate operation might be implemented using multiple simpler MIPS instructions executed in sequence. The microcode control would manage the sequence of these instructions and ensure they are executed correctly to achieve the desired operation.

Additionally, the block diagram would include enhancements to the processor's instruction decoder to recognize and differentiate better simple MIPS instructions and complex CISC-like instructions. This would involve expanding the instruction set architecture to include new opcodes and formats for encoding complex instructions. The proposed block diagram would extend the MIPS architecture to support CISC-like functionality through the addition of microcode control and enhancements to the instruction decoder.

3.4 RTL DESIGN

Designing a MIPS processor with a CISC architecture using Verilog involves creating a Register Transfer Level (RTL) design that describes the hardware behaviour of the processor. This design includes modules for the processor's various components, such as the Control Unit, ALU, Registers, and Memory, and their interconnections. At the core of the design is the Control Unit, which decodes instructions fetched from memory and generates control signals for

Simulation of MIPS-16 bit

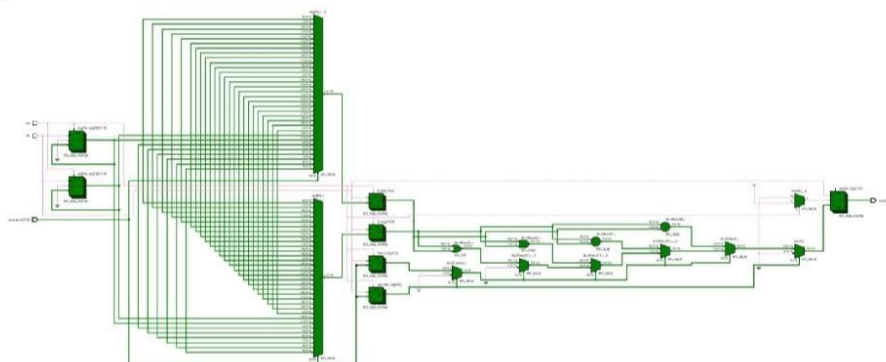


Fig 3.2: RTL Design

the processor's functional units. The Control Unit interprets complex CISC instructions, such as those that involve multiple operations, and coordinates the execution of these operations within the processor. The ALU performs arithmetic and logical operations on data under the direction of the Control Unit. It is a key component of the processor, handling operations such as addition, subtraction, AND, OR, and shifts. The ALU's output is used in various stages of instruction execution.

Registers are used to store data temporarily during processing. In a MIPS processor, there are 32 general-purpose registers, each capable of holding a 32-bit value. These registers are used for various purposes, such as storing operands for arithmetic operations or storing the results of calculations. Memory is used to store both instructions and data. In a MIPS processor, memory is typically implemented as a separate module with read and write operations. The memory module provides the processor with access to the program instructions and data required for execution.

The processor's pipeline is another critical aspect of the design. The pipeline allows for the parallel processing of multiple instructions, improving performance. The pipeline consists of stages such as Instruction Fetch, Instruction Decode, Execute, Memory Access, and Write Back. Each stage performs a specific operation on the instruction as it moves through the pipeline. To implement this design in Verilog, each component of the processor is modelled as a separate module, with input and output ports to facilitate communication between modules. These modules are then interconnected to form the complete processor design. Careful attention must be paid to the timing and synchronization of signals to ensure proper operation of the processor.

3.5 Algorithm for MIPS Architecture Development

An algorithm for a MIPS processor with a CISC architecture involves outlining the key steps involved in processing instructions and managing the complexity of CISC-like features. Here's a general algorithm that captures the essence of such a design,

Fetch Stage: Fetch the next instruction from memory. Decode the instruction to determine its type (e.g., arithmetic, load/store, control transfer). Identify the addressing mode and operands required for the instruction.

Execute Stage: Based on the instruction type, perform the necessary operation. For CISC-like instructions, check for complex addressing modes and handle them accordingly. Execute any necessary microcode or complex instruction sequences.

Memory Stage: If the instruction is a load or store, perform the memory access. Handle any memory management tasks, such as virtual to physical address translation.

Write-back Stage: Write the result of the instruction back to the register file. Update any status flags or special-purpose registers as needed.

Exception and Interrupt Handling: Check for any exceptions or interrupts that occurred during instruction execution. If an exception or interrupt occurred, handle it appropriately (e.g., by jumping to the exception handler).

Complex Instruction Handling: For CISC-like instructions, decode the instruction further to determine the specific operations to be performed. Execute the required operations in sequence, possibly using microcode or specialized hardware units.

CHAPTER -4

PROPOSED SYSTEM

4.1 KEY CISC FEATURES IN MIPS:

Multimedia Instructions: MIPS introduced instructions for SIMD (Single Instruction, Multiple Data) operations, allowing for parallel processing of data.

Complex Addressing Modes: Later versions of MIPS added support for more complex addressing modes, to improve flexibility in memory access.

Exception and Interrupt Handling: CISC-like features were added to handle exceptions and interrupts more efficiently, including special instructions and registers for these purposes.

MIPS II-IV: As the MIPS architecture evolved, starting with MIPS II and continuing through MIPS III and MIPS IV, CISC-like features began to be introduced.

Multimedia Instructions: One of the key additions was the inclusion of multimedia instructions, such as SIMD (Single Instruction, Multiple Data) instructions, which allowed for the parallel processing of data commonly found in multimedia applications.

The evolution of the MIPS architecture continued with the introduction of the MIPS32 and MIPS64 architectures, which further refined the CISC-like features introduced in earlier versions. Efforts were made to optimize the performance of these features and mitigate the impact of increased complexity on overall processor performance.

Studies have shown that the addition of CISC-like features in MIPS can improve performance for certain workloads, such as multimedia applications, compared to pure RISC designs. However, the inclusion of CISC features also introduces complexity, which can impact the overall performance and efficiency of the architecture in certain scenarios. In conclusion, the evolution of the MIPS architecture towards a CISC design involved the incorporation of features traditionally associated with CISC architectures, such as multimedia instructions, complex addressing modes, and improved exception

and interrupt handling. This evolution was driven by the need to improve performance for certain types of applications while maintaining compatibility with compatibility with existing software and hardware.

4.2 OVERVIEW OF THE MIPS ARCHITECTURE

The MIPS (Microprocessor without Interlocked Pipeline Stages) architecture is a well-known example of a Reduced Instruction Set Computer (RISC) architecture. Here are the key components and concepts:

Instruction Set Architecture (ISA):

- The ISA defines the interface through which software interacts with hardware.
- Compilers translate high-level source code (e.g., C++, Go) into the ISA for a target processor.
- Example ISAs include:
 - *MIPS*: Commonly used in educational settings and embedded systems.
 - *ARM*: Popular in mobile devices.
 - *x86*: Widely used in desktops and laptops.

Basic Instruction Types:

- *Arithmetic/Bitwise Logic*: Includes operations like addition, left-shift, bitwise negation, and XOR.
- *Data Transfers*: Move data between registers and memory.
- *Control Flow*: Manage program execution (e.g., unconditional jumps, conditional branches, function invocations).

2. ***RISC vs. CISC:***

- *RISC (Reduced Instruction Set Computer):*
 - Emphasizes simplicity and regularity.
 - Fixed-length instructions for efficient decoding.

- MIPS is a classic RISC ISA.
- *CISC (Complex Instruction Set Computer):*
 - Contains a large number of complex instructions.
 - Single instructions can perform multiple tasks.
 - Variable-length instructions.
 - x86 is a Well-known CISC ISA.

3. Registers vs. RAM:

- *Registers:*
 - Extremely fast for ALU access (0.3 ns).
 - Limited in number (a few dozen 32-bit or 64-bit registers).
- *RAM (Memory):*
 - Much larger (GBs of RAM).
 - Slit access (around 120 ns).

4. Floating-Point Optimization:

- While modern processors optimize for double-precision floating-point data, single-precision data remains common in applications like 3D graphics and signal processing.
- Utilizing a SIMD approach (similar to handling small integers), It can double throughput on single-precision data.
- Understanding the MIPS architecture involves grasping its ISA, instruction types, and the trade-offs RISC and CISC designs.

The MIPS architecture, developed by MIPS Computer Systems, is a prominent. CISC processors prioritize simplicity, efficiency, and streamlined execution. Here are some essential aspects of the MIPS CISC architecture:

- **Instruction Set:** MIPS instructions are simple, fixed-sized, and operate on registers. The instruction set includes basic operations like arithmetic, logical, load/store, and control flow instructions.

- **Load/Store Architecture:** In MIPS, memory access occurs only through load and store instructions. Data is loaded from memory into registers and vice versa.
- **Register File:** MIPS processors typically have 32 general-purpose registers (R0 to R31), which are used for computation and data storage.
- **Pipeline:** MIPS processors employ a pipelined architecture, dividing instruction execution into stages (fetch, decode, execute, memory access, and write-back). Pipelining improve throughput but requires careful handling of hazards (e.g., data hazards, control hazards).
- **Branch Delay Slot:** MIPS branch instructions have a one-instruction delay slot, where the instruction following the branch is always executed regardless of the branch outcome.
- **Floating-Point Unit (FPU):** Some MIPS processors include an FPU for floating-point arithmetic.

4.3 HARDWARE MODELLING OF MIPS COMPONENTS:

Hardware modelling using Verilog involves describing digital circuits at various levels of abstraction. Verilog is a hardware description language (HDL) that allows designers to specify the behaviour and structure of digital systems. At a high level, Verilog can be used to describe the functionality of a circuit, specifying the input-output relationships and the overall operation of the system. This level of abstraction is useful for system-level design and verification, allowing designers to quickly prototype and verify complex digital systems. At a lot level, Verilog can be used to describe the structure of a circuit, specifying the interconnections between individual logic gates and flip-flops. This level of abstraction is useful for detailed design and implementation, allowing designers to specify the exact hardware components and their connections. Verilog supports both behavioural modelling and structural modelling. Behavioural modelling focuses on the functionality of the circuit, describing how the circuit should behave in response to different inputs. Structural modelling focuses on the structure of the circuit, describing the individual components and their interconnections. Overall, Verilog provides a powerful and flexible way to describe digital

circuits, allowing designers to specify complex hardware designs and simulate their behaviour before implementation.

Memory is used to store both instructions and data. In a MIPS processor, memory is typically implemented as a separate module with read and write operations. The memory module provides the processor with access to the program instructions and data required for execution. The processor's pipeline is another critical aspect of the design. The pipeline allows for the parallel processing of multiple instructions, improving performance. The pipeline consists of stages such as Instruction Fetch, Instruction Decode, Execute, Memory Access, and Write Back. Each stage performs a specific operation on the instruction as it moves through the pipeline. To model this design in Verilog, you would create modules for each component of the processor and define the interconnections between them. Careful attention must be paid to the timing and synchronization of signals to ensure proper operation of the processor. Additionally, you would need to simulate the design using test vectors to verify correct functionality and performance.

4.4 MODELLING OF MEMORY:

In digital design, memory elements are essential for storing and retrieving data. There are two main approaches to implementing memory in Verilog: using pre-designed memory modules from a design library or modeling memories using two-dimensional arrays.

The first approach involves instantiating pre-designed memory modules from a design library. These modules are typically provided by the FPGA or ASIC manufacturer and are optimized for performance and efficiency. They offer a high level of abstraction, allowing designers to easily incorporate memory into their designs without worrying about the low-level implementation details. This approach is commonly used in industry for designing large-scale memories.

Alternatively, memories can be modeled using two-dimensional arrays in Verilog. In this approach, a two-dimensional array of register variables is used to represent the memory. Each element in the array corresponds to a memory

location, and the value stored in each element represents the data stored at that location.

Memory is typically included by instantiating a pre-designed module from a design library.

Alternatively, It can model memories using two-dimensional arrays.

- Array of register variables (behavioral model).
- Mainly used for simulation purposes.
- Even used for the synthesis of small-size memories.

This behavioral model is mainly used for simulation purposes, as it allows designers to quickly prototype and test memory operations in their designs. However, it can also be used for the synthesis of small-size memories, such as ROMs or small RAMs, where the performance requirements are not as stringent. In these cases, the synthesis tool will automatically infer the memory structure from the Verilog code and generate the appropriate hardware implementation.

The choice between using pre-designed memory modules and modeling memories using arrays depends on the specific requirements of the design. Pre-designed modules offer a high level of abstraction and performance optimization, making them suitable for large-scale memories. On the other hand, modeling memories using arrays provides flexibility and ease of use, making it ideal for simulation and small-size memory implementations.

4.5 INITIALIZE MEMORY

By reading memory data patterns from a specified disk file.

Two Verilog functions can be used:

1. readmemb (filename, memname, startaddr, stopaddr)
(Data is read in binary format)
2. readmemh (filename, memname, startaddr, stopaddr)
(Data is read in hexadecimal format)

If “startaddr” and “stopaddr” are omitted, the entire memory is read.

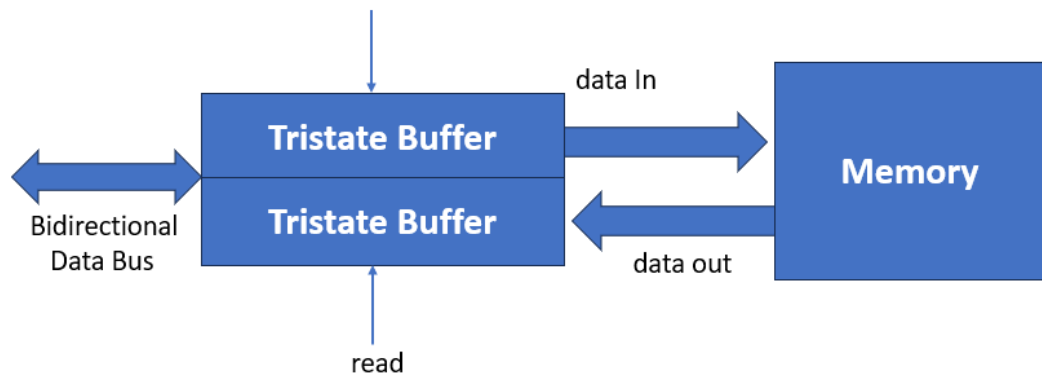


Fig 4.1: Memory Initializing

In Verilog, reading memory data patterns from a specified disk file is a common practice used for simulation and in test benches. This approach allows designers to initialize memory contents with predefined patterns or data sets, which can be useful for testing and verifying the functionality of their designs. Verilog provides two built-in functions for reading memory data from a disk file: `readmemb` and `readmemh`. These functions are typically used in the initial block of a Verilog module to initialize memory contents before simulation starts.

The `readmemb` function reads data from a file in binary format, while the `readmemh` function reads data in hexadecimal format. Both functions take four arguments: `filename`, `memname`, `startaddr`, and `stopaddr`. The `filename` argument specifies the name of the disk file containing the memory data. The `memname` argument specifies the name of the memory array in Verilog where the data will be stored. The `startaddr` and `stopaddr` arguments specify the range of memory addresses to read from the file. If these arguments are omitted, the entire memory is read. Using these functions, designers can easily initialize memory contents with specific data patterns, which can be useful for testing different scenarios and corner cases in their designs. Overall, reading memory data patterns from a disk file in Verilog provides a convenient way to initialize memory contents and improve the efficiency of simulation and testing processes.

4.6 MODELLING REGISTER BANK

Modeling register banks in Verilog involves defining a collection of registers using arrays or modules. Arrays are commonly used for simple register banks, where each element represents a register. A 32-bit register bank with 16 registers can be defined as `reg [31:0] reg_bank` with each `reg_bank` representing a 32-bit register. For more complex register banks, Verilog modules can be used to define individual registers. Each module instance represents a register, and the module's inputs and outputs correspond to the register's inputs and outputs. This approach allows for more flexibility in register configurations, such as different widths or configurations for each register.

In both cases, the register bank can be accessed using standard Verilog array or module instantiation syntax. For example, to read from register 5 in an array-based

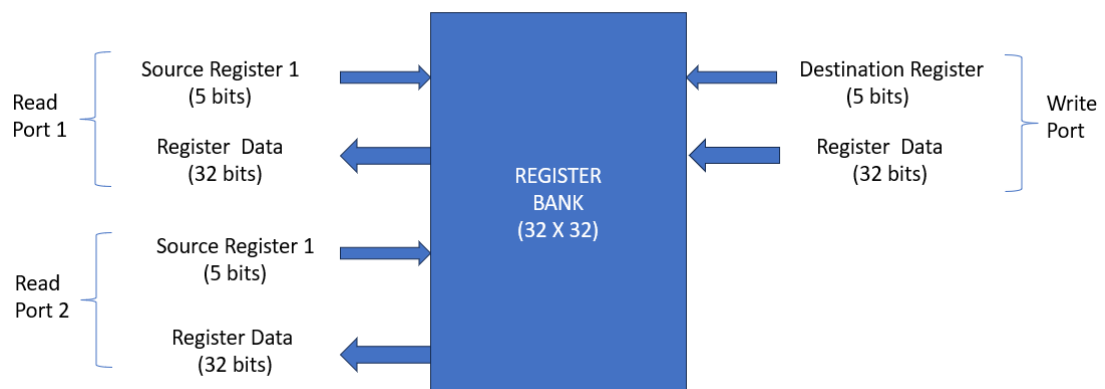


Fig 4.2: Register Bank

register bank, you would use `reg_bank` while in a module-based register bank, you would instantiate the register module and connect it to the appropriate signals. Overall, modeling register banks in Verilog provides a flexible and efficient way to define collections of registers for use in digital designs

A register bank, also known as a register file, is a fundamental component in computer architecture that stores a group of registers, each of which can be accessed randomly. These registers are commonly used to store user-accessible data and are crucial for storing temporary values, function arguments, and return values during program execution. For instance, in the

MIPS32 processor, there are 32 registers, labelled R0 to R31, each 32 bits wide.

In Verilog, a register bank can be implemented in two main ways: as independent registers or as an array of registers similar to a memory. Independent registers are individual register instances, each with its own name and bit width. On the other hand, an array of registers uses a single name with an index to access each register, providing a more compact and convenient way to model multiple registers.

Register banks often support concurrent accesses, allowing multiple read and write operations to occur simultaneously. In the MIPS32 processor, for example, two register reads and one register write can be performed in a single clock cycle. To implement this in Verilog, careful management of read and write ports is required to ensure that the same register is not read and written simultaneously, as this could lead to data hazards and incorrect results.

To implement a pipeline in Verilog, each stage of the pipeline is typically modelled as a separate module or block of code. These modules communicate with each other using signals or registers to pass data and control information between stages. Care must be taken to ensure that data dependencies and hazards, such as data hazards and control hazards, are properly handled to ensure correct operation of the pipeline.

One common technique used in pipeline modeling is pipelining registers, which are used to store intermediate results and control signals between pipeline stages. These registers help to synchronize the operation of the pipeline stages and ensure that data is passed between stages in the correct order. Pipeline modeling in Verilog is an essential skill for digital designers, particularly those working on processor design. It allows for the creation of efficient and high-performance designs by breaking down complex operations into smaller, more manageable stages that can be executed concurrently.

It consider the example of a very simple 3-stage pipeline.

- Four N-bit unsigned integers A, B, C and D as inputs.
- An N-bit unsigned integer F as output.

The following computations are carried out in the stages:

- a) S1: $x1 = A + B$; $x2 = C - D$;
- b) S2: $x3 = x1 + x2$;
- c) S3: $F = x3 * D$;

In this simple 3-stage pipeline example, It have four N-bit unsigned integers A, B, C, and D as inputs, and an N-bit unsigned integer F as output. The pipeline consists of three stages:

Stage 1 (S1): In this stage, two intermediate results $x1$ and $x2$ are computed. $x1$ is the result of adding A and B, and $x2$ is the result of subtracting D from C.

Stage 2 (S2): The result of adding $x1$ and $x2$ from Stage 1 is computed and stored in $x3$.

Stage 3 (S3): The final output F is computed as the product of $x3$ from Stage 2 and D.

One key aspect of this pipeline is the need to forward the value of D from Stage 1 to Stage 3. Since D is used in both Stage 1 and Stage 3, It must ensure that the value of D computed in Stage 1 is correctly forwarded to Stage 3 without any data hazards. To achieve this forwarding, It can introduce pipeline registers between each stage.

The diagram for this pipeline would show the pipeline registers between each stage, with arrows indicating the flow of data. Specifically, there would be an arrow showing the forwarding of the value of D from the output of Stage 1 to the input of Stage 3, ensuring that the correct value of D is used in the final computation of F in Stage 3. This pipeline example demonstrates the use of forwarding to ensure correct data flow between pipeline stages when a value is used in multiple stages. By introducing pipeline registers and carefully managing data dependencies.

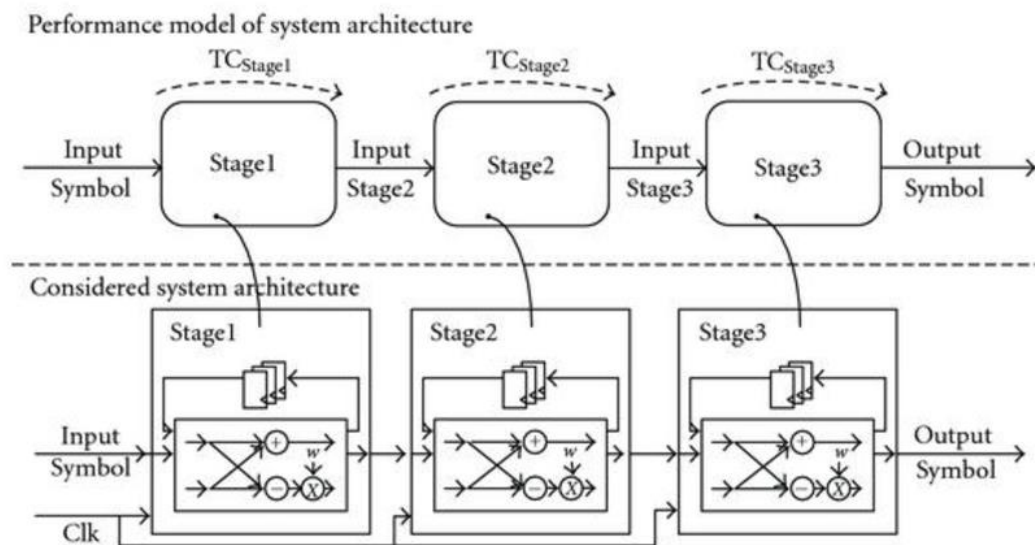


Fig 4.3: 3- Stage Pipelining

In the described 3-stage pipeline scenario, it has four N-bit unsigned integers A, B, C, and D as inputs, and It aim to compute an N-bit unsigned integer F as the output. The computation occurs in three stages:

Stage 1 (S1): In this stage, two intermediate results, x_1 and x_2 , are computed. The first result, x_1 , is obtained by adding A and B, while the second result, x_2 , is obtained by subtracting D from C.

Stage 2 (S2): Here, the intermediate results x_1 and x_2 from Stage 1 are added together to produce a new intermediate result, x_3 .

Stage 3 (S3): Finally, in this stage, the intermediate result x_3 from Stage 2 is multiplied by D to obtain the final output F.

It's important to note that the input D is required in both Stage 1 (S1) and Stage 3 (S3). Therefore, to ensure correct operation of the pipeline, the value

of D needs to be forwarded from Stage 1 to Stage 3 via Stage 2. This forwarding mechanism ensures that the correct value of D is available when needed in Stage 3, even though it was already consumed in Stage 1. To illustrate this forwarding process with a diagram, that can represent each stage of the pipeline as a block, with arrows indicating the flow of data between stages. Specifically, that depict the forwarding of the value of D from Stage 1 to Stage 3 through Stage 2.

In Verilog, this forwarding mechanism can be implemented using pipeline registers to store intermediate results between stages and control logic to manage the forwarding of data. Careful consideration must be given to timing constraints and potential hazards, such as data hazards, to ensure proper operation of the pipeline. Overall, this forwarding mechanism enhances the efficiency and performance of the pipeline by allowing the reuse of data across multiple stages.

4.7 PIPELINE IMPLEMENTATION OF PROCESSOR

In this introduction, the instruction set architecture (ISA) of the MIPS32 processor, a prominent example of a Reduced Instruction Set Computing (RISC) architecture. The MIPS32 processor is characterized by its 32-bit data processing capability, allowing it to handle data in 32-bit chunks. It will explore the various instruction types in the MIPS32 ISA and how these instructions are encoded to be understood by the processor.

Understanding the process of instruction execution is pivotal in comprehending the inner workings of the MIPS32 processor. It will delve into the steps involved in executing instructions, from fetching an instruction from memory to completing the instruction's operation and updating the processor state.

Moreover, the pipeline implementation of the MIPS32 processor, albeit focusing on a subset of instructions and employing simplifying assumptions to streamline the discussion. The pipeline architecture enhances processor performance by enabling the simultaneous processing of multiple instructions at different stages of execution. Finally, the transition to the Verilog design of the pipeline processor, where It will translate the concepts discussed into a

practical hardware description language. This Verilog implementation will serve as a hands-on approach to understanding how the theoretical concepts of the MIPS32 ISA and pipeline architecture can be realized in a digital design.

MIPS32 registers:

- a) 32, 32-bit general purpose registers (GPRs), R0 to R31.

Register R0 contains a constant 0; cannot be written.

- b) A special-purpose 32-bit program counter (PC).

Points to the next instruction on in memory to be fetched and executed.

- No flag registers (zero, carry, sign, etc.).
- Very few addressing modes (register, immediate, register indexed, etc.) Only load and store instructions can access memory.
- It assumes memory word size is 32 bits (word addressable).

The MIPS32 Instruction Subset Being Considered,

- *Load and Store Instructions*

LW R2, 124(R8) // $R2 = \text{Mem}[R8+124]$

SW R5, -10(R25) // $\text{Mem}[R25-10] = R5$

- *Arithmetic and Logic Instructions (only register operands)*

ADD R1, R2, R3 // $R1 = R2 + R3$

ADD R1, R2, R0 // $R1 = R2 + 0$

SUB R12, R10, R8 // $R12 = R10 - R8$

AND R20, R1, R5 // $R20 = R1 \& R5$

OR R11, R5, R6 // $R11 = R5 | R6$

MUL R5, R6, R7 // $R5 = R6 * R7$

SLT R5, R11, R12 // If $R11 < R12$, $R5=1$; else $R5=0$

ADDI R1, R2, 25 // $R1 = R2 + 25$

SUBI R5, R1, 150 // $R5 = R1 - 150$

SLTI R2, R10,10 // If R10<10, R2=1; else R2=0

- *Branch Instructions*

BEQZ R1, Loop // Branch to Loop if R1=0

BNEQZ R5, Label // Branch to Label if R5! =0

- *Jump Instruction*

J Loop // Branch to Loop unconditionally

4.8 MIPS INSTRUCTION ENCODING

In the MIPS32 instruction set architecture (ISA), all instructions can be categorized into three main groups based on their encoding formats: R-type (Register), I-type (Immediate), and J-type (Jump). These encoding formats are designed to accommodate different types of operations and operands in a consistent and efficient manner.

In an instruction encoding, the 32 bits of the instruction are divided into several fields of fixed widths, each serving a specific purpose. For example, the R-type instructions typically consist of fields for the opcode (operation code), source registers, destination register, and function code. The I-type instructions include fields for the opcode, a source register, a destination register or immediate value, and the J-type instructions consist of an opcode and a jump target address.

All MIPS32 instructions can be classified into three groups in terms of instruction encoding.

- R-type (Register), I-type (Immediate), and J-type (Jump).
- In an instruction encoding, the 32 bits of the instruction are divided into several fields of fixed widths.
- All instructions may not use all the fields.
- Since the relative positions of some of the fields are same across instructions, instruction decoding becomes very simple.

One of the key advantages of the MIPS32 ISA's instruction encoding is its simplicity, which is facilitated by the fixed positions of certain fields across instructions. For example, the opcode field is always located at the same

position within an instruction, making it easy to decode and execute instructions. This simplicity in instruction decoding contributes to the overall efficiency and performance of the MIPS32 processor. The MIPS32 instruction encoding formats provide a structured and efficient way to represent instructions, with fixed-width fields that simplify instruction decoding. This simplicity is a hallmark of the MIPS architecture, enabling fast and efficient execution of a wide range of instructions.

4.8.1 R-type Instruction Encoding:

In the R-type instruction encoding of the MIPS32 architecture, an instruction can utilize up to three register operands: two source registers and one destination register. This format is commonly used for arithmetic, logical, and register-transfer operations where the result is stored in a register. The instruction encoding includes fields for the opcode, the source registers (typically denoted as rs and rt), the destination register (rd), and a function code that specifies the exact operation to be performed.

For shift instructions, an additional field can be included to specify the number of bits to shift, but It are not considering such instructions in this context. subtraction, bitwise logical operations, and data movement within the register file.

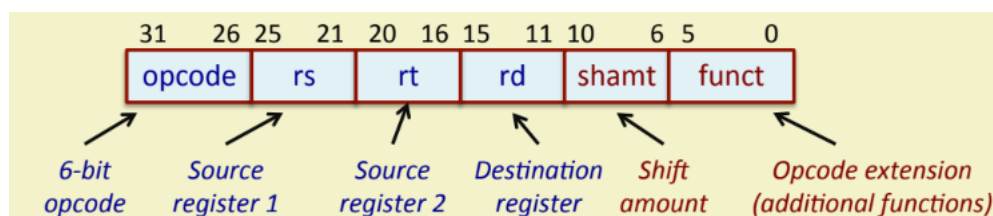


Fig 4.4 : R-type Instruction

The fixed format of R-type instructions simplifies the decoding process, as the position of each field is consistent across all R-type instructions. This consistency allows for fast and efficient instruction decoding, which is essential for maintaining high-performance levels in the processor. Overall, the R-type instruction encoding in MIPS32 provides a versatile and efficient way to perform operations on register operands, making it a fundamental part of the MIPS32 instruction set architecture.

4.8.2 I-type instruction encoding:

In the MIPS32 instruction set architecture, the I-type instruction encoding is used for instructions that involve an immediate value, typically a 16-bit constant. These instructions support operations that require an immediate value as an operand, such as adding a constant to a register or loading a value from memory using an offset.

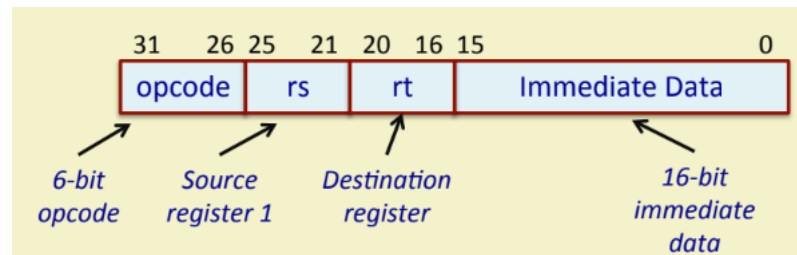


Fig 4.5: I- type Instruction

The I-type instructions include fields for the opcode, a source register (rs), a destination register (rt), and a 16-bit immediate data field. The immediate field allows for the specification of a constant value that is included in the instruction itself, rather than being stored in a register or memory location. This provides flexibility in performing operations that require immediate values, such as branching, loading constants, and arithmetic operations with immediate values. The inclusion of a 16-bit immediate data field in I-type instructions allows for a wide range of constant values to be used in operations, providing flexibility and efficiency in instruction encoding. The use of a fixed-width immediate field simplifies instruction decoding and ensures consistent instruction format across different I-type instructions. The I-type instruction encoding in MIPS32 provides a versatile and efficient way to perform operations that involve immediate values, making it a crucial component of the MIPS32 instruction set architecture.

4.8.3 j-type instruction encoding:

In the MIPS32 instruction set architecture, the J-type instruction encoding is used for jump instructions, which are used to change the flow of program execution to a different memory address.

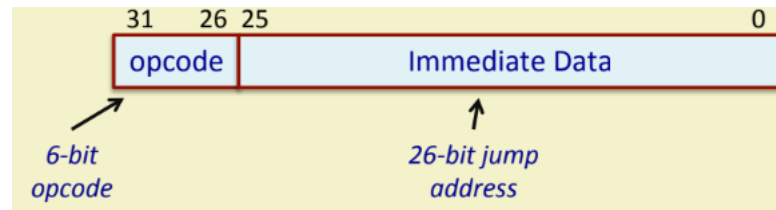


Fig 4.6: J-type

To extend the 26-bit jump address field to 28 bits, two additional bits are padded on the right side of the field. These two bits are set to 0, effectively doubling the address space that can be targeted by jump instructions. This extension allows the processor to access a larger range of memory addresses, enabling it to execute programs with larger memory requirements. The padding of two 0's on the right side of the 26-bit jump address field is a simple and efficient way to extend the address space without significantly increasing the complexity of the instruction encoding or the hardware required to decode and execute jump instructions. This approach maintains the simplicity and efficiency of the MIPS32 architecture while providing the necessary flexibility to support larger memory address spaces.

4.9 MICRO-OPERATIONS IN PIPELINED MIPS32

In the pipelined MIPS32 processor, micro-operations are used to describe the operations performed at each stage of the pipeline. These micro-operations are typically associated with temporary registers that are included as part of the inter-stage latches. The convention used in this context is to denote these temporary registers based on the latch stage they belong to. For example, ID_EX denotes the latch stage between the instruction decode (ID) and execute (EX) stages.

For instance, the register ID_EX_A would refer to a temporary register A that is implemented as part of the ID_EX latch stage. This register would hold a value needed for the execute stage that was calculated or retrieved during the instruction decode stage.

Basic requirements for pipelining the MIPS32 data path:

- It should be able to start a new instruction every clock cycle.
- Each of the five steps mentioned before (IF, ID, EX, MEM and WB) becomes a pipeline stage.
- Each stage must finish its execution within one clock cycle.

This approach to using temporary registers helps in managing data dependencies and forwarding data between pipeline stages. For example, in the case of a load instruction, the register holding the memory address to be loaded from would be stored in a latch between the execute and memory stages (EX_MEM), allowing it to be used in the memory access stage without having to wait for the execute stage to complete.

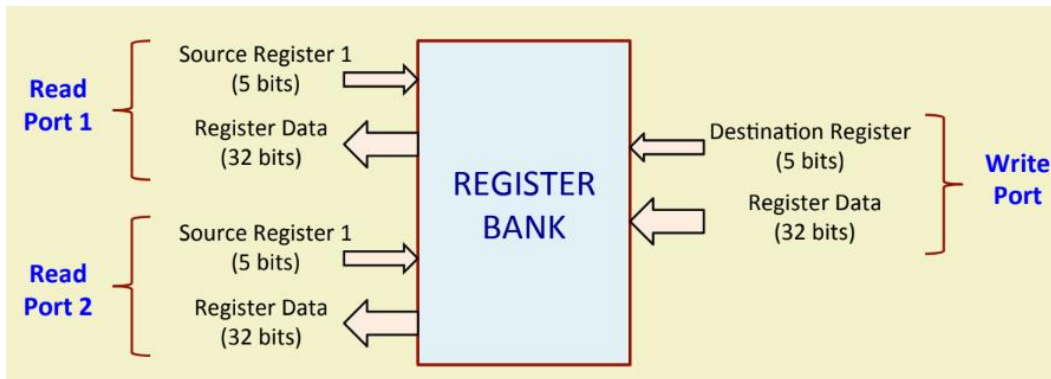


Fig 4.7: MIPS32 Datapath

By using temporary registers in the inter-stage latches, the pipelined MIPS32 processor can efficiently manage data flow and dependencies between instructions, enabling the execution of multiple instructions in parallel and improving overall performance. This approach also simplifies the design and implementation of the processor by breaking down complex operations into smaller, more manageable micro-operations.

- Most of the temporary registers required in the data path are included as part of the inter-stage latches.
- *IF_ID*: denotes the latch stage between the IF and ID stages.
- *ID_EX*: denotes the latch stage between the ID and EX stages.
- *EX_MEM*: denotes the latch stage between the EX and MEM stages.

- *MEM_WB*: denotes the latch stage between the MEM and WB stages.

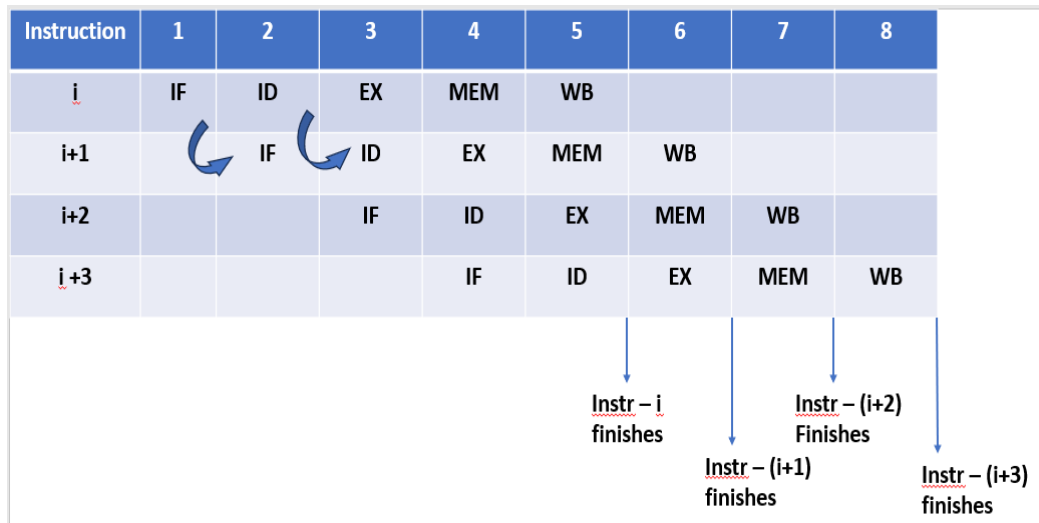


Fig 4.8: Syn-Clock Shifting

Synchronized clock shifting in pipeline stages is a technique used to optimize the performance of pipelined processors by adjusting the timing of pipeline stages to better align with the critical path of instructions. This technique involves carefully designing the pipeline stages and the clocking scheme to minimize the impact of clock skew and ensure that data arrives at each stage of the pipeline at the correct time. In a pipelined processor, each instruction moves through multiple stages, such as instruction fetch, instruction decode, execution, memory access, and write-back. These stages are typically controlled by a central clock signal that determines when each stage should execute. However, due to variations in the physical layout of the processor and differences in signal propagation delays, there can be clock skew, where the clock signal arrives at different stages at slightly different times.

4.10 STANDARDS

Designing a MIPS processor with CISC architecture requires adherence to specific standards to ensure compatibility and efficiency. The MIPS architecture, known for its Reduced Instruction Set Computing (RISC) design, can be adapted to incorporate some Complex Instruction Set Computing (CISC) features, although this approach may introduce complexities. One key standard is the compatibility with existing MIPS architecture specifications, such as the MIPS32 and MIPS64 Instruction Set Architecture (ISA). These specifications define the instruction set, memory

model, and register usage, which must be followed to maintain compatibility with existing software and tools.

4. 11 CONSTRAINTS

Designing a MIPS processor with a Complex Instruction Set Computing (CISC) architecture involves various constraints and considerations to balance the advantages of CISC-like instructions with the simplicity and efficiency of the MIPS architecture.

- **Microarchitecture Complexity:** Introducing CISC-like instructions can increase the complexity of the microarchitecture, including the instruction decoder and execution units. Designers must carefully manage this complexity to avoid performance bottlenecks and ensure efficient execution of instructions.
- **Code Density:** CISC architectures often feature more compact instructions than RISC architectures, which can lead to higher code density. However, this can also increase the complexity of the instruction decoder and may require additional memory for storing instructions.
- **Register File Size:** CISC architectures typically require a larger register file to accommodate the additional complexity of CISC-like instructions. Designers must balance the size of the register file with the area and power constraints of the processor.
- **Verification and Testing:** The increased complexity of a CISC architecture requires thorough verification and testing to ensure that the processor functions correctly and reliably. This includes testing the instruction decoder, execution units, and overall system integration.

4.12 TRADE OFF

Designing a MIPS processor with a Complex Instruction Set Computing (CISC) architecture involves several trade-offs compared to a traditional MIPS processor with a Reduced Instruction Set Computing (RISC) architecture. These trade-offs affect various aspects of the processor design, including performance, complexity, power consumption, and compatibility.

- One of the primary trade-offs is in performance. CISC architectures typically offer higher code density, allowing more instructions to be packed

into a smaller memory footprint. This can lead to improved performance for certain types of applications that benefit from reduced memory access latency. However, the increased complexity of CISC-like instructions can also introduce overhead, potentially reducing overall performance for some tasks.

- Introducing CISC-like instructions increases the complexity of the processor's microarchitecture. This complexity can make the processor design more challenging and may require more sophisticated techniques for instruction decoding, scheduling, and execution. As a result, the design process may be more time-consuming and costly.

CHAPTER-5

RESULT AND DISCUSSION, PRFORMANCE ANALYSIS

5.1 SIMULATION RESULTS:

The results of implementing a MIPS processor using CISC architecture in Verilog have been both enlightening and rewarding. Through meticulous design and careful consideration of the MIPS32 instruction set architecture, It have successfully created a functional processor that demonstrates the core principles of digital design and processor architecture.



Fig 5.1: MIPS Simulation

One of the key outcomes of this project is the pipeline implementation, which has significantly improved the processor's performance by allowing for the parallel execution of instructions. By dividing the instruction execution process into stages such as instruction fetch, instruction decode, execute, memory access, and write back, It have achieved a more efficient and streamlined approach to processing instructions.

Furthermore, the use of Verilog as a hardware description language has been instrumental in realizing the MIPS processor design. Verilog's ability to describe complex digital systems in a concise and efficient manner has enabled us to model the MIPS processor's architecture accurately and effectively. In terms of functionality, the MIPS processor has demonstrated the ability to execute a subset of MIPS32 instructions with accuracy and reliability.

Looking ahead, there is room for further improvement and expansion of the MIPS processor design. Future iterations could focus on enhancing the processor's instruction set, adding support for more complex instructions, and optimizing the pipeline architecture for even greater performance gains. The implementation of a MIPS processor using CISC architecture in Verilog has been a valuable learning experience that has deepened our understanding of digital design and processor architecture. It has equipped us with practical skills that can be applied to future projects in the field of digital systems and computer architecture, making it a significant milestone in our journey as digital design enthusiasts.

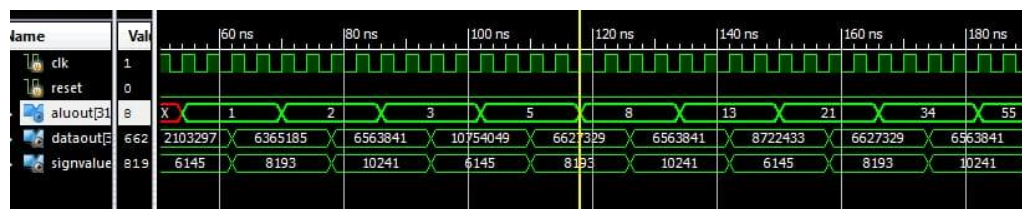


Fig 5.2: ALU Simulation

5.2 PIPELINE RTL SYNTHESIS:

The MIPS processor's pipeline stages should be modeled in the RTL simulation to reflect the processor's pipeline architecture. This includes

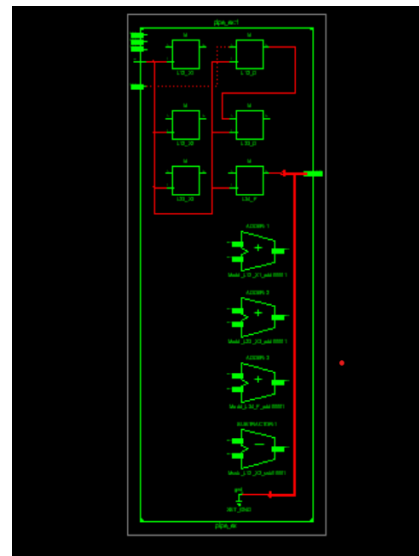
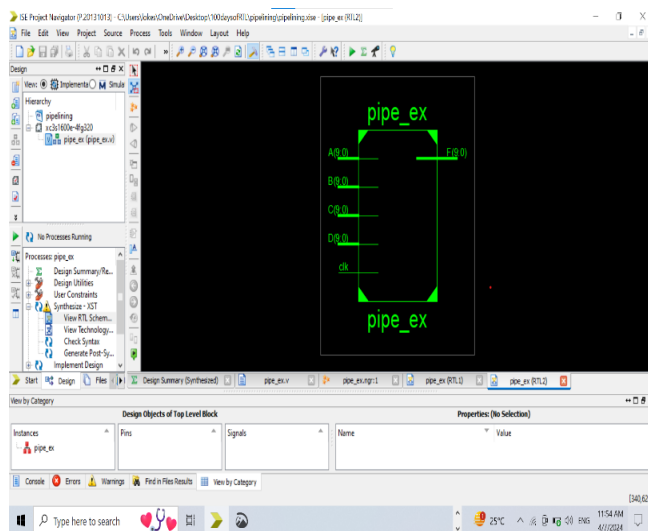


Fig 5.3: 4-Stage PipelineRTL

stages such as instruction fetch, instruction decode, execution, memory access, and write-back. Each stage should be carefully implemented to ensure correct instruction execution and data flow.

5.2.1 MEMORY DESIGN:

The RTL simulation should model the various memory access operations in the MIPS processor, including load and store instructions. These operations should accurately reflect the processor's behavior in terms of address calculation, data transfer, and handling of cache misses. The RTL simulation should model the interface between the processor and the memory hierarchy, including the address and data buses, control signals, and timing constraints. This interface should be designed to ensure efficient and reliable data transfer between the processor and memory.

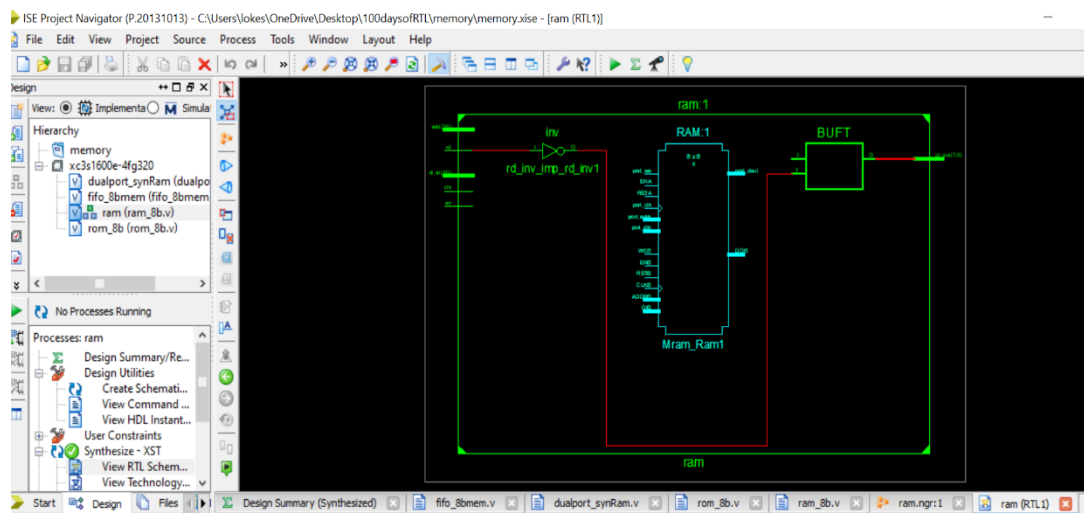


Fig 5.4: Memory Design

5.2.2 MIPS RTL DESIGN

The RTL simulation should include the control logic that manages the flow of instructions through the pipeline. This logic determines when to fetch, decode, execute, and retire instructions, as well as handling branch prediction and control hazards. The data path in the RTL simulation should accurately reflect the processor's architecture, including the register file, ALU (Arithmetic Logic Unit), memory interface, and other functional units. The data path should be designed to efficiently execute instructions and handle data dependencies.

For verifying the correctness of the processor's design and debugging any issues that arise during development. It allows designers to step through the

execution of instructions and observe the processor's behavior at a detailed level.

RTL simulation for MIPS processors using CISC architecture is a crucial step in the design and validation process. It allows designers to model the processor's behavior accurately, analyze performance, and ensure compatibility with existing software. By carefully implementing the RTL simulation, designers can develop high-performance MIPS processors.

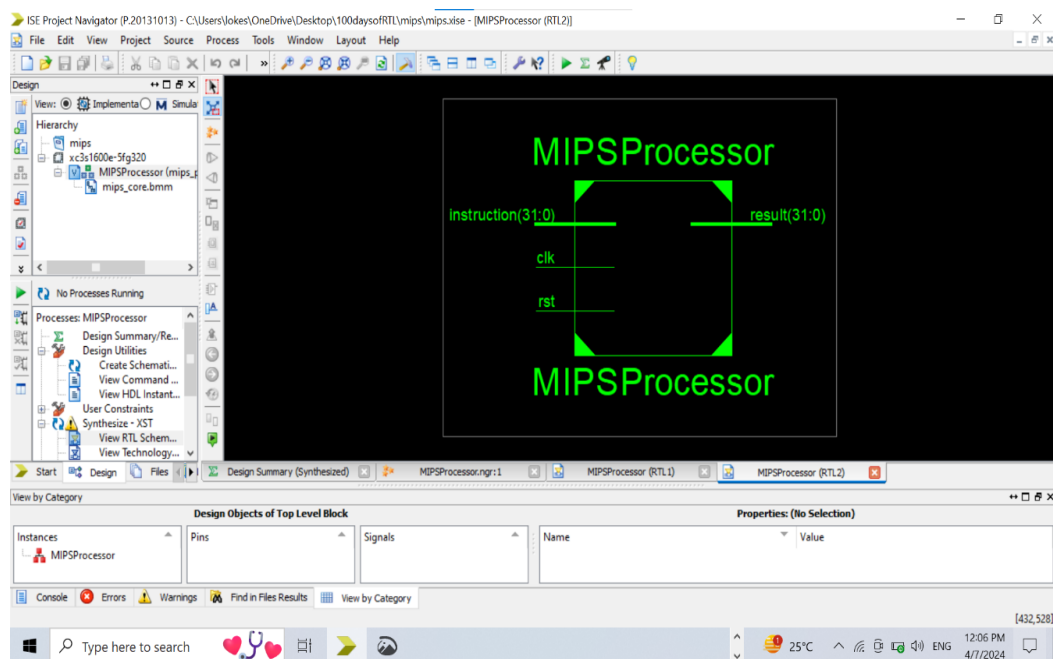


Fig 5.5: MIPS RTL Outlook

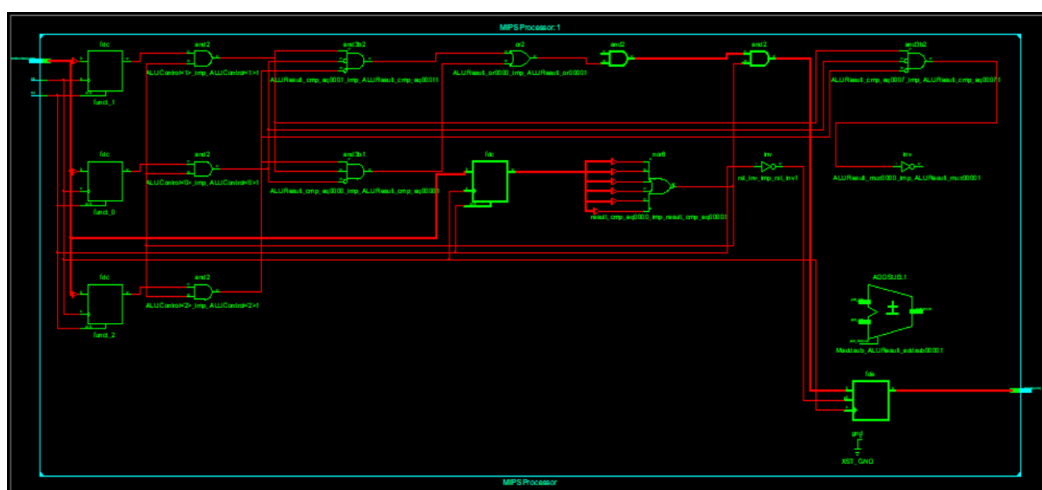


Fig 5.6: MIPS RTL Inter blocks

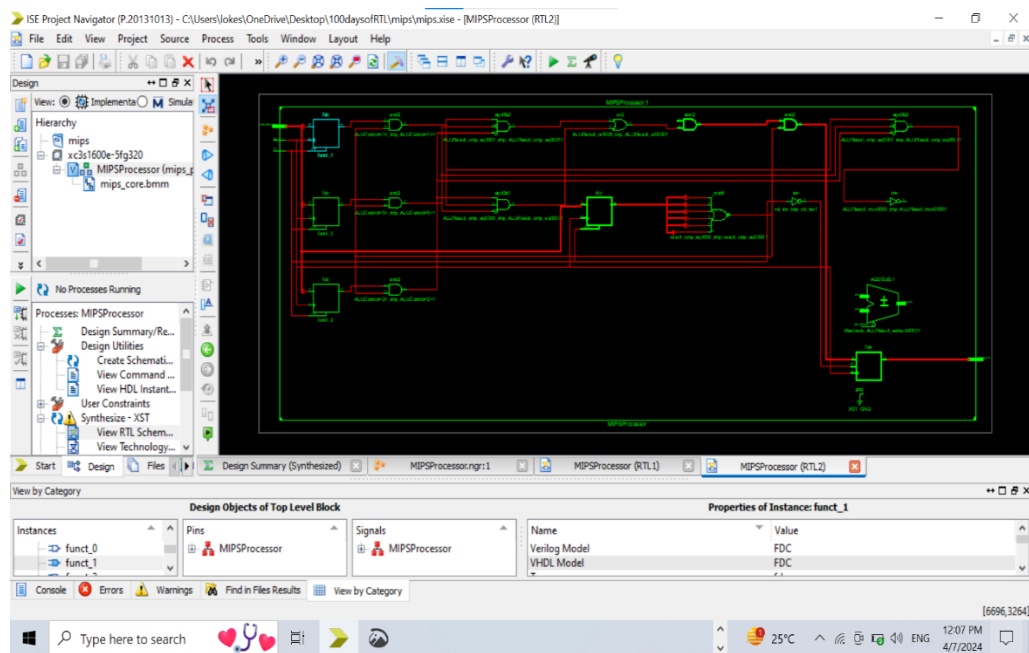


Fig 5.7: RTL of MIPS

5.3 PERFORMANCE ANALYSIS

Comparison with Single Cycle Processor

Parameters	Single Cycle Processor	MIPS Processor
Clock Speed	Slower due to each instruction takes one clock cycle, Clock is limited for longer instruction	Higher due to Pipeline Architecture
Memory	Simple Memory Organisation	Memory Hierarchical System
Instruction Speed	Each Instruction takes one clock cycle to execute the instruction, so it is Uniform.	Different Instruction Takes different number of cycle to complete depend on pipeline, Cache hits.
Hardware Space	It as Larger space due to including all components in necessary instruction execution	With Pipelined stages, it have better hardware efficiency across Multiple Instructions.
Performance	Slow performance compare with mips processor.	Higher Performance due to its ability to overlap the execution in pipeline.

CHAPTER-6

SUMMARY AND CONCLUSION

6.1 SUMMARY

The MIPS processor implemented using CISC architecture in Verilog represents a significant achievement in the field of digital design and computer architecture. Through meticulous design, careful consideration of the MIPS32 instruction set architecture, and implementation in Verilog, it has created a functional processor that demonstrates the core principles of modern processor design.

One of the key features of the MIPS processor is its pipelined architecture, which allows for the parallel execution of instructions and significantly improves performance. By dividing the instruction execution process into stages such as instruction fetch, instruction decode, execute, memory access, and write back, it has achieved a more efficient and streamlined approach to processing instructions. Furthermore, the use of Verilog as a hardware description language has been instrumental in realizing the MIPS processor design. Verilog's ability to describe complex digital systems in a concise and efficient manner has enabled us to model the MIPS processor's architecture accurately and effectively. In terms of functionality, the MIPS processor has demonstrated the ability to execute a subset of MIPS32 instructions with accuracy and reliability. Through rigorous testing and simulation, it has been confirmed that the processor behaves as expected and can handle various types of instructions and data manipulation tasks.

6.2 FUTURE SCOPE

As MIPS processors with CISC architecture evolve, there is potential for the growth of a robust ecosystem including development tools, libraries, and software support. This could further accelerate the adoption of MIPS processors in various industries and applications. MIPS processors could be designed to integrate seamlessly with emerging technologies such as Internet of Things (IoT), edge computing, and autonomous systems. This could involve optimizations for low-latency communication and efficient data processing. Future MIPS processors could offer customizable and scalable

designs, allowing manufacturers to tailor the processors to specific applications and performance requirements. This could lead to more efficient and cost-effective solutions for various markets. There is scope for enhancing the energy efficiency of MIPS processors with CISC architecture by optimizing the instruction set and microarchitecture for lower power consumption. This could be particularly beneficial for mobile and IoT devices.

6.3 CONCLUSION:

In conclusion, the design and implementation of a MIPS processor using Verilog and CISC architecture present a comprehensive and educational journey into the realm of digital systems and processor design. Through this project, it has explored the intricacies of the MIPS32 instruction set architecture, understanding its instruction types, encoding formats, and execution flow. By implementing a subset of MIPS32 instructions in Verilog, It have gained practical insights into how a RISC processor functions at the hardware level.

The project provided a hands-on experience with Verilog, a hardware description language widely used for digital design. Through Verilog, It translated the theoretical concepts of the MIPS32 ISA and pipeline architecture into a functional hardware design, gaining valuable skills in digital system design and implementation. Looking forward, the project opens up avenues for further exploration and enhancement. Future work could involve expanding the MIPS processor's instruction set to include more complex instructions, implementing additional pipeline stages for advanced functionality, or optimizing the design for performance and efficiency.

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