

LOW POWER 3-BIT DECODER DESIGN USING MEMRISTOR

Submitted in partial fulfillment of the requirements for the award of Bachelor of
Engineering degree in Electronics and Communication Engineering

by

K.S.V.S. RAKESH (40130103)

K. GANESH (40130104)



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHOOL OF ELECTRICAL AND ELECTRONICS

SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY

(DEEMED TO BE UNIVERSITY)

CATEGORY -1 UNIVERSITY BY UGC

Accredited with Grade "A++" by NAAC | 12B Status by UGC | Approved by AICTE

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119

APRIL - 2024



SATHYABAMA

INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)

CATEGORY-I UNIVERSITY BY UGC

Accredited "A++" Grade by NAAC | 12B Status by UGC | Approved by AICTE

www.sathyabama.ac.in

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of **K.S.V.S. RAKESH (40130103)**, **K. GANESH (40130104)** who carried out the Project entitled "**LOW POWER 3-BIT DECODER DESIGN USING MEMRISTOR**" under our supervision from November 2023 to April 2024.


Internal Guide

Dr. L. MAGTHELIN THERASE, M.E, Ph.D.,


Head of the Department

Dr. T. RAVI, M.E, Ph.D.,

Submitted for Viva voce Examination held on 17-04-2024

Internal Examiner

External Examiner

DECLARATION

We **K. GANESH, K.S.V.S. RAKESH** hereby declare that the Project Report entitled “**LOW POWER 3-BIT DECODER DESIGN USING MEMRISTOR**” done by us under the guidance of **Dr. L. MAGTHELIN THERASE M.E, Ph.D.**, Dept of Electronics and Communication Engineering, SATHYABAMA INSTITUTE OF SCIENCE AND TECHNOLOGY, CHENNAI, is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

DATE: 17-04-2024

PLACE: Chennai

SIGNATURE OF THE CANDIDATE/S

1. K.S.V.S. Rakesh
2. K. Ganesh

ACKNOWLEDGEMENT

I am pleased to acknowledge my sincere thanks to **The Board of Management of Sathyabama Institute of Science and Technology** for their kind encouragement in doing this project and for completing it successfully. I am grateful to them.

I convey my thanks to **Dr. N.M. NANDHITHA M.E., Ph.D., Dean, School of Electrical and Electronics**, and **Dr. T. RAVI M.E., Ph.D., Head of the Department of Electronics and Communication Engineering** for providing me necessary support and details at the right time during the progressive reviews.

I would like to express my sincere and deep sense of gratitude to my Project Guide **Dr. L. MAGTHELIN THERASE M.E, Ph.D.**, dept. of Electronics and Communication Engineering for her valuable guidance, suggestions and constant encouragement paved way for the successful completion of my project work.

I wish to express my thanks to all Teaching and Non-teaching staff members of the Department of Electronics and Communication Engineering who were helpful in many ways for the completion of the project.

ABSTRACT

In the pursuit of energy-efficient and innovative VLSI designs, the integration of memristor technology has emerged as a promising avenue. This project endeavours to explore the design and implementation of a low-power 3-bit decoder utilizing memristor devices. The memristor's unique properties, such as non-volatility and low energy consumption, offer an unprecedented opportunity for advancing VLSI circuits.

The proposed 3-bit decoder leverages memristors to decode a 3-bit binary input into a unique 3-bit output representation, enabling a compact and efficient decoding solution. Throughout the project, various low-power design methodologies and memristor-based optimization techniques are investigated to minimize power consumption while ensuring reliable performance. This project not only delves into the theoretical underpinnings of memristor technology but also embraces practical challenges in designing memristor-based VLSI circuits. Extensive simulations and verification processes are conducted to validate the decoder's correctness and robustness.

The potential applications of memristor-based decoders extend beyond this specific project, contributing to the broader exploration of memristor technologies and their integration into modern VLSI designs. The outcomes of this study will not only enrich the realm of VLSI but also pave the way for more energy-efficient and technologically advanced integrated circuits, propelling the semiconductor industry towards a sustainable and innovative future.

TABLE OF CONTENTS

CHAPTER No.	TITLE	PAGE No.
	ABSTRACT	V
	LIST OF ABBREVIATIONS	IX
	LIST OF FIGURES	X
	LIST OF TABLES	XII
1	INTRODUCTION	1
	1.1 CMOS LOGIC CIRCUITS	1
	1.2 FEATURES OF VLSI TECHNOLOGY	
	1.2.1 REDUCED CIRCUIT SIZE	3
	1.2.2 INCREASED COST EFFECTIVENESS	3
	1.2.3 HIGH SPEED	4
	1.2.4 LOW POWER CONSUMPTION	4
	1.2.5 IMPROVED PERFORMANCE	5
	1.3 ADVANTAGES OF VLSI USING CMOS	
	1.3.1 LOW POWER CONSUMPTION	5
	1.3.2 LOW POWER DISSIPATION	6
	1.3.3 MINIMAL HEAT PRODUCTION	7
	1.3.4 ULTRA-FAST SWITCHING OPERATIONS	8
	1.3.5 SIMPLE STRUCTURE	8

1.4	DISADVANTAGES OF VLSI DESIGN	
1.4.1	HIGH FABRICATION COST	8
1.4.2	INCREASE IN LEAKAGE CURRENT	9
1.4.3	POWER HANDLING	9
1.4.4	DESIGN COMPLEXITY	10
1.5	APPLICATIONS OF VLSI DESIGN	
1.5.1	COMPUTERS CPU'S	10
1.5.2	IMAGE SENSORS	11
1.5.3	MICRO-CONTROLLERS	12
1.5.4	CMOS BATTERIES	13
1.6	CMOS LOGIC CIRCUITS USING MEMRISTORS	
1.6.1	INTRODUCTION TO MERISTORS	14
1.6.2	ADVANTAGES OF COMBINING OF CMOS AND MERISTORS	14
1.6.3	CHALLENGES AND CONSIDERATIONS	15
1.6.4	APPLICATIONS	15
2	LITERATURE SURVEY	
2.1	GENERAL SURVEY	16
2.2	OVERVIEW OF EXISTING RESEARCH	20
3	AIM AND SCOPE OF THE EXISTING DESIGN	
3.1	AIM OF THE PROJECT	21
3.2	STRUCTURE OF CONVENTIONAL DECODER	22

3.3	IMPLEMENTATION OF CONVENTIONAL DECODER DESIGN	24
3.4	SIMULATION OF CONVENTIONAL DECODER	25
4	IMPLEMENTATION OF THE PROPOSED DESIGN	
4.1	MODEL OF THE MEMRISTOR	27
4.2	CONSTRUCTION OF THE MEMRISTOR	28
4.3	STRUCTURE OF MEMRISTOR DECODER	30
4.4	IMPLEMENTATION OF MEMRISTOR DECODER DEISGN	33
4.5	SIMULATION OF MEMRISTOR DECODER	35
4.6	STANDARDS	36
4.7	CONSTRAINTS	36
4.8	TRADE OFF	37
5	RESULTS AND DISCUSSION	
5.1	MEASURING THE PROPERTIES OF CONVENTIONAL DECODER	39
5.2	MEASURING THE PROPERTIES OF MEMRISTOR DECODER	41
5.3	TABULATION OF THE PROPERTIES OF BOTH DESIGNS	42
5.4	ANALYSIS OF BOTH DESIGNS	43
6	SUMMARY AND CONCLUSION	
6.1	SUMMARY	46
6.2	CONCLUSION	46
	REFERENCES	
	APPENDIX	

LIST OF ABBREVIATIONS

ABBREVIATION	DEFINITION
CMOS	Complementary Metal Oxide Semiconductor
PMOS	P-channel Metal Oxide Semiconductor
NMOS	N-channel Metal Oxide Semiconductor
VLSI	Very Large Scale Integrated Circuits
CCD	Charge Coupled Device
SSD	Solid State Drive
EDA	Electronic Design Automation
MCA	Memristor Crossbar Array
LTSPICE	Linear Technology Simulation Program with Integrated Circuit Emphasis
MRL	Memristor Ratioed Logic
CVD	Chemical Vapour Deposition
ALD	Atomic Layer Deposition
RRAM	Resistive Random Access Memory
PCB	Printed Circuit Board
NVRAM	Non-Volatile Random Access Memory
SCM	Storage Class Memory

LIST OF FIGURES

FIGURE No.	TITLE	PAGE No.
1.1	CMOS LOGIC CIRCUIT	2
1.2	COMPUTER CPU	11
1.3	IMAGE SENSOR	12
1.4	MICRO-CONTROLLER	13
1.5	CMOS BATTERIES	13
3.1	3-BIT DECODER	23
3.2	TRANSISTOR LEVEL CMOS DECODER DESIGN	25
3.3	SIMULATION OF CMOS DECODER	26
4.1	RELATION BETWEEN MEMRISTOR AND PASSIVE COMPONENTS	28
4.2	CONSTRUCTION OF MEMRISTOR	29
4.3	SYMBOL OF MEMRISTOR	30
4.4	HYSTERESIS LOOP OF MEMRISTOR	30
4.5	MEMRISTOR BASED DECODER DESIGN	32
4.6	TRANSISTOR LEVEL MEMRISTOR DECODER DESIGN	34
4.7	SIMULATION OF MEMRISTOR DECODER	35

5.1	GRAPH OF THE POWER OF CMOS DECODER	39
5.2	DELAY OF THE CMOS DECODER	40
5.3	GRAPH OF THE POWER OF MEMRISTOR DECODER	41
5.4	GRAPHICAL ANALYSIS OF POWER	44
5.5	GRAPHICAL ANALYSIS OF DELAY	44
5.6	GRAPHICAL ANALYSIS OF AREA	45

LIST OF TABLES

TABLE No.	TITLE	PAGE No.
3.1	TRUTH TABLE OF 3-BIT DECODER	24
5.1	PROPERTIES OF BOTH DESIGNS	43

CHAPTER 1

INTRODUCTION

Designing a low-power 3-bit decoder using memristors can be an interesting and challenging task. Memristors are non-volatile, two-terminal semiconductor devices that can be used in digital logic circuits. They offer advantages like low power consumption, non-volatility, and potential for high-density integration. Here's a general outline of how you can design a low-power 3-bit decoder using memristors. A memristor-based low-power 3-bit decoder utilizes memristors as programmable resistors to control the flow of current through various paths based on a 3-bit input. Memristors offer advantages like low power consumption and non-volatility. Design involves creating a truth table, voltage-controlled memristors, current limitation mechanisms, programming and configuration, power analysis, optimization, integration, and thorough testing. Specialized knowledge and tools may be required for memristor-based circuit design.

1.1 CMOS LOGIC CIRCUITS

CMOS (Complementary Metal-Oxide-Semiconductor) logic circuits are fundamental components of digital electronics, extensively employed in integrated circuits (ICs). These circuits utilize pairs of complementary transistor-NMOS (N-channel-Metal-Oxide-Semiconductor) and PMOS (P-channel Metal-Oxide-Semiconductor) to perform logical operations. A distinguishing feature of CMOS is its low-power nature, as it consumes minimal power when idle due to its complementary switching behaviour. In CMOS, NMOS transistors turn on for high input (logic 1), while PMOS transistors activate for low input (logic 0), ensuring one type is off when the other is on. This complementary operation, along with high noise immunity and excellent performance, makes CMOS logic circuits a cornerstone of modern digital electronics. internet-based home automation system for remote control and observing the status of home appliances is designed.

CMOS (Complementary Metal-Oxide-Semiconductor) logic circuits represent the backbone of digital electronics due to their exceptional performance

characteristics and efficiency. These circuits are constructed using pairs of complementary transistors-NMOS (N-channel Metal-Oxide-Semiconductor) and PMOS (P-channel Metal-Oxide-Semiconductor). CMOS logic gates, such as AND, OR, NAND, NOR, XOR, and XNOR gates, are fabricated by skill combining these transistors. What sets CMOS apart is its power-efficient operation, primarily achieved through its complementary switching mechanism. When the input signal is high (logic 1), NMOS transistors conduct, while PMOS transistors are off, pulling the output low. Conversely, when the input is low (logic 0), PMOS transistors conduct, pulling the output high while NMOS transistors remain off. This complementary behaviour ensures minimal static power consumption when there is no switching activity. It's this feature, along with high noise immunity and widespread use in ICs, that makes CMOS a cornerstone of modern digital system.

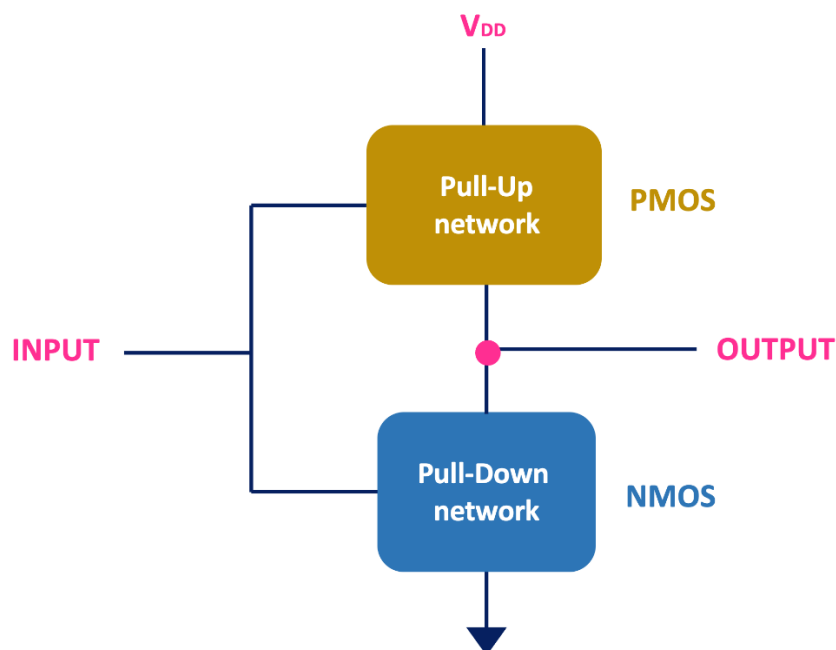


Fig: 1.1: CMOS Logic Circuit

CMOS logic circuits have become the go-to-choice in the design of integrated circuits for a multitude of reasons. Their versatility extends beyond basic logic gates to include flip-flops, multiplexers, and even microprocessors. The low power consumption of CMOS logic circuits is a standout feature, making them ideal for battery-powered devices and reducing heat generation in high-performance computing systems. Additionally, CMOS technology has allowed for the integration

of millions to billions of transistors on a single chip, paving the way for advancements in computing, communication, and consumer electronics.

1.2 FEATURES OF VLSI

- A. Reduced Circuit Size
- B. Increased Cost Effectiveness
- C. Improved Performance
- D. High Speed
- E. Low Power Consumption

1.2.1 Reduced Circuit Size

Reducing circuit size is a paramount goal in modern electronics, and CMOS (Complementary Metal-Oxide-Semiconductor) technology is a driving force behind achieving this objective. CMOS's success in shrinking electronic circuits stems from its ability to scale down transistors, enabling the integration of more components within a smaller physical footprint. This downscaling combined with advancements in manufacturing techniques, results in highly compact and densely populated semiconductor chips. Moreover, CMOS's efficiency in terms of power consumption not only extends the battery life of portable devices but also reduces the need for bulky cooling systems and power-related components, further contributing to the miniaturization of electronic systems.

1.2.2 Increased Cost Effectiveness

One of the cornerstones of CMOS (Complementary Metal-Oxide-Semiconductor) technology is its remarkable cost-effectiveness. This stems from several inherent advantages that have revolutionized the electronics industry. Mass production benefits from standardized fabrication processes and large-scale manufacturing facilities, significantly reducing the cost per unit. Additionally, CMOS's ability to integrate more functions onto a single chip streamlines production, decreasing the bill of materials and assembly costs. Furthermore, the low power consumption of CMOS circuits not only extends battery life but also results in lower operational energy costs, adding to the long-term cost-effectiveness of electronic devices. The longevity and reliability associated with CMOS-based systems

contribute to reduced maintenance and replacement expenses. These factors collectively make CMOS technology a driving force behind the development of cost-effective, high-performance electronics that are accessible to a wide range of applications and consumers.

1.2.3 Improved Performance

Improved performance is at the core of CMOS (Complementary Metal-Oxide-Semiconductor) technology's enduring appeal. This is driven by a multitude of factors, including transistor scaling that enables smaller and more densely packed transistors on semiconductor wafers. These smaller transistors facilitate faster switching speeds, higher processing power, and increased integration density. CMOS logic gates, known for their high-speed operation and low power consumption, are fundamental to the performance boost seen in microprocessors, memory chips, and various communication devices. CMOS's impressive noise immunity ensures signal integrity even in noisy environments. Furthermore, advancements in semiconductor manufacturing processes, coupled with reduced heat generation, lead to efficient and high-performance electronic systems. Customization options also allow CMOS-based devices to cater to specialized applications, making them a driving force behind improved performance across a wide spectrum of electronic products and technologies.

1.2.4 High Speed

High speed is an inherent advantage of CMOS technology that underpins its widespread use in today's electronics landscape. CMOS logic circuits exhibit rapid switching times, making them ideal for high-performance computing, data processing, and communication systems. This swiftness in operation allows microprocessors to execute complex instructions quickly, memory devices to read and write data with minimal delay, and communication chips to transmit information at blazing speeds. CMOS's high-speed characteristics are crucial for modern digital devices, from smartphones and tablets to networking equipment and supercomputers, ensuring that these technologies can keep up with the ever-increasing demands of our data-driven world. The pursuit of even higher speeds

continues to drive innovation in CMOS technology, promising even more remarkable advancements in the near future.

1.2.5 Low Power Consumption

Low power consumption stands as one of the defining strengths of CMOS technology, rendering it indispensable in the modern electronics landscape. CMOS logic circuits are renowned for their ability to perform tasks efficiently while consuming minimal electrical energy. This quality is particularly crucial in battery-operated devices, where extending battery life is paramount. Whether it's the processor in your smartphone, the microcontroller in a wearable device, or the circuitry in energy-efficient appliances, CMOS technology excels at striking the delicate balance between high-performance computing and energy conservation. Additionally, CMOS's low power characteristics help reduce heat generation, enhancing the reliability and longevity of electronic components. As our world increasingly relies on portable and energy-efficient technology, the enduring importance of CMOS technology's low power consumption cannot be overstated.

1.3 ADVANTAGES OF VLSI USING CMOS

- A. Low Power Consumption
- B. Low Power Dissipation
- C. Minimal Heat Production
- D. Ultra-Fast Switching Operations
- E. Simple Structure

1.3.1 Low Power Consumption

Low power consumption is a cornerstone of CMOS (Complementary Metal-Oxide-Semiconductor) technology, playing a pivotal role in shaping the landscape of modern electronics. CMOS circuits have revolutionized the design of portable and battery-powered devices, offering a delicate balance between performance and energy efficiency. This attribute is especially vital in today's world, where sustainability and extended battery life are paramount concerns. CMOS technology allows electronic devices, from smartphones and tablets to IoT sensors and medical implants, to operate for extended periods on a single charge, reducing the need for

frequent recharging or replacement of batteries. Moreover, the lower power dissipation in CMOS circuits leads to reduced heat generation, mitigating thermal issues and enhancing the overall reliability and durability of electronic components. In sectors like data centres and telecommunications, where power efficiency is crucial, CMOS's ability to provide high computational power while conserving energy is a game-changer. As we continue to seek eco-friendly and long-lasting electronic solutions, the enduring importance of CMOS technology's low power consumption is poised to drive innovation across a wide spectrum of applications.

1.3.2 Low Power Dissipation

Low power dissipation is a cornerstone of CMOS technology, offering a solution to the ever-increasing demand for energy-efficient electronics. CMOS circuits are engineered to minimize the amount of power converted into heat during operation. This characteristic not only contributes to extended battery life in portable devices but also reduces the need for elaborate cooling systems in high-performance computing environments. By efficiently utilizing electrical power and keeping heat generation in check, CMOS technology ensures the longevity and reliability of electronic components. This is particularly crucial in densely packed integrated circuits, where excess heat can lead to thermal issues and affect overall performance. Low power dissipation not only benefits consumer electronics but also holds great promise in applications like green computing, where minimizing energy consumption is paramount. As we continue to strive for energy-efficient solutions, CMOS's ability to limit power dissipation stands as a fundamental pillar in the development of sustainable and high-performance electronic systems.

1.3.3 Minimal Heat Production

One of the standout advantages of CMOS technology is its ability to maintain minimal heat production during operation. CMOS circuits are designed to efficiently utilize electrical power, ensuring that only a small fraction is converted into heat. This attribute holds profound implications for the performance and longevity of electronic devices. In an era where compactness and high integration density are prized, CMOS's heat-efficient operation reduces the risk of thermal issues, such as overheating and component degradation. This, in turn, extends the lifespan of

electronic components and enhances overall system reliability. Beyond reliability, the reduced heat generation is instrumental in the development of energy-efficient devices, as it diminishes the need for energy-intensive cooling mechanisms. As a result, CMOS technology has become a linchpin in the design of modern electronics, facilitating sleek and compact devices while ensuring they remain cool, reliable, and power-efficient.

1.3.4 Ultra-Fast Switching Operations

The ability to achieve ultra-fast switching operations lies at the heart of CMOS technology's success story. CMOS logic gates are engineered to toggle states with astonishing speed, making them indispensable in high-performance computing and communication systems. These ultra-fast switching times ensure rapid data processing, seamless multitasking, and low latency in devices like microprocessors, memory modules, and high-speed data links. CMOS technology's agility in switching between logic states enables it to keep pace with the ever-increasing demands of modern technology. Whether it's enabling real-time gaming experiences, facilitating instantaneous data retrieval, or powering lightning-fast communication networks, CMOS's ultra-fast switching capabilities are at the forefront of innovation, transforming the way we interact with and harness the power of electronic devices.

1.3.5 Simple Structure

The complementary operation of these transistors allows for the creation of complex logic gates and functions with minimal components. This simplicity not only streamlines the manufacturing process but also enhances reliability by reducing the likelihood of defects. The straightforward structure of CMOS circuits also leads to lower power consumption, as there are fewer paths for electrical current to follow when a transistor is in the off state. Moreover, this simplicity has paved the way for high levels of integration, enabling the development of powerful microprocessors and memory chips. In essence, CMOS technology's simple yet ingenious structure has revolutionized the electronics industry, serving as the foundation for countless electronic devices that have become integral parts of our daily lives.

1.4 DISADVANTAGES OF VLSI USING CMOS

- A. High Fabrication Cost
- B. Increase In Leakage Current
- C. Power Handling
- D. Design Complexity

1.4.1 High Fabrication Cost

High fabrication cost is a notable concern in the world of semiconductor manufacturing, especially as technology advances and feature sizes shrink. While CMOS technology offers numerous advantages such as low power consumption and high performance, the process of developing and maintaining state-of-the-art fabrication facilities can be financially daunting. The intricate and precise techniques required for semiconductor fabrication demand substantial capital investments in cleanrooms, equipment, and skilled personnel. Additionally, as feature sizes approach the nanometer scale, the complexity of fabrication processes increases, driving up costs further. However, it's essential to note that economies of scale and market demand play a role in mitigating some of these costs over time. The pursuit of advanced CMOS technology continues to require substantial investments but is justified by the continuous innovation and groundbreaking electronic devices it enables.

1.4.2 Increase in Leakage Current

The rise in leakage current is a pressing challenge in the ongoing development of CMOS technology. As transistors become smaller and more densely packed on semiconductor wafers, they are more susceptible to leakage, which occurs when some current flows even when the transistor should be in the off state. This leakage is primarily attributed to quantum tunnelling and subthreshold conduction effects. The consequence of increased leakage is twofold: it contributes to higher power consumption, which is undesirable in energy-efficient devices, and it can lead to heat generation, reducing the reliability and lifespan of electronic components. Managing leakage current has become a paramount concern in semiconductor design, requiring innovative solutions such as the use of high-k dielectrics and strained silicon to mitigate leakage effects and maintain the efficiency and longevity of CMOS-based devices.

1.4.3 Power Handling

Effective power handling is a pivotal factor in the functionality and reliability of electronic devices. In CMOS technology, which is renowned for its efficiency and low power consumption, managing power handling efficiently is essential to maximize battery life and prevent overheating. Devices and circuits must be designed to withstand the power levels they are subjected to, ensuring they operate within safe thermal limits. Overloading electronic components with excessive power can lead to electrical failures, decreased performance, and even permanent damage. Additionally, power handling becomes increasingly critical in high-power applications, such as power amplifiers or high-performance computing, where managing heat dissipation and maintaining system stability are paramount. Engineers and designers continuously strive to strike a delicate balance between power efficiency and the capability to handle power demands effectively, enabling the development of robust, high-performance electronic systems across a wide range of applications.

1.4.4 Design Complexity

Design complexity is a central consideration in CMOS technology, particularly as electronic systems become increasingly sophisticated. While CMOS offers numerous advantages such as high integration density and energy efficiency, it also presents challenges related to the complexity of designing intricate circuits. As transistors shrink and more functionality is packed into smaller chips, the intricacies of routing signals, managing power distribution, and ensuring signal integrity become more demanding. Moreover, advanced CMOS designs often involve custom layouts, complex timing constraints, and intricate verification processes, all of which contribute to design complexity. To address this challenge, engineers rely on cutting-edge design tools, simulation software, and systematic methodologies to streamline the design process. The pursuit of improved performance, lower power consumption, and higher levels of integration requires designers to continually navigate the intricacies of design complexity, finding innovative solutions to meet the evolving demands of the electronics industry.

1.5 APPLICATION OF VLSI USING CMOS

A. Computer CPU'S

- B. Image Sensors
- C. Micro-Controllers
- D. CMOS Batteries

1.5.1 Computer CPU'S

Computer CPUs are a prime example of the application of VLSI using CMOS technology. The integration of billions of CMOS transistors onto a single chip allows CPUs to perform complex calculations and execute instructions at lightning-fast speeds while consuming minimal power. CMOS's low power characteristics and high-performance switching capabilities are



Fig: 1.2: Processor

instrumental in the development of energy-efficient and high-performance CPUs. VLSI techniques enable designers to densely pack transistors and logic gates on the CPU chip, optimizing space and facilitating the execution of intricate tasks. The relentless advancement of VLSI and CMOS technology continues to drive innovation in CPU design, resulting in processors that power everything from personal computers and servers to mobile devices and embedded systems, fuelling the rapid evolution of computing capabilities.

1.5.2 Image Sensors

VLSI CMOS technology has revolutionized the field of image sensing, enabling the creation of high-performance image sensors used in a wide range of applications. CMOS image sensors, unlike their CCD (Charge-Coupled Device)

counterparts, integrate image capture and signal processing functions onto a single chip. This integration provides several advantages, including lower power consumption, compact size, and cost-effectiveness. CMOS image sensors are employed in digital cameras, smartphones, webcams, and automotive cameras, capturing and processing images with remarkable speed and efficiency. Their versatility extends to applications such as medical imaging, surveillance, and machine vision. With ongoing advancements in VLSI CMOS technology, we can anticipate even more sophisticated image sensors, capable of capturing high-resolution images and enabling innovative features like facial recognition and augmented reality experiences.

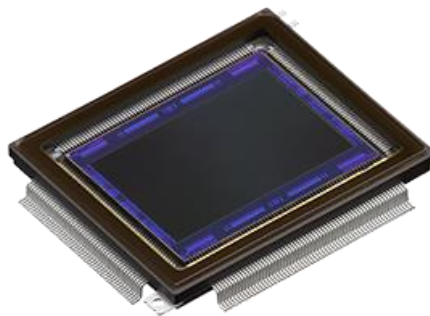


Fig: 1.3: Image sensor

1.5.3 Micro-Controllers

The application of Very Large scale Integration (VLSI) technology using CMOS microcontrollers has revolutionized numerous industries and electronic systems. CMOS microcontrollers, characterized by their low power consumption and high integration density, find extensive use in a diverse array of applications. In embedded systems, they serve as the computational core for controlling automotive systems, industrial automation, and consumer electronics. In the Internet of Things (IoT), CMOS microcontrollers enable energy-efficient data processing in sensor nodes, facilitating the seamless connection of devices. Their small form factor and low power profile make them ideal for wearable technology, such as smartwatches and fitness trackers, which demand extended battery life and compact designs. Moreover, CMOS microcontrollers are the backbone of critical applications like

medical devices, where reliability and power efficiency are paramount. Whether it's enhancing the functionality of smartphones, optimizing vehicle performance, or ensuring the safety of aerospace systems, the versatile application of VLSI using CMOS microcontrollers continues to drive innovation across a wide spectrum of industries.

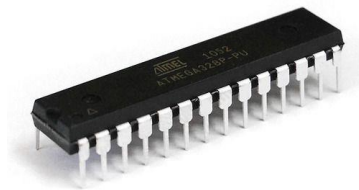


Fig: 1.4: Micro-Controller

1.5.4 CMOS Batteries

CMOS batteries find essential application in VLSI systems by preserving critical system data and real-time clock functionality when the primary power source is unavailable. These small coin-cell batteries are crucial for maintaining system settings, including BIOS configurations and timekeeping, ensuring a seamless user experience during power interruptions or when devices are powered off. Whether in portable devices like laptops and tablets, embedded systems for industrial control or IoT applications, or other VLSI-based electronics, CMOS batteries safeguard the integrity of vital information. However, it's essential to consider their finite lifespan and proper disposal to uphold both system reliability and environmental responsibility. CMOS batteries are an unsung hero in VLSI systems, quietly ensuring that devices continue to function correctly and reliably even in less-than-ideal power conditions.

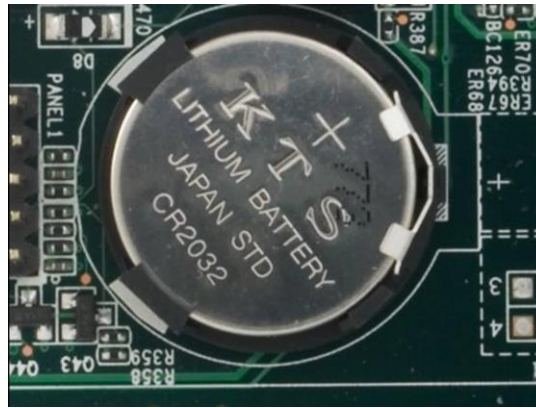


Fig: 1.5: CMOS Battery

1.6 CMOS LOGIC CIRCUITS USING MEMRISTORS

CMOS (Complementary Metal-Oxide-Semiconductor) logic circuits are widely used in digital electronics due to their low power consumption, high noise immunity, and compatibility with modern semiconductor manufacturing processes. Memristors, on the other hand, are a relatively new type of electronic component with unique properties that have the potential to revolutionize digital and analog circuit design. Combining CMOS logic circuits with memristors can offer several advantages, including non-volatile memory, neuromorphic computing capabilities, and improved energy efficiency. Below, I'll provide a detailed explanation of CMOS logic circuits using memristors.

1.6.1 Introduction to Memristors

Memristors are two-terminal non-volatile memory devices that exhibit a unique relationship between the charge passing through them and the resistance they offer. They have the ability to "remember" their resistance state even after power is removed, which is in contrast to traditional resistors that always maintain a constant resistance. Memristors can be used for memory storage, analog computing, and neuromorphic computing due to their ability to emulate synaptic behaviour in biological systems.

1.6.2 Advantages of Combining of CMOS and Memristors

Memristors can be used to create non-volatile memory cells, which means that data can be retained even when the power is turned off. This is useful for applications like solid-state drives (SSDs) and non-volatile memory (NVM) in

embedded systems. Memristors have been explored for neuromorphic computing, where they can emulate the behaviour of biological synapses. This makes them suitable for artificial intelligence and machine learning applications. Memristors consume very little power, making them energy-efficient components. When integrated with CMOS logic, they can help reduce overall power consumption in digital circuits.

1.6.3 Challenges and considerations

Integrating memristors with CMOS technology can be challenging, as it requires developing compatible fabrication processes and overcoming material compatibility issues. Memristors need to be reliable and durable over time, which is a significant concern for commercial applications. Designing circuits that can effectively program and read memristor-based non-volatile memory cells can be complex.

1.6.4 Applications

The combination of CMOS and memristors has applications in memory storage, neuromorphic computing, analog signal processing, and more. Researchers are exploring memristor-based crossbar arrays for in-memory computing, which can accelerate certain types of computations by reducing the need to transfer data between memory and processors. Combining CMOS logic circuits with memristors holds great promise for a variety of applications due to the advantages of non-volatile memory, neuromorphic computing capabilities, and improved energy efficiency. While there are challenges to overcome in terms of integration and reliability, ongoing research and development are pushing the boundaries of what is possible with this emerging technology.

CHAPTER 2

LITERATURE SURVEY

2.1 GENERAL

The following shows a literature survey done for low power 3-bit decoder using memristor for how to design the CMOS logic circuits and how to measure the power consumption, area occupied and delay of the logic circuits. The other surveys are conducted about the memristor characteristics and how to design memristor in various software EDA tools.

2.1.1 Suri Shanmukh, Sompalli RohitKumar, Paluru Hemaprasad and R. Sakthivel “Low Power 3-Bit Encoder Design using Memristor”, IEEE June 24-26, 2022.

This paper presents Designing a low-power 3-bit encoder using memristors involves creating a digital circuit that can efficiently encode a 3-bit binary input into a binary output while taking advantage of the unique properties of memristors to reduce power consumption. Below is a detailed explanation of the steps and considerations involved in this design. A 3-bit encoder is a combinational logic circuit that takes a 3-bit binary input and produces a binary output representing the highest-order bit that is set to 1 (i.e., the most significant bit). For example, if the input is "010," the output would be "10" because the most significant bit set to 1 is the second bit from the left.

Memristors are two-terminal non-volatile memory devices with the ability to store and process data. They can be used to create energy-efficient digital circuits. To achieve low-power operation, the design should focus on minimizing power dissipation in the circuit. This can be achieved by utilizing CMOS logic gates in conjunction with memristors to combine the advantages of low-power CMOS and non-volatile memristor memory. Implementing efficient encoding logic to reduce the number of active components and minimize switching activity. Minimizing leakage current in memristor-based memory cells when they are not actively used. Employing techniques like clock gating to disable parts of the circuit when they are not needed.

Determine the truth table for the 3-bit encoder to define the desired output for all possible input combinations. Design the encoding logic using CMOS gates (e.g., AND, OR, NOT gates) and memristor-based memory cells. Use memristors to store intermediate results or encode information, taking advantage of their non-volatile nature. Implement control logic to manage the read and write operations to the memristor-based memory cells efficiently. Optimize the design for low power by reducing unnecessary transitions and ensuring that memristor-based memory cells are only written to when necessary. Simulate the circuit design using specialized software tools for memristor-based circuits. Test the circuit's functionality and power consumption using various input patterns to ensure it behaves as expected.

2.1.2 Li Qu¹, Xiaole Cui¹, Xiaoyan Xu, Xiaoxin Cui, Ye Ma¹, “The Multi-input MRL Logic Gate and Its Application”, IEEE, 2021.

This paper focuses Multi-Input Memristor-Based Logic (MRL) gates are a type of digital logic gate that use memristors as their key components to perform logical operations with multiple inputs. These gates have gained attention due to their potential applications in emerging computing paradigms, such as neuromorphic computing, non-von Neumann architectures, and energy-efficient digital systems. Below, I'll provide detailed information about multi-input MRL gates and their applications.

Memristors are two-terminal passive electronic components that exhibit a non-linear relationship between the charge and the flux (voltage-integral of current) passing through them. They can change their resistance state based on the voltage applied and the direction of current flow. Multi-input MRL gates accept more than two inputs and produce an output based on the logical combination of these inputs. An MRL NAND gate produces a logic low output when all its inputs are at logic high, similar to a conventional NAND gate. It utilizes memristors to achieve this functionality. An MRL NOR gate produces a logic high output when all its inputs are at logic low, similar to a conventional NOR gate. Multi-input MRL gates are particularly well-suited for neuromorphic computing, where they can emulate the behaviour of biological neurons. The memristor-based gates can be used to model the complex synaptic connections in neural networks.

Memristor-based logic gates offer potential energy savings compared to traditional CMOS gates, especially in applications where power consumption is a critical concern, such as battery-operated devices and IoT sensors. MRL gates have been explored for non-von Neumann computing architectures, which depart from the traditional von Neumann architecture to improve processing speed and energy efficiency. They are also exploring novel computing paradigms and architectures that can leverage the unique characteristics of memristors to solve complex problems more efficiently and with lower power consumption.

2.1.3 Gongzhi Liu, Shuhang Shen, Peipei Jin, Guangyi Wang¹, Yan Liang, IEEE “Design of Memristor-Based Combinational Logic Circuits”, IEEE Circuits, Systems, and Signal Processing, 2021.

This paper proposes an optimization Designing memristor-based combinational logic circuits involves creating digital logic circuits that utilize memristors as fundamental building blocks to perform logical operations. Memristors are two-terminal non-volatile memory devices that can store and process data efficiently, making them promising components for energy-efficient and high-performance digital circuits. Here's a detailed explanation of the design process for memristor-based combinational logic circuits, combinational logic circuits perform logic operations on their inputs to produce outputs based solely on the current input values, without any memory of previous inputs. Common building blocks in combinational logic include AND gates, OR gates, NOT gates, XOR gates, etc. Memristors are two-terminal electronic devices with a unique property that relates the charge passing through them to their resistance. They can be in one of several resistance states, making them suitable for non-volatile memory and logic operations. When designing memristor-based combinational logic circuits, consider the following factors, determine the desired logic functionality of your circuit, which will dictate the arrangement and connections of memristors and other components.

Understand the memristor's behaviour, including resistance switching characteristics, write/read voltages, endurance, and retention, optimize the design for low power consumption, taking advantage of memristors' non-volatile nature to reduce dynamic power, determine how memristors will be integrated into the circuit, considering compatibility with other components like CMOS devices. Ensure that

voltage levels and signal compatibility are maintained throughout the circuit to avoid signal degradation. Start by designing basic logic gates (AND, OR, NOT, etc.) using memristors. The logical operation of these gates can be achieved by controlling the resistance states of memristors in a specific arrangement. Memristor-based logic gates can have different configurations, such as memristor-crossbar arrays, where rows and columns of memristors form a matrix that can be programmed to perform various logic operations. Ensure that the logic gates meet the logical requirements of your combinational logic circuit.

2.1.4 Sachin Maheshwari , Spyros Stathopoulos , Jiaqi Wang, Alexander Serb , Yihan Pan, Andrea Mifsud , Lieuwe B. Leene, Jiawei Shen, Christos Papavassiliou , Timothy G. Constandinou and Themistoklis Prodromakis, “Design Flow for Hybrid CMOS/Memristor Systems Part II: Circuit Schematics and Layout”, 2021.

This paper proposes the capability of in-memory computation, reconfigurability, low power operation as well as multistate operation of the memristive device deems them a suitable candidate for designing electronic circuits with a broad range of applications. Besides, the integrability of memristor with CMOS enables it to use in logic circuits too. In this work, we demonstrate with examples the design flow for memristor-based electronics, after the custom memristor model already being integrated and validated into our chosen Computer-Aided Design (CAD) tool to performing layout-versus-schematic and post-layout checks including the memristive device. We envisage that this step-by-step guide to introducing memristor into the standard integrated circuit design flow will be a useful reference document for both device developers who wish to benchmark their technologies and circuit designers who wish to experiment with memristive enhanced systems.

2.1.5 Megha Nawaria, Sanjay Kumar, Mohit Kumar Gautam , Narendra Singh Dhakad , Rohit Singh, Sonal Singhal, Pawan Kumar, Santosh Kumar Vishvakarma and Shaibal Mukherjee “Memristor-Inspired Digital Logic Circuits and Comparison With 90-/180-nm CMOS Technologies”, IEEE TRANSACTIONS ON ELECTRON DEVICES, 2023.

The paper presents Compact low-power devices with ultrafast processing speed are the fundamental building blocks for the development of the state-of-the-art logic systems and memristor prominently fulfill these demands and plays a major role in digital circuit design. In this work, design, implementation, and performance evaluation of memristor-based logic gates, such as NOT, AND, NAND, OR, NOR, XOR, and XNOR, and combinational logic circuits, such as adder, subtractor, and 2×1 mux, are presented via SPECTRE in Cadence Virtuoso. Herein, we propose an optimized design of memristor-based logic gates and combinational logic circuits and draw a comparative analysis with the conventional 180-nm complementary metal–oxide– semiconductor (CMOS) technology. The utilized memristor model is thoroughly validated with the experimental results of a high-density Y2O3-based memristive crossbar array (MCA), which shows a significantly low values of coefficient of variabilities in device-to-device (D2D) and cycle-to-cycle (C2C) operation.

2.2 OVERVIEW OF EXISTING RESEARCH

CMOS (Complementary Metal-Oxide-Semiconductor) logic circuits are fundamental to digital electronics due to their low power consumption and noise immunity. Memristors two-terminal non-volatile memory devices, have unique properties such as resistance switching that make them attractive for digital circuitry. Combining CMOS and memristors can lead to advantages like non-volatile memory, neuromorphic computing, and energy efficiency. A 3-bit encoder is a digital circuit that converts a 3-bit binary input into a binary output based on the most significant bit set to 1. Designing a low-power 3-bit encoder using memristors involves optimizing power consumption while achieving the desired encoding functionality. Such a design can be valuable for energy-efficient devices and applications.

Multi-input memristor-based logic gates are digital circuits that utilize memristors to perform logical operations with multiple inputs. These gates can be employed in neuromorphic computing, energy-efficient digital systems, and non-von Neumann architectures. Challenges include memristor reliability and integration with existing technologies. Memristor-based combinational logic circuits integrate memristors with traditional CMOS components to perform logical operations. The

design process involves defining requirements, selecting components, creating schematics and layouts, simulation, optimization, and fabrication. These circuits offer energy efficiency and can find applications in various fields, including neuromorphic computing. Designing hybrid CMOS/memristor circuits involves integrating CMOS and memristor components into a single circuit to harness the advantages of both technologies. The design flow includes defining requirements, selecting components, creating schematics, layout planning, simulation, verification, fabrication, testing, and optimization. These circuits have potential applications in advanced computing paradigms and energy-efficient systems.

CHAPTER 3

AIM AND IMPLEMENTATION OF EXISTING SYSTEM

3.1 AIM OF THE PROJECT

The aim of this project is to design a low-power 3-bit decoder using memristor technology, focusing on achieving high energy efficiency and reduced power consumption compared to traditional CMOS-based decoders. The project seeks to leverage the unique properties of memristors, such as non-volatility, low energy operation, and reconfigurability, to develop a decoder circuit suitable for low-power digital systems and IoT (Internet of Things) applications. The electrical properties of memristor devices, including resistance states, switching behaviour, and transient responses. Experimentally determine key parameters such as R_{on} (resistance in the "on" state), R_{off} (resistance in the "off" state), and $R_{initial}$ (initial resistance). To develop a detailed circuit design for the 3-bit decoder, integrating memristors as key components. Utilize simulation tools such as LTspice to model and simulate the decoder circuit, considering factors such as signal integrity, power dissipation, and transient behaviour.

To minimize power consumption in the decoder circuit while maintaining reliable operation. Explore strategies such as voltage scaling, current limiting, and sleep modes to achieve high energy efficiency without compromising performance. Evaluate the performance of the memristor-based decoder in terms of decoding accuracy, speed, and power efficiency. Conduct comprehensive simulations to analyse the decoder's response to different input patterns and operating conditions, comparing it with CMOS-based decoder designs. Assess the reliability and robustness of the memristor-based decoder under various environmental conditions, including temperature variations and process variations. Investigate techniques to mitigate issues such as endurance degradation and variability in memristor devices. Explore potential applications and extensions of the memristor-based decoder technology, such as in-memory computing, neural network acceleration, and energy-efficient IoT devices. Identify areas for further research and development to advance the state-of-the-art in low-power digital systems leveraging memristor technology.

3.2 STRUCTURE OF CONVENTIONAL DECODER DESIGN

In digital electronics, a binary decoder is a combinational circuit that takes a binary input and activates one of several outputs, based on the binary code provided. Binary decoders are used to select specific lines or components in a larger system. The most common types are 2-to-4, 3-to-8, and 4-to-16 line decoders. These are used in applications like address decoding in memory systems and controlling multiple devices using a single control signal. In multimedia technology, decoders are used to interpret and process encoded video and audio data. For example, in video streaming, a video decoder reverses the compression or encoding process to display the video content on a screen. Common video codecs include H.264, H.265 (HEVC), and VP9. Similarly, audio decoders reverse the encoding of audio signals, allowing playback of compressed audio formats like MP3 or AAC.

In data compression, an encoder compresses data to reduce its size, and a decoder reverses this process to recover the original data. This is commonly used in file compression formats like ZIP and in network protocols like HTTP (for web pages). Compression decoders are responsible for expanding compressed data into its original form. In communication systems, a decoder is often used to interpret encoded messages or signals. For example, in error-correcting codes like Reed-Solomon or convolutional codes, a decoder is used to correct errors that may occur during transmission. In this context, decoders play a crucial role in ensuring the integrity of transmitted data. In the context of artificial intelligence and neural networks, a decoder is a part of a sequence-to-sequence model, often used in natural language processing and machine translation.

The decoder accepts binary input lines, which are also called address lines. These input lines determine which output line will be active based on the binary code applied. For example, a 3-to-8 decoder will have 3 input lines (A, B, C). The decoder has multiple output lines (8 in the case of a 3-to-8 decoder). Each output line corresponds to a unique combination of input values. When a specific binary pattern is applied to the input lines, one of the output lines becomes active (goes to a logical high state), while the rest remain inactive (logical low state). The core component of a decoder is its internal logic circuit. This logic circuit processes the

input binary values and determines which output line should be active. The specific logic implemented depends on the type of decoder (e.g., 2-to-4, 3-to-8) and its purpose.

Enable Inputs (optional): Some decoders include enable inputs (often labelled as "E" or "EN"). These enable inputs can be used to control whether the decoder is active or not. When the enable input is inactive (low), all output lines are forced to a low state, regardless of the input values. The decoder's behaviour can be represented by a truth table that defines the relationship between the input binary values and the corresponding active output line(s). Each row in the truth table corresponds to a specific input pattern, indicating which output line(s) are active for that input.

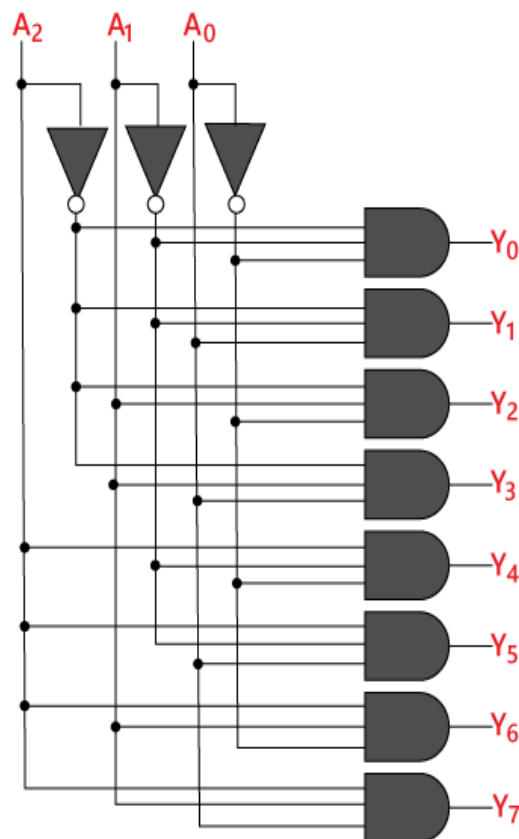


Fig: 3.1: 3-Bit Decoder

Table: 3.1: Truth Table of 3-Bit Decoder

Inputs			Outputs							
X	Y	Z	D ₀	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆	D ₇
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

3.3 IMPLEMENTATION OF CONVENTIONAL DECODER

The conventional 3-bit Decoder is designed using the LTspice software tool, using the CMOS Logic and it is implemented in the software. In the Decoder design the input voltage VDD is given as DC Voltage 5V. The three inputs are referred as the in1, in2, in3 which are given as 5 DC Voltage. The logic behind the decoder is $Y_0 = X_1.X_2.X_3$, it is converted as $X_1 \cdot (X_2 + X_3)$ again it is converted as $X_1 + X_2 + X_3$. Like that remaining outputs are also calculated using simple maths and De-Morgans law. So in this every output is calculated using the help of 3 input NOR Gate, for that we need six transistors (3 p-mos and 3 n-mos) in one NOR gate. Therefor for 8 outputs we need 8×6 48 transistors and 3 CMOS inverters are required to transform the input to negative input. So total 54 transistors are required to design the conventional decoder using cmos logic. The specific structure of a decoder can vary depending on its application and the complexity of the task it needs to perform. The logic circuit determines which output line is active based on the values of A and B. For example, O0 is active when A=0 and B=0, O1 is active when A=0 and B=1, and so on.

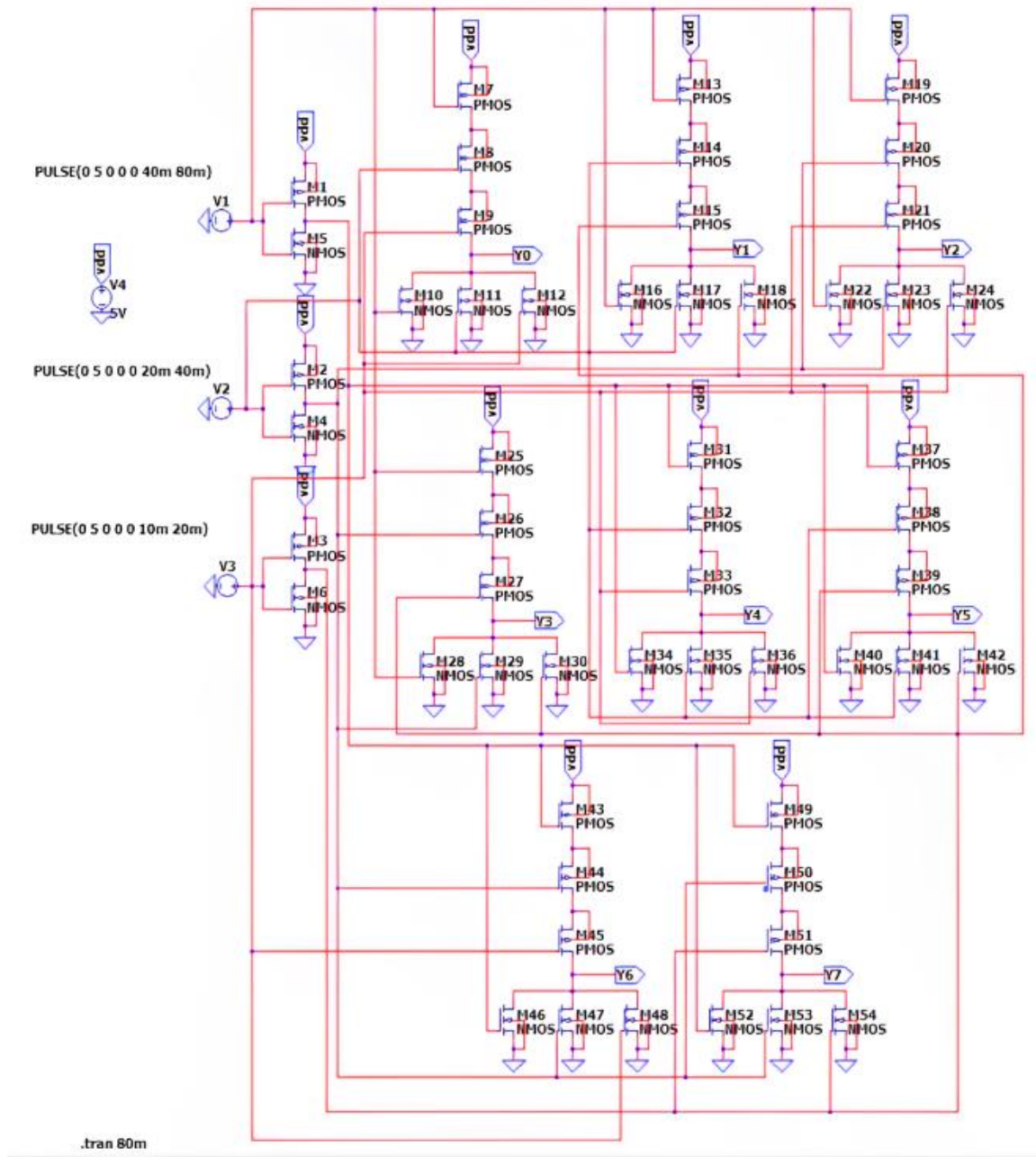


Fig: 3.2: Transistor Level CMOS Decoder design

3.4 SIMULATION OF CONVENTIONAL DECODER

In addition to designing and simulating the memristor-based 3-bit decoder, it's crucial to include simulations of conventional decoders using CMOS technology for comparative analysis. This allows for a comprehensive evaluation of the performance, power consumption, and other key metrics between memristor-based and conventional decoder designs.

Ensure that the circuit design is functionally equivalent to the memristor-based decoder, capable of decoding 3-bit input signals into corresponding output signals. Set up the simulation environment using circuit simulation software such as LTspice. Define the input signals for the conventional decoder, representing all possible combinations of 3-bit input patterns. Specify simulation parameters such as operating voltage, temperature, and timing constraints. Conduct transient analysis simulations to analyse the time-dependent behaviour of the conventional decoder. Capture voltage and current waveforms at key nodes in the circuit to understand signal propagation delays, rise/fall times, and transient effects. Perform power consumption analysis to evaluate the energy efficiency of the conventional decoder. Compare the performance metrics of the memristor-based and conventional decoders, including decoding accuracy, speed, and reliability.

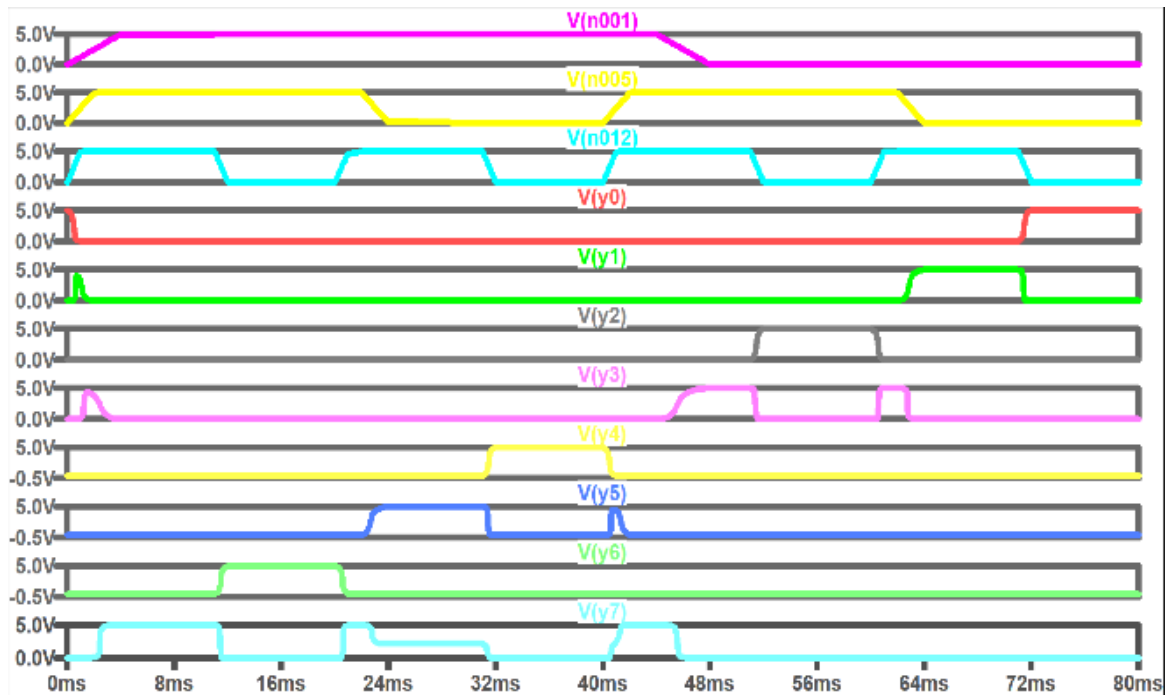


Fig: 3.3: Simulation of CMOS decoder

CHAPTER 4

IMPLEMENTATION OF THE PROPOSED DESIGN

4.1 MODEL OF THE MEMRISTOR

Memristors are fascinating electronic components that exhibit memory-dependent resistance behaviour. Several models have been proposed to describe the behaviour of memristors. Here are some of the prominent ones. Linear Ion-Drift Model is the one of the earliest and simplest models proposed for memristors. It describes memristance changes as a result of ion drift in a solid-state device. Chua's Memristor Model is Proposed by Leon Chua in 1971, this model is based on the relationship between charge and flux-linkage. It describes a memristor as a two-terminal passive circuit element relating the flux $\Phi(t)$ to the charge $q(t)$ through a relationship $m = d\Phi/dq$. Strukov Model incorporates non-linear ion drift effects and is more sophisticated compared to Chua's model. It accounts for non-linear conductance changes in the memristor device, this is a comprehensive memristor model that considers various physical phenomena such as the diffusion of mobile ions, space charge effects, and non-linear ion drift. It provides a detailed description of memristor behaviour under different operating conditions. Yakopcic model focuses on the physics of memristive behaviour and incorporates elements such as internal state variables to describe the dynamics of the device accurately. Biolek Model takes into account the non-linear dopant drift in memristor devices and provides a mathematical framework for understanding their behaviour.

Leon Chua memristor model is appropriate model for designing the CMOS logic circuits using the memristor ratioed logic (MRL). Leon Chua's memristor model, proposed in 1971, is foundational to understanding memristors. Chua postulated the existence of a fourth fundamental circuit element alongside the resistor, capacitor, and inductor. In his model, he established a relationship between charge (q) and magnetic flux (Φ) in a two-terminal device, defining memristance (m) as the rate of change of flux with respect to charge, i.e., $m = d\Phi/dq$. This model implies that the resistance of a memristor depends on the amount of charge that has passed through it, exhibiting memory behaviour where the resistance changes based on the history of the applied voltage/current. Chua's model laid the groundwork for further research and development in the field of memristors,

contributing significantly to the understanding of their unique properties and potential applications in electronic devices and systems.

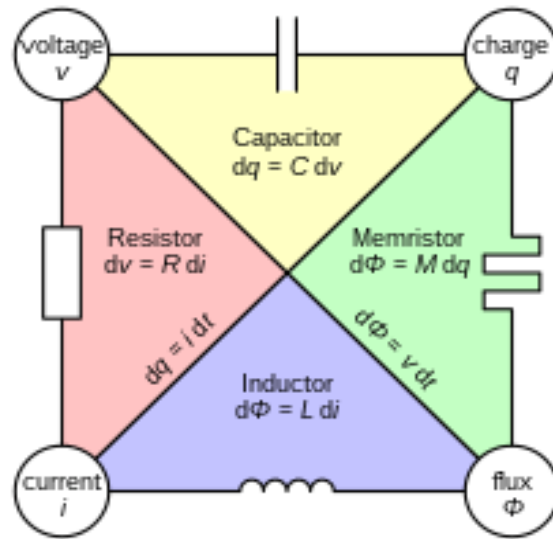


Fig: 4.1: Relation between memristor and passive components

4.2 CONSTRUCTION OF THE MEMRISTOR

Memristors are typically built on a substrate, which could be made of silicon, glass, or other materials suitable for semiconductor fabrication. Memristors often consist of thin film layers of materials with specific electrical properties. Common materials include transition metal oxides like titanium dioxide (TiO_2), tantalum oxide (Ta_2O_5), or hafnium oxide (HfO_2). These thin films are deposited onto the substrate using techniques like sputtering, chemical vapor deposition (CVD), or atomic layer deposition (ALD). Memristors have two electrodes, usually made of conductive materials like platinum (Pt), gold (Au), or titanium (Ti). These electrodes are placed on either side of the thin film layer, creating a sandwich-like structure. The thin film layer between the electrodes is the active region of the memristor. This thin film layer exhibits memristive behaviour, meaning its resistance changes based on the history of the applied voltage or current. In some memristor designs, nanostructures such as nanowires or nanodots are incorporated into the thin film layer to enhance performance or achieve specific functionality. These nanostructures can be formed through techniques like lithography or self-assembly.

Insulating layers may be added to isolate the active region of the memristor and prevent leakage currents or unwanted interactions with neighbouring components. Memristors may be encapsulated with a protective layer to shield them from environmental factors such as moisture, oxidation, or mechanical stress. Electrical connections are made to the electrodes of the memristor, allowing it to be integrated into electronic circuits.

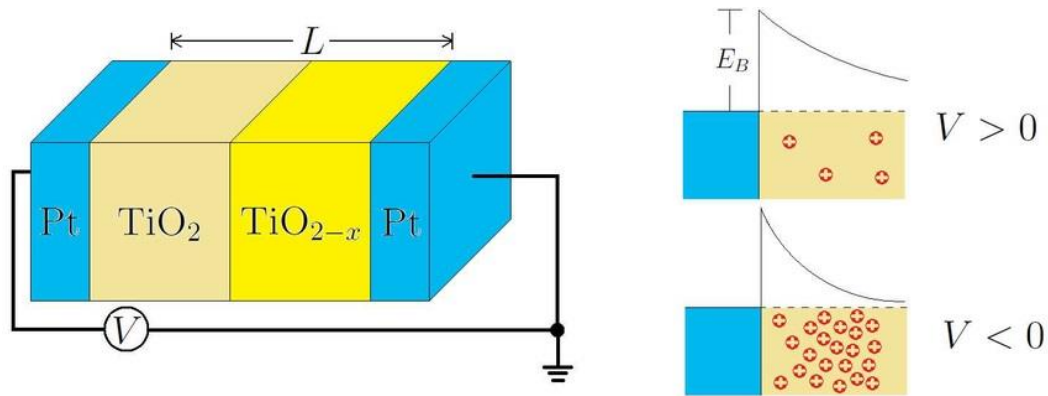


Fig: 4.2: Construction of Memristor

Memristors retain their resistance state even when the power is turned off. This non-volatile behaviour makes them suitable for use in memory devices, where data can be stored without the need for continuous power supply. The resistance of a memristor depends on the history of the applied voltage or current. This means that the resistance can be altered by the amount and direction of charge that has flowed through the device, exhibiting memory-like behaviour. Memristors offer the ability to adjust their resistance value dynamically by applying voltage or current pulses. This tunability enables various applications such as analog computing, adaptive circuits, and neural network emulation. Memristors can switch between different resistance states rapidly, typically in nanoseconds to microseconds, depending on the specific material and device design. This fast switching speed makes them suitable for high-speed memory and computing applications. Compared to traditional memory technologies like flash memory, memristors can operate with lower energy consumption. This is because they do not require continuous power to maintain their resistance state, and switching between states can be achieved with relatively low energy inputs.

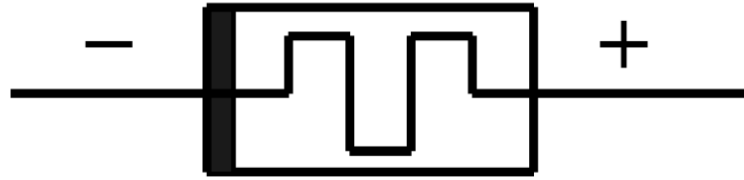


Fig: 4.3: Symbol of Memristor

Memristors can be fabricated at the nanoscale, allowing for high-density integration into electronic circuits. This high density enables the development of compact and energy-efficient memory arrays and computing systems. Memristors exhibit behaviour similar to certain biological systems, particularly in terms of synaptic plasticity—the ability of synapses to strengthen or weaken over time in response to electrical activity. This biological analogy has led to research in neuromorphic computing and brain-inspired computing using memristor-based devices. Memristors can be made from a variety of materials, including oxides, polymers, and organic compounds. This versatility enables the design of memristors with tailored properties for specific applications, such as resistive random-access memory (RRAM), synaptic devices, and programmable analog circuits.

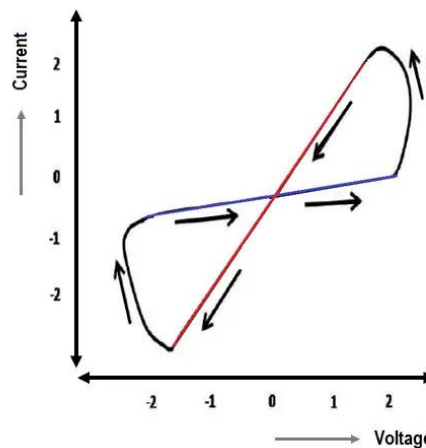


Fig: 4.4: Hysteresis loop of Memristor

4.3 STRUCTURE OF THE MEMRISTOR DECODER

A memristor-based decoder is a decoder circuit that incorporates memristors as key components. Memristors are two-terminal non-volatile memory devices whose resistance state can be changed by applying voltage. They have garnered

significant interest in recent years due to their potential applications in various electronic circuits, including memory storage, neuromorphic computing, and signal processing. When used in decoders, memristors can provide unique advantages in terms of energy efficiency, compactness, and non-volatile storage of decoder configurations. Memristors are used to implement the logic functions within the decoder. Memristors can be programmed to act as resistors with specific resistance values, which can be used to control the flow of current in the circuit. The decoder still has input lines just like a conventional decoder, and these input lines feed into the memristor-based logic.

Similarly, output lines are present, and they are controlled by the state of the memristors. The resistance states of the memristors determine which output lines are active. Memristors are programmed to represent specific logic functions by setting their resistance values. These resistance states are adjusted by applying voltage pulses to the memristors, which changes their resistance in a non-volatile manner. The specific resistance states correspond to the truth table of the decoder. Memristor-based decoders offer the potential for more efficient, compact, and non-volatile solutions for logic decoding tasks, leveraging the capabilities of memristors without going into the specifics of their inner workings. Memristors have the potential to enhance the robustness and reliability of decoders due to their non-volatile nature. This means that even in the event of a power outage or system reset, the decoder's configuration remains intact, reducing the risk of data loss or configuration errors. Memristors are reconfigurable, allowing for changes in the decoder's logic functions without the need for complex hardware alterations. This reconfigurability can lead to more adaptable and versatile decoder systems. Implementing a memristor decoder involves several steps, including component selection, circuit design, prototyping, and testing. Here's a general outline of the implementation. The factors should be considered such as resistance states, switching characteristics, and compatibility with circuit requirements. Select other electronic components such as transistors, resistors, capacitors, and interconnects based on the circuit specifications and performance objectives.

Develop a detailed circuit design for the memristor decoder, incorporating memristors as key components for memory storage and state retention. Use

standard digital logic gates (e.g., AND, OR, NAND, NOR) and flip-flops to implement the decoding logic based on your decoder's functionality.

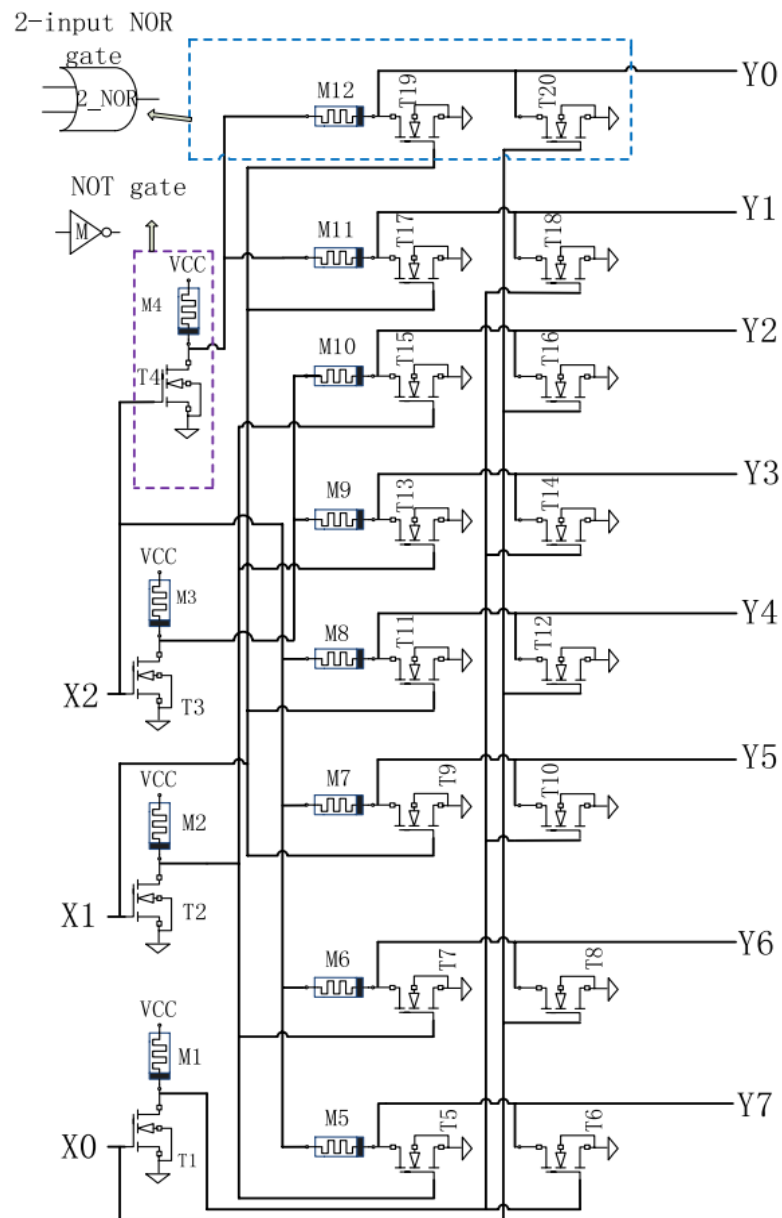


Fig: 4.5: Memristor based decoder design

4.4 IMPLEMENTATION OF THE MEMRISTOR DECODER

Implementing a memristor decoder involves several steps, including component selection, circuit design, prototyping, and testing. Here's a general

outline of the implementation. Define the specifications and requirements of the decoder, including the number of inputs and outputs, decoding logic, power constraints, and performance objectives. Memristor devices based on their characteristics such as resistance states, switching behaviour, and compatibility with your circuit requirements. Implementing the decoding logic based on the desired functionality of the decoder, ensuring proper decoding of input signals into corresponding output signals. Integrate memristors into the circuit design as memory elements or storage devices for storing decoding states or configuration settings. Determine the placement and connections of memristors within the decoder circuit, ensuring proper interaction with other circuit components.

We have to consider factors such as resistance states, switching characteristics, and compatibility with your circuit requirements. The three inputs are referred as the in1, in2, in3 which are given as 5 DC Voltage. The logic behind the decoder is $Y_0 = X_1.X_2.X_3$, it is converted as $X_1 \cdot (X_2 + X_3)$. We have to design the two input NOR gate for X2 and X3. X1 is connected with memristor on top of the NOR gate. Like that remaining outputs are also calculated using simple maths and De-Morgans law. So in this every output is calculated using the help of 2 input NOR Gate, for that we need two transistors (2 n-mos and 1 memristor) in one NOR gate. Therefor for 8 outputs we need $8 \times 2 = 16$ transistors and 3 CMOS inverters are required to transform the input to negative input. So total 19 transistors and 11 memristor are required to design the memristor decoder using cmos logic.

Utilize simulation tools such as LTspice or to model and validate the circuit design, ensuring proper functionality and performance. Fabricate a prototype of the memristor decoder circuit using printed circuit board (PCB) technology or other prototyping methods. Ensure proper layout and routing of signal traces, power distribution, and grounding to minimize signal integrity issues and noise.

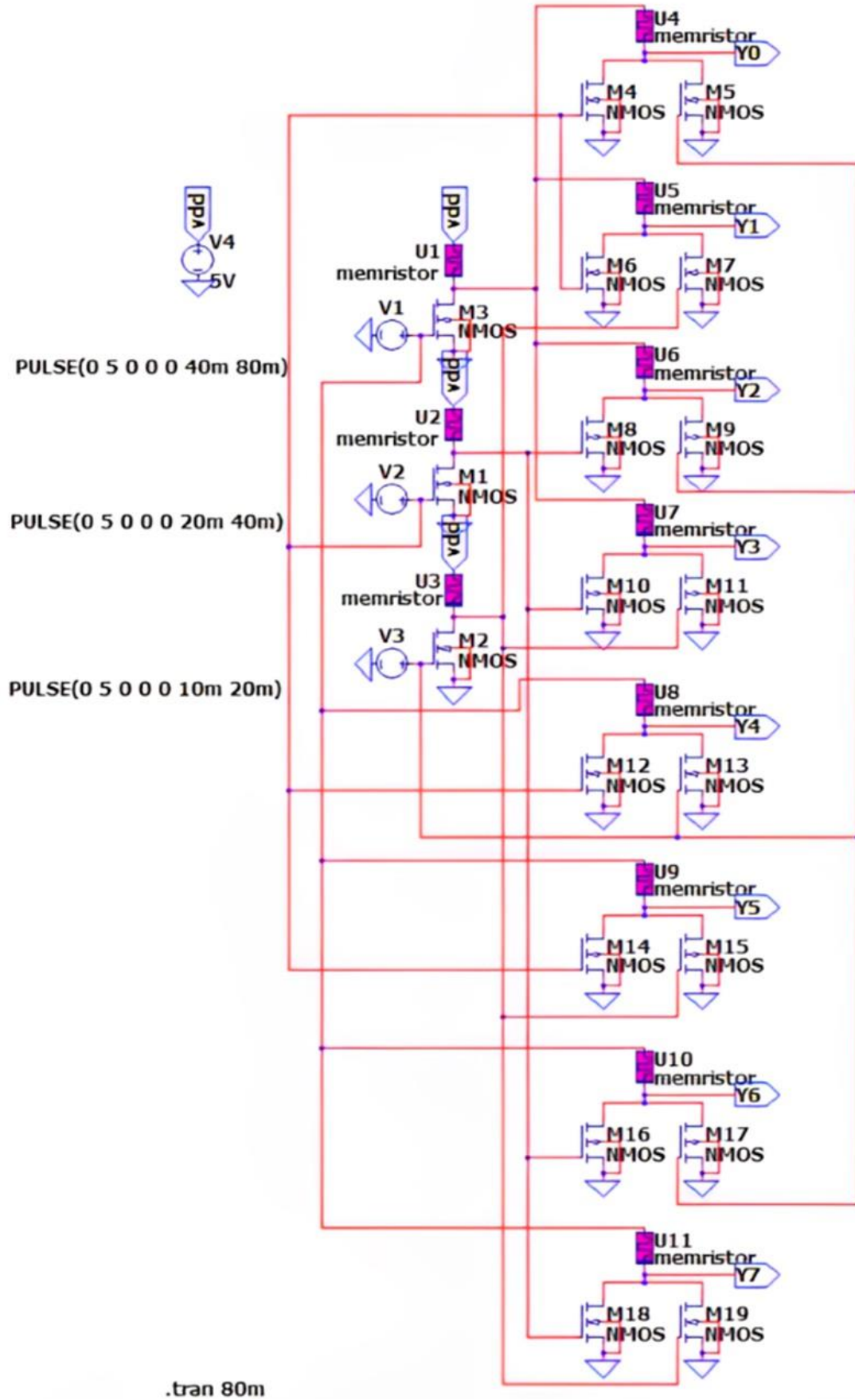


Fig: 4.6: Transistor Level Memristor Decoder Design

4.5 SIMULATION OF MEMRISTOR DECODER

In addition to designing and simulations of 3-bit memristor decoder using memristor technology for comparative analysis. This allows for a comprehensive evaluation of the performance, power consumption, and other key metrics between memristor-based and conventional decoder designs.

Ensure that the circuit design is functionally equivalent to the memristor-based decoder, capable of decoding 3-bit input signals into corresponding output signals. Set up the simulation environment using circuit simulation software such as LTspice. Define the input signals for the memristor decoder, representing all possible combinations of 3-bit input patterns. Specify simulation parameters such as operating voltage, temperature, and timing constraints. Conduct transient analysis simulations to analyse the time-dependent behaviour of the conventional decoder. Capture voltage and current waveforms at key nodes in the circuit to understand signal propagation delays, rise/fall times, and transient effects. Perform power consumption analysis to evaluate the energy efficiency of the memristor decoder. Compare the performance metrics of the memristor-based and conventional decoders, including decoding accuracy, speed, and reliability.

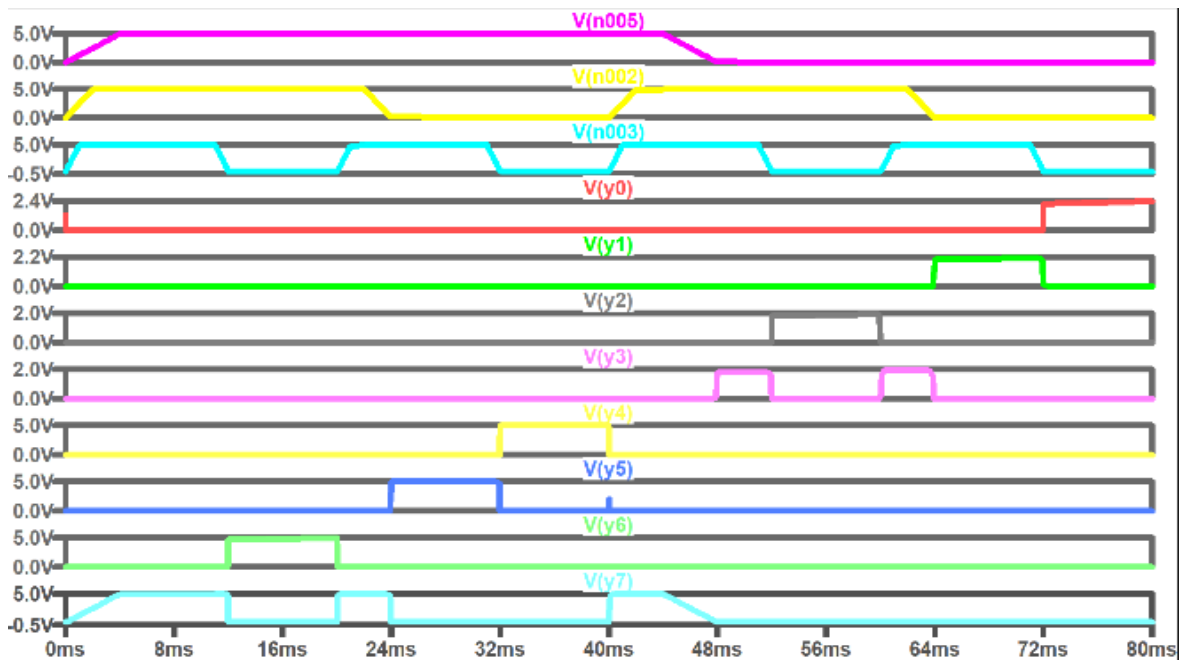


Fig: 4.7: Simulation of Memristor Decoder

4.6 STANDARDS

A. IEEE Standards

- *IEEE 1149.x (JTAG)*: Provides standards for boundary-scan testing, which can be useful for testing and debugging integrated circuits, including decoders.
- *IEEE 1076 (VHDL)*: Specifies the VHDL hardware description language, commonly used for modelling and simulating digital systems, including decoders.
- *IEEE 1364 (Verilog)*: Specifies the Verilog hardware description language, another common language for digital circuit modelling and simulation.
- *IEEE 1800 (System Verilog)*: Extends Verilog with additional features for system-level modelling and verification, relevant for complex decoder designs.

B. ISO/IEC Standards

- *ISO/IEC 7816 (Smart Cards)*: Specifies standards for integrated circuit cards, including protocols and interfaces, relevant for decoder designs involving smart card interfaces.
- *ISO/IEC 14443 (RFID)*: Specifies standards for radio frequency identification (RFID) systems, which may be relevant for decoder designs incorporating RFID technology.

4.7 CONSTRAINTS

- **Technology Compatibility:** Ensure compatibility between memristor technology and CMOS logic, considering factors such as voltage levels, signal compatibility, and integration challenges.
- **Memristor Characteristics:** Work within the constraints of available memristor devices, including their resistance states, switching behaviour, endurance, and variability. Consider the limitations of memristor technology, such as write endurance, retention time, and variability, when designing the decoder circuit.

- **Circuit Complexity:** Manage the complexity of integrating memristors with CMOS logic, considering design constraints such as circuit size, routing complexity, and manufacturing feasibility.
- **Power Consumption:** Strive to minimize power consumption while maintaining desired functionality, considering the energy efficiency trade-offs between memristor-based and CMOS-based components.
- **Signal Integrity:** Address signal integrity issues arising from the integration of memristors with CMOS logic, such as signal degradation, noise susceptibility, and timing constraints.
- **Fabrication Constraints:** Consider fabrication constraints such as process compatibility, yield optimization, and manufacturing scalability when designing the decoder circuit for practical implementation.
- **Performance Requirements:** Meet performance requirements such as decoding accuracy, speed, and reliability while adhering to the constraints imposed by memristor technology and CMOS logic.
- **Testing and Validation:** Develop robust testing methodologies to validate the functionality, performance, and reliability of the memristor-based decoder design, considering the unique characteristics of memristor devices.
- **Cost Considerations:** Evaluate the cost implications of using memristors with CMOS logic, considering factors such as device cost, fabrication expenses, and overall project budget constraints.
- **Research and Development Limitations:** Acknowledge any limitations or uncertainties in current memristor technology and CMOS integration techniques, highlighting areas for future research and development.

4.8 TRADE OFF

- **Power Consumption vs. Performance:** Increasing performance (e.g., decoding speed) may lead to higher power consumption, as more energy is required to operate the decoder circuit at faster speeds. Balancing power consumption with performance requirements is essential to meet functional objectives while maintaining energy efficiency.

- **Area Efficiency vs. Complexity:** Increasing circuit complexity to achieve greater functionality may result in a larger area footprint, as more components and interconnects are required. Optimizing circuit layout and design to minimize area while maximizing functionality is crucial to ensure efficient use of resources and space.
- **Memristor Reliability vs. Performance:** Enhancing memristor reliability (e.g., endurance, retention) may involve sacrificing performance characteristics such as speed or write/read endurance. Striking a balance between reliability and performance ensures the longevity and stability of the decoder circuit while meeting operational requirements.
- **Cost vs. Performance:** Implementing advanced memristor technology with CMOS logic may incur higher fabrication and development costs compared to traditional CMOS-based designs. Evaluating the cost-effectiveness of using memristors with CMOS logic relative to the performance benefits and long-term operational savings is essential for project feasibility.
- **Integration Complexity vs. Design Flexibility:** Integrating memristors with CMOS logic introduces additional complexity in circuit design, layout, and fabrication processes. Balancing integration complexity with design flexibility allows for the implementation of innovative solutions while minimizing development challenges and time-to-market.
- **Fabrication Yield vs. Device Variability:** Improving fabrication yield to reduce manufacturing costs may result in increased device variability, leading to performance variations among individual memristor devices. Implementing robust quality control measures and device characterization techniques helps mitigate variability issues and ensure consistent performance across decoder circuits.
- **Technology Adoption vs. Development Risk:** Adopting emerging memristor technology for decoder design offers potential performance advantages but also entails inherent development risks and uncertainties. Assessing the readiness and maturity of memristor technology, along with associated development risks, guides informed decision-making and risk management strategies.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 MEASURING THE PROPERTIES OF THE CONVENTIONAL DECODER

Perform a DC analysis simulation to measure the currents flowing through different components in the decoder circuit. Using the ".op" simulation directive to calculate the DC operating point of the circuit and display currents through power-supply sources or individual components. Using Ohm's Law ($P = VI$) to calculate the power dissipation in resistive components based on the measured currents and voltages. Sum up the power dissipated by all components to determine the total power consumption of the decoder circuit. The parameters which we took for the comparison of conventional decoder and memristor decoder are power consumption, propagation delay, area occupied and no of components. Conventional decoder is consist of 27 PMOS and 27 NMOS transistors. To calculate the power consumed by both circuit designs, by plotting the power ($p = V(V_{dd}) * I(V_4)$) will give the overall power consumed by the circuit design. After plotting the power analysis place the cursor on title and press CTRL + Click gives the average integral power of the circuit design.

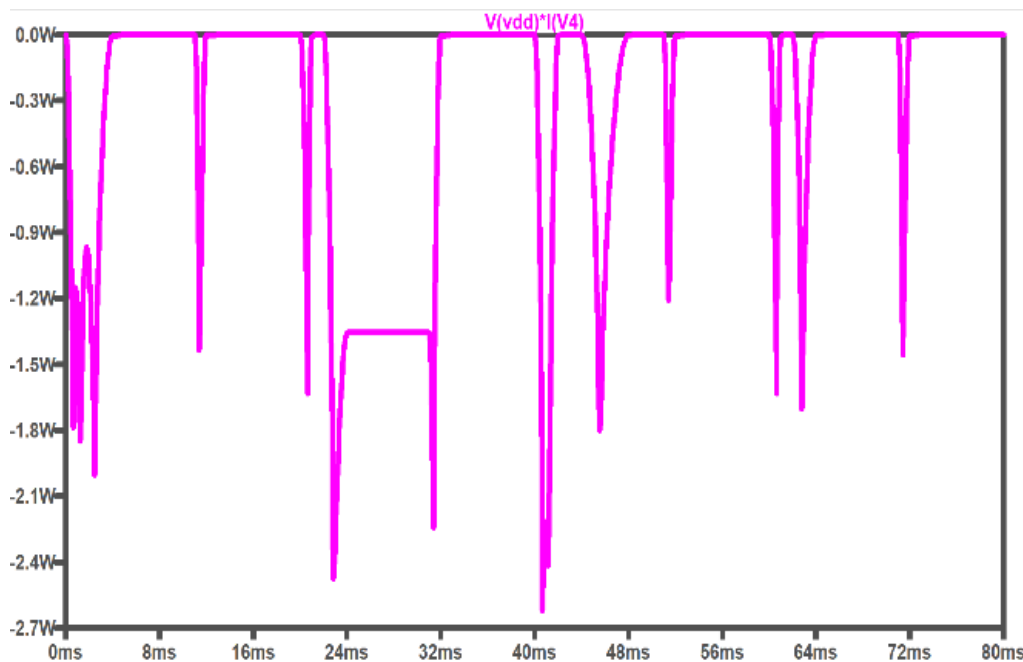


Fig: 5.1: Graph of the Power of CMOS decoder

To estimate the physical size of individual components in the decoder circuit, using the datasheets or manufacturer specifications to determine the typical dimensions of these components. Visualize the layout of the decoder circuit using LTspice graphical interface or external layout design tools. Estimate the overall area occupied by the circuit layout based on the size and placement of individual components. To measure the area occupied by the circuit designs in Ltspice. The parameters PMOS transistor length $L = 0.01 \mu\text{m}$ and width $W = 40 \mu\text{m}$ and NMOS transistors length $L = 0.01 \mu\text{m}$ and width $W = 16 \mu\text{m}$. Therefore the area occupied by the conventional decoder is 15.12 mm^2

Perform a transient analysis simulation to measure the propagation delay of signals through the decoder circuit. Apply input signals representing different input patterns and observe the corresponding output responses to identify signal transition times. Propagation delay refers to the time it takes for a signal to travel from its source to its destination in an electronic circuit. It is a critical parameter in digital circuits, especially in synchronous systems, where the timing of signals is crucial for proper operation. Propagation delay is typically measured between specific points in the circuit, such as between the input and output of a logic gate or between the clock input and the output of a flip-flop. In simple the time taken by the output waveform to change when there is any change in input waveform. To measure the propagation delay of the circuit design in Ltspice, and measure the T_{phl} and T_{plh} . These are the propagation delays of low to high and high to low of a output waveform when the input waveform varies. The average delay is obtained by calculating the average of T_{phl} and T_{plh} .

$$\text{Average delay} = (T_{\text{phl}} + T_{\text{plh}})/2$$

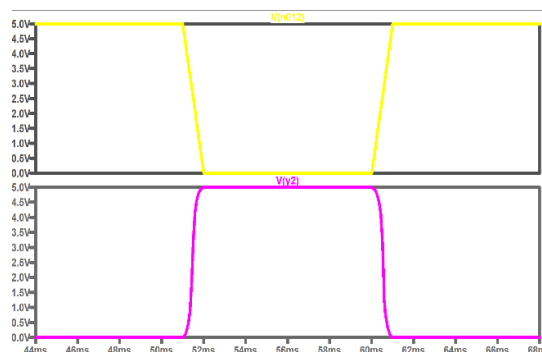


Fig: 5.2: Delay of the CMOS decoder

5.2 MEASURING THE PROPERTIES OF THE MEMRISTOR DECODER

Performing a DC transient analysis simulation to measure the currents flowing through different components in the decoder circuit. Using the ".op" simulation directive to calculate the DC operating point of the circuit and display currents through power-supply sources or individual components. Using Ohm's Law ($P = VI$) to calculate the power dissipation in resistive components based on the measured currents and voltages. Sum up the power dissipated by all components to determine the total power consumption of the memristor decoder circuit. The parameters which we took for the comparison of conventional decoder and memristor decoder are power consumption, propagation delay, area occupied and no of components. Conventional decoder is consist of 16 NMOS transistors and 3 PMOS transistors whereas memristor decoder is consists only 11 memristors. To calculate the power consumed by both circuit designs, by plotting the power (p) = $V(V_{dd}) * I(V_4)$ will give the overall power consumed by the circuit design. After plotting the power analysis place the cursor on title and press CTRL + Click gives the average integral power of the circuit design. Therefore the total power is calculated by plotting the graph of the power in Ltspice.

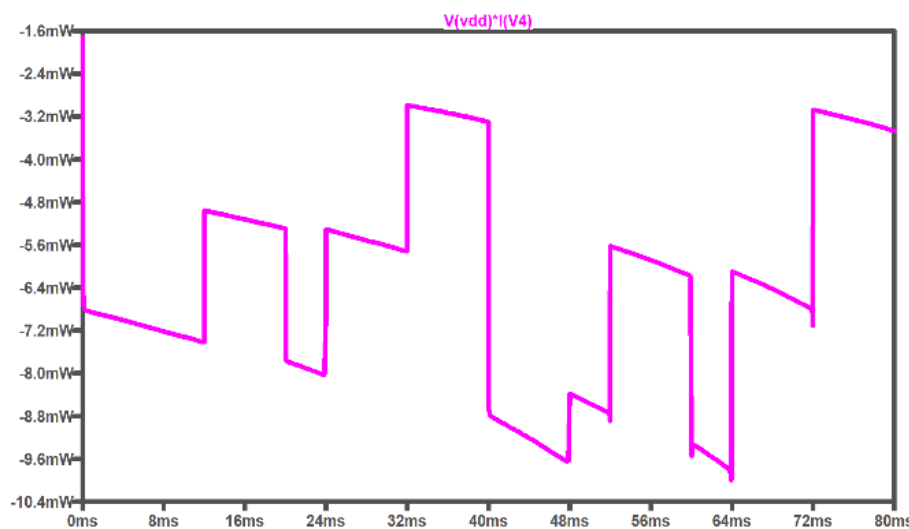


Fig: 5.3: Graph of the power of Memristor decoder

To estimate the physical size of individual components in the memristor decoder circuit, using the datasheets or manufacturer specifications to determine

the typical dimensions of these components. Visualize the layout of the decoder circuit using LTspice's graphical interface or external layout design tools. Estimate the overall area occupied by the circuit layout based on the size and placement of individual components. To measure the area occupied by the circuit designs in Ltspice. The parameters PMOS transistor length $L = 0.01 \mu\text{m}$ and width $W = 40 \mu\text{m}$ and NMOS transistors length $L = 0.01 \mu\text{m}$ and width $W = 16 \mu\text{m}$ and memristor has area $2 \times 2 \text{ nm}^2$. Therefore the area occupied by the memristor decoder is 7.6 mm^2 .

Propagation delay refers to the time it takes for a signal to travel from its source to its destination in an electronic circuit. It is a critical parameter in digital circuits, especially in synchronous systems, where the timing of signals is crucial for proper operation. Propagation delay is typically measured between specific points in the circuit, such as between the input and output of a logic gate or between the clock input and the output of a flip-flop. In simple the time taken by the output waveform to change when there is any change in input waveform. To measure the propagation delay of the circuit design in Ltspice, and measure the T_{phl} and T_{plh} . These are the propagation delays of low to high and high to low of a output waveform when the input waveform varies. The average delay is obtained by calculating the average of T_{phl} and T_{plh} .

5.3 TABULATION OF THE PROPERTIES OF BOTH DESIGNS

The Simulation results of the Conventional Decoder and Memristor Decoder are executed using the Transient Analysis of the Ltspice. The transient analysis is a simulation technique used to analyse the time-dependent behaviour of electronic circuits in response to transient signals or input stimuli. In the context of a low-power 3-bit decoder design using memristors, transient analysis would involve studying how the decoder circuit responds to changes in input signals over time. Here the interval starts from 0 milliseconds to 80 milliseconds. To compare the properties of both the memristor-based decoder and the conventional decoder, we can create a tabulation summarizing key metrics such as number of components, power consumption, area, and time delay.

Table: 5.1: Properties of both designs

PROPERTY	DECODER WITH CMOS LOGIC	DECODER WITH MEMRISTOR LOGIC
No of Components	54 (27 PMOS + 27 NMOS)	30 (19 NMOS + 11 Memristors)
Power Consumption	313.95 milliwatts	6.21 milliwatts
Time Delay	627 microseconds	101.2 microseconds
Area Occupied	15.12 square millimetres	7.6 square millimetres

5.4 ANALYSIS OF BOTH DESIGNS

To compare and analyse both the memristor-based decoder and the conventional decoder designs, let's consider several aspects including power consumption, area, time delay, and other relevant factors. Memristor based Decoder generally lower power consumption compared to conventional CMOS-based designs due to the non-volatile nature of memristors and their ability to retain state without continuous power supply. Reduced power dissipation during operation, especially in standby or idle states, leading to overall energy efficiency gains. Conventional Decoder typically higher power consumption compared to memristor-based designs, particularly when using CMOS-based components that require continuous power to maintain state. Increased power dissipation due to leakage currents and dynamic power consumption in active components such as transistors.

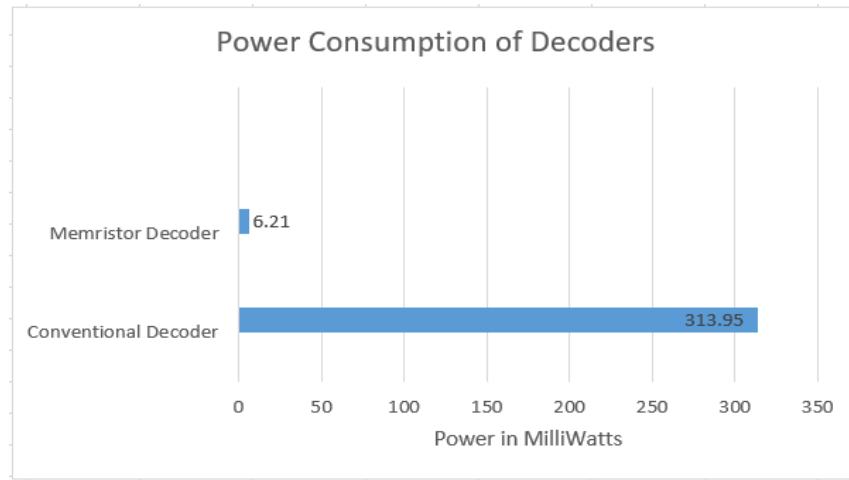


Fig: 5.4: Graphical analysis of Power Consumption

Memristor based decoder potentially smaller footprint compared to conventional designs, as memristors can serve as both memory and logic elements, reducing the need for additional components. Compact layout possible due to the integration of memristors with decoding logic, leading to area savings and potentially enabling integration in space-constrained applications. Conventional Decoder typically larger area footprint compared to memristor-based designs, especially when using CMOS-based components that require multiple layers of interconnects and complex routing. Increased area occupancy due to the presence of additional components such as transistors, resistors, and capacitors in the decoding logic.

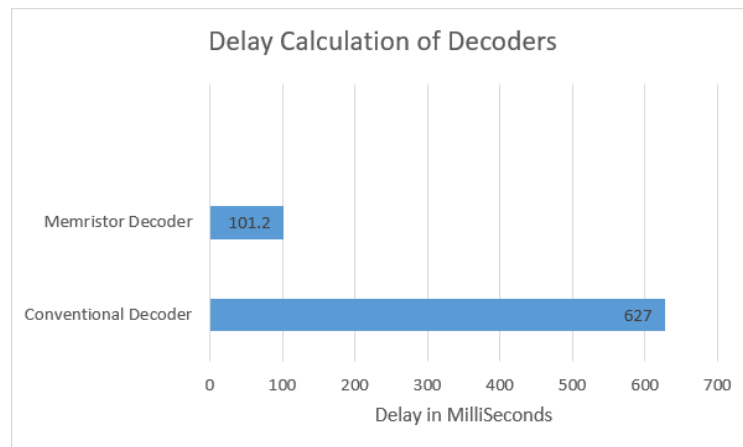


Fig: 5.5: Graphical analysis of Delay

Memristor-Based Decoder generally comparable or slightly higher time delay compared to conventional designs, depending on the specific characteristics of the memristor devices and circuit topology. Potential for optimization to minimize time delay through circuit design techniques such as pipeline staging, parallel processing, and timing analysis. Conventional Decoder typically shorter time delay compared to memristor-based designs, especially in CMOS-based implementations where signal propagation is faster due to the inherent characteristics of transistors. Possibility for further optimization to reduce time delay through techniques such as clock gating, transistor sizing, and circuit-level optimizations. Reliability and robustness may vary depending on the specific CMOS-based components used in the design and their susceptibility to aging, wear-out, and environmental factors. Greater vulnerability to transient faults and single-event upsets compared to memristor-based designs, particularly in radiation-prone environments.

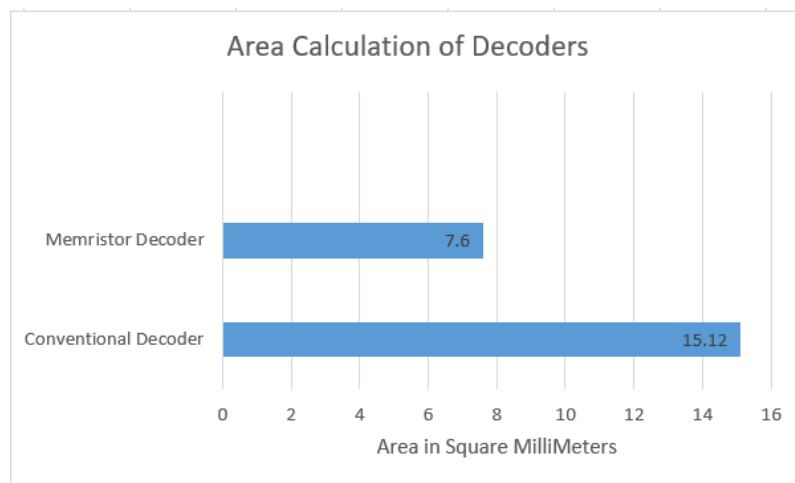


Fig: 5.6: Graphical analysis of Area

CHAPTER 6

SUMMARY AND CONCLUSION

6.1 SUMMARY

Memristor-based decoders represent an emerging technology with ongoing research and development. As the technology matures, it is expected to find applications in various domains, including artificial intelligence, signal processing, and advanced memory systems. In some implementations, memristors are arranged in crossbar arrays, which simplify the wiring and enable the efficient implementation of complex logic functions by adjusting the resistance states at the intersection points of the crossbars. Memristor-based decoders have the potential to be more energy-efficient than traditional semiconductor-based logic circuits, which can be particularly valuable in energy-constrained or battery-powered devices.

Memristor-based decoders can be more energy-efficient compared to traditional decoder implementations, which is advantageous in power-constrained applications. Memristors retain their configuration, ensuring that decoder settings are preserved even during power outages or system resets. Memristors can be integrated into compact and small-scale decoder circuits, saving space in electronic systems. Memristors enable easy reconfiguration of decoder logic, allowing for adaptable and versatile systems without significant hardware changes. The non-volatile nature of memristors enhances the reliability of decoders, reducing the risk of data loss or configuration errors. The use of crossbar arrays simplifies wiring and facilitates the implementation of complex logic functions. Memristor-based decoders play a crucial role in neuromorphic computing, where they can efficiently model synapses and neural networks. Memristor-based decoders represent an emerging and promising technology with ongoing research and development, leading to innovation in various fields.

6.2 CONCLUSION

In conclusion, this project memristor-based decoder presents several compelling advantages and opportunities in the field of digital electronics and

emerging technologies. These memristor-based decoders offer promising results, including energy efficiency, non-volatile configuration, compact design, reconfigurability, high reliability, and applications in neuromorphic computing. As an emerging technology, memristor-based decoders have the potential to revolutionize various domains, from memory systems to advanced computing applications. While there are ongoing challenges and research efforts to optimize and scale this technology, the unique properties of memristors make them a valuable candidate for future decoder and logic circuit designs. The specific benefits and outcomes of a memristor-based decoder project will depend on the objectives, application, and level of implementation. However, the inherent advantages of memristors, coupled with their ability to address issues related to energy efficiency, non-volatility, and reconfigurability, make such projects highly promising for the future of digital electronics and computing.

The future work on this project memristor-based decoders can be extensive and diverse, depending on the specific goals and applications. Here are several potential avenues for future work, continue research and development to optimize memristor technology for improved performance, reliability, and scalability. This includes refining fabrication processes to produce more consistent and durable memristors. Expand the application of memristor-based decoders in energy-efficient computing systems. Investigate how memristors can be integrated into processors, memory hierarchies, and data storage systems to reduce energy consumption in computing tasks. Further research memristor-based memory systems, including non-volatile RAM (NVRAM) and storage-class memory (SCM) applications. Develop memristor-based memory devices that offer high-speed, non-volatile data storage for various computing platforms.

REFERENCES

- [1] Alammari.K, Ahmadi.A, and Ahmadi.M, “Hybrid memristor-cmos based up-down counter design,” in 2020 27th IEEE International Conference on Electronics Circuits and Systems (ICECS). IEEE, 2020, pp.
- [2] Chua.L, “Memristor-the missing circuit element,” IEEE Transactions on circuit theory, vol. 18, no.5, pp. 507–519,1971.
- [3] Gonghi Liu, Shuhang Shen, Peipei Jin, Guangyi Wang and Yan Liang “Design of Memristor based Combinational Logic Circuits” Springer Science + Business Media, LLC, part of Springer Nature 2021, 14 June 2021.
- [4] Kvatinsky.S, Satat.G, Wald.N, Friedman.E.G, Kolodny.A, and Weiser.U.C, “Memristor based material implication (imply) logic: Design Principles and methodologies,” IEEE Transactions on Very Large Scale Integration (VLSI)Systems, vol.22, no.10, pp.2054-2066, 2013.
- [5] Kvatinsky.S, Wald.N, Satat.G, Kolodny.A, Weiser.U.C, and Friedman.E.G, “Mrl—memristor ratioed logic,” in 2012 13th International Workshop on Cellular Nanoscale Networks and their Applications. IEEE, 2012, pp.1–6.
- [6] Mandal.S, Sinha.J, and Chakraborty.A, “Design of memristor Cmos based logic gates and logic circuits,” in 2019 2nd International Conference on Innovations in Electronics, Signal Processing and Communication (IESC). IEEE, 2019, pp.215–220.
- [7] Mbarek.K, Rziga.F.O, Ghedira.S, and Besbes.K, “Design and properties of logic circuits based on memristor devices,” in 2020 IEEE International Conference on Design & Test of Integrated Micro & Nano Systems (DTS). IEEE, 2020, pp.1–5.
- [8] Megha Nawaria, Sanjay Kumar, Mohit Kumar Gautam , Narendra Singh Dhakad , Rohit Singh, Sonal Singhal, Pawan Kumar, Santosh Kumar Vishvakarma and Shaibal Mukherjee “Memristor-Inspired Digital Logic Circuits and Comparison With 90-/180-nm CMOS Technologies”, IEEE Transactions on Eelectron Devices, 2023.
- [9] Mehri Teimoori, Arash Ahmadi, Shahpour Alirezaee, Majid Ahmadi, “A Novel Hybrid CMOS-Memristor Logic Circuit Using Memristor Ratioed Logic”, 2016 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE).
- [10] Omkar Reddy Kichchannagari, Gracin.D, Ravi.V and Ananiah Durai.S “Design of Combinational Logic Circuits Using Memristor and CMOS Logic” International

Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075 (Online), Volume-8 Issue-5, March 2019.

- [11] Sachin Maheshwari , Spyros Stathopoulos , Jiaqi Wang, Alexander Serb , Yihan Pan, Andrea Mifsud , Lieuwe B. Leene, Jiawei Shen, Christos Papavassiliou , Timothy G. Constandinou and Themistoklis Prodromakis”, “Design Flow for Hybrid CMOS/Memristor Systems Part II: Circuit Schematics and Layout”, 2021.
- [12] Sachin Maheshwari, Spyros Stathopoulos, Jiaqi Wang, Alexander Serb, Yihan Pan, Andrea Mifsud, Lieuwe B. Leene, Jiawei Shen, Christos Papavassiliou, Timothy G. Constandinou, Themistoklis Prodromakis “Design Flow for Hybrid CMOS/Memristor Systems—Part II: Circuit Schematics and Layout”,IEEE Transactions on circuits and systems I: Regular papers, vol. 68, No. 12, December 2021.
- [13] Sasi. A, Ahmadi. M, and Ahmadi. A, “Low power memristor-based shift register design,” in 2020 27th IEEE International Conference on Electronics Circuits and Systems (ICECS). IEEE,2020, pp.1–4.
- [14] Senthamizh Selvi R, Resmi R Nair, Sooraj I, Subhishvar S, “An Efficient Low Power Full Adder Architecture using Memristor”, 2023 4th International Conference on Smart Electronics and Communication (ICOSEC).
- [15] Singh. A, “Memristor based xnor for high speed area efficient 1-bit full adder, ”in 2017 International Conference on Computing, Communication and Automation (ICCCA). IEEE, 2017, pp.1549–1553.
- [16] Slipkoand.V.A, Pershin.Y.V, “Importance of the window function choice for the predictive modelling of memristors”, IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 6, pp. 2167 2171,2019.
- [17] Sneha Mohan Patil, S. Prabhakaran.R.S, “Memory array with complementary resistive switch with memristive characteristics” 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI)47.
- [18] Strukov. D.B, Stewart.D.R, Borghetti. J, Li. X, Pickett.M, Ribeiro. G.M, Robinett.W, Snider.G, Strachan.J.P, Wueta.W, “Hybrid cmos / memristor circuits,” in 2010 IEEE International Symposium on Circuits and Systems(ISCAS). IEEE, 2010, pp.1967–1970.
- [19] Suri Shanmukh, Sompalli RohitKumar, Paluru Hemaprasad and R.Sakthivel “Low Power 3-Bit Encoder Design using Memristor” 2022 2nd International

Conference on Intelligent Technologies (CONIT) Karnataka, India. June 24-26, 2022.

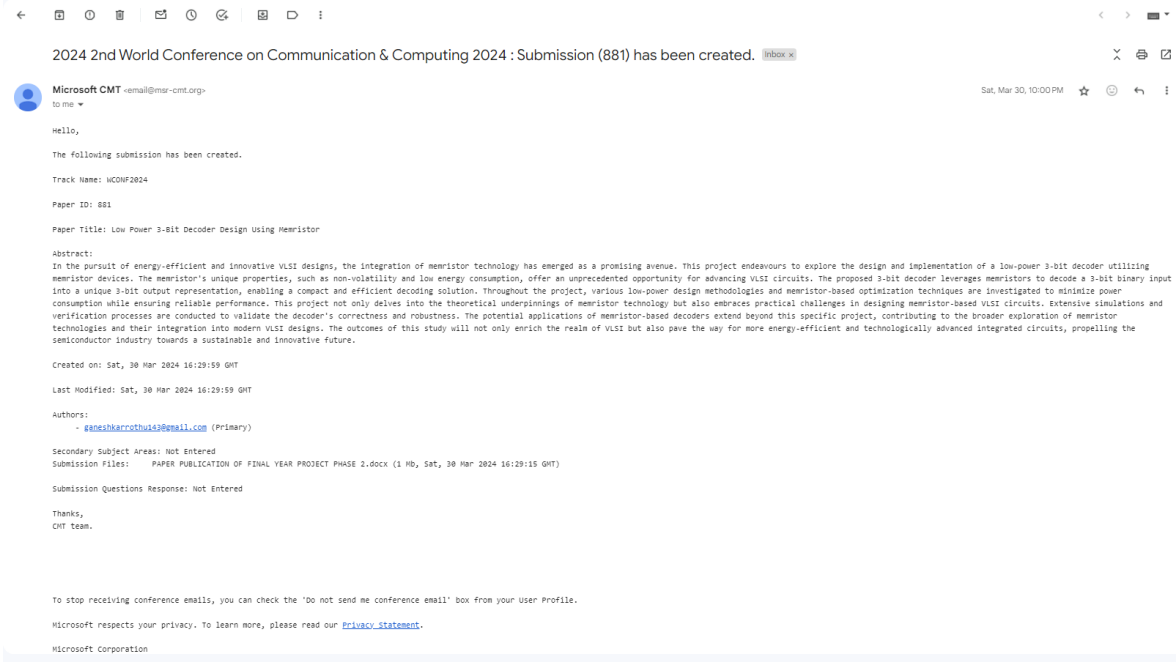
- [20] Xiaoping Wang, Bowen Xu, and Lin Chen, "Efficient Memristor Model Implementation for Simulation and Application", IEEE Transactions on computer-aided design of integrated circuits and systems, vol. 36, No. 7, July 2017.

APPENDIX

A. PLAGIARISM REPORT OF PAPER:

L.Magthelin.docx			
ORIGINALITY REPORT			
7%	4%	6%	%
SIMILARITY INDEX	INTERNET SOURCES	PUBLICATIONS	STUDENT PAPERS
PRIMARY SOURCES			
1	Chris Yakopcic. "Fabrication and testing of memristive devices", The 2010 International Joint Conference on Neural Networks (IJCNN), 07/2010 Publication	1%	
2	Mohammad Hamdani, Rifqi Fajar Giyana, A. A. N. Ananda Kusuma, Toto Bachtiar Palokoto. "On Modeling a Bottleneck Link using Dummynet", 2023 International Conference on Radar, Antenna, Microwave, Electronics, and Telecommunications (ICRAMET), 2023 Publication	1%	
3	www.umass.edu Internet Source	1%	
4	Xuan Hu, Michael J. Schultis, Matthew Kramer, Archit Bagla, Akshay Shetty, Joseph S. Friedman. "Overhead Requirements for Stateful Memristor Logic", IEEE Transactions on Circuits and Systems I: Regular Papers, 2019 Publication	1%	

B. PAPER SUBMISSION TO THE CONFERENCE:



Submissions

Search help articles

Help Center

Select Your Role : Author

WCONF2024

KARROTHU GANESH

Author Console

Create new submission

1 - 1 of 1

Show:

25

50

100

All

Clear All Filters

Paper ID	Title	Files	Actions
881 Clear Clear	Low Power 3-Bit Decoder Design Using Memristor Hide abstract In the pursuit of energy-efficient and innovative VLSI designs, the integration of memristor technology has emerged as a promising avenue. This project endeavours to explore the design and implementation of a low-power 3-bit decoder utilizing memristor devices. The memristor's unique properties, such as non-volatility and low energy consumption, offer an unprecedented opportunity for advancing VLSI circuits. The proposed 3-bit decoder leverages memristors to decode a 3-bit binary input into a unique 3-bit output representation, enabling a compact and efficient decoding solution. Throughout the project, various low-power design methodologies and memristor-based optimization techniques are investigated to minimize power consumption while ensuring reliable performance. This project not only delves into the theoretical underpinnings of memristor technology but also embraces practical challenges in designing memristor-based VLSI circuits. Extensive simulations and verification processes are conducted to validate the decoder's correctness and robustness. The potential applications of memristor-based decoders extend beyond this specific project, contributing to the broader exploration of memristor technologies and their integration into modern VLSI designs. The outcomes of this study will not only enrich the realm of VLSI but also pave the way for more energy-efficient and technologically advanced integrated circuits, propelling the semiconductor industry towards a sustainable and innovative future.	Submission files: PAPER PUBLICATION OF FINAL YEAR PROJECT PHASE 2.docx	Submission: Edit Submission Edit Conflicts Delete Submission