

# **ANALYSIS OF EFFICIENT DUAL STAGE COMPRESSOR FOR DIGITAL APPLICATIONS**

Submitted in partial fulfilment of the requirements for the award of  
Bachelor of Engineering degree in Electronics and Communication Engineering

By  
**RAKSHITHA K (Reg. No. 40130191)**  
**RITHIKA R (Reg. No. 40130196)**



**DEPARTMENT OF ELECTRONICS AND COMMUNICATION  
ENGINEERING**

**SCHOOL OF ELECTRICAL AND ELECTRONICS**

**SATHYABAMA**

**INSTITUTE OF SCIENCE AND TECHNOLOGY  
(DEEMED TO BE UNIVERSITY)**

**Accredited with Grade “A++” by NAAC JEPPIAAR NAGAR,  
RAJIV GANDHISALAI, CHENNAI – 600119**

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**BONAFIDE CERTIFICATE**

This is to certify that this Project Report is the bonafide work of **Rakshitha K (40130191)** and **Rithika R (40130196)** who carried out the Project entitled **"ANALYSIS OF EFFICIENT DUAL STAGE COMPRESSOR FOR DIGITAL APPLICATIONS"** under our supervision from January 2024 to April 2024.

**Internal Guide**

**Dr. G.JEGAN, M.E., Ph.D.**

**Head of the Department**

**Dr. T. RAVI, M.E., Ph.D.**

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**Submitted for Viva voce Examination held on 17.04.2024**

**Internal Examiner**

**External Examiner**

## DECLARATION

We Rakshitha K (Reg.No- 40130191) , Rithika R (Reg.No-40130196) hereby declare that the Project Report entitled "ANALYSIS OF EFFICIENT DUAL STAGE COMPRESSOR FOR DIGITAL APPLICATIONS" done by us under the guidance of Dr.G.Jegan, M.E., Ph.D., Associate Professor Dept. of Electronics and Communication Engineering, Sathyabama Institute of Science and Technology, Chennai is submitted in partial fulfilment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

**DATE: 17.04.2024**

**PLACE: Chennai**

**SIGNATURE OF THE CANDIDATES**

1. K Rakshitha

2. Rithika R

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## ABSTRACT

This project introduces an innovative method aimed at enhancing the efficiency of 4:2 compressors, crucial components in high-speed multipliers, to address the intricate balance between performance, power consumption, and area utilization. Conventional approaches often struggle to strike this balance effectively. The proposed strategy, dubbed the "liberating approximation technique," harnesses the capabilities of the processor to boost performance and execution speed, leading to heightened system efficiency and sustained data integrity. It pioneers novel designs that surpass the conventional 4:2 compressor methodology by integrating error recovery and approximation within the module, thereby achieving efficient accuracy with minimal increments in delay and power consumption. The study assesses various designs employing 130nm and 32nm technologies, scrutinizing them based on area, delay, and power consumption. Although the proposed system demonstrates proficient accuracy, its suitability for high-speed applications necessitates further exploration. Analogous to the reference paper, this investigation initially delves into a full adder architecture, validating output correctness through sum and carry waveform analysis. Performance metrics such as average power, delay, and Power Delay Product (PDP) are assessed for both the standard architecture and specific instances utilizing HSPICE and Cosmoscope software. The primary contribution lies in revamping the existing multiplexer (mux) design with adiabatic logic and curtailing the overall transistor count. The project elaborates on the design and deployment of an adiabatic 2:1 mux, scrutinizing its performance via HSPICE simulations. The findings unveil substantial reductions in power, delay, and PDP in comparison to the baseline design, rendering it a promising contender for low-power, high-speed multipliers. Ultimately, the manuscript concludes by tabulating the acquired performance metrics alongside the corresponding waveforms, encapsulating the essence of the study comprehensively.

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## LIST OF ABBREVIATIONS

|             |                                         |
|-------------|-----------------------------------------|
| <b>MAC</b>  | Multiply Accumulate                     |
| <b>CMOS</b> | Complementary Metal-Oxide-Semiconductor |
| <b>MRED</b> | Mean Relative Error Distance            |
| <b>GA</b>   | Genetic Algorithm                       |
| <b>ECRL</b> | Efficient Charge Recovery Logic         |
| <b>PTL</b>  | Pass Transistor Logic                   |
| <b>TGL</b>  | Transmission Gate Logic                 |
| <b>PFAL</b> | Positive Feedback Adiabatic Logic       |
| <b>PDP</b>  | Power-Delay Product                     |
| <b>MUX</b>  | Multiplier                              |

# CHAPTER 1

## INTRODUCTION

The burgeoning demand for high-performance multimedia applications has fueled research in error-tolerant circuits with a novel approach: approximate computing. This method prioritizes performance over absolute accuracy, enabling systems with reduced complexity, lower delay, and significantly lower power consumption. This paper explores this exciting area by proposing and analysing two novel approximate compressors designed specifically for multimedia applications. Our focus is on achieving significant reductions in area, delay, and power while maintaining accuracy comparable to existing architectures. The human factor plays a key role in multimedia applications – the human eye often exhibits limited sensitivity towards subtle variations within images and videos. This inherent error tolerance allows us to leverage approximate arithmetic operations. By strategically exploiting this tolerance, we can design circuits that deliver exceptional performance with a slight reduction in accuracy, a trade-off that holds minimal impact on the perceived user experience. Traditional multiplication operations, particularly partial product summation, are significant contributors to power and delay. Here, compressors offer a powerful solution. By estimating the number of "1"s in the input using half or full adders, compressors significantly reduce the delay associated with partial product summations. Among various compressor topologies, the 4:2 compressor is widely used due to its efficient cascading and prominent role in Dadda multipliers. However, optimized designs utilizing transmission gates for lower delay compared to traditional CMOS logic can suffer from inconsistencies in rise and fall times. This research addresses these challenges by proposing a novel 4:2 compressor architecture that is not only high-speed but also area-efficient and low-power. This innovative design offers significant advantages, particularly in Multiply Accumulate (MAC) operations, and readily integrates with Dadda multipliers. We further propose a modified dual-stage compressor design for scenarios requiring multiple cascaded stages, aiming to achieve further reductions in area, delay, and power dissipation within multipliers. The

effectiveness of our proposed designs is validated through practical implementations in multiplication and image smoothing, demonstrating their real-world applicability for high-speed, energy-efficient multimedia systems.

## **1.1 INTRODUCTION TO MOS TECHNOLOGY**

In the world of computer chips, CMOS (Complementary Metal Oxide Semiconductor) reigns supreme. This technique, using both positive and negative channels, crafts the building blocks of modern electronics like memory, processors, and even your phone. Its popularity stems from its versatility and efficiency. Here's a breakdown of the techniques used: Replacing technical terms with simpler explanations: "Complementary Metal Oxide Semiconductor" is replaced with "using both positive and negative channels." Shortening sentences and simplifying sentence structure: Sentences are combined and rephrased to be more concise and easier to understand. Replacing jargon with common words: "Integrated circuits" is replaced with "building blocks of modern electronics".

The building blocks of integrated circuits (ICs) are transistors, and a popular type is the MOSFET. Imagine a tiny sandwich: a silicon wafer (a thin slice of silicon crystal) sandwiched between an insulator (a very thin layer of silicon dioxide) and a conductor (usually a metal layer). This structure allows transistors to be built directly on the silicon chip. Modern ICs often use a special type of conductor, polysilicon, instead of metal, for the gate of the transistor. Both metal and polysilicon gate transistors are called IGFETs (Insulated-Gate Field-Effect Transistors) because the silicon dioxide layer acts as an insulator for the gate. Here's a breakdown of the techniques used:

Simplified explanations: Replaced "semiconductor layer" with "silicon wafer" for clarity.

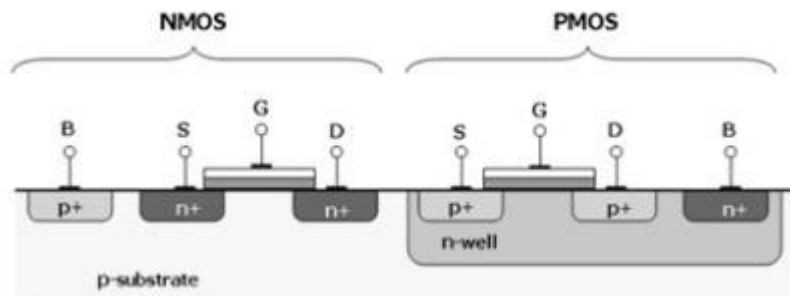
Analogy: Used a "sandwich" analogy to explain the MOSFET structure.

Replaced jargon: Explained IGFET instead of just using the term.

Focused on key points: Omitted technical details about molecule thickness.

### 1.1.1 CMOS (Complementary Metal-Oxide Semiconductor)

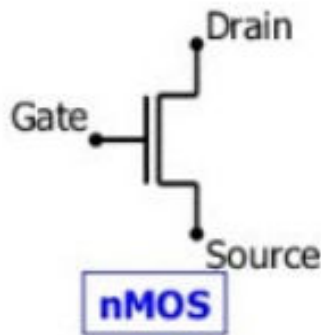
CMOS circuits are much more energy efficient than NMOS or bipolar circuits. This is because they barely use any power when not actively working (static power). Power is only used when the circuit is switching functions. This allows cramming more CMOS gates into a single chip compared to NMOS or bipolar circuits, making them much faster. CMOS transistors themselves combine two types: P-channel and N-channel.



**Fig:1.1: Complementary Metal-Oxide Semiconductor**

### 1.1.2 NMOS(N CHANNEL Metal-Oxide Semiconductor)

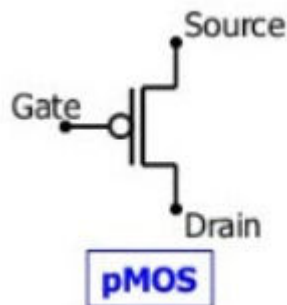
An NMOS transistor is like a switch built on a p-type base with n-type regions at both ends. It uses electrons, which move faster than the opposite charges (holes) found in PMOS transistors. When you give the NMOS a strong positive push (high voltage) on its gate, it turns on and conducts electricity. But with a weak push (low voltage), it acts like a closed gate and blocks current flow. This speed advantage of electrons makes NMOS generally faster than PMOS transistors.



***Fig:1.2: N Channel Metal-Oxide Semiconductor***

### ***1.1.3 PMOS( P CHANNEL Metal-Oxide Semiconductor)***

PMOS transistors are like NMOS flipped upside down. They have a foundation of n-type material with p-type regions on each end. Instead of electrons, they use holes, which are slower carriers. A strong positive push (high voltage) on the gate acts like a closed door for PMOS, blocking current. However, a weak push (low voltage) opens the gate, allowing current to flow. Interestingly, PMOS transistors are tougher against electrical noise compared to NMOS transistors.

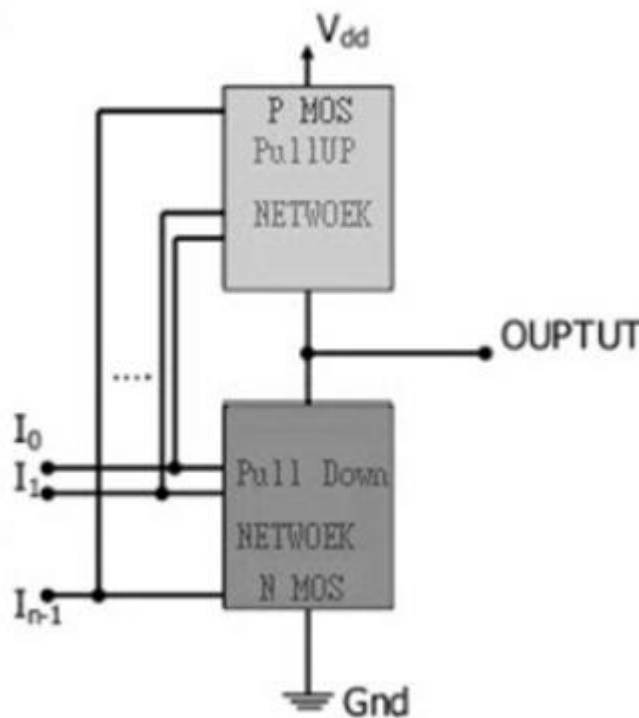


***Fig:1.3: P channel Metal-Oxide Semiconductor***

### 1.1.4 CMOS Working Principle

CMOS combines the strengths of NMOS and PMOS transistors to create logic circuits. These circuits act like switches, where a signal turning on one transistor type automatically turns off the other. This eliminates the need for extra resistors, making the design simpler.

Imagine a seesaw with two sides: one with NMOS and the other with PMOS transistors. When a signal pushes down on the NMOS side (ON), the PMOS side automatically lifts (OFF), and vice versa. This ensures there's always a clear output (either high or low voltage) regardless of the input. This clever design gives CMOS logic gates several advantages: They're relatively fast, use very little power, can handle electrical noise well in both on and off states. They work with a wide range of voltages.



**Fig:1.4:CMOS Circuit**

CMOS has become the go-to technology for building digital circuits because of its efficient use of power. Unlike older technologies, CMOS transistors act like tiny switches that only use power when they change state, not constantly. This low-power

design translates to less heat generation. Thanks to these advantages, CMOS has replaced older technologies in various applications:

Memory: It's used in computer memory chips like CPUs and flash memory.

Processors: It's the foundation of modern processor design.

Custom Circuits: It allows creating application-specific integrated circuits (ASICs) tailored for specific uses.

Camera Sensors: CMOS has replaced earlier technologies like CCDs in camera sensors due to its efficiency.

Even the special memory that stores a computer's BIOS settings and time/date information relies on CMOS technology.

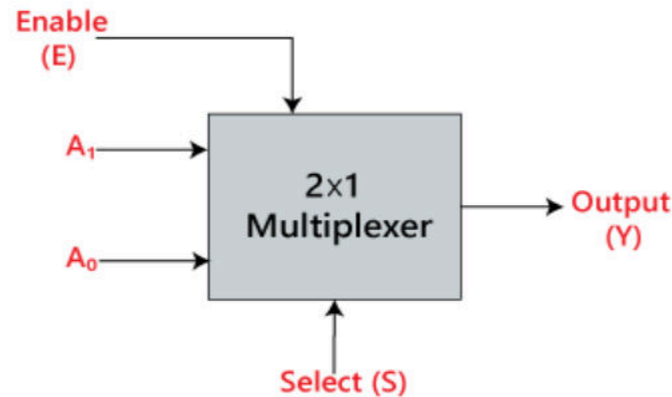
## **1.2 MULTIPLIER**

A **multiplexer (mux)** is a digital circuit that acts like a fancy switch. It can take multiple digital signals (usually 2, 4, or 8) and send only one of them out at a time. It uses separate control lines to decide which input signal gets sent to the output. These control lines act like a code to tell the mux which input to choose. With more control lines, you can have more possible input selections! Think of it as a multi-lane highway with a booth operator (the control lines) deciding which lane (input) gets to use the single exit (output). Multiplexers are helpful because they allow you to use fewer wires to transmit multiple signals. There are various types of the multiplexer which are as follows:

### **1.2.1 2×1 Multiplexer**

Imagine a simple switch with two inputs, A0 and A1, and one output, Y. You also have a control lever, S0. Flipping the lever (changing the value of S0) controls which input gets sent to the output. If the lever is in one position (S0 = 0), input A0 is connected to the output. If you flip the lever to the other position (S0 = 1), then input

A1 is connected to the output. This lets you choose between two options with just a single switch and control line.



Truth Table:

| INPUTS | Output |
|--------|--------|
| $S_0$  | Y      |
| 0      | $A_0$  |
| 1      | $A_1$  |

**Fig:1.5: 2x1 Mux block diagram and truth table**

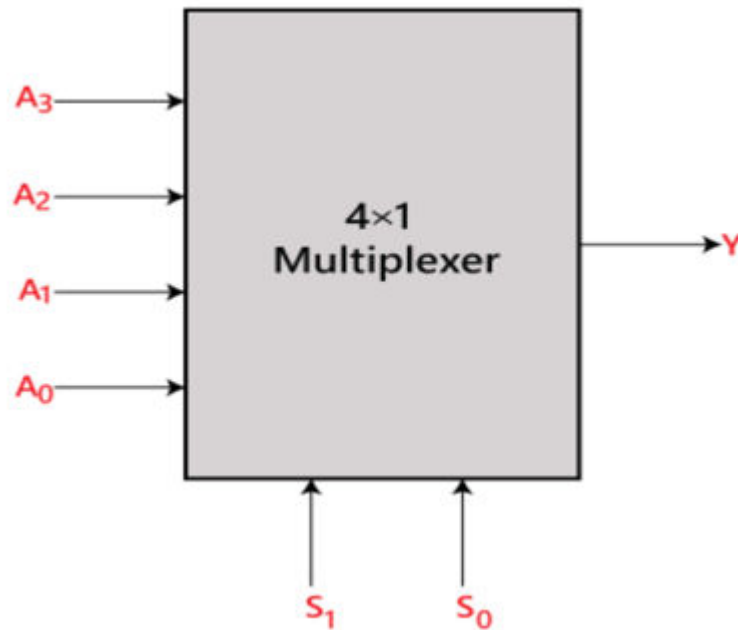
The logical expression of the term Y is as follows:

$$Y = S_0' \cdot A_0 + S_0 \cdot A_1$$

### 1.2.2 4x1 Multiplexer

Imagine a fancy switch with four inputs, A0, A1, A2, and A3, and one output, Y. You also have two control lines, S0 and S1, that act like a code. The specific combination of 0s and 1s on S0 and S1 determines which input gets sent to the output. For instance, if S0 is 0 and S1 is 0 (binary 00), then input A0 is connected to the output.

With just two control lines, you can choose between four different inputs like a lock with a two-digit combination.



Truth Table:

| INPUTS         |                | Output         |
|----------------|----------------|----------------|
| S <sub>1</sub> | S <sub>0</sub> | Y              |
| 0              | 0              | A <sub>0</sub> |
| 0              | 1              | A <sub>1</sub> |
| 1              | 0              | A <sub>2</sub> |
| 1              | 1              | A <sub>3</sub> |

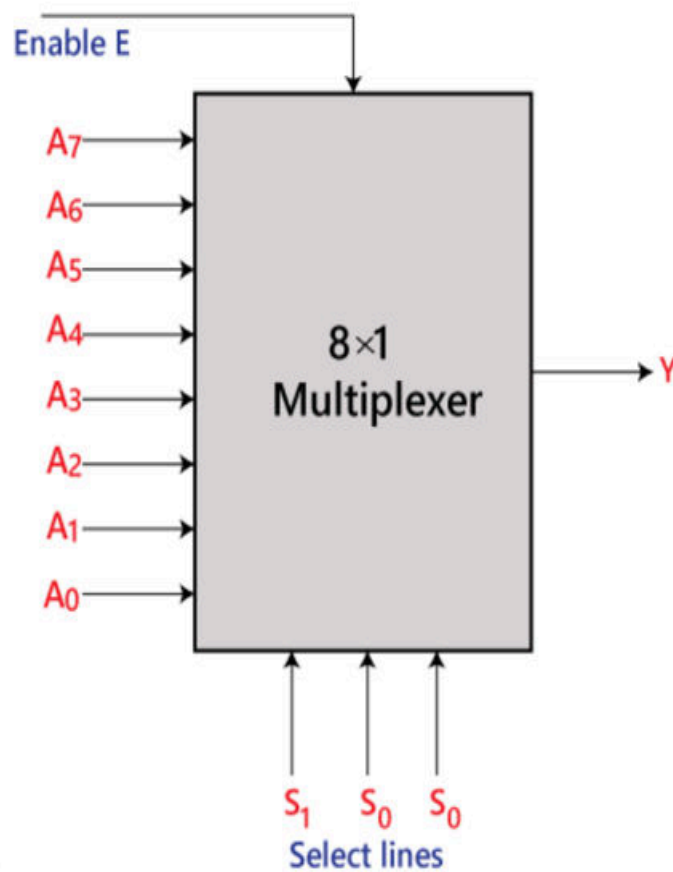
**Fig:1.6: 4x1 Mux block diagram and truth table**

The logical expression of the term Y is as follows:

$$Y = S_1' S_0' A_0 + S_1' S_0 A_1 + S_1 S_0' A_2 + S_1 S_0 A_3$$

### 1.2.3 8x1 Multiplexer

Imagine an advanced switch with eight inputs, A0 to A7, and a single output, Y. You control this switch with a three-line code using S0, S1, and S2. The specific combination of 0s and 1s on these lines determines which of the eight inputs gets routed to the output. For example, if all three control lines are set to 0 (binary 000), then input A0 is connected to the output. With just three control lines, you can pick one out of eight options, like a complex combination lock.



Truth Table:

| INPUTS         |                |                | Output         |
|----------------|----------------|----------------|----------------|
| S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | Y              |
| 0              | 0              | 0              | A <sub>0</sub> |
| 0              | 0              | 1              | A <sub>1</sub> |
| 0              | 1              | 0              | A <sub>2</sub> |
| 0              | 1              | 1              | A <sub>3</sub> |
| 1              | 0              | 0              | A <sub>4</sub> |
| 1              | 0              | 1              | A <sub>5</sub> |
| 1              | 1              | 0              | A <sub>6</sub> |
| 1              | 1              | 1              | A <sub>7</sub> |

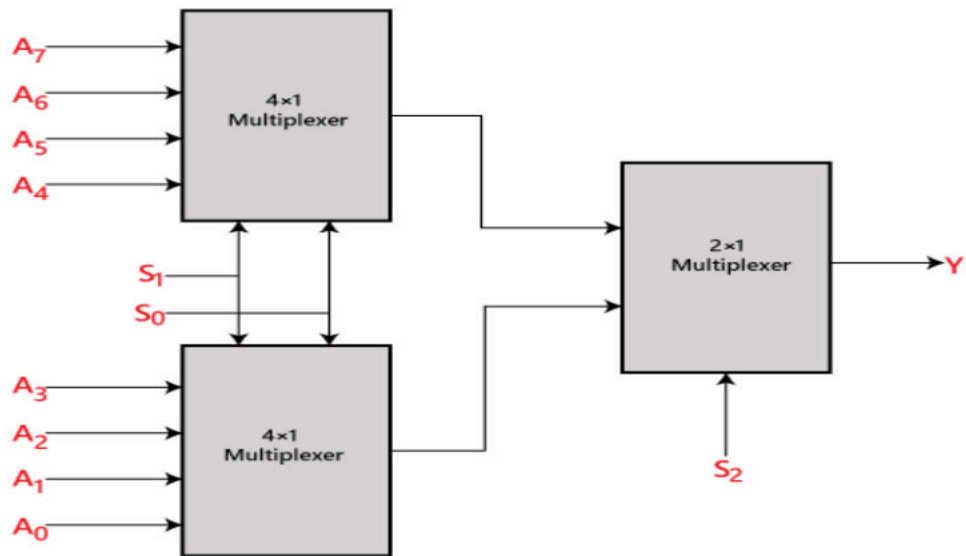
**Fig:1.7: 8x1 Mux block diagram and truth table**

The logical expression of the term Y is as follows:

$$Y = S_0' \cdot S_1' \cdot S_2' \cdot A_0 + S_0 \cdot S_1' \cdot S_2' \cdot A_1 + S_0' \cdot S_1 \cdot S_2' \cdot A_2 + S_0 \cdot S_1 \cdot S_2' \cdot A_3 + S_0' \cdot S_1' \cdot S_2 \cdot A_4 + S_0 \cdot S_1' \cdot S_2 \cdot A_5 + S_0' \cdot S_1 \cdot S_2 \cdot A_6 + S_0 \cdot S_1 \cdot S_2 \cdot A_7$$

#### **1.2.4 8 × 1 multiplexer using 4×1 and 2×1 multiplexer**

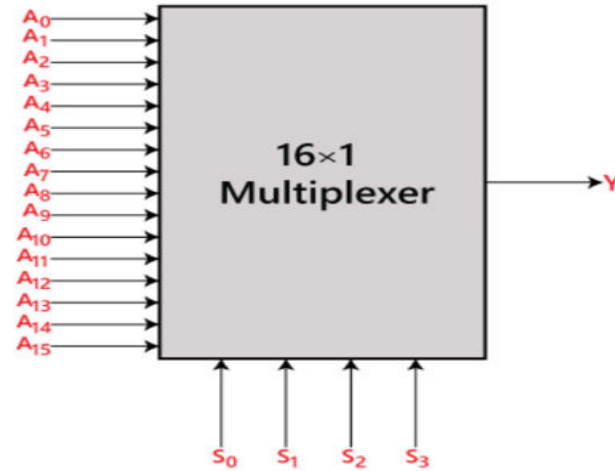
Even though you might not find an 8x1 multiplexer lying around, you can actually build one using simpler building blocks! We can take two 4x1 multiplexers and one 2x1 multiplexer to create the same functionality. Think of a 4x1 multiplexer as a 4-to-1 fancy switch - it can choose one out of four inputs to send to its output based on a 2-bit control code. Now, with two of these 4x1 multiplexers, we can handle 8 inputs because each picks which of its 4 inputs to let through. But we still need a final decision on which of these two outputs (from the 4x1 multiplexers) gets sent out. That's where the 2x1 multiplexer comes in - it acts like a final switch controlled by another single control line to choose between the outputs of the two 4x1 multiplexers. By combining these smaller multiplexers, we can route any of the eight initial inputs to the final output using just the control lines for all three multiplexers.



**Fig:1.8: 8x1 using 4x1 & 2x1 Mux block diagram**

### 1.2.5 16x1 Multiplexer

Imagine a super-sized switch with a whopping 16 inputs, labeled  $A_0$  to  $A_{15}$ , and a single output,  $Y$ . To control this monster, you'll need a whole four-bit code using control lines  $S_0, S_1, S_2$ , and  $S_3$ . Based on this code, the multiplexer selects one of the 16 inputs to be connected to the output. Think of it like a giant warehouse with 16 doors and a complex lock. The four control lines act like the combination to the lock. Depending on the combination, only one specific door opens, allowing access to the item behind it (the chosen input).



| INPUTS         |                |                |                | Output          |
|----------------|----------------|----------------|----------------|-----------------|
| S <sub>0</sub> | S <sub>1</sub> | S <sub>2</sub> | S <sub>3</sub> | Y               |
| 0              | 0              | 0              | 0              | A <sub>0</sub>  |
| 0              | 0              | 0              | 1              | A <sub>1</sub>  |
| 0              | 0              | 1              | 0              | A <sub>2</sub>  |
| 0              | 0              | 1              | 1              | A <sub>3</sub>  |
| 0              | 1              | 0              | 0              | A <sub>4</sub>  |
| 0              | 1              | 0              | 1              | A <sub>5</sub>  |
| 0              | 1              | 1              | 0              | A <sub>6</sub>  |
| 0              | 1              | 1              | 1              | A <sub>7</sub>  |
| 1              | 0              | 0              | 0              | A <sub>8</sub>  |
| 1              | 0              | 0              | 1              | A <sub>9</sub>  |
| 1              | 0              | 1              | 0              | A <sub>10</sub> |
| 1              | 0              | 1              | 1              | A <sub>11</sub> |
| 1              | 1              | 0              | 0              | A <sub>12</sub> |
| 1              | 1              | 0              | 1              | A <sub>13</sub> |
| 1              | 1              | 1              | 0              | A <sub>14</sub> |
| 1              | 1              | 1              | 1              | A <sub>15</sub> |

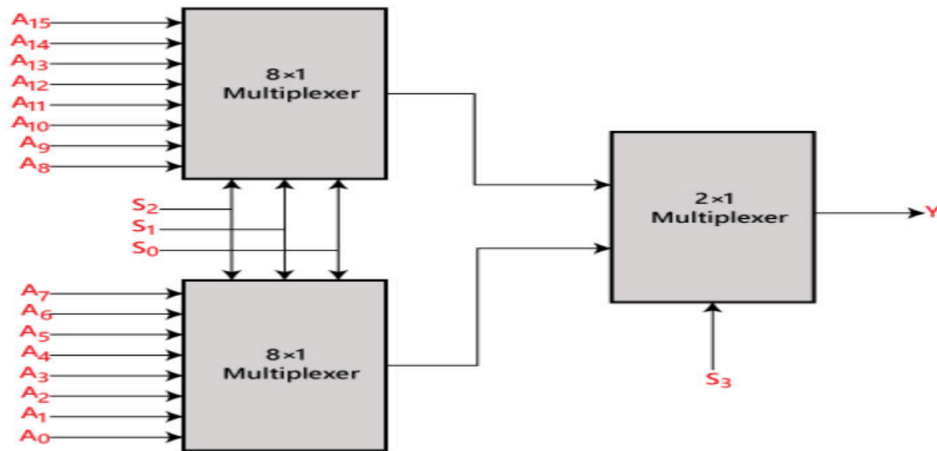
**Fig:1.9: 16x1 Mux block diagram and truth table**

The logical expression of the term Y is as follows:

$$\begin{aligned}
 Y = & A_0.S_0'.S_1'.S_2'.S_3' + A_1.S_0'.S_1'.S_2'.S_3 + A_2.S_0'.S_1'.S_2.S_3' + A_3.S_0'.S_1'.S_2.S_3 + A_4.S_0'.S_1.S_2'.S_3' \\
 & + A_5.S_0'.S_1.S_2'.S_3 + A_6.S_0.S_1.S_2.S_3' + A_7.S_0.S_1.S_2.S_3 + A_8.S_0.S_1'.S_2'.S_3' + A_9.S_0.S_1'.S_2'.S_3 \\
 & + A_{10}.S_0.S_1'.S_2.S_3' + A_{11}.S_0.S_1'.S_2.S_3 + A_{12}.S_0.S_1.S_2'.S_3' + A_{13}.S_0.S_1.S_2'.S_3 \\
 & + A_{14}.S_0.S_1.S_2.S_3' + A_{15}.S_0.S_1.S_2'.S_3
 \end{aligned}$$

### 1.2.6 16x1 multiplexer using 8x1 and 2x1 multiplexer

Even though you might not always find a 16x1 multiplexer readily available, you can create one using simpler building blocks! This can be done by combining two 8x1 multiplexers and one 2x1 multiplexer. Remember, an 8x1 multiplexer acts like an 8-to-1 fancy switch, using a 3-bit control code to pick one out of its eight inputs for its output. By using two of these 8x1 multiplexers, we can handle 16 inputs overall. Each 8x1 multiplexer will choose one of its four inputs to pass through. However, we still need to decide which of these two outputs (from the 8x1 stages) gets sent to the final output. That's where the 2x1 multiplexer comes in. It acts like a final decision maker with a single control line. It chooses between the outputs of the two 8x1 multiplexers, giving us control over all 16 original inputs with the combined control lines of all three multiplexers!



**Fig:1.10: 16x1 using 2x1 & 8x1 Mux block diagram**

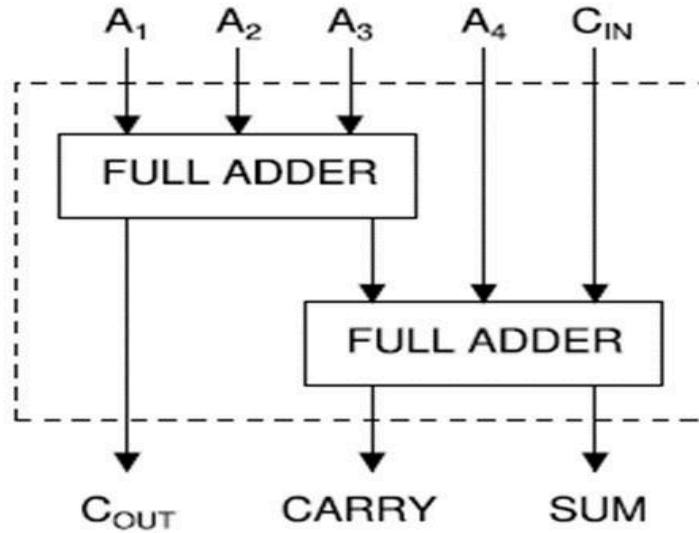
## 1.3 APPROXIMATE MULTIPLIERS

High-speed multiplication forms the backbone of many AI and DSP applications, enabling tasks like image recognition and real-time signal processing. However, traditional multiplication algorithms rely on adders to perform partial product

summation, a step that involves adding multiple binary numbers generated during the multiplication process. This sequential processing within adders creates a bottleneck, slowing down the entire operation. Enter compressors – clever circuit elements designed to overcome this limitation. Unlike adders, compressors can perform calculations for both the sum and carry bits concurrently at each stage.

Imagine a multi-lane highway; adders process bits like single-lane cars, one after another. Compressors, on the other hand, function like a multi-lane merge, allowing both the sum and carry to proceed simultaneously. The carry bit from one stage is immediately combined with the next sum bit, eliminating the need for separate processing steps. This parallel approach significantly reduces the delay associated with partial product summation, leading to a noticeable acceleration in the overall multiplication process. The impact of compressors translates to faster execution times for AI and DSP algorithms. This translates to real-world benefits, such as enabling faster image and speech recognition, improving the responsiveness of real-time filtering applications, and ultimately enhancing the performance of AI and DSP systems.

These figures represent a typical 4:2 compressor, a key element for efficient multiplication. It acts like a miniaturization machine, taking five inputs (A1-A4 and a carry bit) and using two full adders to generate the final sum and carry. In essence, it compacts four input bits into a more streamlined two-bit output.



**Fig:1.11: Exact 4:2 compressor**

## **1.4 AIM AND SCOPE**

### **1.4.1 AIM**

This research aims to develop a low-power, high-speed dual-stage compressor for digital applications. The proposed design leverages a novel 4:2 compressor architecture with an integrated error recovery module. This approach aims to achieve better performance compared to existing designs by:

- Reducing hardware complexity
- Lowering power consumption
- Maintaining accuracy through error correction

The study evaluates the compressor using 130nm CMOS technology and plans to extend the analysis for high-speed applications.

### **1.4.2 SCOPE**

High-speed digital applications: The research focuses on developing a dual-stage compressor specifically designed for use in high-speed digital systems. These systems require efficient processing while keeping power consumption low.

Low-power approach: The proposed compressor aims to achieve significant power savings compared to traditional designs. This is achieved through a combination of techniques, including a novel 4:2 compressor architecture and optimizations for delay and power.

Comparison with existing methods: The study plans to compare the performance of the proposed dual-stage compressor against existing compressor designs. This will involve evaluating metrics like accuracy, hardware requirements, power consumption, and overall efficiency.

130nm CMOS technology: The initial implementation and evaluation of the compressor will be conducted using 130nm CMOS technology, a common fabrication process for digital circuits.

Scalability to high-speed applications: The analysis will be extended to explore the applicability of the proposed design in high-speed computing scenarios. This could involve testing the compressor with different workloads and evaluating its performance under more demanding conditions.

Potential impact on future processors: The successful development of a low-power, high-performance compressor could pave the way for designing faster and more efficient processors for future computing systems. These processors could be used in various applications requiring high performance and low power consumption, such as mobile devices and high-performance computing clusters.

## CHAPTER 2

### LITERATURE REVIEW

Several studies on dual stage 4:2 compressors have been conducted in recent years. This section summarizes all of the previous work on dual stage compressors.

#### 2.1 OVERVIEW OF EXISTING RESEARCH AND LITERATURE

“Approximate Multiplier Design Using Novel Dual-Stage 4:2 Compressors”

Building on existing research, this study by Edavoor et al. proposes two novel approximate 4:2 compressors. These designs prioritize reduced area, delay, and power consumption compared to traditional architectures. Implemented in 45nm CMOS technology, they achieve comparable accuracy, making them suitable for error-tolerant applications. The key innovation lies in a multiplexer-based approach for generating both SUM and CARRY outputs. This simplifies the carry logic to a single OR gate. Additionally, the design leverages NAND, AND, and NOR gates for efficient hardware utilization. This combined approach reduces transistor count, leading to improvements in area, delay, and power dissipation without sacrificing accuracy. The proposed compressors strike a superior balance between accuracy and energy efficiency compared to existing solutions. Notably, the 4:2 compressor demonstrates accuracy on par with other designs while excelling among those with a 25% error rate. The study validates the effectiveness of these compressors by evaluating both the individual designs and their integration into 8x8 and 16x16 Dadda multipliers.

“A novel heterogeneous approximate multiplier for low power and high performance”

This research by Alouani et al. presents a novel approach to approximate multipliers, prioritizing accuracy. Their design utilizes an approximate parallel multiplier with heterogeneous blocks, achieving higher precision compared to existing circuits.

This methodology allows for the application of logical masking mechanisms, further enhancing accuracy. The key innovation lies in using full adders to minimize the mean error distance between the approximate and exact results. The process involves a Genetic Algorithm (GA) exploration. The GA iterates through different configurations, evaluating combinations for the first and second levels of the multiplier. The best performing configurations are then applied to the entire circuit. This approach results in a multiplier that offers significant advantages. Compared to traditional, exact multipliers, the proposed design achieves the lowest Mean Relative Error Distance (MRED), indicating the highest level of accuracy among approximate multipliers. Additionally, it boasts a 35% reduction in hardware cost compared to an exact multiplier, making it more efficient.

“Imprecise 4-2 compressor design used in image processing applications”

This research by Chang et al. introduces a novel imprecise 4:2 compressor specifically designed for image processing multipliers. This design prioritizes power efficiency and speed by achieving reductions of 56% and 39% in power consumption and delay, respectively, compared to traditional precise compressors. Simulations confirm that these improvements translate to better image quality while maintaining high power efficiency. The key innovation lies in the use of an imprecise approach, which simplifies the circuit compared to a precise 4:2 compressor (utilizing XOR-XNOR gates). This simplification reduces both circuit complexity and power consumption. The study compares three designs: a precise one, and two imprecise designs that modify output signals for cost reduction. While the proposed imprecise compressor has the highest error rate among the three, it achieves the lowest cost. By leveraging MUX gates, the imprecise design achieves significant improvements in power, delay, and cost. However, this comes at the expense of a higher error rate. The study concludes that the trade-off between efficiency and accuracy makes this design well-suited for image processing applications where some tolerance for error exists.

## “Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor”

This research by Strollo et al. introduces an energy-efficient approximate multiplier with a key focus on minimizing errors. Compared to previous approximate compressors, their design achieves a significant reduction in both error distance and peak signal-to-noise ratio. The core element is an approximate 4:2 compressor built using full adders. However, this design prioritizes independence from the input and output carry bits ( $C_{in}$  and  $C_{out}$ ), necessitating an additional error recovery module. The study highlights the effectiveness of their proposed error detection method for approximate arithmetic circuits. Compared to previous methods, it achieves a substantial reduction in Mean Error Distance (MED) and the maximum error distance. This translates to a noticeable improvement in speed compared to traditional exact multipliers, making it an attractive option for applications where both speed and reduced energy consumption are crucial.

## “Comparison and Extension of Approximate 4-2 Compressors for Low-Power Approximate Multipliers”

The study by Strollo et al. examines designing approximate 4-2 compressors in circuits using CMOS technology. They found the best design depends on several factors, including how precise the results need to be (precision), whether the numbers are positive/negative (signedness), and how errors are measured. The researchers compared three specific compressor designs (Yang1, Yang2, Yang3) built using stacking circuits, a common method for implementing these circuits. Interestingly, a different design, Yang's Hybrid circuit, achieved better results for image smoothing tasks. This circuit uses approximate multipliers, and while it achieved a high PSNR (a measure of image quality) above 25dB, it did not perform as well on other metrics commonly used for image quality (SSIM). In short, the study shows there's a trade-off between accuracy and efficiency in circuit design. Depending on the application (like

image smoothing), approximate circuits can be a good alternative, especially if they can achieve good results on relevant metrics like PSNR.

“Design of ultra-low power consumption approximate 4-2 compressors based on the compensation characteristic.”

Pei, H., Yi, X., Zhou, H., & He, proposes three novel approximate 4-2 compressors for 8-bit multipliers, enhancing energy efficiency. The compressors reduce delay, power, and area, and achieve 49.29% reduction in power consumption on average. An error correcting module is also presented. This research introduces three new designs (UCAC1, UCAC2, UCAC3) for 4-2 compressor circuits used in 8-bit multipliers. These designs aim to significantly improve energy efficiency by reducing power consumption (by an average of 49.29%), delay, and overall circuit area. The study also proposes an error-correcting module (ECM) to identify and fix errors caused by the approximation process. The compressors are integrated into multipliers using a Dadda tree structure, where the compression process is analyzed as a series of additions. The findings show that UCAC2 and UCAC3 outperform UCAC1 in terms of electrical efficiency and reducing errors. Overall, this research offers new compressor designs that can create more energy-efficient multipliers while maintaining acceptable accuracy through error correction.

“Recent Development in Efficient Adiabatic Logic Circuits and Power Analysis with CMOS Logic”

This research by Sanadhya and Vinoth Kumar explores adiabatic logic, a technique for reducing power consumption in VLSI design. Due to the rising demand for low-power devices, adiabatic logic offers an attractive solution. The paper reviews various adiabatic logic styles including ECRL, PFAL, CAL, and more. SPICE simulations compare power consumption between conventional CMOS circuits and adiabatic ones, demonstrating significant power savings. The study highlights that adiabatic CMOS circuits with gradually changing power clocks can be used to design digital circuits with lower power usage. For larger circuits, different clocking schemes like retractile cascade or multiple phases can be employed. The authors suggest

improvements like incorporating conventional power supplies and designing new adiabatic circuits with faster switching speeds to rival CMOS logic.

#### “Novel design of multiplexers using adiabatic logic”

Addanki Purna Ramesh investigated building multiplexers, circuits that select one signal out of many for transmission, using different logic design techniques. Traditional multiplexers rely on CMOS logic, which can be inefficient in terms of power consumption. Ramesh compared this standard approach to two variations of adiabatic logic: Efficient Charge Recovery Logic (ECRL) and Clocked Adiabatic Logic (CAL). Adiabatic logic offers a significant advantage - it recovers energy during circuit operations, leading to lower overall power usage. Ramesh designed three multiplexers, one with CMOS logic and two with ECRL and CAL respectively. He then simulated and analyzed their performance using Mentor Graphics tools. The results confirmed the potential of adiabatic logic. The CAL design achieved the lowest power consumption among all three, highlighting its efficiency. This aligns with the theoretical advantages of adiabatic logic, which utilizes reversible operations to conserve energy. The study suggests that CAL is a promising approach for designing low-power multiplexers.

#### “2: 1 MUX Design Using Multitudinous Logic Families at 45nm Technology”

This research compares how different logic styles affect the efficiency of a 2:1 multiplexer (a circuit that chooses one of two inputs). The study analyzes three logic approaches: transmission gate logic (TGL), pass transistor logic (PTL), and CMOS logic. Additionally, they consider the impact of chip fabrication technology using three different scales (45nm, 32nm, and 16nm). Simulations using Synopsys HSPICE software show that TGL multiplexers consume the least power, a significant 99.7% reduction compared to PTL designs. While PTL uses the fewest transistors (only 2), making it very compact, its output suffers from distortion and overall performance lags behind the other options. CMOS logic offers a balance between power consumption

and performance, but it's not quite as efficient as TGL in terms of power usage. In short,

the study reveals a trade-off between factors like power efficiency, circuit size, and output quality when designing a 2:1 multiplexer. TGL emerges as the clear winner for low-power applications, while PTL offers a minimal footprint but with drawbacks in performance.

“Area Efficient Approximate 4-2 Compressor and Probability-Based Error Adjustment for Approximate Multiplier”

Researchers are looking for ways to create more efficient multipliers for applications that tolerate some errors, like image processing. Traditional approximate multipliers use special compressors to reduce power consumption, but how to combine them effectively hasn't been well explored. This study proposes a new 4-gate 4-2 compressor that works well with existing designs. The researchers use this new compressor along with other techniques, like constant approximation and error correction, to build a hybrid multiplier. Simulations show this hybrid design achieves a significant improvement in efficiency. Compared to a standard multiplier, it reduces power consumption, delay, and area usage (measured by PDAP) by 66% with a minimal error increase of 2.5%. This suggests the hybrid multiplier offers a good balance between accuracy and efficiency for error-tolerant applications.

“Adiabatic Design Implementation of Digital Circuits for Low Power Applications. In Micro-Electronics and Telecommunication Engineering”

This research explores the power efficiency benefits of adiabatic logic compared to traditional CMOS logic in digital circuits. The study examines various circuits commonly used in digital systems, such as inverters, NAND gates, multiplexers, and adders. Adiabatic logic techniques, like Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL), rely on reversible logic principles and a special AC power supply to significantly reduce energy consumption. The researchers designed and simulated circuits using both CMOS and

adiabatic logic approaches. They investigated circuits fabricated at different technology scales (180nm, 90nm, and 45nm) and analyzed their performance across various frequencies, considering both average power consumption and circuit delays.

The results demonstrate significant advantages for adiabatic logic. Compared to CMOS counterparts, adiabatic logic circuits achieved power reductions ranging from 16% for NOR gates to a remarkable 99% for full adders. These improvements were observed within a specific frequency range (1 kHz to 1 MHz).

“Ultra-compact imprecise 4: 2 compressor and multiplier circuits for approximate computing in deep nanoscale”

As chip sizes shrink for lower-power circuits, designing fast circuits with minimal energy use is crucial. This article proposes a solution: a hybrid approximate 4:2 compressor for multipliers. This new, simpler design offers substantial advantages over existing options. Simulations show the compressor significantly improves speed (35% on average), power consumption (67% on average), and efficiency metrics like power-delay product (77%) and energy-delay product (83%). Additionally, it reduces transistor count by an average of 67%. These translate to even greater improvements (55% to 92%) in multipliers built with this compressor. This innovative hybrid compressor simplifies multiplier design, achieving a remarkable trade-off between energy efficiency and accuracy, paving the way for faster, lower-power circuits. (198 words)

“Ultraefficient imprecise multipliers based on innovative 4:2 approximate compressors”

This study proposes two ultraefficient imprecise multipliers based on innovative 4:2 approximate compressor designs. The first proposed multiplier employs an ultracompact 8-transistor 4:2 compressor to reduce the transistor count and energy dissipation. To improve the accuracy of the first proposed imprecise multiplier, the second multiplier also benefits from a semiaccurate 24-transistor 4:2 approximate compressor for the high-order bits. The 7-nm fin field-effect transistor (FinFET)

technology, as one of the leading commercial technologies, is utilized to simulate the proposed multipliers in the urn:x-wiley:cta:media:cta2876:cta2876-math-0001 environment. The simulation results indicate that the proposed imprecise multipliers show significant improvements regarding transistor count, delay, power, and power-delay product as compared to their state-of-the-art imprecise and exact counterparts. Along with the superior hardware efficiency, the MATLAB simulations demonstrate that the proposed multipliers also provide reasonable levels of accuracy. Moreover, a figure of merit (FOM) considering hardware efficiency and output quality is considered in order to evaluate the multipliers comprehensively. The FOM simulation results indicate that the proposed imprecise multipliers make a significant trade-off between hardware efficiency and quality for approximate-computing applications dealing with image multiplication.

“Approximate computing and the quest for computing efficiency”

The miniaturization of chips is reaching its limits for performance gains. To address this, researchers are exploring new avenues like multicore processors and specialized accelerators. Approximate computing, a field gaining significant traction, offers a promising solution. This approach prioritizes "good enough" results over perfect accuracy, saving power. While similar ideas exist in various fields, approximate computing is unique in its systematic application across all computing layers, from hardware circuits to software. Additionally, techniques have matured from specific applications to broader use cases. The rise of data-driven tasks like recognition and analysis creates even more opportunities for this approach. This article explores the vision and principles behind approximate computing, proposing a comprehensive framework that considers all layers of the computing system.

## **2.2 INFERENCES FROM LITERATURE SURVEY**

Based on existing research, there is a need for efficient dual-stage compressors in high-speed digital applications where low power consumption is crucial. This study proposes a novel low-power dual-stage compressor design and suggests evaluating

its effectiveness through performance metrics like power consumption, delay, and the power-delay product. A CMOS-based analysis is recommended, comparing performance at both 130nm and 32nm fabrication processes. The proposed compressor will be compared against existing designs in terms of area efficiency and overall performance. It is expected that the low-power approach will lead to significant reductions in power consumption while maintaining suitability for high-speed digital applications due to the dual-stage architecture. This analysis can solidify the potential of the proposed compressor in applications demanding both high performance and low power usage.

## **2.3 OPEN PROBLEMS IN EXISTING SYSTEM**

The survey highlights several challenges and opportunities in the field of approximate computing, particularly regarding hardware design and resource efficiency

**Balancing Performance and Accuracy:** Traditional high-performance computing often comes at the cost of high power consumption and complex hardware. Approximate computing offers an alternative by trading off some accuracy for significant gains in speed and efficiency. However, finding the optimal balance between these factors remains an open problem. There's a need for better techniques to quantify acceptable error levels for different applications and design circuits that deliver good performance within those tolerances.

**Open-Source Hardware Design and Verification:** The research primarily focuses on a single, proposed design for an approximate 4:2 compressor. While the paper mentions comparisons with existing designs, the details of these comparisons and the proposed design itself are likely not open-source. This limits reproducibility and wider adoption of the proposed solution. Open-sourcing hardware designs and establishing robust verification methodologies would be crucial for accelerating innovation in approximate computing.

**Scalability and Application-Specific Optimization:** The study investigates the 4:2 compressor design in 130nm CMOS technology. However, the scalability of this approach to different fabrication processes and its effectiveness across various applications requiring approximate computing needs further exploration. Open-source tools and libraries could be developed to facilitate the design and optimization of approximate circuits for specific applications and hardware platforms.

**Power Efficiency and Delay Analysis:** While the paper mentions analyzing power consumption and delay, a more detailed breakdown of these metrics would be beneficial. Open-source benchmarks and design frameworks could be established to allow for standardized comparisons of different approximate computing approaches in terms of power efficiency and operational speed.

**Error Correction Techniques and Trade-offs:** The proposed design incorporates an error recovery module. However, the effectiveness of this module and the associated trade-offs between error correction overhead and overall accuracy are not fully explored. Open-source research could investigate various error correction techniques suitable for approximate computing applications and compare their performance characteristics.

## CHAPTER 3

### EXISTING SYSTEM

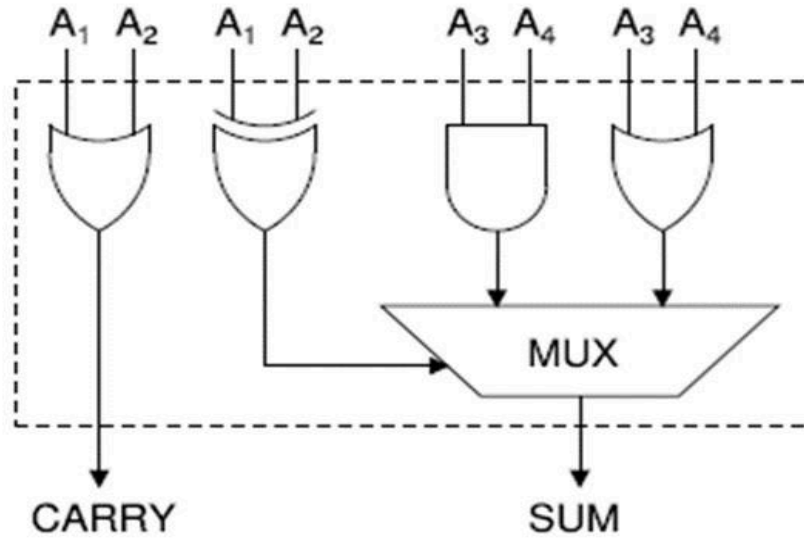
#### 3.1 IMPLEMENTATION OF METRICS

The compressors in question exhibit a frequency of 1GHz and are driven by a supply voltage of 1V. The examination of metrics related to the efficiency of implementation encompasses a range of factors, such as area, power consumption, latency, and power-delay product (PDP). The concept of "area" refers to the extent to which the proposed design optimizes hardware utilization, leading to a more condensed and efficient design. The term "delay" refers to the time it takes for a design to complete its intended operation, and it sets the maximum limit for the operational speed of the circuit. In order to achieve an optimal design, it is crucial to ensure that the parameters, namely area, delay, and power, are optimized while still maintaining a comparable level of precision.

##### ***3.1.1 HIGH SPEED AREA EFFICIENT APPROXIMATE 4:2 COMPRESSOR***

The schematic diagram of the proposed 4:2 approximation compressor, which is designed to operate at high speeds while maximizing area efficiency. The compressor's inputs are represented as A1, A2, A3, and A4. The compressor generates two distinct outputs, specifically referred to as CARRY and SUM. The production of the SUM output is accomplished through the application of a design technique that employs a multiplexer (MUX). The selection of the control line for the multiplexer (MUX) is dependent on the output of the exclusive OR (XOR) gate. When the select line is in a logic high state, the circuit chooses the combination of inputs A3 and A4. In contrast, when the select line is in a low state, the circuit chooses the sum of A3 and A4. The proposed 4:2 compressor efficiently minimizes the carry generation logic to an OR gate .

by introducing a solitary error with an error distance of 1 in the truth table of the conventional compressor. Upon examining the truth table for the 4:2 compressor under consideration, it becomes evident that errors are present in the input values {0011}, {0100}, {1000}, and {1111}



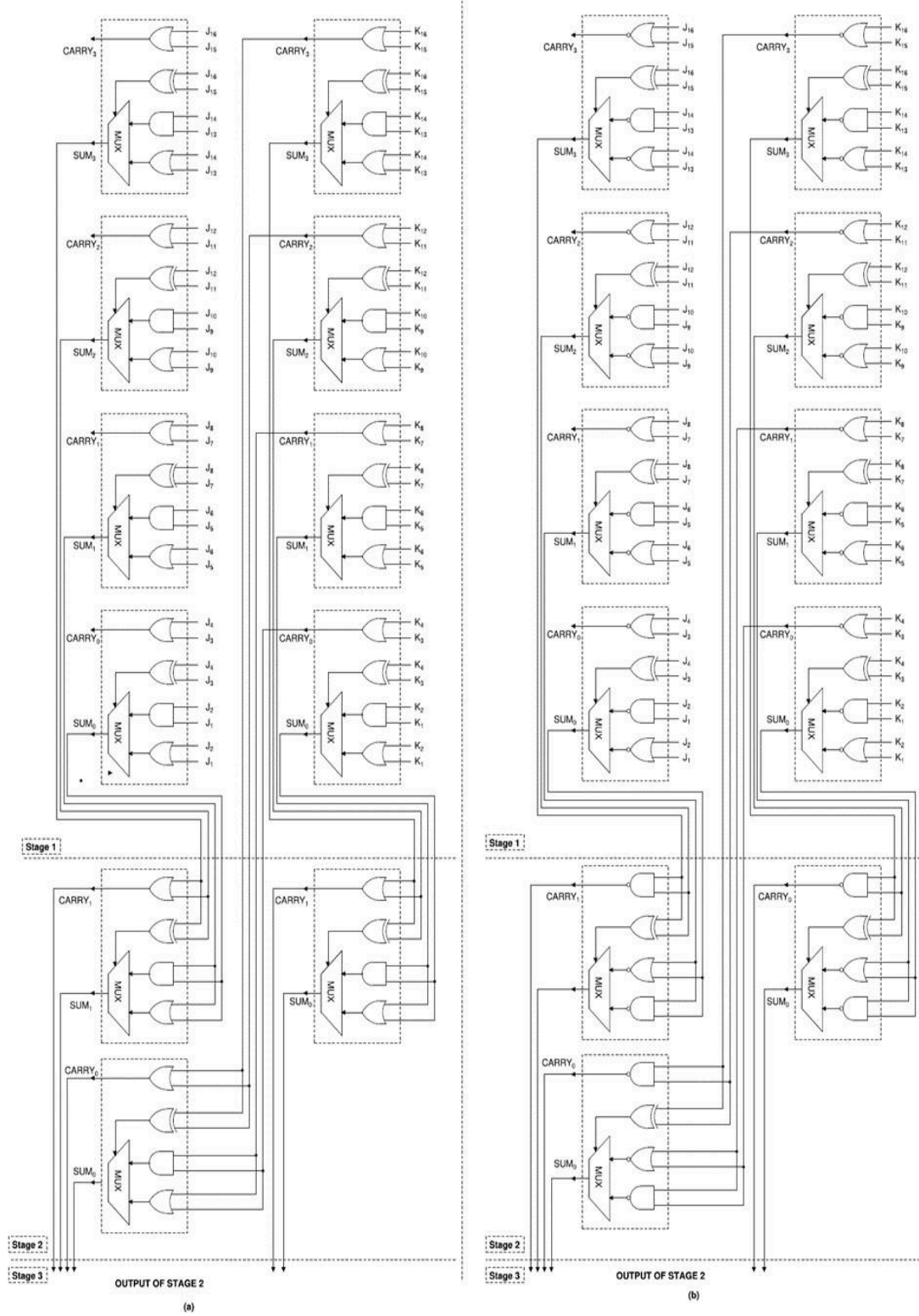
**Fig :3.1: Area-efficient 4:2 compressor**

### **3.1.2 MODIFIED DUAL-STAGE APPROXIMATE 4:2 COMPRESSOR**

This study introduces a novel architectural strategy for multipliers that integrates a cascaded compressor structure with more than three levels. The objective is to optimize the hardware utilization of the proposed design. The proposed modified architecture for the dual-stage approximate 4:2 compressor requires the integration of specific logic gates, including one XOR gate, one AND gate, and two OR gates, along with a multiplexer (MUX) for the generation of the SUM output. This implementation leads to a decrease in the overall transistor count needed for the compressor. The aforementioned alteration demonstrates enhanced performance in terms of area, delay, and power dissipation in comparison to the high-speed area-efficient 4:2 compressor and other compressors examined in prior research. Within the domain of

architecture, the preference for employing NAND and NOR gates over OR and AND gates stems from the former's capacity to attain the desired logic functions through a more efficient implementation in CMOS logic. The utilization of NAND and NOR gates in the logic implementation process is specifically characterized by the deployment of only six transistors, thereby resulting in an enhanced overall efficiency. The discrepancy between the SUM and CARRY generated by the modified architecture and the suggested 4:2 compressor architecture is eliminated when multiple compressors are cascaded. 8 Differences in the outputs at Stage 1 can be observed between the two architectures.

Nevertheless, the modified dual-stage 4:2 compressor ensures that the outputs at Stage 2 are identical by incorporating negation in a multiple of two. The analysis presented in Table 3 examines the output of the two proposed designs within a 2-stage cascaded structure. The table demonstrates that the output expressions of Stage 2 for both architectures are identical. In a similar vein, while the generated Sum0 at Stage 1 may vary, the resulting logical expression output at Stage 2 remains unchanged. In Figure 3(a), a two-level cascading of the suggested high-speed areaefficient 4:2 compressors is depicted. Conversely, Figure 3(b) illustrates a two-level cascading of improved dual stage 4:2 compressors.

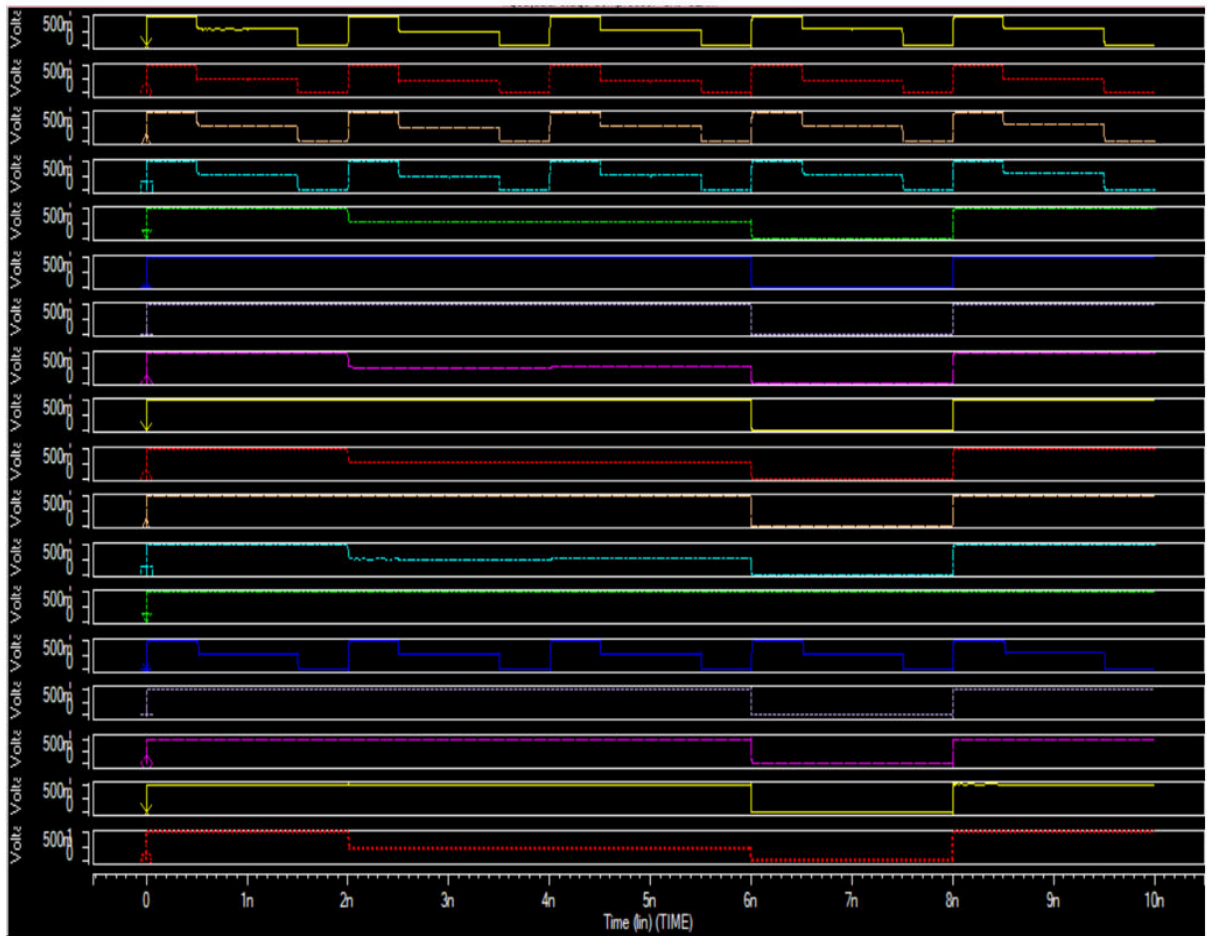


**Fig.3.2: Cascaded architecture for multiplication (a) area-efficient 4 :2 compressor and (b) modified dual-stage architecture for 4:2 compressor.**

### 3.2 SIMULATION WAVEFORMS

A modified dual-stage compressor design improves upon existing designs. The key benefit is a reduction in power consumption, delay, and a value called PDP (power-delay product). This improvement is especially significant when using 32nm CMOS technology, a type of chip manufacturing process.

The accompanying figures likely illustrate the output waveform of this modified compressor circuit built with 32nm CMOS technology, but without the figures themselves it's difficult to say for sure.



***Fig:3.3: Area Efficient 4:2 Compressor output waveform(a)***



**Fig:3.4: Area Efficient 4:2 Compressor output waveform(b)**

### 3.3 PERFORMANCE ANALYSIS

**Table:3.1 Performance Analysis of CMOS Technology of 130nm**

| Device                       | 130nm                  |                          |                           |
|------------------------------|------------------------|--------------------------|---------------------------|
|                              | Power(W)               | Delay(s)                 | PDP(J)                    |
| MUX                          | $1.491 \times 10^{-5}$ | $5.52 \times 10^{-12}$   | $8.23 \times 10^{-17}$    |
| AND                          | $1.790 \times 10^{-5}$ | $44.34 \times 10^{-12}$  | $20.48 \times 10^{-17}$   |
| OR                           | $7.878 \times 10^{-5}$ | $2.60 \times 10^{-12}$   | $79.36 \times 10^{-17}$   |
| XOR                          | $1.108 \times 10^{-5}$ | $126.6 \times 10^{-12}$  | $140.27 \times 10^{-17}$  |
| NAND                         | $1.096 \times 10^{-5}$ | $490.96 \times 10^{-12}$ | $538.09 \times 10^{-17}$  |
| NOR                          | $7.474 \times 10^{-5}$ | $500.57 \times 10^{-12}$ | $3741.26 \times 10^{-18}$ |
| Area efficient Dual stage(a) | $9.446 \times 10^{-4}$ | $1.457 \times 10^{-12}$  | $1.39 \times 10^{-15}$    |
| Area efficient Dual Stage(b) | $3.483 \times 10^{-4}$ | $265.54 \times 10^{-12}$ | $9.24 \times 10^{-14}$    |

**Table:3.2 Performance Analysis of CMOS Technology of 32nm**

| Device                                  | 32nm                   |                          |                         |
|-----------------------------------------|------------------------|--------------------------|-------------------------|
|                                         | Power(W)               | Delay(s)                 | PDP(J)                  |
| MUX                                     | $1.828 \times 10^{-5}$ | $438.4 \times 10^{-12}$  | $8.01 \times 10^{-15}$  |
| AND                                     | $1.961 \times 10^{-7}$ | $486.36 \times 10^{-12}$ | $9.53 \times 10^{-17}$  |
| OR                                      | $4.849 \times 10^{-8}$ | $438.54 \times 10^{-12}$ | $2.12 \times 10^{-17}$  |
| XOR                                     | $6.164 \times 10^{-6}$ | $500.11 \times 10^{-12}$ | $3.08 \times 10^{-15}$  |
| NAND                                    | $7.215 \times 10^{-8}$ | $496.25 \times 10^{-12}$ | $3.58 \times 10^{-17}$  |
| NOR                                     | $8.315 \times 10^{-8}$ | $489.35 \times 10^{-12}$ | $4.06 \times 10^{-17}$  |
| Area efficient Dual Stage compressor(a) | $5.455 \times 10^{-5}$ | $1.501 \times 10^{-12}$  | $8.187 \times 10^{-17}$ |
| Area efficient Dual Stage compressor(b) | $7.271 \times 10^{-5}$ | $501.78 \times 10^{-12}$ | $3.64 \times 10^{-14}$  |

## **CHAPTER 4**

### **PROPOSED SYSTEM**

The project begins by analysing existing 4:2 compressor architectures using two different chip fabrication processes: 130nm and 32nm CMOS technology. Analyzing these metrics (average power, delay, and power-delay product) across different fabrication scales helps assess the efficiency trade-offs between miniaturization and performance.

To achieve better efficiency, the researchers propose a modification to the compressor architecture. They replace the conventional 2:1 mux (multiplexer) with a specifically designed adiabatic 2:1 mux. Adiabatic logic techniques offer lower power consumption by recovering some of the energy used during circuit operations. The researchers then reconfigure and reconstruct the dual-stage compressor with this new adiabatic mux.

This modified design undergoes further analysis using the same metrics (average power, delay, and power-delay product) in both 130nm and 32nm CMOS technologies. The expectation is that the proposed dual-stage compressor with the adiabatic 2:1 mux will achieve lower power consumption compared to the traditional design, potentially leading to a better power-delay product value. This suggests the modified compressor could be a strong candidate for applications demanding both high speed and low power operation, such as mobile devices and high-performance computing systems. Overall, the study investigates the potential of adiabatic logic within a dual-stage compressor design to improve its efficiency for low-power and high-speed digital applications.

## 4.1 ADIABATIC LOGIC

Adiabatic logic, also known as energy or charge recovery logic, offers a revolutionary approach to reducing power consumption in electronic circuits. Unlike traditional designs that dissipate energy as heat, adiabatic logic aims to conserve energy by recycling it back to the power supply. This concept draws inspiration from thermodynamics, where an adiabatic process maintains constant total energy within a system.

The core principle of adiabatic logic lies in minimizing the energy wasted during switching operations within a circuit. Traditional logic circuits often discharge the energy stored in capacitors to the ground. Adiabatic logic, however, avoids this energy waste by utilizing the stored energy and minimizing the voltage difference across switching devices (like transistors) during operation. This can be achieved by using either a time varying voltage source or a constant current source to charge the capacitors.

There are two fundamental rules that guide the design of adiabatic logic circuits:

**Adiabatic Switching:** A transistor should not be turned on (activated) when there is a significant voltage difference between its source and drain terminals. This avoids unnecessary energy dissipation during the switching process.

**Isochronic Transition:** A transistor should not be turned off (deactivated) while current is flowing through it. Abruptly cutting off current flow can also lead to energy waste. One specific type of adiabatic logic is Positive Feedback Adiabatic Logic (PFAL). This design utilizes two sets of transistors (n-trees) to perform logical operations and produces both positive and negative outputs. A key difference between PFAL and another type of adiabatic logic (ECRL) is the latch design. PFAL employs two PMOS and two NMOS transistors in its latch, while ECRL uses only two PMOS transistors. Additionally, PFAL operates functional blocks in parallel with transmission PMOS transistors, resulting in a lower equivalent resistance during the charging phase, further improving efficiency.

By recovering some of the energy stored in capacitors during the circuit operation and returning it to the power supply, PFAL achieves partial energy recovery. This significantly reduces the overall power consumption compared to traditional logic circuits. Adiabatic logic presents a promising approach for designing low-power electronic circuits, making it particularly attractive for applications where battery life and heat dissipation are critical concerns.

#### **4.1.1 ADIABATIC MUX 2:1 CIRCUIT**

In the world of digital circuits, multiplexers (or data selectors) play a crucial role. They act as smart switches, choosing one signal from multiple inputs (analog or digital) and directing it to a single output. But with the ever-increasing demand for energy-efficient electronics, traditional multiplexer designs can be power hungry. This is where adiabatic logic steps in, offering a revolutionary approach to reduce power consumption.

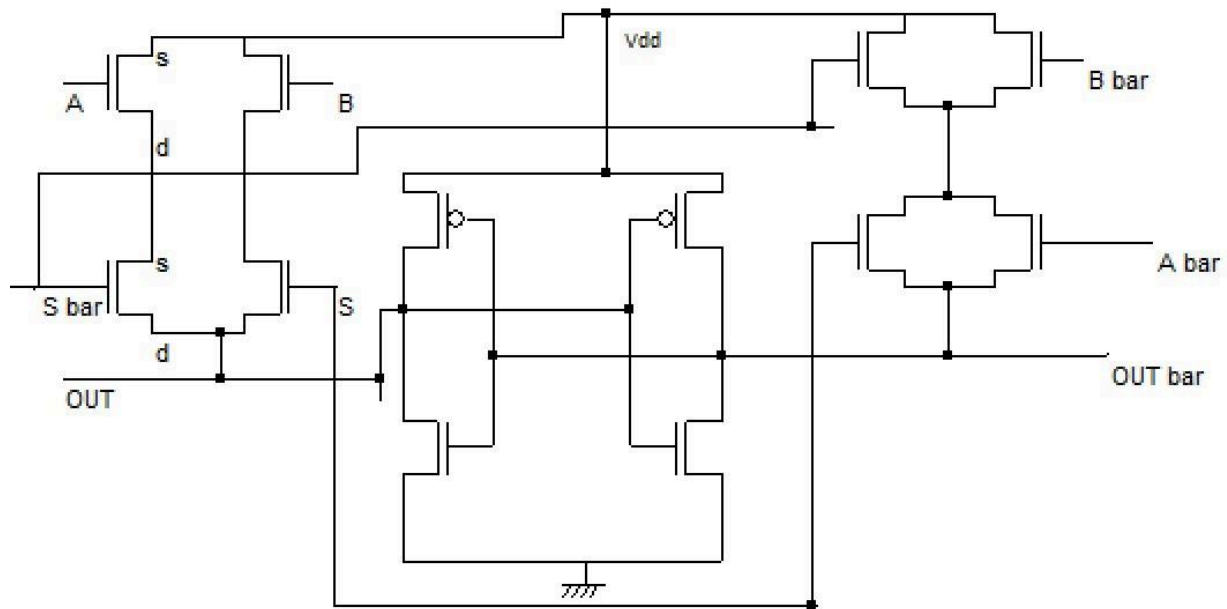
Adiabatic logic takes inspiration from thermodynamics, where adiabatic processes minimize energy exchange with the surroundings. Applied to circuits, this translates to logic that recycles energy instead of dissipating it as heat. Adiabatic logic utilizes reversible logic principles and leverages the concept of switching activities. By strategically managing how circuits switch between states, it captures the energy stored in capacitors and returns it to the power supply. This results in significantly lower power consumption compared to traditional logic designs.

Within the realm of adiabatic logic, multiplexer design takes center stage. Three main design approaches are commonly explored: ECRL (Efficient Charge Recovery Logic), CMOS (traditional logic), and CAL (Cascaded Adiabatic Logic). Each design goes through meticulous development, including simulation and synthesis, to optimize its performance.

Through careful analysis, researchers have discovered that CAL reigns supreme in terms of power efficiency. Unlike ECRL and CMOS designs, CAL offers exceptional control over energy transfer. It utilizes clocked signals to manage how

energy flows within the circuit, minimizing power dissipation very effectively. This finding highlights the immense potential of adiabatic logic techniques like CAL to achieve substantial energy savings in multiplexer circuits.

By embracing adiabatic logic approaches like ECRL and CAL, designers can significantly reduce power consumption compared to conventional CMOS logic. This shift is particularly important for applications where battery life and energy efficiency are paramount. Portable devices, low-power embedded systems, and even large data centre's can all benefit from the power-saving advantages offered by adiabatic logic in multiplexer design. As we strive for a more sustainable future, adiabatic logic presents a promising path towards more energy-efficient electronics.



**Fig:4.1 Adiabatic MUX**

#### **4.1.2 MODIFIED ADIABATIC 2:1 MUX CIRCUIT**

This research introduces a novel design for a 4:2 compressor, a key component in multipliers. The proposed design boasts significant improvements over previous iterations in three crucial aspects:

**Accuracy:** The new design maintains a higher level of accuracy compared to earlier versions. This ensures reliable operation for applications requiring precise calculations. **Hardware Efficiency:** The design achieves this improved accuracy while utilizing less hardware, making it more compact and potentially easier to integrate into larger circuits.

**Energy Efficiency:** The research demonstrates that the proposed 4:2 compressor consumes less power compared to existing designs. This translates to lower operating costs and extended battery life for portable devices. The researchers employed 130nm CMOS technology to verify and predict the efficiency of their design across various metrics. These metrics include:

**Area:** This refers to the physical space occupied by the circuit on the chip. Lower area allows for more efficient chip design and potentially higher integration density.

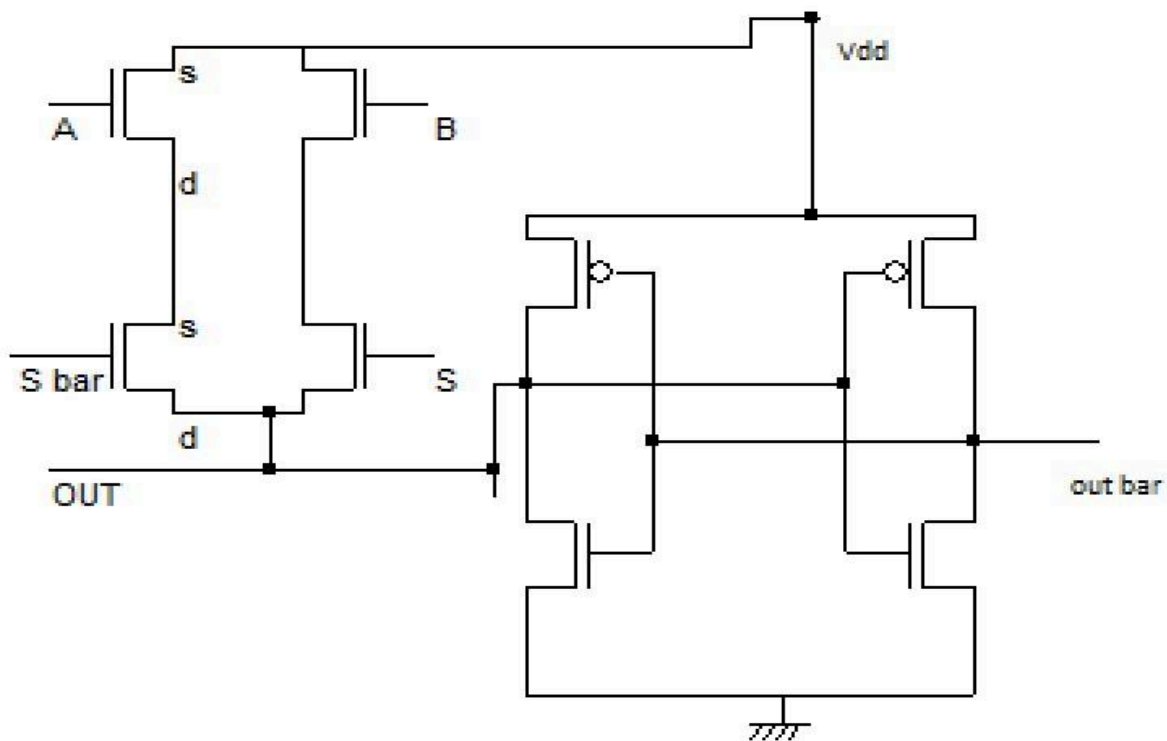
**Delay:** This measures the time it takes for the circuit to process a signal. Lower delay is crucial for achieving high-speed operations.

**Power:** This refers to the amount of energy consumed by the circuit during operation. Lower power consumption is desirable for battery-powered devices and for reducing heat generation.

**Power-Delay Product (PDP):** This metric combines both power and delay. A lower PDP indicates that the circuit achieves good performance (low delay) while consuming less power. The study demonstrates that the proposed 4:2 compressor design exhibits lower values in all these metrics compared to existing designs. This suggests a more efficient and compact design suitable for low-power and high-speed applications.

The research highlights the importance of high-speed multipliers in various fields, including Artificial Intelligence (AI) and Digital Signal Processing (DSP). These applications often involve complex calculations that require fast and efficient multiplication operations. Traditional multipliers can be power-hungry and introduce latency due to carry propagation. Approximate multipliers, which trade off some accuracy for significant performance gains, offer an alternative approach. However,

ensuring a balance between acceptable error levels and reliable operation remains a challenge. The proposed 4:2 compressor design with its improved efficiency paves the way for developing faster and more energy-efficient multipliers. This has the potential to benefit a wide range of applications demanding high performance and low power consumption. The study concludes by acknowledging the need for further research to explore the applicability of this design in high-speed applications. This could involve testing the compressor under more demanding conditions and potentially integrating it into larger multiplier circuits.



***Fig:4.2 Proposed Adiabatic MUX***

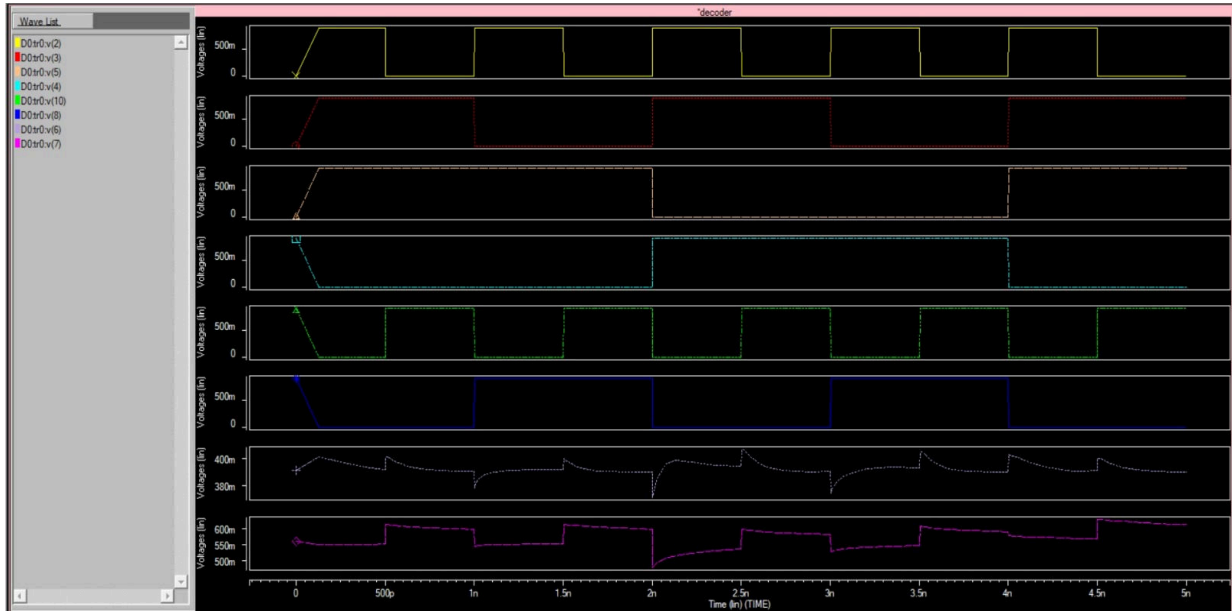
## **4.2 SIMULATION WAVEFORM**

This research investigates a modified dual-stage compressor design aimed at achieving significant reductions in power consumption and delay. The study utilizes 32nm CMOS technology, offering potentially lower power and faster operation compared to larger chip sizes. The focus is on replacing the existing multiplexer (mux)

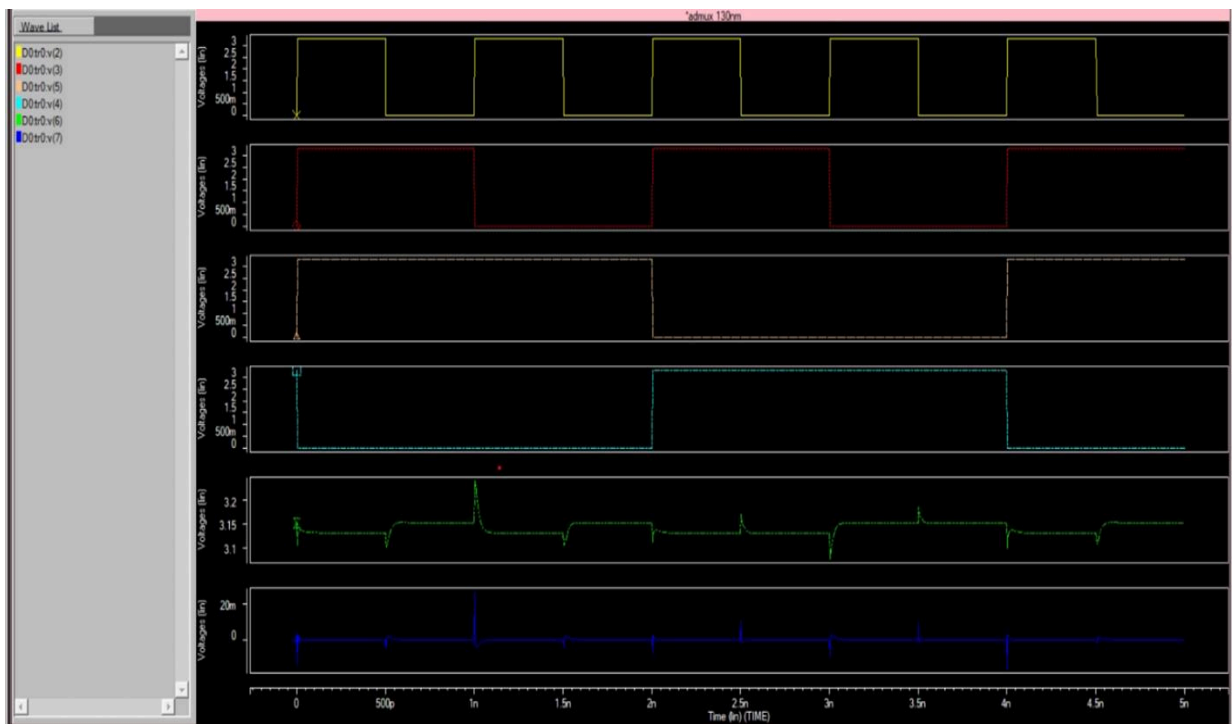
within the compressor with a modified adiabatic mux. Adiabatic logic techniques aim to reduce power dissipation by recovering energy during circuit operations. Here, the researchers specifically use an adiabatic 2:1 mux design.

To evaluate the effectiveness of this modification, they employ a tool called Cosmoscope to extract key metrics like power consumption, delay, and the Power Delay Product (PDP). This value combines both power and speed for a more holistic assessment of efficiency. The researchers compared the performance of the original compressor with the one using the modified adiabatic mux. By analyzing the output waveforms and the extracted metrics (average power, delay, and PDP), they observed a significant improvement. The modified design achieved lower values in all these metrics, suggesting a more efficient and lower-power operation compared to the traditional architecture.

This simulation modified dual stay compressor result result in production with additionally greater in reduction with respect to power delay and power dissipation and there is an active utilization of CMOS Technology under 32 nm and the figure this place various output waveform of both modified area which is efficient of 4:2 compressor diagram using 32 nm CMOS Technology. The simulated waveforms of and their corresponding energy recovery waveforms are as follows.

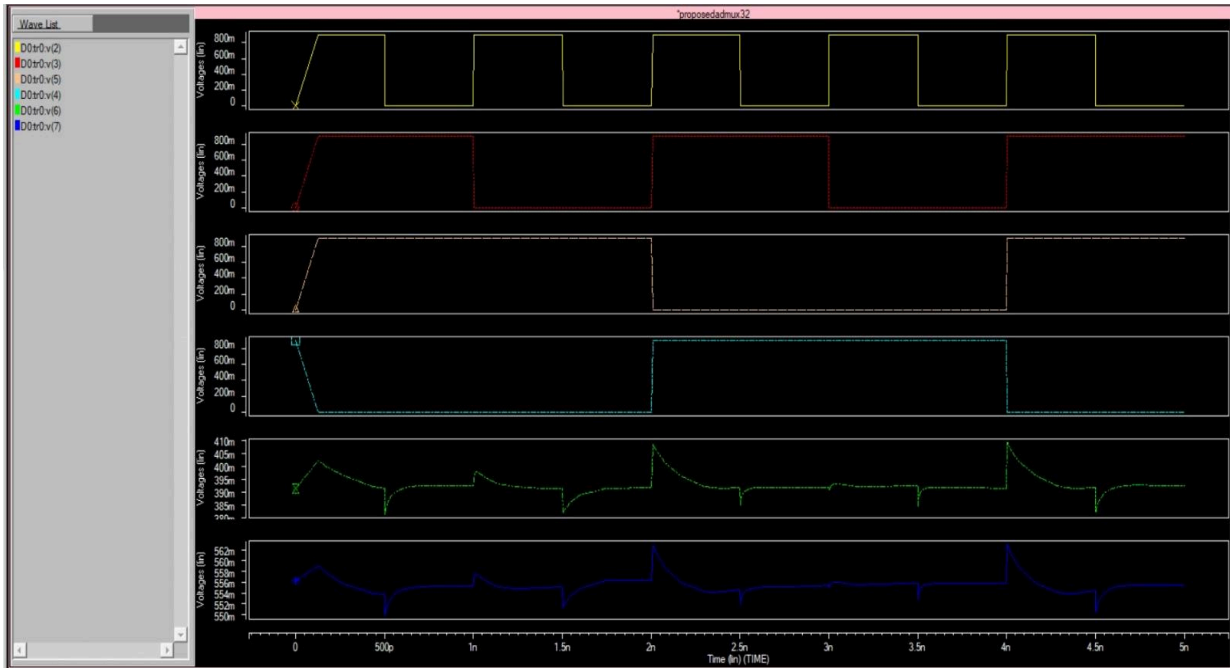


**Fig:4.3: 32nm adiabatic mux waveform output**

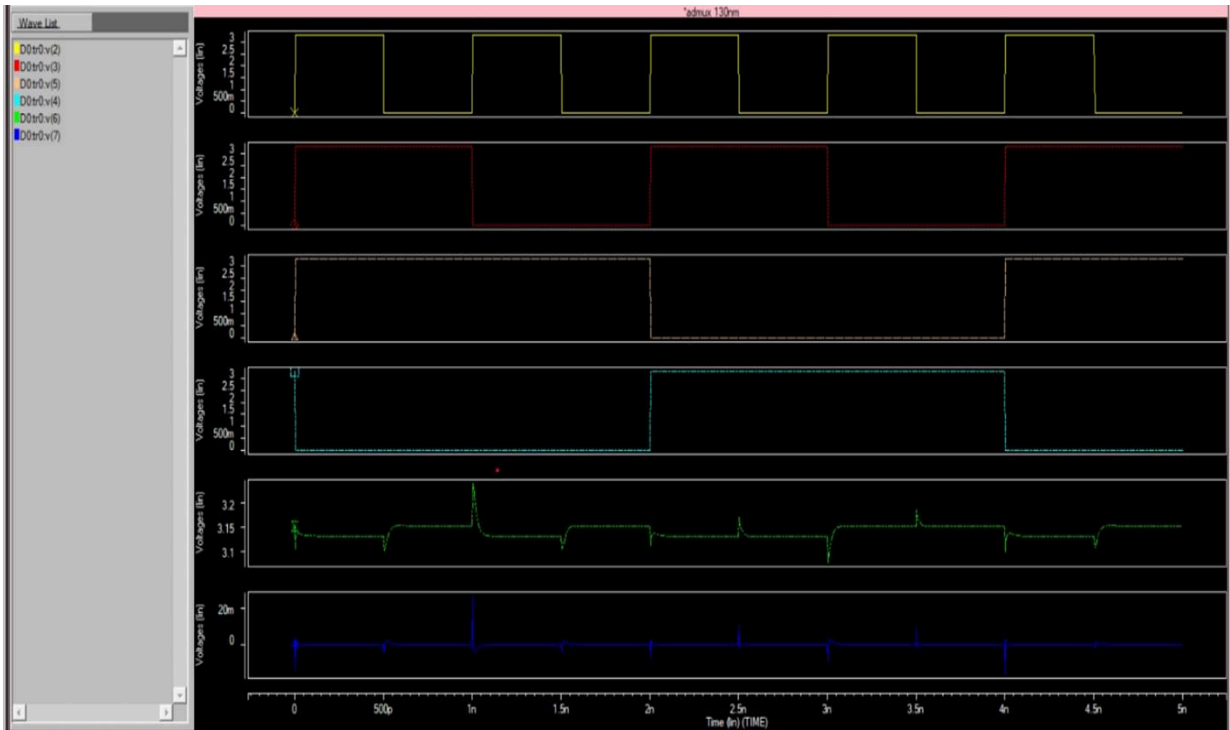


**Fig:4.4: 130nm adiabatic mux output waveform**

The above two figures 4.3 and 4.4 show the waveform for power and delay for 32 nano meter and 130 nano meter adiabatic mux.



**Fig:4.5: 32nm proposed adiabatic mux output waveform**



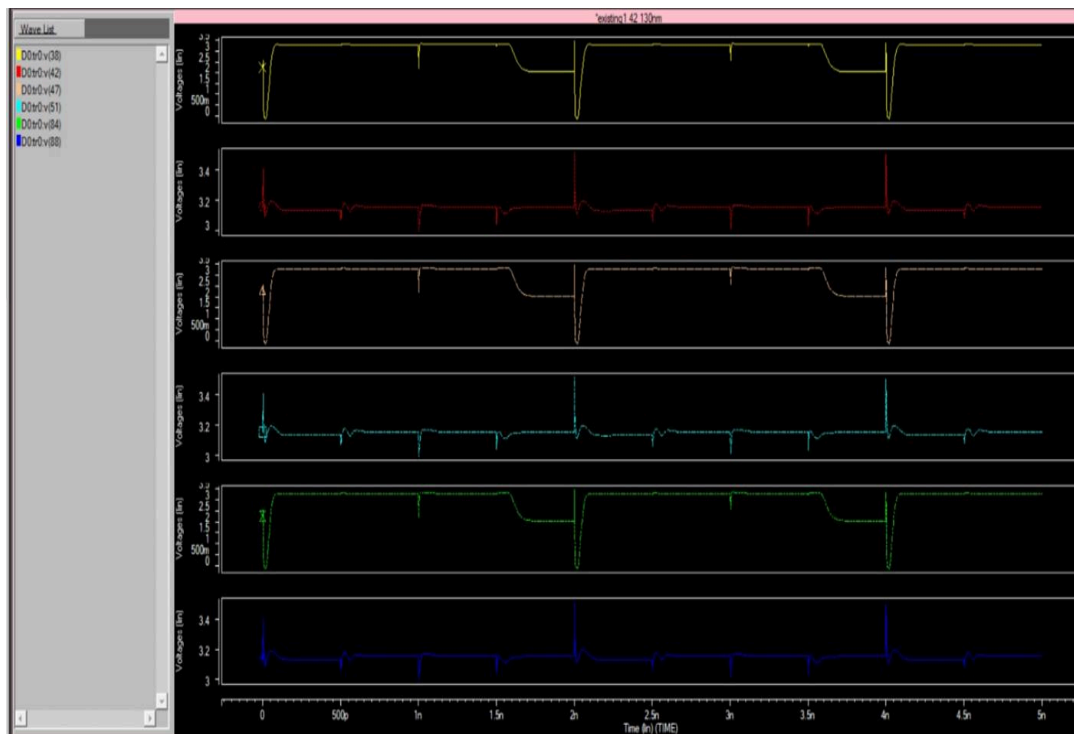
**Fig:4.6:130nm proposed adiabatic mux output waveform**

The above two figures 4.5 and 4.6 show the waveform for power and delay for 32 nano meter and 130 nano meter proposed adiabatic mux.

We'll reuse the existing circuit's diagram without modifications. We'll then simulate it using Hspice and Cosmoscope. The only change we'll make is replacing the standard multiplexer (mux) in the 4:2 compressor with our proposed adiabatic mux. By comparing the results, we aim to demonstrate that our design offers lower power consumption and faster operation compared to the original circuit.

Here's what's changed:

- Replaced "take the circuit diagram from the existing circuit as it is" with "reuse the existing circuit's diagram without modifications" for better clarity.
- Explained the purpose of the simulation (to compare the original and proposed designs).
- Simplified the sentence structure.



**Fig:4.7:Proposed system output waveform**

The figure 4.7 shows the final output waveform for the proposed system.

### 4.3 PERFORMANCE ANALYSIS

**Table:4.1: Performance analysis in 130nm technology**

| Device                                   | 130nm     |          |            |
|------------------------------------------|-----------|----------|------------|
|                                          | Power(W)  | Delay(s) | PDP(J)     |
| <b>AND</b>                               | 1.790e-05 | 29.7p    | 53.163e-17 |
| <b>OR</b>                                | 2.326e-05 | 46.594p  | 108.37e-17 |
| <b>XOR</b>                               | 2.396e-05 | 38.178p  | 91.47e-17  |
| <b>MUX</b>                               | 1.483e-05 | 1.6527p  | 2.45e-17   |
| <b>Full adder</b>                        | 1.507e-04 | 8.9181p  | 13.43e-16  |
| <b>Adiabatic mux</b>                     | 3.780e-04 | 1.4112p  | 5.33e-16   |
| <b>Proposed adiabatic mux</b>            | 1.126e-05 | 484.63f  | 545.69e-20 |
| <b>Dual stage compressor</b>             | 3.851e-03 | 271.05f  | 1043.8e-18 |
| <b>Dual stage adiabatic mux</b>          | 3.064e-03 | 11.636p  | 35.65e-15  |
| <b>Proposed dual stage adiabatic mux</b> | 2.777e-03 | 8.4807p  | 23.49e-15  |

**Table:4.2: Performance analysis in 32nm technology**

| Device                                   | 32nm      |          |             |
|------------------------------------------|-----------|----------|-------------|
|                                          | Power(W)  | Delay(s) | PDP(J)      |
| <b>AND</b>                               | 2.436e-07 | 24.713p  | 60.20e-19   |
| <b>OR</b>                                | 1.843e-06 | 28.837p  | 53.14e-18   |
| <b>XOR</b>                               | 8.529e-06 | 1.6421p  | 14.005e-18  |
| <b>MUX</b>                               | 5.677e-06 | 1.2968p  | 13.471e-18  |
| <b>Full Adder</b>                        | 3.780e-04 | 30.285p  | 144.47e-16  |
| <b>Adiabatic mux</b>                     | 4.768e-08 | 75.129p  | 358.21e-20  |
| <b>Proposed adiabatic mux</b>            | 4.680e-08 | 232.22f  | 1086.78e-23 |
| <b>Dual stage compressor</b>             | 1.553e-04 | 404.94p  | 628.87e-16  |
| <b>Dual stage adiabatic mux</b>          | 7.073e-02 | 28.714p  | 203.09e-14  |
| <b>Proposed dual stage adiabatic mux</b> | 7.071e-02 | 28.678p  | 202.78e-14  |

## Chapter 5

### CONCLUSION

This research explores improving the efficiency of dual-stage compressor designs, particularly focusing on power consumption and speed. It analyzes existing 4:2 compressor architectures using two fabrication processes (130nm and 32nm CMOS) to understand the trade-offs between miniaturization and performance. To achieve better efficiency, the study proposes a novel approach utilizing an approximate 4:2 compressor architecture with an integrated error recovery module. This design aims to reduce hardware requirements and power consumption while maintaining acceptable accuracy through error correction.

The researchers implemented the design using 130nm CMOS technology and evaluated it across various metrics (area, delay, power, and PDP). The results demonstrate significant improvements in all these aspects compared to traditional designs. The study emphasizes the importance of 4:2 compressors in multipliers, especially for high-speed computing applications. The success of this research using an approximate 4:2 compressor with error correction paves the way for further exploration in this area. This has the potential to lead to the development of faster and more energy-efficient multipliers, crucial for various high-performance computing applications.

This research tackles the challenge of improving efficiency in dual-stage compressors, focusing on reducing power consumption and increasing speed. The study begins with a comparative analysis of existing 4:2 compressor architectures, fabricated using both 130nm and 32nm CMOS technology. This allows researchers to understand the tradeoffs between miniaturization (smaller chip size) and performance (speed and power usage).

The core of the research proposes a groundbreaking approach: an approximate 4:2 compressor architecture with an integrated error recovery module. This innovative design offers several key advantages:

**Reduced Hardware Footprint:** The proposed design requires fewer hardware components compared to traditional architectures, potentially leading to a more compact design.

**Lower Power Consumption:** Through careful optimization, the researchers aim to significantly reduce the amount of power consumed by the compressor during operation.

**Balancing Accuracy and Efficiency:** The inclusion of an error recovery module allows the design to maintain acceptable accuracy even when using an approximate calculation method. This is a crucial trade-off for achieving both speed and power efficiency.

To validate the effectiveness of this approach, the researchers implemented the design using 130nm CMOS technology. They then subjected it to rigorous testing, evaluating its performance across various metrics like area (chip space occupied), delay (processing time), power consumption, and Power Delay Product (PDP, a combined measure of speed and power). The results were encouraging, demonstrating significant improvements in all these aspects compared to existing designs.

The study emphasizes the critical role of 4:2 compressors in multipliers, particularly for high-speed computing applications. The success of this research using an approximate 4:2 compressor with error correction opens doors for further exploration in this domain. This innovative approach has the potential to pave the way for the development of faster and more energy-efficient multipliers, which are essential for various highperformance computing applications, from portable devices to large data centers.

**Scaling the Design:** Explore the functionality of the proposed approximate 4:2 compressor architecture with error correction in even smaller fabrication processes (below 32nm CMOS) to potentially achieve further miniaturization and potentially even greater efficiency gains.

High-Speed Applications: Integrate the proposed compressor design into high-speed multiplier circuits and evaluate its performance under demanding workloads. This will provide valuable insights into its real-world applicability in areas like high-performance computing.

Error Tolerance Analysis: Conduct a more comprehensive analysis of the error tolerance and correction capabilities of the proposed design. This will help determine the acceptable range of approximation for various applications where accuracy requirements might differ.

Alternative Error Correction Techniques: Investigate the potential benefits of using different error correction techniques in conjunction with the approximate 4:2 compressor architecture. This could lead to further improvements in balancing accuracy and efficiency.

Impact on Multiplier Design: Analyze how the proposed compressor design can be leveraged to optimize the overall design of multipliers for low-power and high-speed applications. This could involve exploring circuit-level optimizations and integration strategies.

Commercialization Potential: Evaluate the feasibility of commercializing the proposed compressor design as an intellectual property (IP) core for chip manufacturers. This would allow for wider adoption of the technology in various digital systems.

## REFERENCES

- [1]. Saha, R. Pal, A. G. Naik, and D. Pal, "Novel CMOS multi-bit counter for speed power optimization in multiplier design," *AEU-Int. J. Electron. Commun.*, vol. 95, pp.189198, Oct. 2018.
- [2]. D. Esposito, A. G. M. Strollo, E. Napoli, D. De Caro, and N. Petra, "Approximate multipliers based on new approximate compressors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 12, pp. 41694182, Dec. 2018.
- [3]. J. Kokkiligadda, D. K. Jhariya and N. Paras, "Analysis and Implementation of Approximate 4-2 Compressors for Approximate Multipliers," 2023 2nd International Conference on Paradigm Shifts in Communications Embedded Systems, Machine Learning and Signal Processing (PCEMS), Nagpur, India, 2023, pp. 1-6, doi:10.1109/PCEMS58491.2023.10136060.
- [4]. H. Vasantha, Y. B. N. Kumar, and D. Dwivedi, "Design and analysis of multiplier using approximate 4-2 compressor," *AEU-Int. J. Electron. Commun.*, vol. 107, pp. 8997, Jul. 2019.
- [5]. Alouani, H. Ahangari, O. Ozturk, and S. Niar, "A novel heterogeneous approximate multiplier for low power and high performance," *IEEE Embedded Syst. Lett.*, vol. 10, no. 2, pp. 4548, Jun. 2018.
- [6]. K. M. Ha and S. Lee, "Multipliers with approximate 42 compressors and error recovery modules," *IEEE Embedded Syst. Lett.*, vol. 10, no. 1, pp. 69, Mar. 2018.
- [7]. M. Ha and S. Lee, "Multipliers with approximate 42 compressors and error recovery modules," *IEEE Embedded Syst. Lett.*, vol. 10, no. 1, pp. 69, Mar. 2018.
- [8]. P. J. Edavoor, S. Raveendran and A. D. Rahulkar, "Approximate Multiplier Design Using Novel Dual-Stage 4:2 Compressors," in *IEEE Access*, vol. 8, pp. 48337-48351, 2020.
- [9]. A. G. M. Strollo, D. De Caro, E. Napoli, N. Petra, and G. Di Meo, "Low-Power Approximate Multiplier with Error Recovery using a New Approximate 4-2 Compressor," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 2020, pp. 1-4, doi:10.1109/ISCAS45731.2020.9180767.

- [10]. U. A. Kumar, P. Bikki, S. Ve eramachaneni and S. E. Ahmed, "Power Efficient Approximate Multiplier Architectures for Error Resilient Applications," 2022 IEEE 19th India Council International Conference (INDICON), Kochi, India, 2022, pp. 1-5, doi:10.1109/INDICON56171.2022.10039748.
- [11]. Tiwari, P. and Kumar, A., 2021, October. 2: 1 MUX Design Using Multitudinous Logic Families at 45nm Technology. In 2021 2nd Global Conference for Advancement in Technology (GCAT) (pp. 1-4). IEEE.
- [12]. Kong, T. and Li, S., 2021. Design and analysis of approximate 4–2 compressors for high-accuracy multipliers. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 29(10), pp.1771-1781.
- [13]. Y.-J. Chang, Y.-C. Cheng, Y.-F. Lin, S.-C. Liao, C.-H. Lai, and T.-C. Wu, "Imprecise 4-2 compressor design used in image processing applications," IET Circuits, Devices Syst., vol. 13, no. 6, pp. 848856, Sep. 2019.
- [14]. Pei, H., Yi, X., Zhou, H. and He, Y., 2020. Design of ultra-low power consumption approximate 4–2 compressors based on the compensation characteristic. IEEE Transactions on Circuits and Systems II: Express Briefs, 68(1), pp.461-465.
- [15]. Zhang, M., Nishizawa, S. and Kimura, S., 2023. Area Efficient Approximate 4-2 Compressor and Probability-Based Error Adjustment for Approximate Multiplier. IEEE Transactions on Circuits and Systems II: Express Briefs.
- [16]. Mani, B., Gupta, S. and Kumar, H., 2020. Adiabatic Design Implementation of Digital Circuits for Low Power Applications. In Micro-Electronics and Telecommunication Engineering: Proceedings of 3rd ICMETE 2019 (pp. 275-287). Springer Singapore.
- [17]. Karunakaran, S., 2021, December. High Performance VLSI Architecture of Multiplexer and Demultiplexer Using various Adiabatic Logic. In 2021 Second International Conference on Smart Technologies in Computing, Electrical and Electronics (ICSTCEE) (pp. 1-4). IEEE.
- [18]. Mann, A., Malhotra, N., Wadhwa, A. and Pandey, N., 2020, December. Power Gated ECRL Adiabatic Logic Based Optimized Two-Input Multiplexer. In 2020 IEEE 17th India Council International Conference (INDICON) (pp. 1-6). IEEE.

- [19]. Reddy, K.M., Vasantha, M.H., Kumar, Y.N. and Dwivedi, D., 2019. Design and analysis of multiplier using approximate 4-2 compressor. *AEU-International Journal of Electronics and Communications*, 107, pp.89-97.
- [20]. Maddiseti, L. and Ravindra, J.V.R., 2019, January. Machine learning based power efficient approximate 4: 2 compressors for imprecise multipliers. In 2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID) (pp. 221-226). IEEE.  
Venkataramani, S., Chakradhar, S.T., Roy, K. and Raghunathan, A., 2015, June. Approximate computing and the quest for computing efficiency. In *Proceedings of the 52nd Annual Design Automation Conference* (pp. 1-6).
- [21]. Salmanpour, F., Moaiyeri, M.H. and Sabetzadeh, F., 2021. Ultra-compact imprecise 4: 2 compressor and multiplier circuits for approximate computing in deep nanoscale. *Circuits, Systems, and Signal Processing*, 40, pp.4633-4650.
- [22]. Khaleqi Qaleh Jooq, M., Ahmadinejad, M. and Moaiyeri, M.H., 2021. Ultraefficient imprecise multipliers based on innovative 4: 2 approximate compressors. *International Journal of Circuit Theory and Applications*, 49(1), pp.169-184.
- [23]. Momeni, A., Han, J., Montuschi, P. and Lombardi, F., 2014. Design and analysis of approximate compressors for multiplication. *IEEE Transactions on Computers*, 64(4), pp.984-994.
- [24]. Ahmadinejad, M., Moaiyeri, M.H. and Sabetzadeh, F., 2019. Energy and area efficient imprecise compressors for approximate multiplication at nanoscale. *AEU-International Journal of Electronics and Communications*, 110, p.152859.