

BIOSENSING BASED ON JUNCTIONLESS MOSFET FOR HEALTHCARE APPLICATION

Submitted in partial fulfillment of the requirements for the award of

**Bachelor of Engineering Degree in
Electronics and Communication Engineering**

By

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**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
SCHOOL OF ELECTRICAL AND ELECTRONICS**

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

JEPPIAAR NAGAR, RAJIV GANDHI SALAI, CHENNAI - 600 119.

SEPTEMBER 2021



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

BONAFIDE CERTIFICATE

This is to certify that this Professional Training Report is the bonafide work of V. Gayathri (39130140) and E. Swathi (39130459) who carried out project entitled "BIOSENSING BASED ON JUNCTIONLESS MOSFET FOR HEALTHCARE APPLICATIONS" under my supervision from JUNE 2022 to SEPTEMBER 2022.

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DECLARATION

I, Gayathri. V and Swathi. E hereby declare that the Professional Training Report on "Biosensing Based On Junction Less MOSFET for healthcare application" done by us under the guidance of Dr. M . Sumathi M.E., Ph.D. at Sathyabama Institute of Science and Technology is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

DATE: 20.04.2023

PLACE: CHENNAI

SIGNATURE OF THE CANDIDATE

Handwritten signatures of the candidates, Gayathri V and Swathi E, in blue ink.

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ABSTRACT

The Proposed work deals about mathematical modelling to be obtained for the surrounding gate Junction less Field Effect Transistor that can be used in biosensor applications. The Semiconductor device analyzed here employs surrounding gate junction less MOSFETs made of two dissimilar materials.

The main objective of the surrounding gate is to identify the protein level in human cells. This model introduces novel dual material structure embedded with a nanocavity to make it suitable for biosensing applications. The biosensor sensitivity of the device can be analyzed and the analysis can be performed using MATLAB.

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CHAPTER 1

INTRODUCTION

MOSFET is a potential and promising device, and is highly dependable for the analog and digital circuits. As a transistor, it amplifies the power consumption in a circuit. Of late, Short channel effect is a major problem, encountered in nanometer IC scaling size. Short Channel effect is caused by the electric field lines, which propagate between source and drain affecting the control of channel region of the gate. Drain Induced Barrier Lowering (DIBL) is one of such effects, occurring due to increase in drain voltage at shorter channel length. This is identified in the depletion region with the growth of the body size resulting an extension of the gate. The MOSFET is a unipolar device since the conduction path is established between the source and drain, and this area is commonly referred to as the Channel. Gate bias voltage controls the width of the channel. The gate of the MOSFET is basically divided from the full-body by insulating the layer. The input voltage applied at the gate's terminal has a major effect on the conductivity between the source and the drain. This is the most popular technique for amplification and switching. MOSFET has many merits when compared with the normal BJT. One among them is that the MOSFET needs no input current to control the larger amount of current.

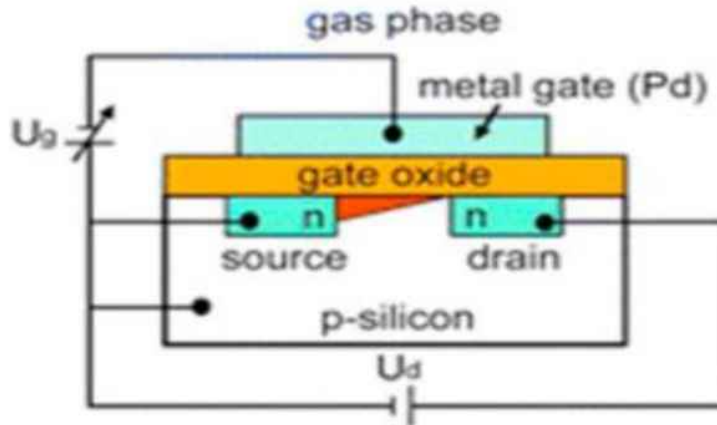
Junctionless Surrounding Gate MOSFET (JSGMOSFET) , one among the recently launched devices, has the channel surrounded by the gate material in all the regions offering better performance. JSGMOSFET is designed to be a common case junction-based device with an enhanced current drive for preventing current barriers. These devices are economical due to non-annealing and non-ion implantation, and are like conventional MOSFET yet with different operational characteristics.

The finite difference approximations for derivatives are one of the simplest and of the oldest methods to solve differential equations. Finite difference method (FDM) uses an approximation of the differential of the difference equation. The main preference of FDM is the fact that it is a very exact method. This project aims at providing the surface potential by applying finite-differentiation method. The model is verified with a correlative analysis of the model results and the simulation results, derived from TCAD.

1.1 ABOUT MOSFET

MOSFETs are the most frequent form of insulated gate FETs (IGFET) which are exploited in various types of electronic circuits for switching and amplifying electronic signals. They are the core of integrated circuits and are capable of being used in a single chip because of their small sizes. The key characteristic of MOSFETs is their metal oxide gate electrode. An ultra-thin layer of insulating material (usually SiO_2) insulates this controlling gate from the main channel which is located in the middle of the drain and source, making the MOSFET's input resistance exceptionally high. Therefore, no current flows into the gate and the device acts like a voltage-controlled resistor. MOSFETs can easily become damaged due to the accumulation of large amounts of static charge resulting from high input resistance. Thus, they need to be used carefully. For example, a commercial biosensing device based on MOSFET for the recognition of C-reactive protein (CRP) was created by Lyu and colleagues. The binding of the CRP to its specific antibody was sensed by quantifying the drain current of the system. The manufactured MOSFET biosensor paved the way for the emergence of cheap and simple FET-based biosensors. Or in another research work done by Mostafa et al., MOSFET-fixed cantilevers were designed to spot *Bacillus thuringiensis*. Attachment of this target to the cantilever which is modified by gold caused variations in the current of MOSFET drain as a result of the flexing of the cantilever. It is important to mention that the electronic attributes of the target were also accountable for the alteration in the current of the drain. Their reported limit of detection was 10 mL.

MOSFET



1.2 2D POISSON'S EQUATION

The work function of gate material used in a junction less transistor is always on the higher side. Thin silicon film shown of the device structure is partitioned into two different regions supposing to derive the analytical expression representing potential distribution. This is obtained by solving the 2-D Poisson's equation as:

$$\begin{aligned}
 & \frac{U(x_{i-1}, y_j) - 2U(x_i, y_j) + U(x_{i+1}, y_j)}{(hx)^2} \\
 & + \frac{U(x_i, y_{j-1}) - 2U(x_i, y_j) + U(x_i, y_{j+1})}{(hy)^2} \\
 & = f(x, y)
 \end{aligned} \tag{1}$$

where $f(x, y)$ is a constant term.

The general equation of the Finite Difference method is considered for solving the Poisson's Equation. The general equation of the Finite difference method is compared with the Potential distribution. The potential distribution in the silicon region is given by

$$\frac{1}{r} \frac{d}{dr} \left[r \frac{d\varphi(r, z)}{dr} \right] + \frac{d^2 \varphi(r, z)}{dz^2} = \frac{qN_D}{\epsilon_{si}} \left[e^{\frac{(\varphi(r, z) - V)}{v_t}} - 1 \right] \quad (2)$$

where q is the electronic charge, ϵ_{si} is the permittivity of silicon, v_t is the thermal voltage, $\varphi(r, z)$ is the electrostatic potential, N_D is the doping concentration in the channel region and V is the electron quasi-Fermi potential. Here $v_t = \frac{1}{4} kT/q$ where k is the Boltzmann constant and T is the temperature. The values for u , x and y are taken as follows:

$$\begin{array}{ccccc} & & U = \varphi & & \\ x_{i-1} = -R & x_i = 0 & & x_{i+1} = +R & \\ y_{j-1} = 0 & y_j = L_1 & & y_{j+1} = L_2 & \end{array}$$

Comparing Eq. 1 and 2 along with the above values the surface potential distribution in the silicon is enabled by solving the 2-D Poisson's equation. Determination of surface potential is carried out by doing certain assumptions and boundary conditions. They are as given below.

- 1) Electric field is given as

$$\left. \frac{d\varphi(r, z)}{dr} \right|_{r=0} = 0$$

- 2) The potential distribution at top ($r = -R$) and bottom ($r = R$).
- 3) The total length of the gate is $L = L_1 + L_2$.
M1 lies at $0 \leq Z \leq L_1$, $0 \leq r \leq R$.
- 4) The potential value at the source end is zero.

$$\varphi(r, z) = 0 \text{ since } r = 0$$

- 5) The potential at the drain end is V_{ds}

$$\varphi(r, z)L = L_1 + L_2 = V_{ds}$$

M2 lies at 0, $0 \leq r \leq R$.

The considered two-dimensional view of Junctionless Dual Material Surrounding Gate is exhibited. There is a possibility to solve Poisson's equation using the finite differentiation approximation, when the channel potential values are picked out at a minimum among three discrete points namely ($r = -R$, $r = 0$, $r = +R$) along the r -axis. It can be solved by choosing the channel potential values at three discrete points ($z = 0$, $z=L_1$, $z=L_2$) along the z -axis. Solving (Eq.2) using above approximations gives

$$\frac{\varphi(-R, z) - 2\varphi(0, z) + \varphi(R, z)}{R^2} + \frac{\varphi(r, 0) - 2\varphi(r, L_1) + \varphi(r, L_2)}{L^2} - \frac{qN_D}{\epsilon_{si}} \left[e^{\frac{(\varphi(r, z) - V)}{v_t}} - 1 \right] \quad (3)$$

An assumption is made that the electric field and surface potential under both the gates M1 and M2 are non-interfering with each other. Thus, the DMSG JLFET undergoes a split into two single material gates JLFET's and model their behaviors independently. Eliminating the second term in the equation (Eq. 3) and assuming that the exponential value of z is minimum, the following equations are obtained.

$$\frac{\varphi(r, 0) - 2\varphi(r, L_1) + \varphi(r, L_2)}{L^2} = 0 \quad (4)$$

$$\frac{qN_D}{\varepsilon_{si}} \left[e^{\frac{(\varphi(r, z) - V)}{v_t}} - 1 \right] = \frac{qN_D}{\varepsilon_{si}} \left[e^{\frac{(\varphi(r) - V)}{v_t}} - 1 \right] \quad (5)$$

Using this approach, Eq. (3) can be decomposed as given in the following:

$$\frac{\varphi_1(-R) - 2\varphi_1(0) + \varphi_1(R)}{R^2} = \frac{qN_D}{\varepsilon_{si}} \left[e^{\frac{(\varphi(r) - V)}{v_t}} - 1 \right] \quad (6)$$

$$\frac{\varphi_2(-R) - 2\varphi_2(0) + \varphi_2(R)}{R^2} = \frac{qN_D}{\varepsilon_{si}} \left[e^{\frac{(\varphi(r) - V)}{v_t}} - 1 \right] \quad (7)$$

$$\frac{\varphi(r, 0) - 2\varphi(r, L_1) + \varphi(r, L_2)}{L^2} = 0 \quad (8)$$

Equation (Eq.6) and (Eq.7) represent the 1-D Poisson's Equation along the r-axis, of which (Eq. 6) represent for region 1 (under M1) and (Eq. 7) represents for region 2 (under M2). When region 1 alone is considered, (Eq. 6) can be written in a general form as given in the following:

$$\frac{\varphi(-R) - 2\varphi(0) + \varphi(R)}{R^2} = \frac{qN_D}{\varepsilon_{si}} \left[e^{\frac{(\varphi(r) - V)}{v_t}} - 1 \right] \quad (9)$$

where φ is the potential at the center of the channel, while $\varphi(-R)$ and $\varphi(+R)$ are the surface potentials (φ_s). It shall be recollected that as the channel becomes fully depleted, then the surface potential is negative. Hence, the exponential term in (Eq. 9) becomes very small and gets neglected.

$$\frac{\varphi_s - 2\varphi_o + \varphi_s}{R^2} = -\frac{qN_D}{\epsilon_{si}} \quad (10)$$

$$2\varphi_s - 2\varphi_o = -\frac{qN_DR^2}{\epsilon_{si}} \quad (11)$$

$$2(\varphi_s - \varphi_o) = -\frac{qN_DR^2}{\epsilon_{si}} \quad (12)$$

$$\varphi_s - \varphi_o = -\frac{qN_DR^2}{2\epsilon_{si}} \quad (13)$$

Now φ_o can be replaced by $V_{gs} - V_{th}$, which gives

$$\varphi_s = V_{gs} - V_{th} - \frac{qN_DR^2}{2\epsilon_{si}} \quad (14)$$

where V_{th} is the threshold voltage of the JLFET. The threshold voltage is treated as the gate voltage at which the depletion mode changes from full to partial in the device. Regarding partially depleted channel, the relation between φ_o and φ_s is made by using the depletion approximation, as illustrated in the following:

$$\varphi_s = \varphi_o - \frac{qN_Dx_d^2}{2\epsilon_{si}} \quad (15)$$

where x_d is the depletion width in the partially depleted channel given by

$$x_d = \sqrt{\frac{2\epsilon_{si}(V_{gs} - V_{th})}{qN_D}} \quad (16)$$

The Charge density Q_{sc} in the partially depleted channel is given by

$$Q_{sc} = 2qN_Dx_d = -2C_{ox}(V_{gs}-V_{FB}-\varphi_{S1})^2 \quad (17)$$

Substituting the Eq. (15) in above equation

$$2qN_D\sqrt{\frac{2\varepsilon_{si}(V_{gs}-V_{th})}{qN_D}} = -2C_{ox}(V_{gs}-V_{FB}-\varphi_{S1})^2 \quad (18)$$

By squaring on both sides and then by simplifying, the value for $V_{gs} - V_{th}$ is obtained.

$$V_{gs}-V_{th} = \frac{C_{ox}^2}{2\varepsilon_{si}qN_D} (V_{gs}-V_{FB}-\varphi_{S1})^2 \quad (19)$$

where C_{ox} is the gate oxide capacitance.

1.3 PARAMETER ANALYSIS

1.Surface Potential Model

Depletion approximation is applied in modeling the surface potential at the junction ($L=L1 + L2$) of regions 1 and 2. The width x_j of the depletion region at the junctions of regions 1 and 2 is given by

$$x_j = \sqrt{\frac{2\varepsilon_{si}(\varphi_{s,2}-\varphi_{s,1})}{qN_D}} \quad (20)$$

The surface potential model for both regions 1 and 2 can be written as follows.
For Region 1 :

$$\varphi_{S1} = \varphi_0 + \frac{C_{ox}^2}{2\varepsilon_{si}qN_D} (V_{gs}-V_{FB}-\varphi_{S1})^2 \quad (21)$$

For Region 2:

$$\varphi_{S2} = \varphi_0 + \frac{C_{ox}^2}{2\varepsilon_{si}qN_D} (V_{gs} - V_{FB} - \varphi_{S2})^2 \quad (22)$$

2. Electric Field

The Electric Field is an important parameter that defines the performance of the device towards short channel effects. The field along the channel length can be determined for the various regions by differentiating the surface potential and therefore the resultant Electric field for both the regions are

$$E_1(z) = \frac{C_{ox}^2}{\varepsilon_{si}qN_D} (V_{gs} - V_{FB} - \varphi_{S1}) \quad (23)$$

$$E_2(z) = \frac{C_{ox}^2}{\varepsilon_{si}qN_D} (V_{gs} - V_{FB} - \varphi_{S2}) \quad (24)$$

3. Threshold Voltage

The threshold voltage is defined as the minimum voltage applied between the gate and the source to create a conducting path between source and drain terminals. Here the surface potential was obtained by solving the two-dimensional Poisson's equation. The analytic threshold model was derived for, the minimum surface potential. This method has been used to obtain the threshold voltage of a Junction less MOSFET.

The threshold voltage for DMSG JL MOSFET is

$$V_{th} = \frac{2(vx + uy) + z + \sqrt{(2(vx + uy) + z)^2 - (1-4ux)(z^2-4vy)}}{(1-4ux)} \quad (25)$$

where

$$u = \frac{\ell^{-L_{eff}/\lambda} - 1}{2\sinh(L_{eff}/\lambda)} \quad (26)$$

$$v = \frac{V_{DS} - c(\ell^{-L_{eff}/\lambda} - 1)}{2\sinh(L_{eff}/\lambda)} \quad (27)$$

$$x = \frac{1 - \ell^{L_{eff}/\lambda}}{2\sinh(L_{eff}/\lambda)} \quad (28)$$

$$y = \frac{-V_{DS} + e(\ell^{L_{eff}/\lambda} - 1)}{2\sinh(L_{eff}/\lambda)} \quad (29)$$

$$z = V_{FB} - \frac{qN_D T_{si}}{4C_{ox}} - \frac{qN_D T_{si}^2}{16\epsilon_{si}} \quad (30)$$

Hence, L_{eff} is the effective channel length of the MOSFET.

4. Drain Current Model

To calculate the Drain current, it is considered that the DMSG JL is constructed by connecting two SMSG JL in series. So, the length of the channel is taken as $L = L1 + L2$. When the voltage of the drain to source is greater than the voltage in the drain to saturation region, the velocity saturation pinch off point move towards the source and the voltage difference is dropped across the distance. This reduces the channel length when compared to the physical channel this in turn increases the drain current. Thus, including the channel length modulation effect, the saturation current is obtained. The simplification of drain current of a DMSG JLFET in the linear region is done. The drain current is generally provided by the drift tendency and is given as

$$I_{ds} = \frac{2\pi R Q(z) \mu \left(\frac{dE(z)}{dz} \right)}{1 + (1/E_{sat}) \left(\frac{dE(z)}{dz} \right)} \quad (31)$$

$$Q(z) = C_{ox} (V_{gs} - V_{th} - V(z)) \quad (32)$$

$$E_{sat} = V_{sat} / \mu \quad (33)$$

where dE/dz is the Electric field, $2\pi R$ is the device width, $Q(z)$ is the charge density, E_{sat} is the critical field, $V(z)$ is the channel position along the z direction. Substituting the Eq. 32, 33 in 31. The drain current will be obtained as

$$I_{ds} = \frac{2\pi R \mu_{eff} C_{ox} [V_{gs} - V_{th} - (V_{ds}/2)] V_{ds}}{L(1 + (V_{ds}/LE_{eff}))} \quad (34)$$

where V_{ds} is the drain to source voltage which is given as.

$$V_{ds} = V_1 + V_2$$

and

$$\mu_{eff} = \frac{L}{[(L_1/\mu_{n1}) + (L_2/\mu_{n2})]}$$

$$E_{eff} = \frac{2V_{sat}}{\mu_{eff}}$$

The drain current in the saturation region is given as

$$I_{dsat} = 2\pi R V_{sat} Q_{insat} \quad (35)$$

where I_{dsat} is the saturation drain current and Q_{insat} inversion charge at $V_{ds} = V_{dsat}$ and is given as

$$Q_{insat} = C_{ox}(V_{gs} - V_{th} - V_{dsat}) \quad (36)$$

Using Eq. (36) in Eq. (35) drain current at saturation region become

$$I_{dsat} = 2\pi RC_{ox}V_{sat}(V_{gs} - V_{th} - V_{dsat}) \quad (37)$$

where V_{th} is the threshold voltage is given by

$$V_{th} = \frac{-V_{\varphi 1} + \sqrt{V_{\varphi 1}^2 - 4\xi V_{\varphi 2}}}{2\xi} \quad (38)$$

where $V_{\varphi 1}$, $V_{\varphi 2}$ and ξ are given in and

$$V_{dsat} = \frac{V_{gs} - V_{th}}{1 + (V_{gs} - V_{th})/LE_{eff}} \quad (39)$$

With the channel length getting reduced, short channel effects (SCEs) such as Drain Induced Barrier Lowering (DIBL) occur. These effects make an adverse impact on the device behavior affecting the normal function.

5. The Sub-Threshold Swing

The Sub-threshold Swing is the estimation parameter for characteristics related to sub-threshold of a device. It is the factor which predicts the volume of gate bias for increasing in the units of volts so that the sub-threshold voltage can be raised by ten times. The extraction of the sub-threshold swing of I-V characteristics can be done as

$$SS = \frac{\partial V_{gs}}{\partial \log(I_d)}$$

Here, it is to be noted that the Sub-threshold swing value must be the utmost minimal for good switching characteristics of the device.

CHAPTER 2

LITERATURE REVIEW

LITERATURE SURVEY

1: Suveetha Dhanaselvam P, Balamurugan NB (2014) Performance analysis of fully depleted triple material surrounding gate (TMSG) SOI MOSFET. J Comput Electron 13:449–455. For more than 30 years, the IC industry has followed a steady path of constantly shrinking the device geometries and increasing chip size. A new gate structure called the dual material gate (DMG) MOSFET was proposed which eliminates the effects of reduction of chip size. A 2D analytical approach of DMG is proposed in this paper and the solution to the Poisson equation is obtained using parabolic expansion method. Using the boundary conditions, the surface potential and electric field potential distribution is obtained for different work function and channel lengths.

2: Buvaneswari B, Balamurugan NB (2019) 2D Analytical modeling and simulation of dual material DG MOSFET for biosensing application. In the recent times, the performance of MOSFET in the nanoscaled region attains improvisations through several alternative device structures. Amongst many advanced MOSFET structures, the Double Gate (DG) MOSFET is one such structure which mitigates short channel effects because of its excellent scalability. Among the various structures, FET- based biosensors have shown an accelerated growth recently. Even though many analytical models are available for the Dual Material DG (DMDG) MOSFET structures, this work endeavours to introduce an analytical modeling of nanocavity embedded DMDG structure for the first time. The expression for surface potential is obtained by solving the 2-D Poisson's equation using a parabolic-potential approach. The threshold voltage is determined from the minimum surface potential

model. Sensitivity is computed in terms of relative change in the threshold voltage and it is derived using the model. The influence of various device geometrical parameters like length and thickness of the nanocavity on the sensitivity has been investigated. Further, a comparison of the sensitivity of DG MOSFET and DMDG MOSFET has also been made and the derived results are validated against TCAD simulation results.

3: Singh S, Raj B, Vishvakarma SK (2018) Analytical modeling of split gate junctionless transistor for a biosensor application. *Sens Biosens Res* 18:31–36 . In this paper an analytical model of dual material surrounding split gate junctionless transistor for application as a biosensor is introduced. The simulation results show fair compatibility with the analytical models developed for the channel center potential and threshold voltage at channel length of 45 nm and 20 nm. For the detection of the bio-molecules, concept of dielectric modulation has been used. The model shows a satisfactory value of sensitivity in the range of 0–0.27 and 0–0.8 for relative permittivity of biomolecules varying from 1 to 9 at channel length of 45 nm and 20 nm respectively, thus making it an attractive option for use as biosensor. This model has been demonstrated with the aid of TCAD device simulations.

4. Guangxi PX, Ding Z, Liu R, Wang L, Tang T-A (2014) Analytical models for electric potential, threshold voltage, and subthreshold swing of junctionless surrounding-gate transistors. *IEEE Transact Electron Dev* 61(3):688–695 . Analytical models for electric potential, threshold voltage, and subthreshold swing of the junctionless surrounding-gate field-effect transistors are presented. Poisson equation is solved and the electric potential is obtained. With the potential model, explicit expressions for threshold voltage and subthreshold swing are obtained. The analytical results are compared with those from simulations and excellent agreements are observed. The analytical models are useful not only for fast

circuit simulations, but also for device design and optimization.

5: Karthigai Pandian M, Balamurugan NB (2014) Analytical threshold voltage modelling of surrounding gate silicon nanowire transistors with different geometries. *J Electric Eng Technology* 9(6):742–751. In this paper, we propose new physically based threshold voltage models for short channel Surrounding Gate Silicon Nanowire Transistor with two different geometries. The model explores the impact of various device parameters like silicon film thickness, film height, film width, gate oxide thickness, and drain bias on the threshold voltage behavior of a cylindrical surrounding gate and rectangular surrounding gate nanowire MOSFET. Threshold voltage roll-off and DIBL characteristics of these devices are also studied. Proposed models are clearly validated by comparing the simulations with the TCAD simulation for a wide range of device geometries.

6: Aggarwal S, Singh R (2012) Dual metal gate and conventional MOSFET at sub nm for analog application. *Int J VLSI Design Commun Syst (VLSICS)* 3(1):111–117. The use of nanometer CMOS technologies (below 90nm) however brings along significant challenges for circuit design (both analog and digital). By reducing the dimensions of transistors many physical phenomenon like gate leakage, drain induced barrier lowering and many more effects comes into picture. Reducing the feature size in the technology of device with the addition of ever more interconnect layers, the density of the digital as well as analog circuit will increase while intrinsic gate switching delay is reduced . We have simulated conventional and DMG MOSFET at 30nm scale using Silvaco TAD tool and obtained result. A two dimensional device simulation was

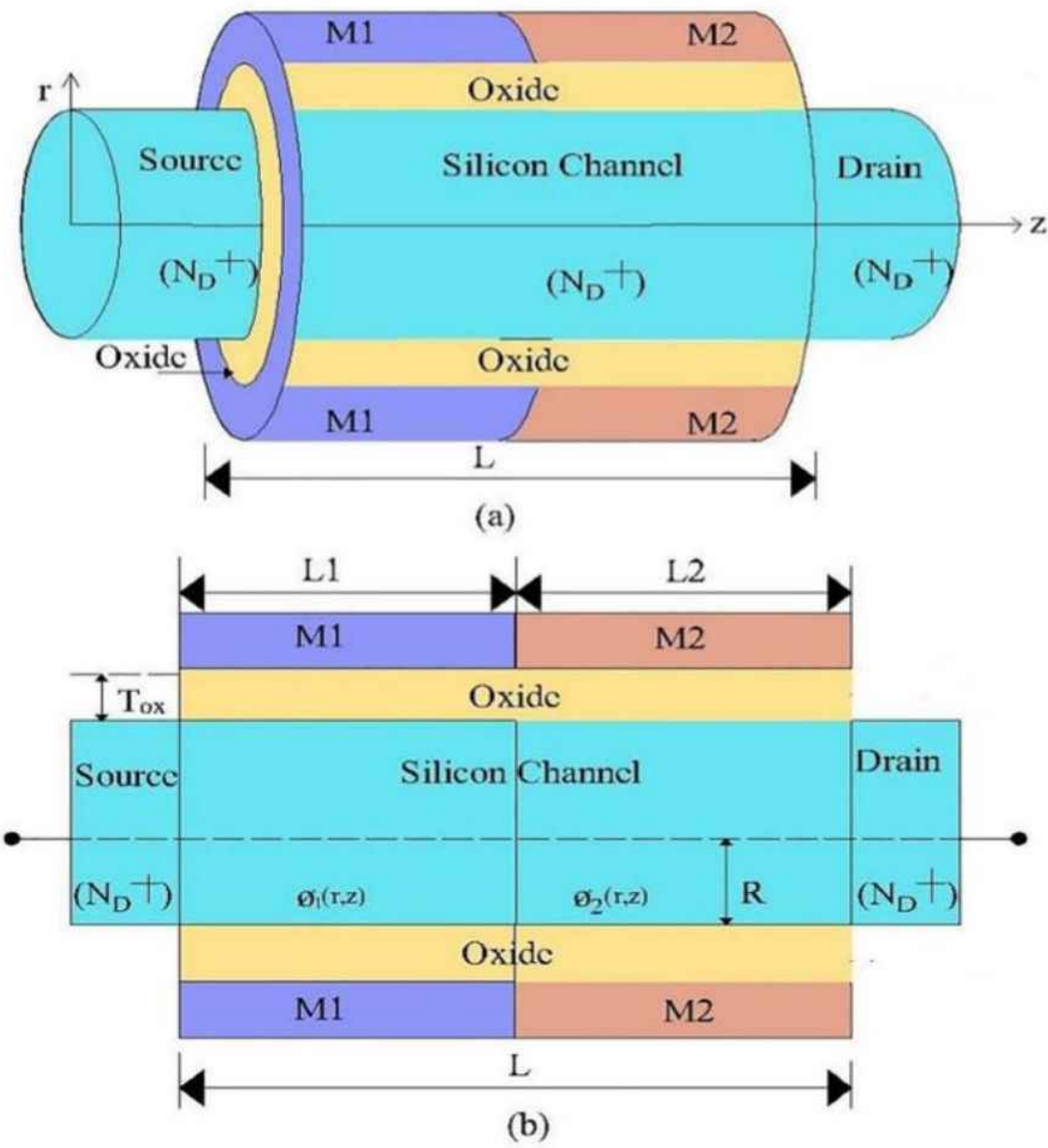
carried out and observed that DMG MOSFET has a low leakage current as compared to conventional MOSFET and find suitable application in analog circuits.

7: Jagadesh Kumar M, Orouji AA, Dhakad H (2006) New dual-material SG nanoscale MOSFET: analytical threshold-voltage model. IEEE Transact Electron Dev 53(4):920–922. A new analytical model for the surface potential and threshold voltage of a surrounding-gate MOSFET with dual-material gate is presented to investigate the short-channel effects. The model results accurately predict the threshold-voltage "roll off" for channel lengths even less than 90nm. The accuracy of the model results is verified using two-dimensional simulation.

CHAPTER 3

METHODOLOGY

3.1 BLOCK DIAGRAM OF PROPOSED WORK



PROPOSED WORK:

The proposed model was verified with the proper simulation of the device, by using the Sentaurus TCAD device simulator. Next, in order to prove the accuracy of the results from the proposed method, simulations were drifted out on the surface potential model, the plots of the surface potential against channel length for varied values such as T_{si} , T_{ox} and N_D . From the analysis of the results acquired from the proposed model, it was observed that there has been a correlation between these results and the simulation results. More specifically, the correlation was observed in case of both the fully depleted channel and the partially depleted channel .

CHAPTER 5

CONCLUSION

Recent analyses on securing a systematic and analytical solution for Poisson's equation illustrated some constraints and complexities. However, in this paper, an attempt is made to showcase the possibility of exploring such a solution. This paper proposes a recently developed two-dimensional analytical model for threshold voltage on Dual Material Surrounding Gate Junctionless MOSFET. From this proposed study, the surface potential for different voltages and the electric field for various channel lengths are derived. The subthreshold results from the simulations and the model results clearly exhibit both the considerable and the appreciable improvement in switching characteristics of the device. This in turn decreases the short channel effects. The results further show that the increase of thickness in silicon effects a reduction of the peak electric field in the device. In fact, this reduction at the ends of the device is the chief factor for the performance efficiency of DMSG JLFET. To be more specific, the reduction provides a solution for the depletion in the device body and to protect the gate from extension. Thus, the proposed model DMSG JLFET is justifiable and adoptable for solving Poisson's equation with regard to the parameters of Surface Potential, Electric Field, Threshold Voltage and Drain current. Further, this proposed model envisages a pattern for sustaining the potential barrier in the channel and the threshold voltage. Finally, the proposed Multigate model preserves the device from degradation of the switching and operational characteristics.

4.1 FUTURE SCOPE

Since MOSFET has higher sensitivity and conductivity it has more Application in Healthcare. Cancer is the second dominant fatal disease globally with above 200 known categories and more than 1600 deaths taking place each day . Despite the ever-growing technology, the number of survived cancer patients is still low as a consequence of detection at advanced levels and the unsatisfactory prognosis of cancer .The common diagnostic approaches, including ultrasound, CT scan,PET, magnetic resonance imaging, and biopsy are incompetent for early cancer detection. The top down construction technique of this FET-based biosensor made the researcher have control over its electrical characteristics. Furthermore, this approach is CMOS-compatible which enables mass production of the proposed biosensor for high throughput, real time, cheap, and precise assays. The surface of the device was modified with APTES, GA, and anti-CEA, and a microfluidic channel was added on top of it. This approach was successful enough to detect down to 10 pg/mL of the analyte . Or Gao and colleagues designed a microfluidic sensing platform based on CMOS-compatible SiNW-FET for the identification of lung cancer biomarkers ((miRNA)126 and CEA). Utilizing nanowires enabled single-molecule level detection with high sensitivity and specificity in biofluids . The other CMOS-compatible silicon nanowire tunneling field-effect transistor (SiNW-TFET) biosensor was reported by Gao et al. for pH and cytokeratin 19 fragment (CYFRA21-1) detection. It was capable of recognizing down to 12.5 aM of the target protein in the serum sample. These successful studies demonstrate the power of FET-based platforms for a wide range of POC applications .

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