

PERFORMANCE METRICS OF GRAPHENE BASED FIELD EFFECT TRANSISTOR USING SPICE COMPATIBLE MODEL

Submitted in partial fulfilment of requirements for the award of
Bachelor of Engineering in
Electronics and Communication Engineering

by

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHOOL OF ELECTRICAL AND ELECTRONICS

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

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APRIL 2023



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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bonafide work of ANAGHA JACOB (39130020) and ANTO KENSIYA S (39130028) who carried out the project entitled "**PERFORMANCE METRICS OF GRAPHENE BASED FIELD EFFECT TRANSISTOR USING SPICE COMPATIBLE MODEL**" under our supervision from August 2022 to April 2023

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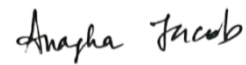
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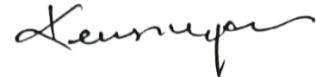
DECLARATION

We, ANAGHA JACOB (39130020) and ANTO KENSIYA S (39130028) hereby declare that the Project Report entitled **“PERFORMANCE METRICS OF GRAPHENE BASED FIELD EFFECT TRANSISTOR USING SPICE COMPATIBLE MODEL”** done by us under the guidance of Dr. MATHAN N., M.Tech., Ph.D, Assistant Professor is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

1.



2.



DATE: 15.04.2023

PLACE: CHENNAI

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ABSTRACT

The relevance of VLSI in performance computing, telecommunications and consumer electronics has been expanding progressively. In order to build complex digital logic circuits it is often essential to sub divide multi-million transistors design into manageable pieces. Circuit partitioning is a general approach used to solve problems that are too large and complex to be handled at once. In partitioning, the problem is divided into small and manageable parts recursively, until the required complexity level is reached. In the area of VLSI circuit complexity is rapidly multiplying together with the reducing chip size. The integrated chips being produced today are highly sophisticated. There are many diverse problems that occur during the development phase of an IC that can be solved by using circuit partitioning which aims at obtaining the sub circuits with minimum interconnections between them. This project proposes unidirectional and bidirectional latch based thermometer code shift registers. They reduce both the area and the power consumption by replacing the D flip-flops with the proposed unidirectional and bidirectional thermometer code shift registers will be simulated using a 16nm GNR FET Technology. Parameters like Power, Delay and Power Delay Product will be compared on both conventional unidirectional and bidirectional shift registers and proposed system respectively.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Thermometer-code shift-register is widely used in mixed signals circuits, such as successive approximation register analog-to-digital converters (SAR-ADC), digital DC-DC buck converters, and digital low-dropout (LDO) regulators. Recently, its bit-width and clock frequency increase significantly, because the more accurate and fast operations are required in the mixed signal circuits. This causes large area and large power consumption due to many flip-flops.

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The relevance of VLSI in performance computing, telecommunications and consumer electronics has been expanding progressively. In order to build complex digital logic circuits, it is often essential to sub divide multi-million transistors design into manageable pieces. Circuit partitioning is a circuit complexity is rapidly multiplying together with the reducing chip size. The integrated chips being produced today are highly sophisticated.

There are many diverse problems that occur during the development phase of an IC that can be solved by using circuit partitioning which aims at obtaining the sub circuits with minimum interconnections between them.

This project proposes unidirectional and bidirectional latch-based thermometer code shift registers. They reduce both the area and the power

consumption by replacing the D flip-flops with the proposed unidirectional and bidirectional 64-bit thermometer code shift registers were simulated using a 65nm CMOS process.

They reduce the areas and the power consumptions compared to the conventional unidirectional and bidirectional 64-bit shift registers respectively general approach used to solve problems that are too large and complex to be handled at once. In partitioning, the problem is divided into small and manageable parts recursively, until the required complexity level is reached.

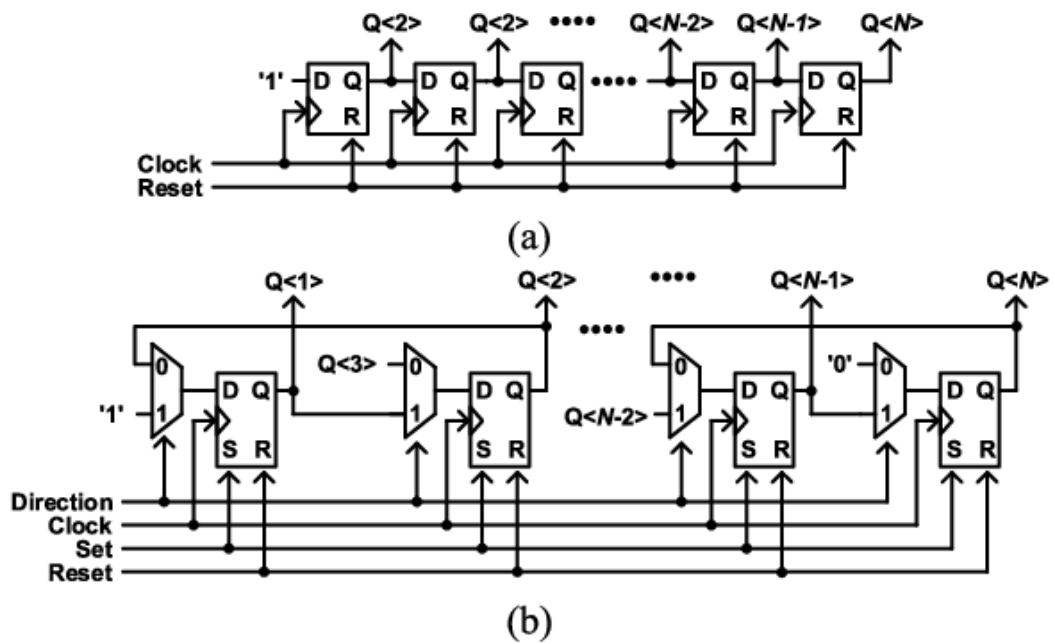


Fig. 1.1. conventional N-bit thermometer-code shift-registers (a) Unidirectional
(b) bidirectional

**Fig. 1.1.1 Conventional N-bit thermometer-code shift-registers (a)
Unidirectional (b) bidirectional**

Fig. 1.1 .1 Conventional shows conventional unidirectional and bidirectional N-bit thermometer-code shift-registers consisting of D flip-flops and 2-to-1 multiplexers. Fig 2 shows the schematics of the unidirectional and bidirectional D flip-flops (D-FFs) for the thermometer-code-shift registers. the unidirectional and

bidirectional D-FFs contain two latches including set and reset signals. They consist 24 and 34 transistors.

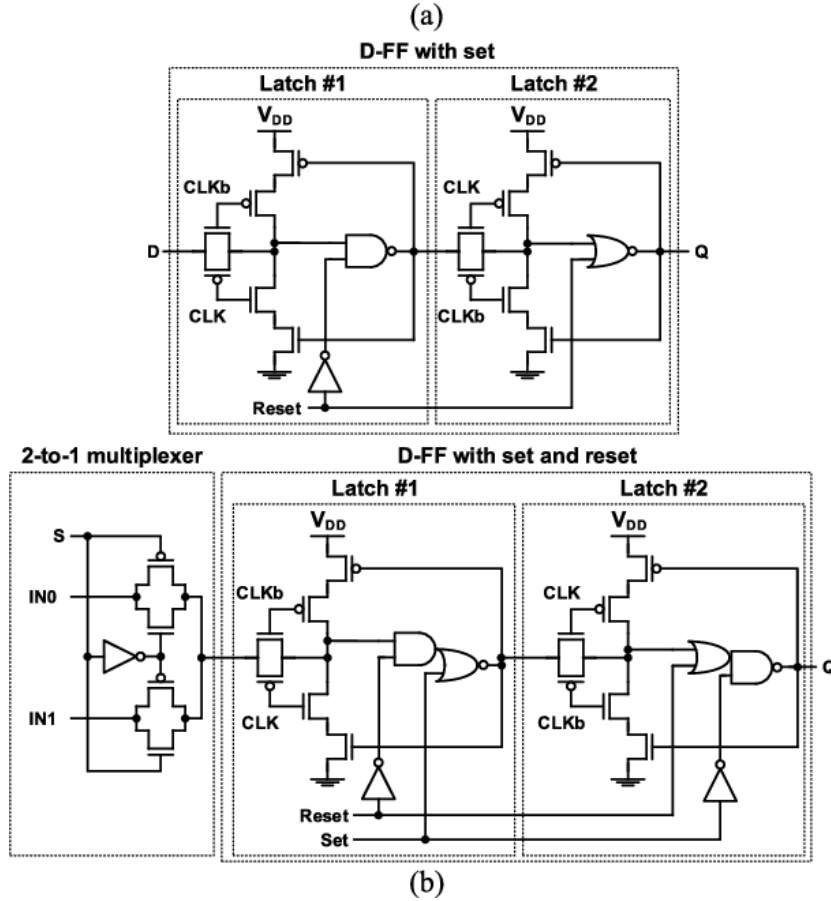


Fig. 1.1.2 (a) Unidirectional D flip-flop (b) Bidirectional D flip-flop

Fig. 1.2 shows the schematics of the unidirectional and bidirectional D flip-flops (D-FFs) for the thermometer-code shift-registers. The unidirectional and bidirectional D-FFs contain two latches including set and reset signals. They consist of 22 and 34 transistors. Fig. 1.3 shows the schematics and operation waveforms of the unidirectional and bidirectional pulsed-latches. The unidirectional pulsed-latch (Q and Qi) receives the differential data inputs (D and Db), when the pulsed clock signal (Calculus) is high.

The bidirectional pulsed-latch (Q and Qb) receives the differential left data inputs (DL and DLb) or the differential right data inputs (DR and DRb), when the pulsed clock signal for right-shifting or left-shifting (CLK_pulse_R). The bidirectional shift register mainly includes two serial i/ps like the data input with

serial right shift (DR) and the data input with serial left shift (DL) with a select mode input (M). Whenever the data needs to shift on the right side then input is given to the DR. Similarly, if the data needs to shift on the left side then input is given from DL.

When a mode control has a high signal then it allows the data to shift to the right side whereas the mode signal has a low signal then it shifts the data to the left side. If the i/p data is shifted left with 1 position then it is multiplied by 2 and if i/p data is shifted right with 1 position, it is divided by 2.

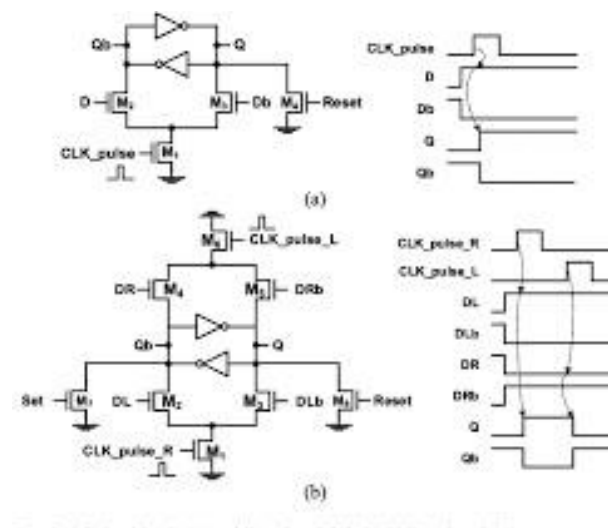


Fig 1.1.3 Pulsed latch (a) Unidirectional (b) bidirectional

1.2 MOTIVATION

Flip flops can be used to store a single bit of binary data (1 or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A Register is a device which is used to store such information. It is a group of flip flops connected in series used to store multiple bits of data. The information stored within these registers can be transferred with the help of shift register. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made

to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data. Thermometer Code Shift Register reduce the area and power consumption by replacing D Flip-flop. Now modify the flip-flop and compare both the flip-flop, the modified flip-flop will be the expected output. This will be checked in GNRFET and CMOS technology .In GNRFET the electrons will be free to move, the conduction will be fast and the speed is efficient. This will be applied on flip-flop, shift register and thermometer code shift register and check the result.

1.3 FLIP-FLOP

A circuit that has two stable states is treated as a flip-flop. These stable states are used to store binary data that can be changed by applying varying inputs. The flip flops are the fundamental building blocks of the digital system. Flip flops and latches are examples of data storage elements. In the sequential logical circuit, the flip flop is the basic storage element.

1.3.1 SR Flip Flop

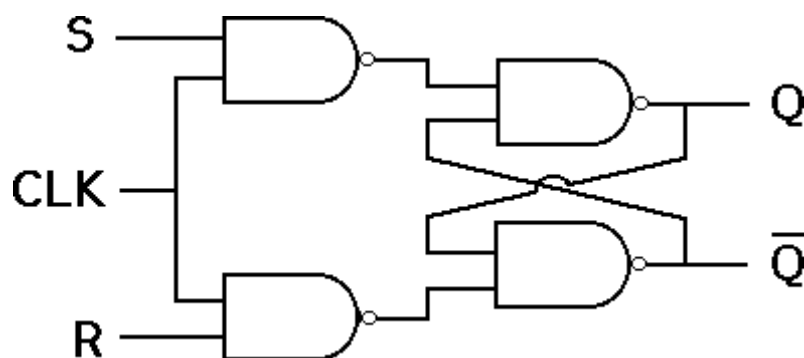


Fig 1.3.1 SR Flip-flop

This is the most common flip-flop among all. This simple flip-flop circuit has a set input (S) and a reset input (R). In this system, when you Set “S” as active, the output “Q” would be high, and “Q” would be low. Once the outputs are established, the wiring of the circuit is maintained until “S” or “R” go high, or power is turned off.

1.3.2 JK Flip-Flop

Due to the undefined state in the SR flip-flops, another flip-flop is required in electronics. The JK flip-flop is an improvement on the SR flip-flop where $S=R=1$ is not a problem.

The input condition of $J=K=1$ gives an output inverting the output state. However, the outputs are the same when one tests the circuit practically.

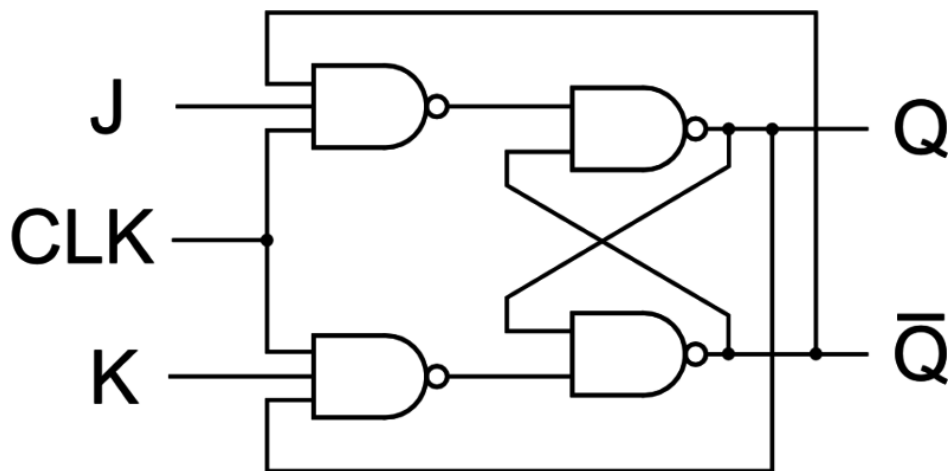


Fig 1.3.2 JK Flip-Flop

In simple words, If J and K data input are different (i.e. high and low), then the output Q takes the value of J at the next clock edge. If J and K are both low, then no change occurs. If J and K are both high at the clock edge, then the output will toggle from one state to the other. JK Flip-Flops can function as Set or Reset Flip-flops.

1.3.3 D Flip-Flop

D flip-flop is a better alternative that is very popular with digital electronics. They are commonly used for counters and shift registers and input synchronization.

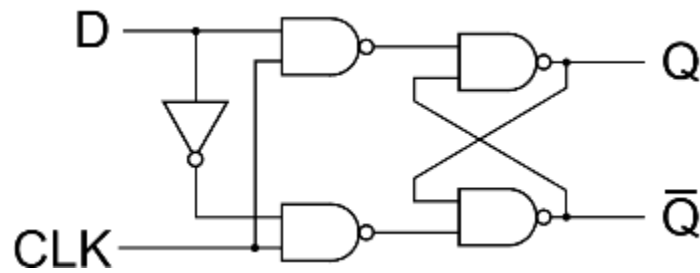


Fig 1.3.3 D Flip-Flop

In the D flip-flops, the output can only be changed at the clock edge, and if the input changes at other times, the output will be unaffected.

1.3.4 T Flip-Flop

A T flip-flop is like a JK flip-flop. These are basically single-input versions of JK flip-flops. This modified form of the JK is obtained by connecting inputs J and K together. It has only one input along with the clock input.

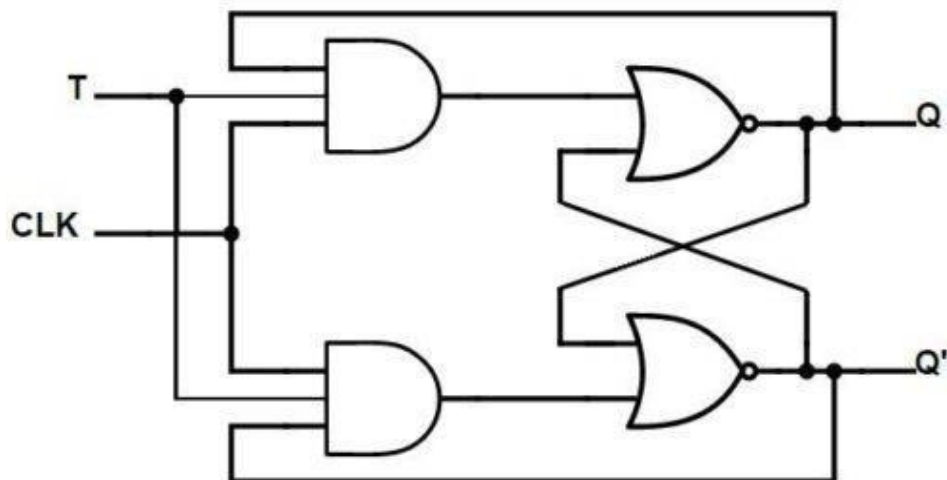


Fig 1.3.4 T Flip-Flop

1.4 SHIFT REGISTER

Flip flops can be used to store a single bit of binary data (1 or 0). However, in order to store multiple bits of data, we need multiple flip flops. N flip flops are to be connected in an order to store n bits of data. A Register is a device which is

used to store such information. It is a group of flip flops connected in series used to store multiple bits of data.

The information stored within these registers can be transferred with the help of shift registers. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses.

1.4.1 Serial-In Serial-Out Shift Register (SISO)

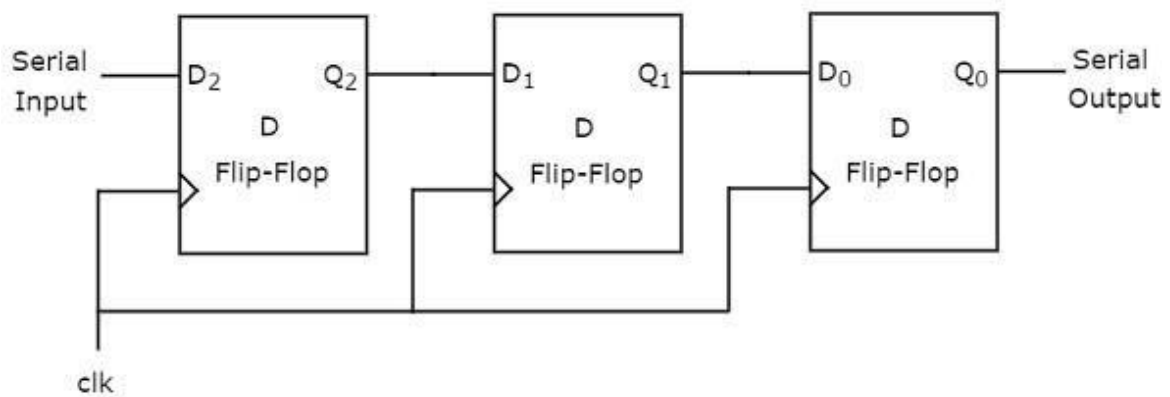


Fig 1.4.1 Serial-In Serial-Out Shift Register (SISO)

The shift register, which allows serial input one bit after the other through a single data line and produces a serial output is known as Serial-In Serial-Out shift register. Since there is only one output, the data leaves the shift register one bit at a time in a serial pattern, thus the name Serial-In Serial-Out Shift Register. The logic circuit given below shows a serial-in serial-out shift register. The circuit consists of four D flip-flops which are connected in a serial manner. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

1.4.2 Serial-In Parallel-Out shift Register (SIPO)

The shift register, which allows serial input one bit after the other through a single data line and produces a parallel output is known as Serial-In Parallel-Out shift register. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop. In this shift register, we can send the bits serially from the input of left most D flip-flop. Hence, this input is also called as serial input. For every positive edge triggering of clock signal, the data shifts from one stage to the next. So, we can receive the bits serially from the output of right most D flip-flop. Hence, this output is also called as serial output.

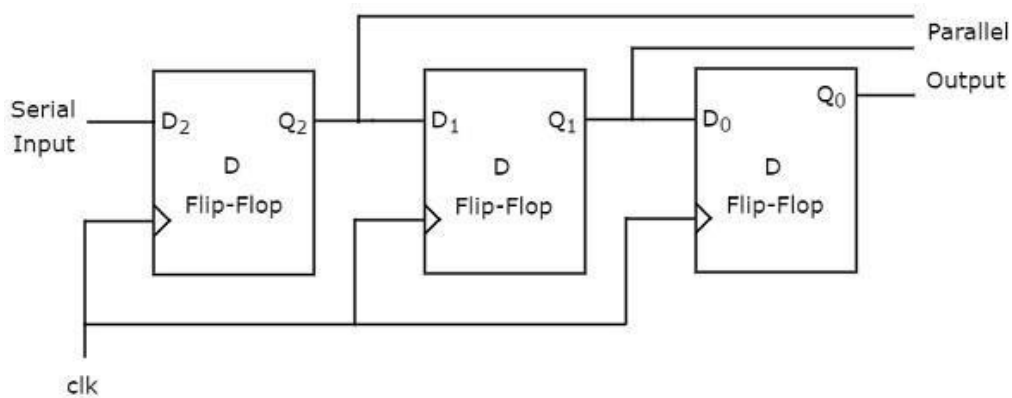


Fig 1.4.2 Serial-In Parallel-Out shift Register (SIPO)

The logic circuit given above shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

1.4.3 Parallel-In Serial-Out Shift Register (PISO)

The shift register, which allows parallel input data is given separately to each flip flop and in a simultaneous manner and produces a serial output is known as Parallel-In Serial-Out shift register.

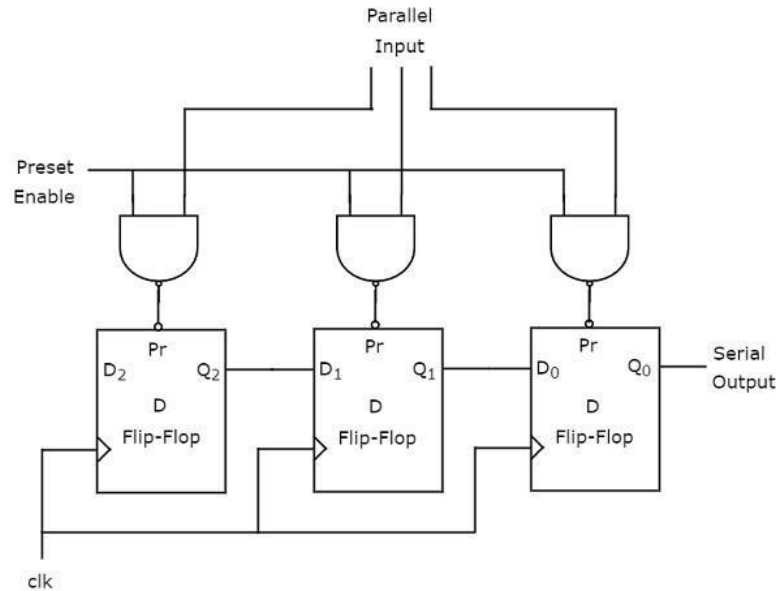


Fig 1.4.3 Parallel-in-serial-out shift Register

The logic circuit given above shows a parallel-in-serial-out shift register. The circuit consists of four D flip-flops which are connected. The clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a multiplexer at the input of every flip flop. The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

1.4.4 Parallel-In Parallel-Out Shift Register (PIPO)

The shift register, which allows parallel input data is given separately to each flip flop and in a simultaneous manner and also produces a parallel output is known as Parallel-In parallel-Out shift register.

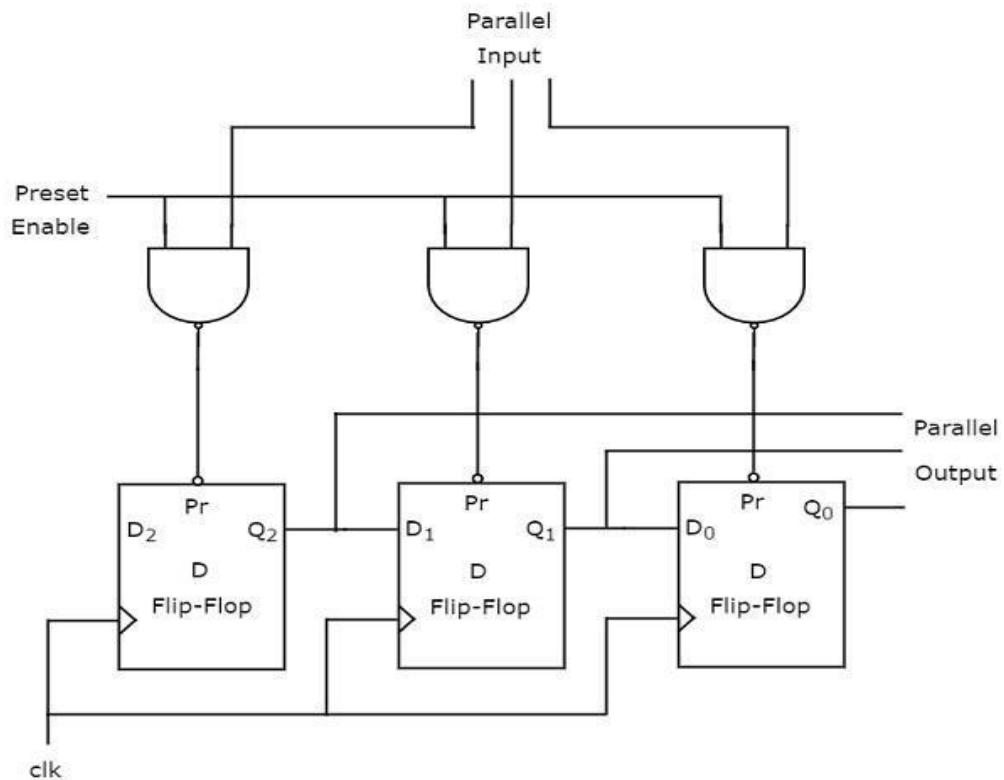


Fig 1.4.4 Parallel-in-parallel-out shift Register

The logic circuit given above shows a parallel-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal and clock signals are connected to all the 4 flip flops. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.

1.4.5 Bidirectional Shift Register

If we shift a binary number to the left by one position, it is equivalent to multiplying the number by 2 and if we shift a binary number to the right by one position, it is equivalent to dividing the number by 2. To perform these operations we need a register which can shift the data in either direction.

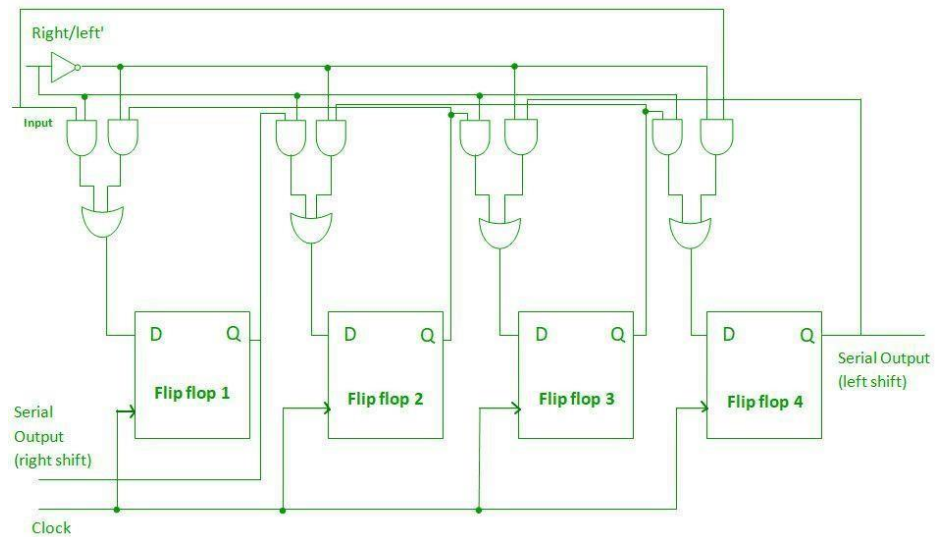


Fig 1.4.5 Bidirectional shift register

Bidirectional shift registers are the registers which are capable of shifting the data either right or left depending on the mode selected. If the mode selected is 1(high), the data will be shifted towards the right direction and if the mode selected is 0(low), the data will be shifted towards the left direction.

The logic circuit given below shows a Bidirectional shift register. The circuit consists of four D flip-flops which are connected. The input data is connected at two ends of the circuit and depending on the mode selected only one and gate is in the active state.

1.5 ORGANIZATION OF THE PROJECT

CHAPTER 1 discuss about VLSI, Motivation, Flip-flop, shift register. It also discusses about the various shift register and organization of the project work.

CHAPTER 2 delivers detailed literature survey related to the project, literature summary, problem definition, objectives of the project.

CHAPTER 3 describes the working and existing techniques of thermometer code shift register.

CHAPTER 4 discusses the proposed thermometer code shift register, simulation of Hspice.

CHAPTER 5 provides the simulation results and performance analysis of the existing and proposed project work. It does a full comparative analysis on how the proposed work is better off than the existing design.

CHAPTER 6 provides the conclusion project work. It also gives the schema of the future work that is how the project could be enhanced further. Finally, the references referred to lead the project are given in brief.

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

This chapter discusses about extensive literature survey on Performance metrics of graphene based field effect transistor using spice compatible model.

2.1 LITERATURE SURVEY

Ki-Chan Woo et.al., (2018) determines unidirectional and bidirectional latch-based thermometer-code shift-registers. They reduce both the area and the power consumption by replacing the D flip-flops with the proposed unidirectional and bidirectional thermometer-code latches. The proposed unidirectional and bidirectional 64-bit thermometer-code shift-registers were simulated using a 65nm CMOS process. They occupy $167\mu\text{m}^2$ and $226\mu\text{m}^2$. They consume $5.4\mu\text{W}$ and $6.5\mu\text{W}$ at a 100MHz clock frequency with $V_{DD}=1.2\text{V}$. They reduce the areas by 71% and 76% and the power consumptions by 83% and 85% compared to the conventional unidirectional and bidirectional 64-bit shift-registers, respectively. Thermometer code shift registers is widely used in mixed signal circuits, such as successive approximation register analog to digital converters, and digital low dropout regulators. Recently its bit width and clock frequency increases significantly, because the more accurate and fast operations are required in the mixed signal circuits. This causes large area and large power consumption due to many flip-flops. The unidirectional and bidirectional N-bit pulsed-latch based shift registers can be implemented with the unidirectional and bidirectional N pulsed-latches. Therefore, the pulsed-latch based shift registers can reduce both the area and power consumption by replacing D-FFs with the pulsed latches and pulsed clock signals. However, they require additional temporary storage latches and several non-overlap delayed pulse clock signals.

Chun-Cheng Liu et.al., (2017) implements a low-power 10-bit 50-MS/s successive approximation register (SAR) analog-to-digital converter (ADC) that uses a monotonic capacitor switching procedure. Compared to converters that use the conventional procedure, the average switching energy and total capacitance are reduced by about 81% and 50%, respectively. In the switching procedure, the input common-mode voltage gradually converges to ground. An improved comparator diminishes the signal-dependent offset caused by the input common-

mode voltage variation. The prototype was fabricated using 0.13- μm 1P8M CMOS technology. At a 1.2-V supply and 50 MS/s, the ADC achieves an SNDR of 57.0 dB and consumes 0.826 mW, resulting in a figure of merit (FOM) of 29 fJ/conversion-step. The ADC core occupies an active area of only 195 μm^2 . Successive approximation register analog to digital converter require several comparison cycles to complete one conversion, and therefore have limited operational speed applications. Although flash and two step ADCs are preferred solutions for low resolution high speed applications have been demonstrated as feasible alternatives. For single channel architectures, the non-binary and passive charge sharing architectures work at several tens of MS/s and medium resolutions with excellent power efficiency and small area.

X. Zhang et.al., (2014) implements a 0.6 V input, 0.3-0.55 V output buck converter in 40 nm CMOS, for low-voltage low-power wireless sensor network systems. A low power CCM/DCM controller of the buck converter enables automatic selection of DCM or CCM operation depending on load situation, therefore improving the power efficiency. A dual-mode-body-biased (DMBB) zero-crossing detector with both forward body bias mode and zero body bias mode is designed to enable DCM operation with both low supply voltage and normal supply voltage. An ultra-low-power hysteresis voltage detector is proposed for body bias modes selection. The proposed buck converter achieves a peak efficiency of 94% with an output current range of 50 μA to 10 mA. Thanks to the DCM operation, the efficiency at an output current of 10 μA is improved by 20% and 9%, with an output voltage of 0.35 V and 0.5 V, respectively. Combining the PV module with the battery-powered system can effectively extend the battery life time. The PV energy harvesting provides an attractive solution for battery less system. In these low-power applications, scaling the power supply of digital circuits down to sub/near/threshold region is a promising technique to achieve significant power reduction. Various types of step down voltage converters have been developed for low-voltage operations. By using digital control circuits, the operating voltage can be reduced to 0.5V with low quiescent current.

Byung –Do Yang et.al., (2015) determines a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem

between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 256-bit shift register using pulsed latches was fabricated using a 0.18 μm CMOS process with $V_{DD} = 1.8\text{V}$. The core area is 6600 μm^2 . The power consumption is 1.2 mW at a 100 MHz clock frequency. The proposed shift register saves 37% area and 44% power compared to the conventional shift register with flip-flop. The size of the image data continues to increase due to the high demand for the high quality image data, the word length of the shift registers to process large image data in image processing ICs. As the word length of the shift register become important design considerations. The smallest flip-flop is suitable for shift register to reduce the area and power consumption, the pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches. The shift register solves timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal.

Jin-Fa Lin and Yin-Tsung Hwang et.al., (2017) determines an ultralow-power true single-phase clocking flip-flop (FF) design achieved using only 19 transistors is proposed. The design follows a master-slave-type logic structure and features a hybrid logic design comprising both static-CMOS logic and complementary pass-transistor logic. In the design, a logic structure reduction scheme is employed to reduce the number of transistors for achieving high power and delay performance. Despite its circuit simplicity, no internal nodes are left floating during the operation to avoid leakage power consumption. In this design, a virtual V_{DD} design technique, which facilitates a faster state transition in the slave latch, is devised to enhance time performance. In circuit implementation, transistor sizes are optimized with respect to the power-delay product (PDP). A TSMC 90-nm CMOS process was selected as the implementation technology. In this paper, the performance levels of seven FF designs were compared. The timing parameters of each FF were first characterized. Post-layout simulation results indicated that the proposed design excelled in various performance indices such

as PDP, clock-to-Q delay, average power consumption, and leakage power consumption. Moreover, the design was determined to have the smallest layout area. The key idea is providing an additional discharge path between the master and slave latches, which not only shortens the transition time to enhance the power and speed performance, but also reduces circuit complexity for better timing parameters. Extensive simulations were conducted and various performance indices such as power consumption, PDP, setup time delay, and CQ delay were evaluated. The proposed design was determined to excel in almost every performance index, except for hold time performance. In particular, the proposed design consistently outperformed other designs under different voltage and switching activity settings. This thus proves the efficiency of the proposed FF design.

Leen Q asem, Dima Kilani, Baker Mohammad and Mihai sanduleanu et.al., (2017) determines the digital LDO (DLDO) regulator utilizing a time-based comparator rather than a voltage-based comparator in order to exploit the advantages of time domain and produce a more robust regulator. The time-based comparator compares between the reference and the load voltage levels and generates a digital bit that turns on/off the PMOS power switch. It consists of three main blocks: starved inverter, phase detector and SR latch. The starved inverter acts as a voltage to time converter where it converts both reference and load voltages into time waveforms. Then, the phase detector detects the difference between the two voltage values and generates a digital signal that enables the SR latch. Finally, the SR latch activates/deactivates the PMOS power switch to support the desired load voltage level. The time-based DLDO has an input voltage range between 0.8V and 0.6V and generates a load voltage range between 0.7V to 0.5V for a load current between 50 μ A and 300 μ A. The design is done in 65nm TSMC. The detailed simulation results confirmed a peak current efficiency of 99% by consuming a quiescent current of 1 μ A at $V_L=0.5V$. The load transient response time of 2.4ns at $V_L=0.7V$. The PMU includes various techniques to save the overall power consumption of the device. One of these techniques is voltage scaling which allows the SoC to operate at optimum power performance point [3]. Since the SoC has multiple subsystems such as multimedia, communication and processing, there is a need to derive multiple voltages at different levels to support

power efficiency for each subsystem. There are various techniques reported in the literature to control the PMOS switch of the DLDO regulator.

Zixin Zeng et.al., (2022) determines a data intensive industry, S&T intelligence is greatly affected by big data. How to build a S&T intelligence analysis system to adapt to the scientific paradigm, method and technology of big data has become an urgent problem in the field of S&T intelligence. With the guiding of system science, this paper discusses the characteristics of intelligence analysis in the era of big data, and presents a S&T intelligence analysis system architecture based on big data from the perspective of structure, elements and functions. Intelligence analysis in the era of big data has the characteristics of demand sensitivity, multi-source data, analysis intelligence, real-time computing, service embeddedness, result confidentiality and so on. In view of these characteristics, an architecture of S&T intelligence analysis system based on big data, which facilitates statistical analysis and mining of multi-source heterogeneous data through various big data processing platform and algorithms, and transforms information into useful decision-making intelligence that can support action, so as to realize the functions of intelligence identification, tracking, comparison, evaluation and forecast. The current system architecture will be further refined and improved in the future combined with related work.

Guo-Ming Sung et.al., (2015) determines a 12-bit 200-MS/s CMOS digital transmitter based on the requirement of very-high-bit-rate digital subscriber loop (VDSL). The entire architecture of the digital transmitter is composed of a digital-to-analog converter (DAC) and a fully differential current-mode line driver, which is fabricated in TSMC 90-nm 1P9M CMOS technology. The proposed 12-bit DAC is split into three stages. The first and second stages are a 6-bit sub-DAC and a 3-bit sub-DAC, which are implemented in thermometer code, and the last stage is a 3-bit sub-DAC, which is implemented in binary code for reducing the layout area and relaxes the circuit complexity. A small current source is used not only to isolate the output of digital circuit but also to reduce the current glitch. The DAC operates with a differential output current, which ranges from -4.095 mA to $+4.095\text{ mA}$, and its power consumption is about 5.0074 mW . The chip size is about $0.667 \times 0.613\text{ mm}^2$. Furthermore, an impedance synthesis is utilized to eliminate the matching

resistor which works with extra power consumption. The capacitive feed-forward path is introduced to reduce the crossover distortion and to increase linearity. According to the simulated results, the output voltage of line driver is 4 V PP with a differential load of 100 Ω . The power consumption is about 5.4579 mW.

Pranav R Patel et.al., (2018) indicates that the direct digital synthesis (DDS) architectures are becoming more prevalent as modern digital-to-analog converter (DAC) and programmable logic devices evolve to support higher bandwidths. The DDS architecture provides the benefit of digital control but at a cost of generating spurious content in the spectrum. The generated spurious content may cause intermodulation distortion preventing proper demodulation of the received signal. The distortion may also interfere with the neighboring frequency bands. This article presents the various DDS architectures and explores the DDS architecture which provides the most digital reconfigurability with the lowest spurious content. End-to-end analytical equations, numerical and mathematical models are developed to determine the location and power levels of spurs. Afterwards, the analytical equations, numerical and mathematical models are shown to be consistent with the experimental data. A developer can use the information to design a DDS architecture that meets their minimum requirements. The mathematical model is used to determine the power level of these spurs before the frequency folding occurs. When the sampling frequency at RF and divisible by the sampling frequency at IF, the spurs appear at every multiple of the sampling frequency at IF, and the power of spurs is a multiple of the phase resolution. This information can be used by the developer to minimize any kind of intermodulation distortion to the generated signal or in the neighboring bands.

Tippawan Meepung et.al.,(2016) determines the development of knowledge and skills of learners and teachers is a guideline for the development of new technologies and innovations which therefore affects the development of the knowledge-based economy. To make existing resources on campus to bring in values in a strategic manner by applying research to industrial use, it must use a support mechanism in the form of a digital technology ecosystem to transform the

traditional university operating model into a university that supports entrepreneurship. And in order for the university to develop and build strength from within: policies are needed to allocate appropriate internal resources and the understanding of intellectual property should be established. The results publishing with technology and mutual relationship between the industry and the government then should directly affect economic growth. The university is comprised of large and complex systems. Enterprise Architecture is a strategic planning tool for organizing technology in an organization. By following the principles and practices to Framework development of enterprise architecture developers, it results in an overall system in the organization for systematic design which is consisted of Business architecture, Data architecture, Applications architecture, and Technology architecture.

Yuling Chen et.al., (2014) indicates the modern electronic equipment is usually in a complex electromagnetic environment, and mutual interference is serious, especially in the modern battlefield, there are many military electronic equipment and the interference is complicated. Therefore, analog systems with poor anti-interference performance and flexibility are gradually unable to adapt to the complex communication environment. Therefore, research on digital systems with flexibility and strong anti-interference ability has become an inevitable trend in the development of modern communication equipment. In this regard, the purpose of this article is to study the application of FPGA array structure digital signal processing platform in the field of communication. This article first introduces the related concepts of FPGA technology and the basic working principle of the FPGA array structure digital signal processing platform. Afterwards, in order to realize the practical application of FPGA array structure digital signal processing platform in the communication field, a simple communication architecture platform based on FPGA is built. It is the application of FPGA array structure digital signal processing platform in the field of communication. Afterwards, in order to realize the practical application of FPGA array structure digital signal processing platform in the communication field, a simple communication architecture platform based on FPGA.

Patrick Valet et.al., (2015) implements a static digital pre-distortion (DPD) method for a current-steering digital-to-analog converter (CS-DAC). The proposed model utilizes the knowledge of the current cell array architecture to calculate the static mismatch currents of the cells. The converter corrects the static error with its own current cells without incorporating an additional calibration DAC (CALDAC) or programmable current sources. This results in a reduction in area, power and simulation run times because of the simpler circuit design. The proposed method is able to use an information signal for the calibration phase, thus it is possible to be implemented as a background calibration. The evaluation of the proposed DPD is done via simulations in MATLAB with a 14-bit static CS-DAC model. The results show a performance gain of the signal-to-noise-plus-distortion ratio (SNDR) of up to 16dB. The comparison to other state-of-the-art CS-DAC static calibration methods also shows competitive results. Further research needs to be done to gain knowledge on the effectiveness of the MBA with measurements on real silicon.

Hanwool Jeong et.al., (2014) determines a self-timed pulsed latch (STPL) is proposed for low VDD operation. By comparing input and output, the transparency window is adaptively generated in STPL, which resolves the hold time problem of the conventional pulsed latch. The measurement results from the test chip fabricated in the 65-nm technology proves that the hold time is reduced by 77% and the minimum operating supply voltage is lowered by 300 mV compared with the conventional pulsed latch. In addition, the measurement results show that the STPL can reduce the sequential overhead, because the STPL is free from setup time issue from which the conventional master–slave-based flip-flop (MSFF) suffers. The simulation results show that the input-to-output delay of STPL, which also determines the sequential overhead, is smaller by 45% in 0.6 V compared with that of the MSFF structure. From battery-powered portable devices, such as smartphones and IOT devices, to high-performance processors for recently spotlighted applications, such as artificial intelligence and crypto-mining, the low-power circuit design becomes important. As the dynamic power of electronic circuits has a quadratic dependence on the supply voltage (VDD), scaling VDD is the most effective approach to achieve the goal of low power consumption. However, in the low VDD region, sequencing elements—pulsed

latches or flip-flops—suffer from unacceptably increased sensitivity to process variation and significant speed degradation. To resolve this problem, a pulsed latch can be used instead of MSFF. Because of negative or near zero t_{setup} , a pulsed latch is robust to the timing overhead increased by t_{setup} variation. However, the pulsed latch suffers from a large hold time (thold) problem. In a low V_{DD} region, the width of pulse triggering latches—or transparent window—significantly varies. To guarantee a stable data capture operation, a large timing margin is required on the size of the transparent window.

Yutai Sun et.al (2016)., indicates that the belief propagation (BP) decoding has the advantage of providing soft information iteratively, which allows polar codes to be applicable in scenarios requiring high throughput. However, the unsatisfactory error-correction performance makes the BP polar decoding unable to compete with the successive cancellation list (SCL) decoding that is the baseline algorithm in 3GPP. The BP flip (BPF) decoding offers one option to address this issue through additional decoding attempts with a few bits flipped. However, current BPF decoders yield less efficient flipping accuracy. Considering the complex bit correlation and unanalyzable erroneous bit probability of BPF decoding, we propose a long short-term memory (LSTM) network-assisted BPF (LSTM-BPF) decoding algorithm. Given the soft information output by the original BP decoding, the trained LSTM network achieves more accurate erroneous bit prediction ability. The simulation results show that compared with the state-of-the-art BPF decoders, the LSTM-BPF decoder improves the hit rate of the error bits by 10%, thereby obtaining more than 0.1 dB gains at a frame error rate (FER) of 10^{-4} for polar codes with length 128 and code rate 0.5. The efficient hardware architecture of the proposed LSTM-BPF decoder is designed. By introducing a critical set to reduce the size of the network, the LSTM accelerator could significantly reduce the required computation and storage resources, thereby reducing the inference time. a BPF algorithm based on LSTM network is proposed, and the error correction performance is improved. At the same time, the corresponding hardware architecture is also designed. In future work, we will focus on the apply the LSTM network to the higher-order BPF decoding.

Kannadhasan Suriyan et.al., (2020) determines wasteful patterns that lead to fault dropping squander a tone of energy in the linear-feedback shift register and circuit under examination in a random research region. Random switching actions in the CUT and scan pathways between applications with two consecutive vectors are another significant cause of energy loss. This study proposes a unique built-in selftest (BIST) technique for scan-based circuits that might help save energy. Only the available vectors are produced in a fixed series thanks to a mapping logic that alters the state transitions. As a consequence, and without reducing fault coverage, the time it takes to execute trials has decreased. Experiments on circuits demonstrated that during random testing, the linear feedback shift register saves a significant amount of power. The built-in self-test technology is used to monitor VLSI circuits, removing the requirement for extra research facilities. This technique allows several circuits to be tested online at the same time. The purpose of the proposed project is to build a logic module that stores input test vectors in static random access memory SRAM cells and reduces switching operations, resulting in faster testing and lower concurrent test latency. The stated approach may be used with any kind of integrated circuit. Instead of requiring the circuit to be turned off, the input vector monitoring concurrent built-in self-test system monitors it while it is running. As a consequence, they may have difficulties similar to offline built-in self-test methodologies, such as longer testing periods and higher power consumption. The amount of development flaws grows as feature sizes decrease, making fault identification more challenging. VLSI testing is getting more required and sophisticated as more devices are integrated on a large scale in order to confirm that they are running correctly.

Rustam khalirbaginov et.al., (2017) determines that all-digital phase-locked loop (ADPLL) design method based on standard cells. A new portable architecture introduced. Its motor is a fully synthesizable description of a digital controlled oscillator (DCO) with variable length ring oscillator (VLRO) as coarse part and fine-tune unit based on path selector of different pin-to-pin delays in NAND standard cell. Time to digital converter (TDC) circuit with a two- level structure has been added to reduce the oscillator frequency initial coarse-tune time. TDC allows finding the desired output frequency in two reference clock cycles. The two- level structure reduces the hardware costs of implementing this

block. The circuit is designed using standard library cells only and is described in Verilog HDL. This enables design automation and simplifies the design of digital signal processing circuits for modern System-on-a-Chip. The Verilog HDL parametrized description of the ADPLL allows to reconfigure design for any other requirements and tech node. This enables design automation and simplifies the design of digital signal processing circuits for modern System-on-a-Chip.

2.2 LITERATURE SUMMARY

The code converter includes a plurality of serial shift registers arranged to convert an input to a thermometer output. The code converter further includes a plurality of clock control circuits each configured to provide a clock to a corresponding one of the shift registers. A method of generating a signal in thermometer code is provided. The code converter further includes means for enabling a subset of the shift registers. The method includes enabling a subset of a plurality of shift registers and converting an input to a thermometer output by the plurality of shift registers. Aspects of a code converter are disclosed. It is understood that other aspects of apparatus and methods will become readily apparent to those skilled in the art from the following detailed description, wherein various aspects of apparatus and methods are shown and described by way of illustration. As will be realized, these aspects may be implemented in other and different forms and its several details are capable of modification in various other aspects.

2.3 PROBLEM DEFINITION

To analyze an efficient graphene based field effect transistor for digital applications.

2.4 OBJECTIVES OF THE PROJECT

- To increase the efficiency of the Low-Area and Low-Power Latch-Based Thermometer Code Shift Register.
- In order to improve Efficiency Low Power Techniques will be applied in all Circuits.
- To compare, the characteristics of MOSFET Technology in terms of Power, Delay and Power Delay Product.
- To identify the Feasibility of Low-Area and Low-Power Latch-Based Thermometer Code Shift Register.

CHAPTER 3

EXISTING METHODOLOGY

In the existing work there is a Shift register designed using Flip flop and XOR. In the proposed work the shift register is designed using a modified Flip flop with the sleepy keeper technique which has low power consumption and lesser delay compared to the existing design.

3.1 CMOS TECHNOLOGY

CMOS, which is short for Complimentary Metal-Oxide Semiconductor, is a predominant technology for manufacturing integrated circuits. This dominance of CMOS Technology in the fabrication of Integrated Circuits or ICs will continue for decades to come. Generally, the CMOS Technology is associated with VLSI or Very Large-Scale Integrated Circuit, where a few millions or even billions of transistors (Moseys to be specific) are integrated into a single chip or die. The reasons for the dominant use of CMOS Technology in the fabrication of VLSI chips are reliability, low power consumption, considerably low cost and most importantly scalability. You might have heard of the famous Moore's Law described by Gordon Moore, according to whom, the number of devices on a chip will double every 18 to 24 months. Even though Gordon Moore did not imply it to CMOS, the Moore's Law has been successfully fulfilled due to the CMOS technology.

The CMOS Technology uses both NMOS and PMOS to realize various logic functions. Both the N-channel MOSFET and the P-channel MOSFET are designed in such a way that they have matching characteristics (during ON and OFF state). The main advantage of CMOS technology over Bipolar or the previous popular NMOS technologies is its extremely low power consumption in static conditions as they draw power only during switching operation. This allows integrating much larger number of logic gates on the VLSI IC when compared to Bipolar or NMOS technologies.

Today, CMOS technology is the dominant IC fabrication technology in VLSI industry and is used for making high end microprocessors, microcontroller, memory modules, sensors and Application Specific Integrated Circuits (ASICs) the combination of NMOS and PMOS devices in a CMOS logic makes it easier to

design different logic functions. With the improvements in CMOS IC fabrication technologies, the size of the transistor can be scaled down in size. Downscaling the size of the transistor implies that more logical functions can be integrated into the same IC without compromising the speed and power. Initially, the CMOS IC Technology was used in the fabrication of Digital Logic ICs. The development towards low cost and increased functionality has led to CMOS technology being used in Analog ICs and Mixed Signal Designs.

3.1.1 MOS Logic Families

The following is a list of the MOS Logic Families.

- PMOS Family (uses p-Channel MOSFET)
- NMOS Family (uses n-Channel MOSFET)
- CMOS Family (uses both p-Channel MOSFET and n-Channel MOSFET)

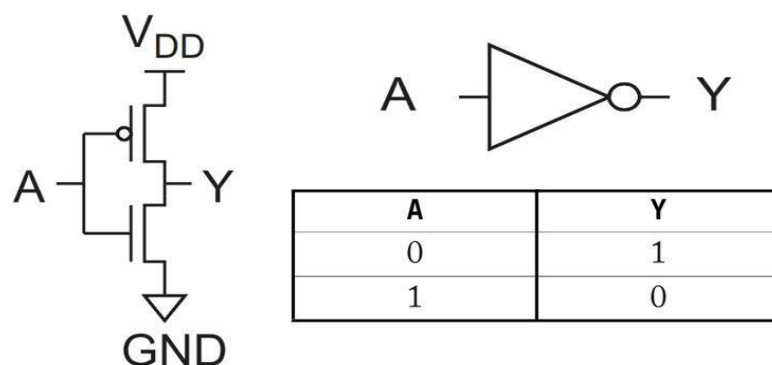


Figure 3.1.1 Circuit of CMOS inverter and gate symbol

3.1.2 PRINCIPLE BEHIND CMOS LOGIC

The name complementary in CMOS refers to the fact that both NMOS and PMOS Transistors are used in the same design. The main principle behind a CMOS logic gate is that the NMOS Transistors act as Pull-down network to connect Output to GND and the PMOS Transistors act as Pull-up network to connect V_{DD} to Output.

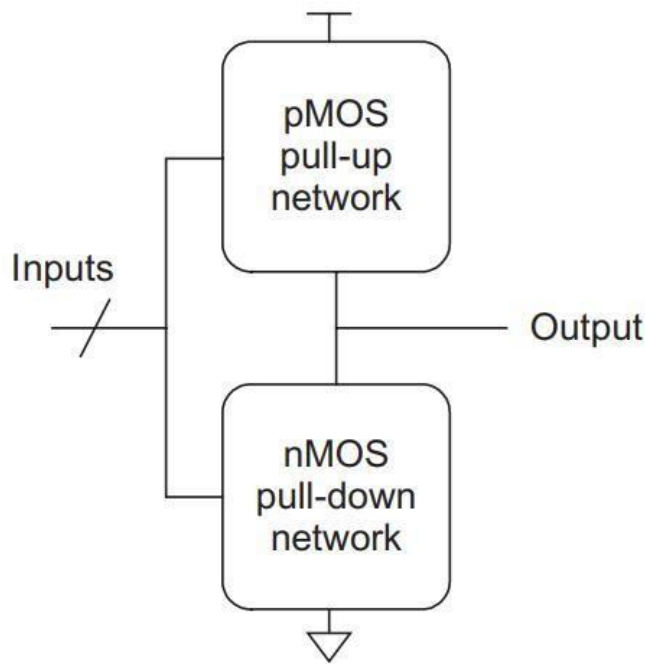


Figure 3.1.2 Circuit of CMOS inverter and gate symbol

CMOS logic is arranged in such a way that only one of the pull-up or pull-down networks is ON while the other is OFF with the help of a single input. CMOS Inverter is also known as the NOT Gate. From the above circuit, you can see that a CMOS Inverter consists of an N-channel MOSFET (NMOS) and a P-channel MOSFET (PMOS). When the input A is LOW i.e. Logic 0, the NMOS Transistor is OFF and the PMOS Transistor is ON. The P-channel MOSFET provides a path for the V_{DD} to appear at the Output. Hence, the output is HIGH i.e. Logic 1. Similarly, when the input is HIGH, NMOS is ON and PMOS is OFF. The output is connected to GND and the output is low.

3.1.3 PMOS LOGIC

P-type metal-oxide-semiconductor logic uses p-channel (+) metal-oxide-semiconductor field effect transistors (MOSFETs) to implement logic gates and other digital circuits. PMOS transistors operate by creating an inversion layer in an n-type transistor body. This inversion layer, called the p-channel, can conduct holes between p-type "source" and "drain" terminals e output is LOW.

The p-channel is created by applying voltage to the third terminal, called the gate. Like other MOSFETs, PMOS transistors have four modes of operation: cut-off (or sub threshold), triode, saturation (sometimes called active), and velocity saturation.

While PMOS logic is easy to design and manufacture (a MOSFET can be made to operate as a resistor, so the whole circuit can be made with PMOS FETs), it has several shortcomings as well. The worst problem is that there is a direct current (DC) through a PMOS logic gate when the PUN is active, that is, whenever the output is high, which leads to static power dissipation even when the circuit sits idle.

Also, PMOS circuits are slow to transition from high to low. When transitioning from low to high, the transistors provide low resistance, and the capacitive charge at the output accumulates very quickly (similar to charging a capacitor through a very low resistance). But the resistance between the output and the negative supply rail is much greater, so the high-to-low transition takes longer (similar to discharge of a capacitor through a high resistance). Using a resistor of lower value will speed up the process but also increases static power dissipation.

Additionally, the asymmetric input logic levels make PMOS circuits susceptible to noise. Most PMOS integrated circuits require a power supply of 17-24volt DC. The Intel 4004 PMOS microprocessor, however, uses PMOS logic with polysilicon rather than metal gates allowing a smaller voltage differential. For compatibility with TTL signals, the 4004 uses positive supply voltage $V_{SS}=+5V$ and negative supply voltage $V_{DD} = -10V$. Though initially easier to manufacture, PMOS logic was later supplanted by NMOS logic using n-channel field-effect transistors. NMOS is faster than PMOS. Modern integrated circuits are CMOS logic, which uses both p-channel and n-channel transistors.

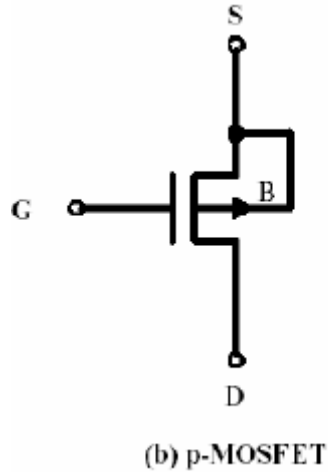


Figure 3.1.3 PMOS Symbol

3.1.4 NMOS LOGIC

N-type metal-oxide-semiconductor logic uses n-type (-) MOSFETs (metal-oxide-semiconductor field-effect transistors) to implement logic gates and other digital circuits. These NMOS transistors operate by creating an inversion layer in a p-type transistor body. This inversion layer, called the n-channel, can conduct electrons between n-type "source" and "drain" terminals. The n-channel is created by applying voltage to the third terminal, called the gate. Like other MOSFETs, NMOS transistors have four modes of operation: cut-off (or sub threshold), triode, saturation (sometimes called active), and velocity saturation.

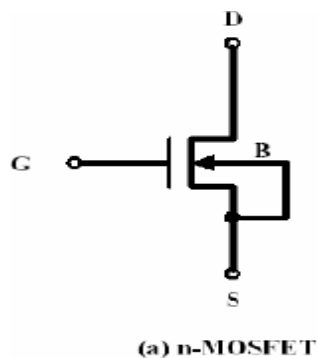


Figure 3.1.4 Circuit of NMOS

3.2 Linear feedback shift register

A Linear Feedback Shift Register (LFSR) is a shift register wherein its input bit is a linear function of its previous state and input bit is driven by the exclusive-or (XOR) of few bits of the overall shift register value. The linear feedback shift register is one of the most frequently used modules in Test Pattern Generator (TPG) and signature analysis (or Output Response Analyser) for BIST applications. One of the key reasons behind employing LFSR in TPGs is that these are more area efficient than a counter i.e., LFSR requires less combinational logic per flip-flop.

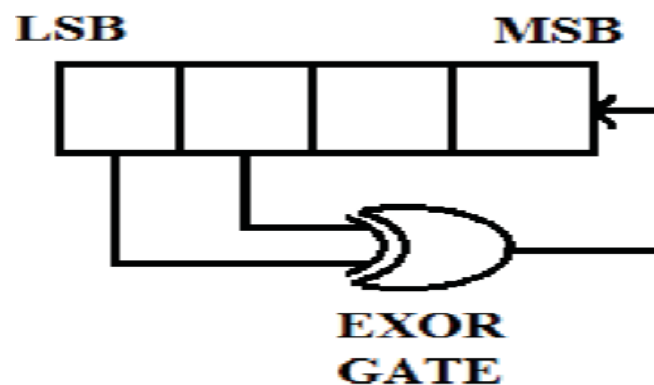


Figure 3.2 LFSR

3.2.1 Operations and Characteristics of LFSR

To start with LFSR must be initialized; it should be initialized or seeded to a non-zero value. LFSRs at any cost cannot have the value of zero as each shift of a zeroed LFSR will leave it as zero. When LFSR holds '1' and is shifted once, its value will always be the value of the polynomial mask. When LFSR a better sequence of numbers can be produced and the lower bits will be used for the random numbers. This tends to solve the problem of obtaining zeros, but there is all zeros in the register except that in most significant bit, then the next several shifts shows the high bit shift to the low bit with zero fill. A fundamental LFSR does not produce very good random numbers. On picking a larger even then the numbers do not exhibit good statistical properties. On the other hand, one can use a subset of the LFSR for a random number to increase the permutations of the numbers and as well to improve the random properties of the LFSR output. The statistical property may be improved by shifting the LFSR more than once

before getting a random number. As well, shifting the LFSR by a factor of its period will reduce the total period length by that factor

The maximum-length of an LFSR sequence is $(2^n - 1)$ and does not generate all zeros pattern (gets stuck in that state). A maximum-length sequence pseudo random. In this case, the number of ones will be equal to the number of (0s+1). An LFSR is defined completely by its polynomial. A generated sequence of binary numbers can be represented employing a generation function (polynomial). The initial value of the LFSR is called the 'seed'. The behaviour of an LFSR is determined by its initial "seed" and its feedback coefficients that are represented by polynomials

3.3 Types of LFSR implementation

In LFSRs, 'n' refers to the degree of the polynomial and it results in an 'n-bit' LFSR. The construction of LFSR is defined by the characteristic polynomial and the degree of the polynomial indicates the number of flip-flops and the number of non-zero coefficients. LFSR implementation is performed in two types,

Internal Feedback Shift Register

External Feedback Shift Register

3.3.1 Internal Feedback Shift Register

In this case, XOR gates feed into different registers within the LFSR and are not sequential. XORs are just present inside the shift register. For the characteristic polynomial defined by,

$$A(X) = 1 + x + x^3 + x^4$$

Where, 'x' is the coefficients of the polynomials. The internal feedback shift register

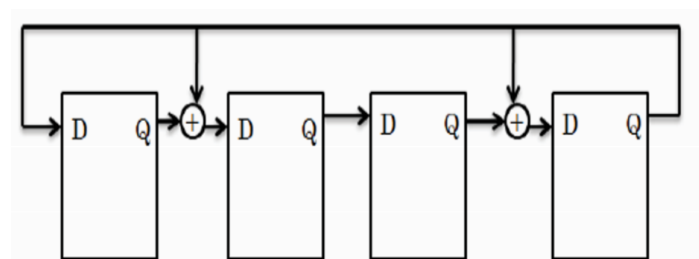


Figure 3.3.1 Internal feedback shift register

3.3.2 External Feedback Shift Register

The second way of implementing LFSR is that, all XOR gates are fed sequentially into one another and it gets ends up as the input to the least significant bit of the LFSR. XORs acts as the external from the shift register. For the characteristic polynomial defined in the external feedback shift register

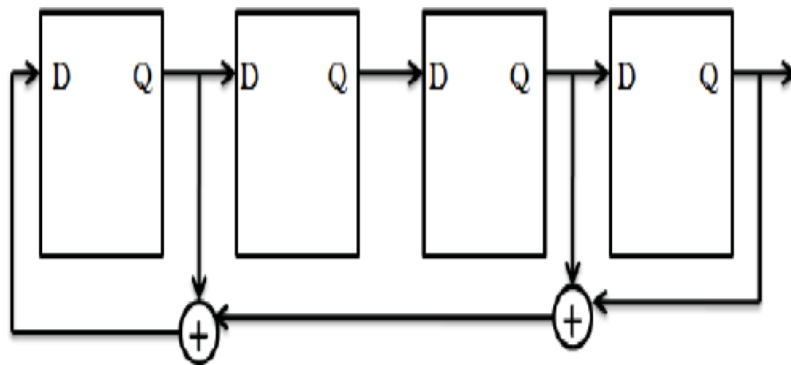


Figure 3.3.2 External feedback shift register

The shift registers consists of four flip-flops and hence the degree of polynomial is '4'. The characteristic polynomials are defined by XOR positions. The 'XOR' feedback connections to the 'i-th' flip-flop are the coefficient of X_i . When there exists connection, the coefficient of X_i will be '1' and if no connection is there, then the value of X_i is '0'. The coefficients always get included in the characteristic polynomial. The state of the LFSR is the polynomial of degree $n-1$.

3.4 HSPICE SOFTWARE

Hewlett Simulation Program with Integrated Circuit is the full name of HSPICE. Integrated circuits, unlike board-level designs composed of discrete parts, are impossible to breadboard before manufacture. Further, the high costs of photolithographic masks and other manufacturing prerequisites make it essential to design the circuit to be as close to perfect as possible before the integrated circuit is first built. Simulating the circuit with SPICE is the industry-standard way to verify circuit operation at the transistor level before committing to

manufacturing an integrated circuit. For example, it will draw out circuits and simulate what happens when the circuits are powered up and behave under different emergency conditions.

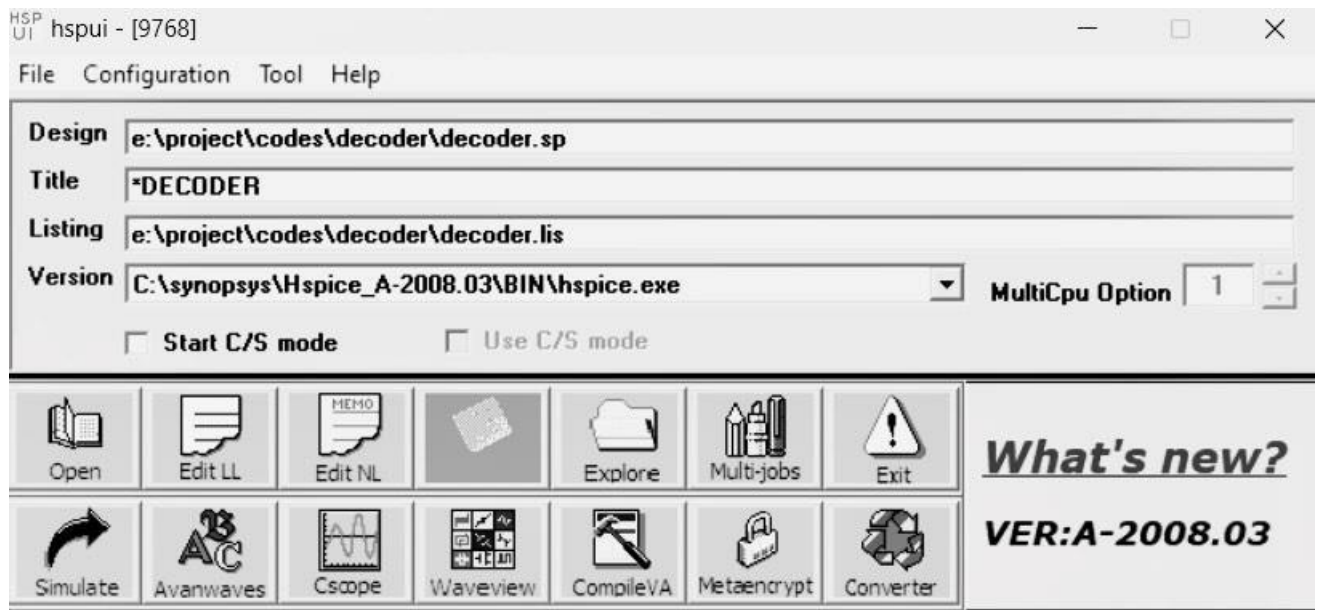


Fig 3.4 Hspice Software

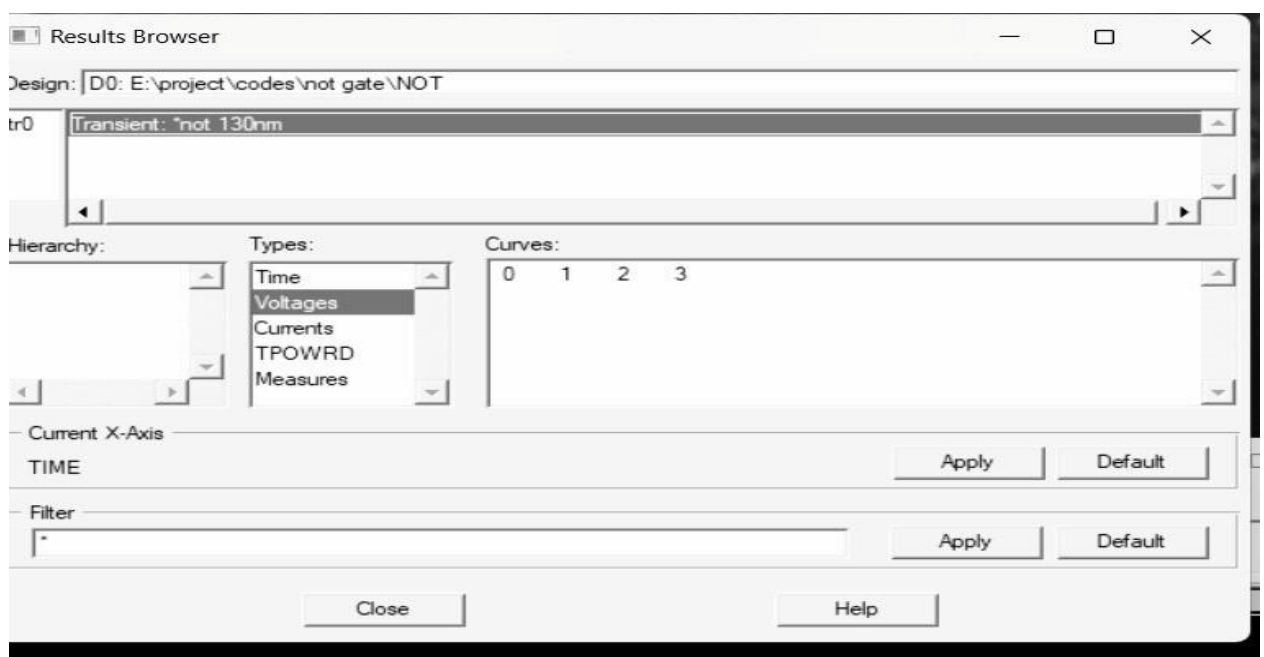


Fig 3.4.1 Result Browser of Hspice Software

3.4.2 SIMULATED WAVEFORM

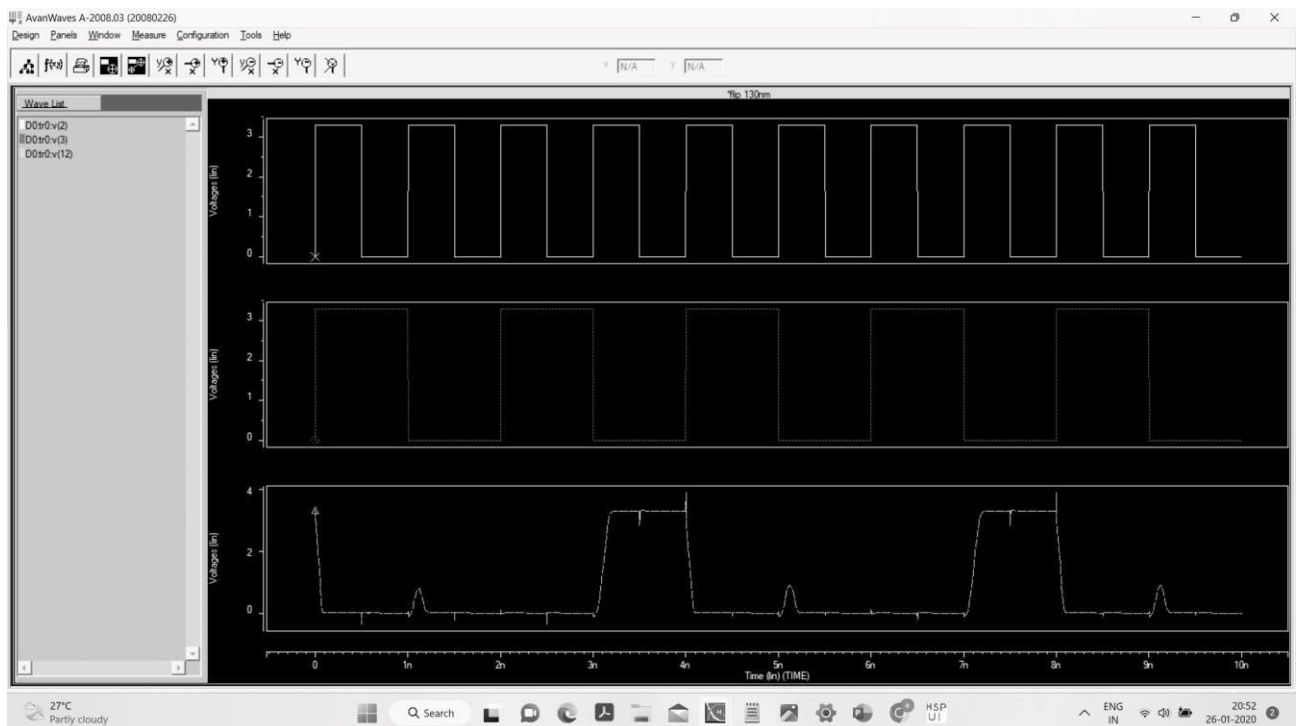


Fig 3.4.2 Simulated Waveform

3.5 COSMOSCOPE

Cosmoscope is a software which is used to calculate the delay value. In software development it is often very useful to be able to find the callers of a function because this is the way to understand how code works and what other parts of the program expect from a function. Cosmoscope can find the callers and callees of functions, but it is not a compiler and it does that by searching the text for keywords. This has the disadvantages that macros and duplicate symbol names can generate an unclear graph.

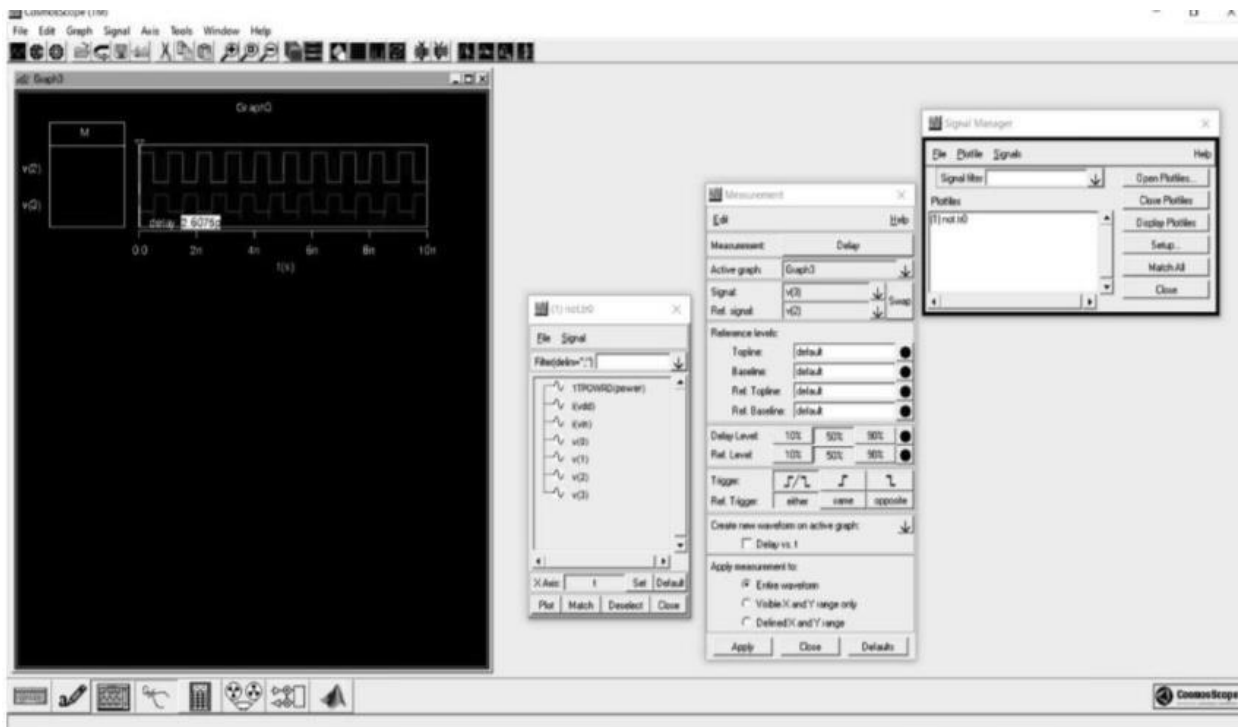


Fig 3.5 Cosmoscope

3.5.1 POWER

Electric power is the rate at which electrical energy is transmitted by an electric circuit per unit of time. It is the pace at which work is completed. Electrical power is the rate at which electrical energy is transmitted by an electric circuit per unit time in terms of an electrical circuit.

The unit of the Electric Power = Watt

$$\text{Power} = V \cdot I (W)$$

$$I = Q/t$$

Where:

W	=	power	in	watts
V	=	current	in	amps
Q	=	charge	in	coulombs
T	=	time	in	seconds

3.5.2 DELAY

The time it takes for a signal to reach its destination is referred to as delay. The time it takes for the consequence of a shift in input to be noticeable at the output is known as the delay of a logic gate.

3.5.3 POWER DELAY PRODUCT

Power Delay Product is the product of the power and delay. Also known as switching energy, it is the product of power consumption P (averaged over a switching event) times the input–output delay or duration of the switching event D . It has the dimension of energy and measures the energy consumed per switching event. In a CMOS circuit the switching energy and thus the PDP for a 0-to-1-to-0 computation cycle is $C_L \cdot V_{DD}^2$. Therefore, lowering the supply voltage V_{DD} lowers the PDP.

Energy-efficient circuits with a low PDP may also be performing very slowly, thus energy–delay product (EDP), the product of E and D (or P and D^2), is sometimes a preferable metric.

In CMOS circuits the delay is inversely proportional to the supply voltage V_{DD} and hence EDP is proportional to V_{DD} . Consequently, lowering V_{DD} also benefits EDP.

$$\text{PDP} = \text{Power} * \text{Delay}$$

CHAPTER 4

PROPOSED METHODOLOGY

4.1 PROPOSED THERMOCODE SHIFT REGISTER

In order to improve efficiency, existing system as Thermometer code shift register will be analyzed using 130nm, 32nm, CMOS technology. Further, thermometer code shift register will be modified and analyzed using 130nm, 32nm CMOS technology. In terms of power, speed and power delay product. Also the proposed system will be analyzed and compared using 32nm GNRFET technology. This outperforms an efficient thermometer code shift register for high speed and low power applications.

4.2 GNRFET

The graphene nano-ribbon field effect transistor (GNRFET) is an emerging technology that received much attention in recent years. Recent work on GNRFET circuit simulations has shown that GNRFETs may have potential in low power applications. Graphene nanoribbons are strips of graphene with width less than 100 nm.

Graphene nanoribbons can be analyzed by scanning tunneling microscope, Raman spectroscopy infrared spectroscopy, and X-ray photoelectron spectroscopy. For example, out-of-plane bending vibration of one C-H on one benzene ring, called SOLO, which is similar to zigzag edge, on zigzag GNRs has been reported to appear at 899 cm^{-1} , whereas that of two C-H on one benzene ring, called DUO, which is similar to armchair edge, on armchair GNRs has been reported to appear at 814 cm^{-1} as results of calculated IR spectra.

However, analyses of graphene nanoribbon on substrates are difficult using infrared spectroscopy even with a Reflection Absorption Spectrometry method. Thus, a large quantity of graphene nanoribbon is necessary for infrared spectroscopy analyses. Zigzag edges are known to be more reactive than armchair edges, as observed in the dehydrogenation reactivities between the compound with zigzag edges (tetracene) and armchair edges (chrysene). Also, zigzag edges tends to be more oxidized than armchair edges without gasification.

The zigzag edges with longer length can be more reactive as it can be seen from the dependence of the length of acenes on the reactivity. Graphene nanoribbons and their oxidized counterparts called graphene oxide nanoribbons have been investigated as nano-fillers to improve the mechanical properties of polymeric nanocomposites. Increases in the mechanical properties of epoxy composites on loading of graphene nanoribbons were observed. An increase in the mechanical properties of biodegradable polymeric nanocomposites of poly(propylene fumarate) at low weight percentage was achieved by loading of oxidized graphene nanoribbons, fabricated for bone tissue engineering applications.

Hybrid imaging modalities, such as photoacoustic (PA) tomography (PAT) and thermoacoustic (TA) tomography (TAT) have been developed for bio imaging applications. PAT/TAT combines advantages of pure ultrasound and pure optical imaging/radio frequency (RF), providing good spatial resolution, great penetration depth and high soft-tissue contrast. GNR synthesized by unzipping single- and multi-walled carbon nanotubes have been reported as contrast agents for photoacoustic and thermoacoustic imaging and tomography.

Large quantities of width-controlled GNRs can be produced via graphite nanotomy, where applying a sharp diamond knife on graphite produces graphite nanoblocks, which can then be exfoliated to produce GNRs as shown by Vikas Berry. GNRs can also be produced by "unzipping" or axially cutting nanotubes. In one such method multi-walled carbon nanotubes were unzipped in solution by action of potassium permanganate and sulfuric acid. In another method GNRs were produced by plasma etching of nanotubes partly embedded in a polymer film.^[8] More recently, graphene nanoribbons were grown onto silicon carbide substrates using ion implantation followed by vacuum or laser annealing. The latter technique allows any pattern to be written on substrates with 5 nm precision. GNRs were grown on the edges of three-dimensional structures etched into silicon carbide wafers. When the wafers are heated to approximately 1,000 °C (1,270 K; 1,830 °F), silicon is preferentially driven off along the edges, forming nanoribbons whose structure is determined by the pattern of the three-dimensional surface. The ribbons had perfectly smooth edges, annealed by the fabrication process. Nanoribbons narrower than 10 nm grown on

a germanium wafer act like semiconductors, exhibiting a band gap. Inside a reaction chamber, using chemical vapor deposition, methane is used to deposit hydrocarbons on the wafer surface, where they react with each other to produce long, smooth-edged ribbons.

The ribbons were used to create prototype transistors. At a very slow growth rate, the graphene crystals naturally grow into long nanoribbons on a specific germanium crystal facet. By controlling the growth rate and growth time, the researchers achieved control over the nanoribbon width. The method unintentionally overlapped some nanoribbons, allowing the study of multilayer GNRs. Such overlaps could be formed deliberately by manipulation with a scanning tunneling microscope. Hydrogen depassivation left no band-gap. Covalent bonds between the Si surface and the GNR leads to metallic behavior. The Si surface atoms move outward, and the GNR changes from flat to distorted, with some C atoms moving in toward the Si surface. The electronic states of GNRs largely depend on the edge structures (armchair or zigzag). In zigzag edges each successive edge segment is at the opposite angle to the previous. In armchair edges, each pair of segments is a 120/-120 degree rotation of the prior pair.

Zigzag edges provide the edge localized state with non-bonding molecular orbitals near the Fermi energy. They are expected to have large changes in optical and electronic properties from quantization. Graphene nanoribbons possess semiconductive properties and may be a technological alternative to silicon semiconductors capable of sustaining microprocessor clock speeds in the vicinity of 1 THz field-effect transistors less than 10 nm wide have been created with GNR with an ratio $>10^6$ at room temperature.

4.3 UNIDIRECTIONAL AND BIDIRECTIONAL LATCHES

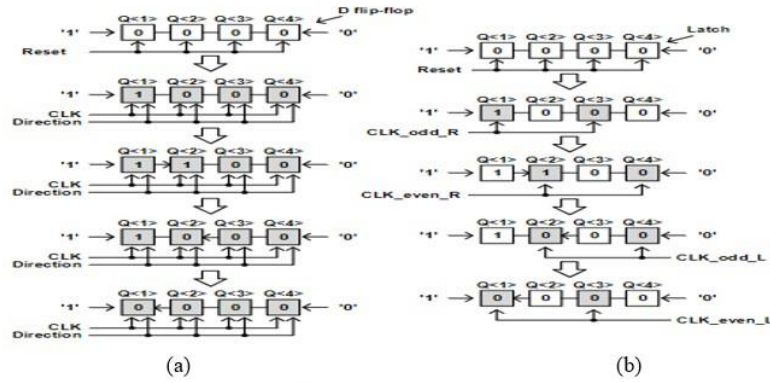


Figure 4.3.1 (a) Proposed bidirectional 4-bit D-FF based thermometer-code shift-register (b) Bidirectional 4-bit latch-based thermometer-code shift-register

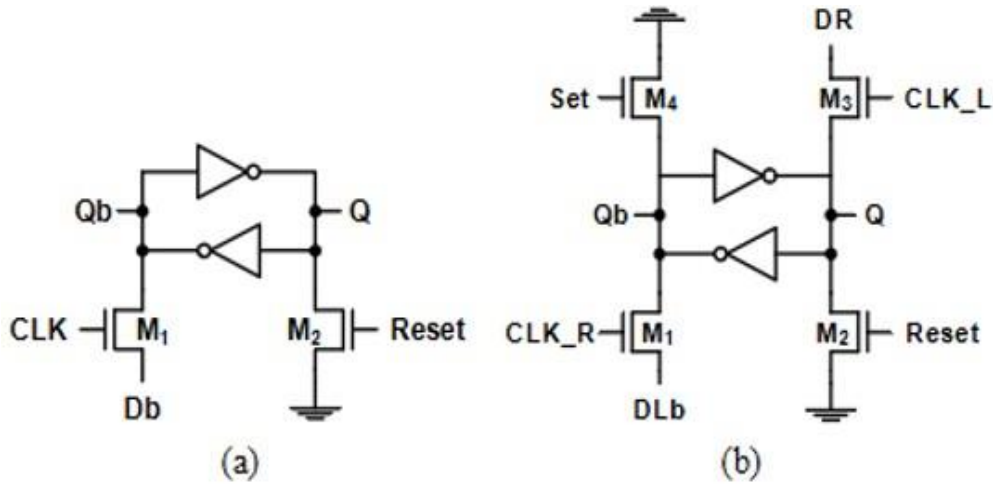


Figure 4.3.2 Thermometer code latches (a) Unidirectional (b) bidirectional.

When it is bi directional the clock is high (CLK='1') and the inverted data input from the left latch is ground (Db='0'). It resets the latch (Q and Qb) by discharging Q to ground via M2, when the Reset signal is high. The bidirectional latch receives the data '1' from the left latch and the data '0' from the right latch. It updates the data Q to the data '1' by discharging Qb to ground via M1, when the

inverted data input from the left latch ($DLb=0$) is ground and the clock for right-shifting (CLK_R) is high. It updates the data Q to the data '0' by discharging Q to ground via $M3$, when the data input from the right latch ($DR=0$) is ground and the clock for left-shifting (CLK_L) is high. It resets the latch (Q and Qb) by discharging Q to ground via $M2$, when the Reset signal is high. It sets the latch (Q and Qb) by discharging Qb to ground via $M4$, when the Set signal is high.

Fig 4.3.1(a) shows the unidirectional 64-bit thermometer-code shift-register. It consists of a clock signal generator and N unidirectional (UD) thermometer-code latches. The UD latch receives the inverted data output (Qb) of the left latch. The clock signal generator in Fig. 4.3.1(a) makes two clock signals (CLK_{odd} and CLK_{even}), which enable odd and even UD latches, alternately, as shown in Fig. 4.3.1(b). Fig. 4.3.2(b) shows the bidirectional 64-bit thermometer-code shift-register.

It consists of a bidirectional clock signal generator and N bidirectional (BD) thermometer-code latches. The bidirectional latch receives the inverted data output (Qb) from the left latch and the data output (Q) from the right latch. The bidirectional clock signal generator in Fig. 4.3.1(b) makes four clock signals according to the direction signal. It shifts the data '1' right or the data '0' left according to two clock signals for right-shifting (CLK_{odd_R} and CLK_{even_R}) or two clock signals for left-shifting (CLK_{odd_L} and CLK_{even_L}), respectively, as shown in Fig. 4.3.2(b).

The mode control input is connected to logic 1 for parallel loading operation whereas it is connected to 0 for serial shifting. With mode control pin connected to ground, the universal shift register acts as a bi-directional register. For serial left operation, the input is applied to the serial input which goes to AND gate-1. Whereas for the shift right operation, the serial input is applied to D input.

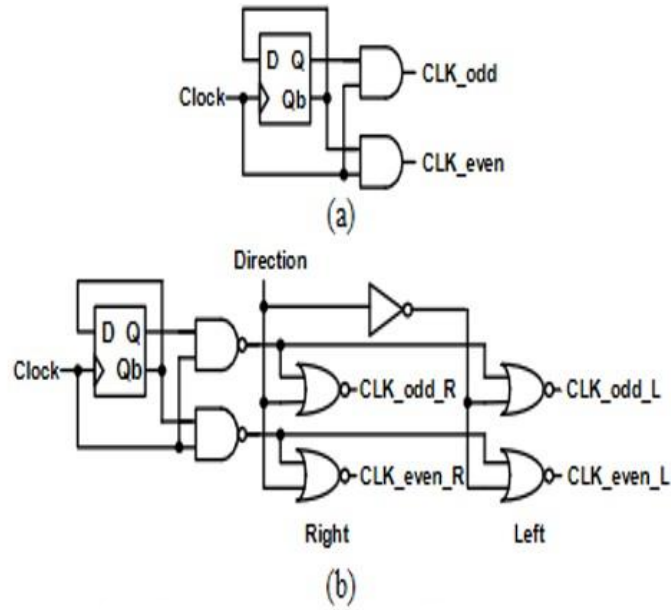


Figure 4.3.3 Clock signal generator (a) unidirectional (b) bidirectional

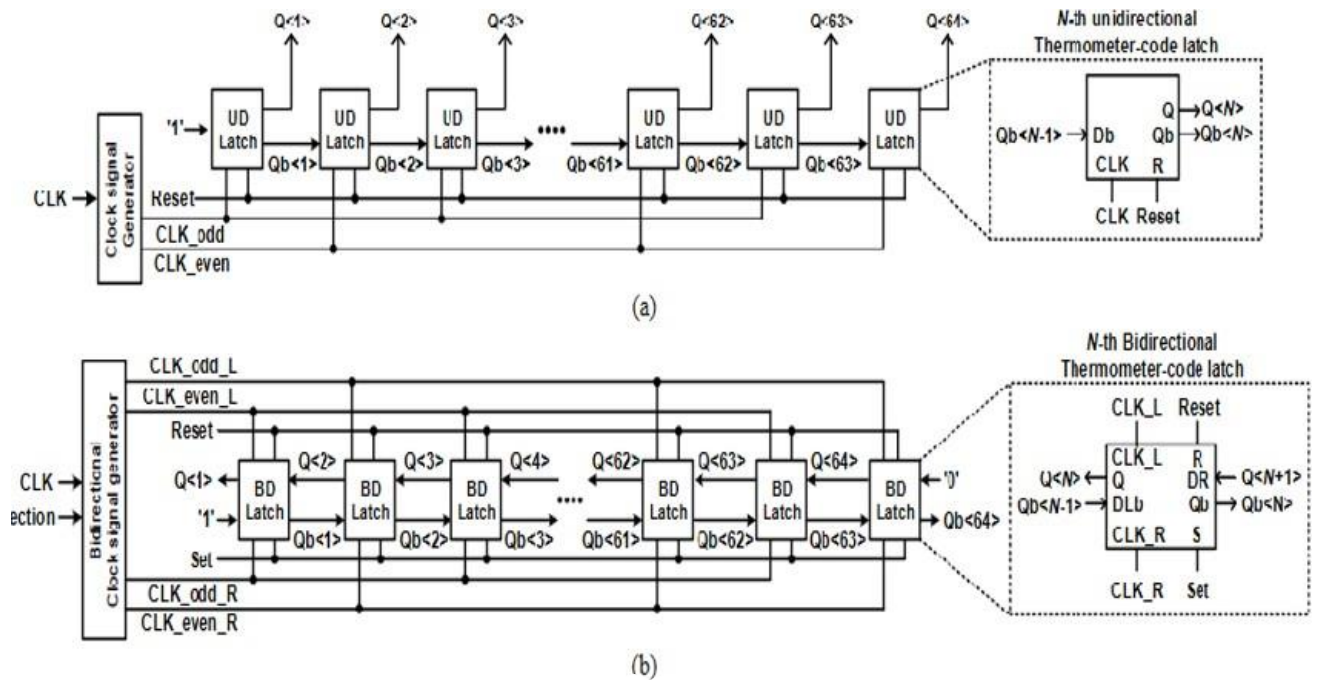


Figure 4.3.4 64-bit thermometer-code-shift-registers(a) Unidirectional (b) bidirectional

The bidirectional thermometer-code shift-register shifts the data '1' right with CLK_odd_R and CLK_even_R or the data '0' left with CLK_odd_L and CLK_even_L, according to the direction signal. They shift one bit data per clock cycle by enabling alternately the odd and even latches with CLK_odd and CLK_even, respectively. Therefore, they have the hold time as much as a half clock period. This removes the timing problem among latches.

4.4 LOW POWER D FLIP-FLOP

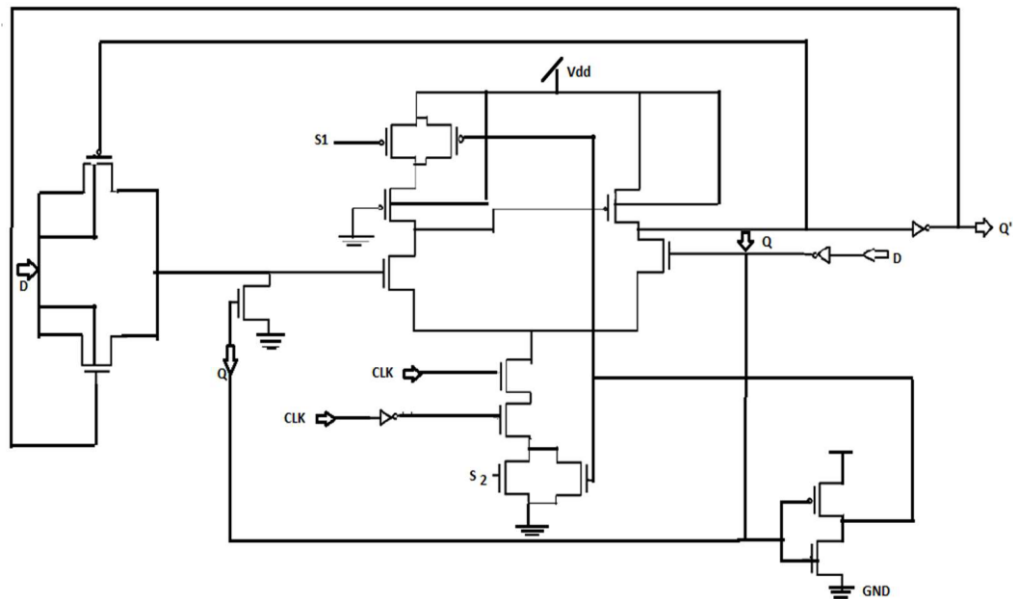


Figure 4.4 Modified Clocked Pair Shared Flip Flop (CPSFF)

The proposed architecture consists of Clocked Pair Shared Flip flop (CPSFF). It is a type of D- Flip flop. It uses 4 clocked transistors. It reduces the clock load compared to data map flip flop in which seven clocked transistors are utilized. In CPSFF first and second stages share the clocked pair. The flip flop has been modified using leakage feedback approach. Leakage feedback approach has its roots from sleep approach. In sleep approach, two transistors, one PMOS and one NMOS are additionally used. PMOS is connected to VDD and NMOS is connected to ground. The two transistors are called as additional sleep transistors. The circuit is turned off by cutting of power rails by sleep transistors. When the circuit is active the sleep transistors are turned ON and are turned OFF when the circuit is idle. Similarly leakage feedback technique employs sleep transistors. However it uses additional two transistors to maintain the logic state during the sleep mode. In this logic, in sleep mode even when the sleep transistors are

turned OFF one of the transistors in parallel to them, keeps the connection with sufficient power rail. The two transistors are driven by the output of the inverter which is in turn driven by the output of the circuit that is implemented using leakage feedback. Thus on employing this technique the power consumption of the flip flop is reduced and on using this flip flop in proposed architecture power consumption of the architecture is reduced making it an ultralow power architecture.

CHAPTER 5

RESULT AND DISCUSSIONS

The existing and proposed architecture are simulated by using Avan Waves simulator. Output of the existing thermometer code shift register and proposed thermometer code shift register are analyzed from the results and it is concluded that the proposed architecture reduced the power consumption compared with the existing system. The synthesis is done using Hspice.

5.1 SIMULATION RESULTS OF XOR GATE

Fig 5.1 shows the simulation results of the XOR gate. The input waveforms A, B and C is the output

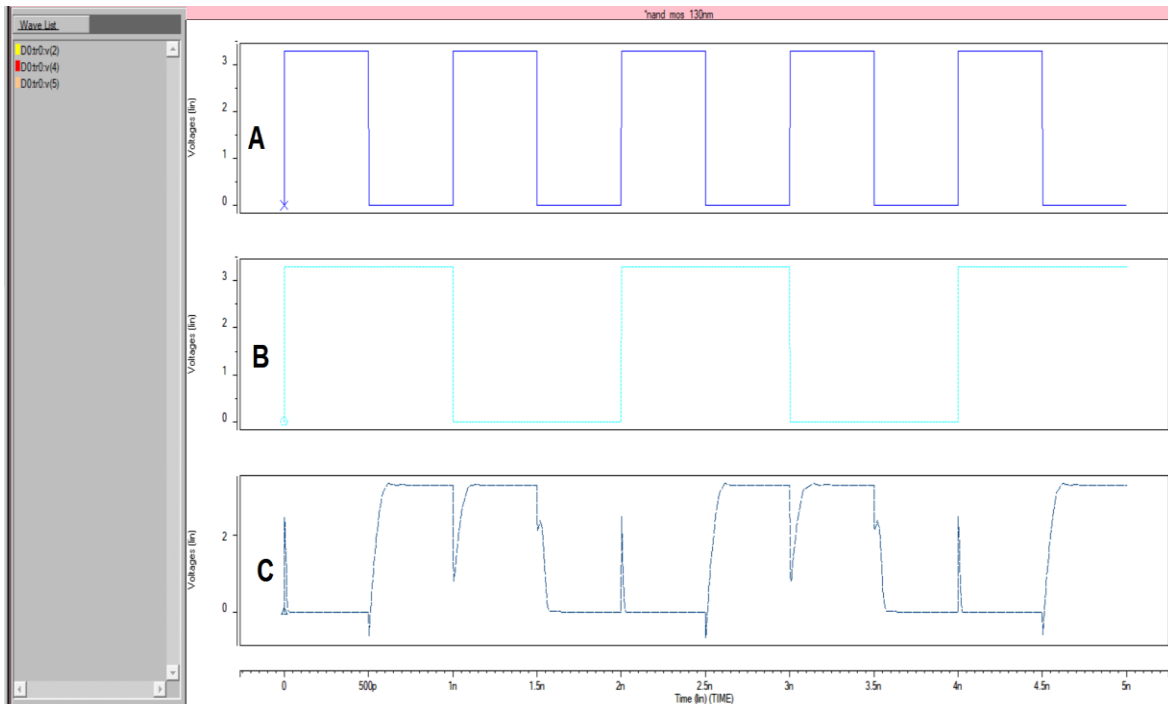


Figure 5.1 Simulation of XOR gate

5.2 SIMULATION RESULTS OF D FLIP FLOP

Fig 5.2 shows the simulation results of the 2 bit RCA circuit. The input waveforms A, B and output waveforms C, C0 are as shown.

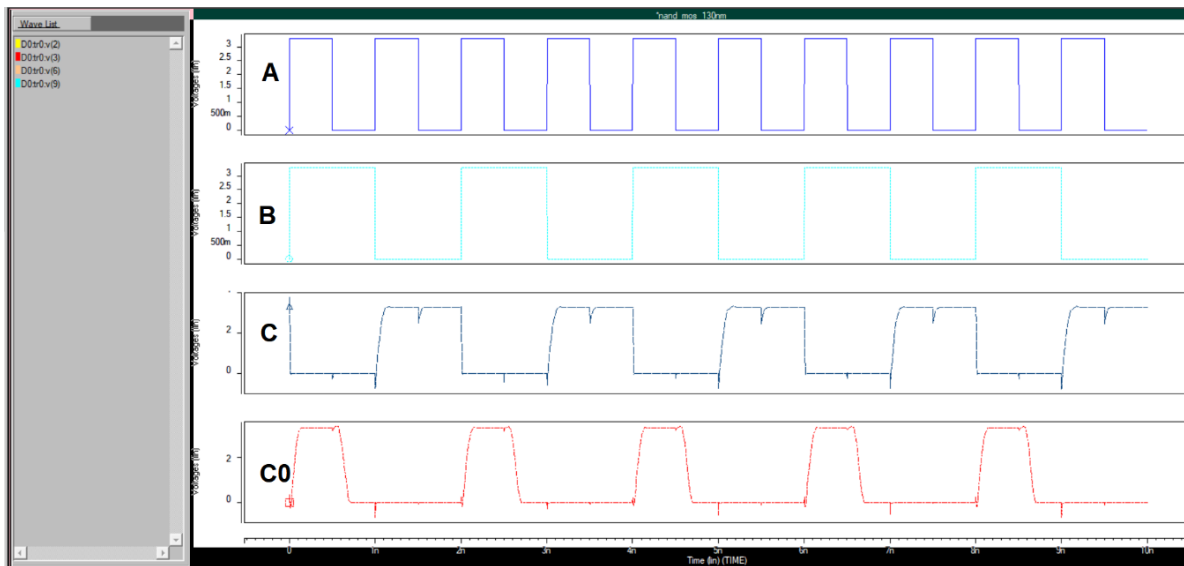


Figure 5.2 Simulation of D Flip- flop

5.3 SIMULATION RESULTS OF MASTER LATCH FLIP FLOP

Fig 5.3 shows the simulation results of the MASTER LATCH FLIP FLOP. The input waveforms A, B and output waveforms C are as shown.

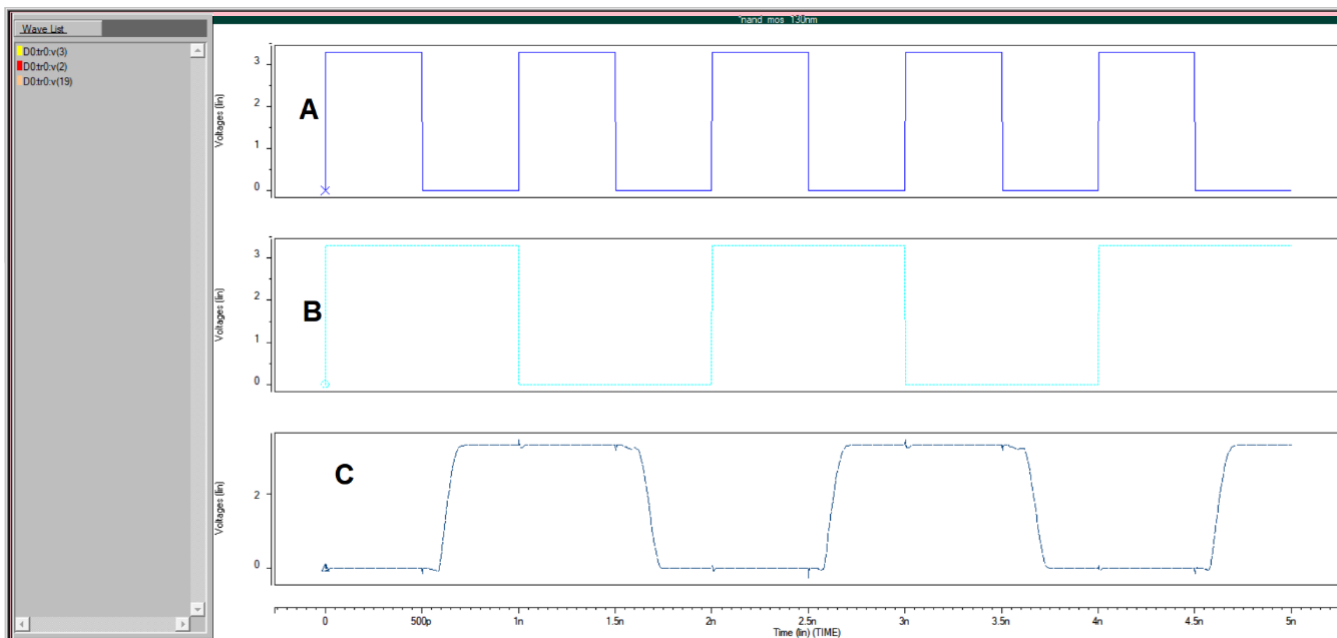


Figure 5.3 Simulation results of master latch flip-flop

5.4 SIMULATION RESULTS OF SHIFT REGISTER

Fig 5.4 shows the simulation results of the shift register. The input waveforms A, B and output waveforms B0,B1,B2,B3 are as shown.

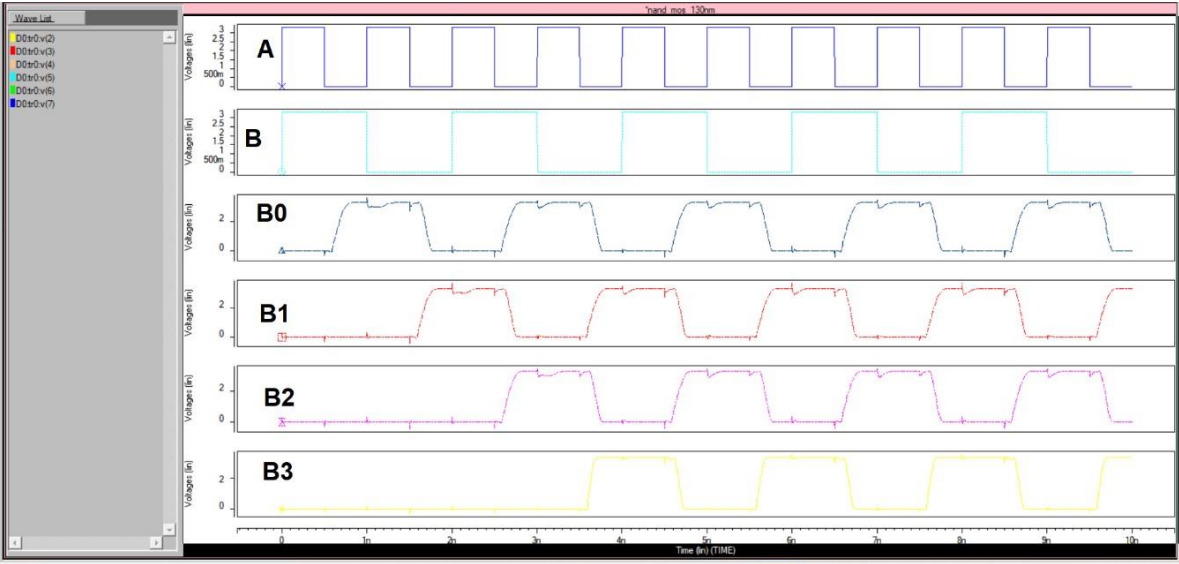


Figure 5.4 Simulation of shift register

5.5 SIMULATION RESULTS OF LFSR

Fig 5.5 shows the simulation results of the LFSR. The input waveforms A and output waveforms B0, B1,B2,B3 are as shown.

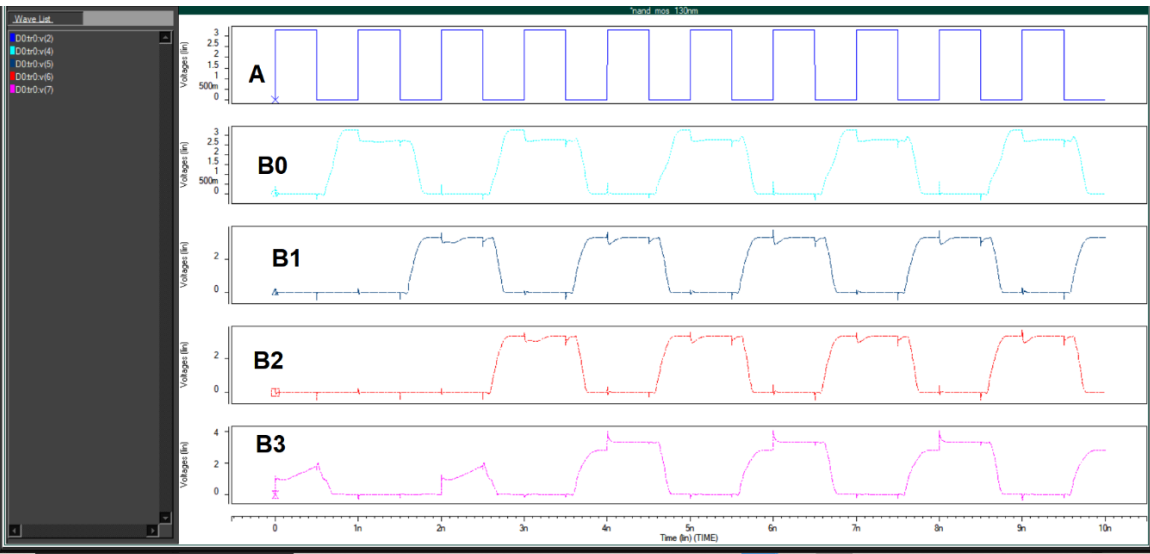


Figure 5.5 Simulation of LFSR

5.6 SIMULATION RESULTS OF 2 TO 1 MUX

Fig 5.6 shows the simulation results of 2 to 1 mux. It consists of a selection line and 2 inputs I0 and I1. The output and input waveforms are as shown.

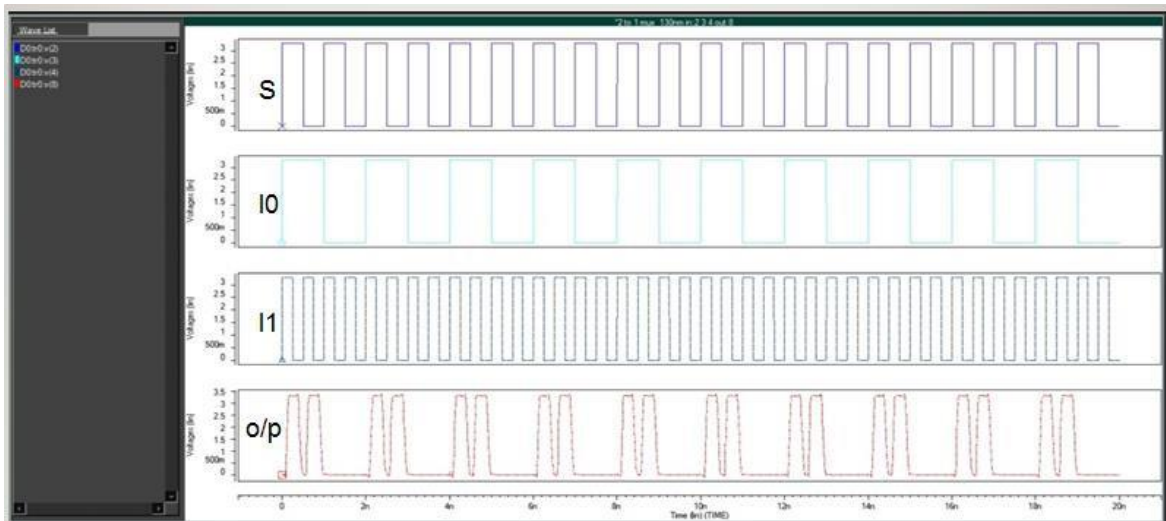


Figure 5.6 Simulation of 2 to 1 mux

5.7 SIMULATION RESULTS OF LFSR WITH MULTIPLEXER

Fig 5.7 shows the simulation results of LFSR with multiplexer. It consists A,B are inputs and B1 and B0 are outputs

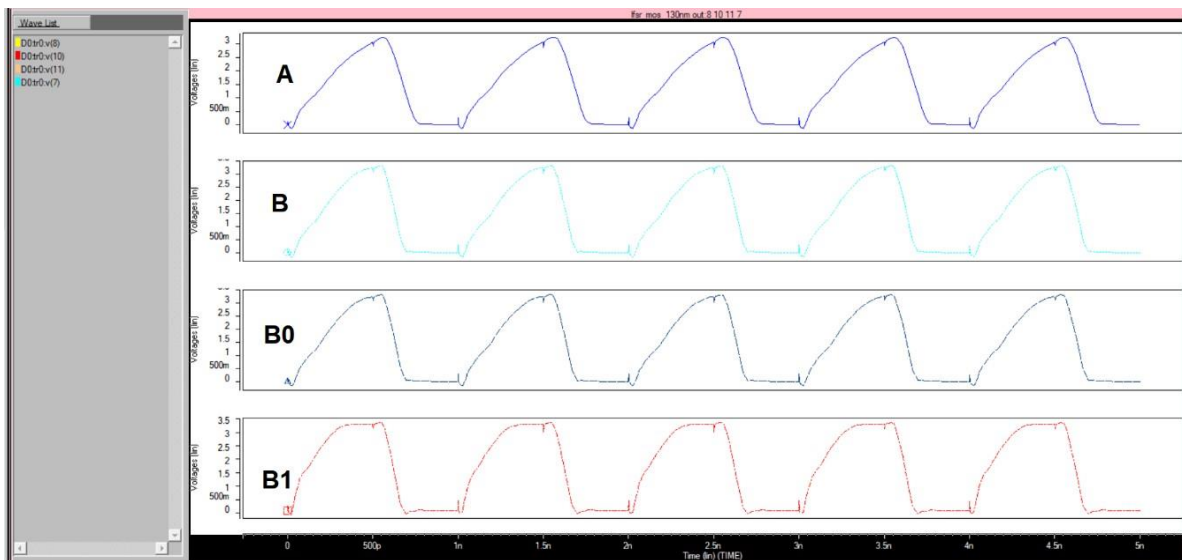


Figure 5.7 Simulation of LFSR with multiplexer

5.8 SIMULATION RESULTS OF MODIFIED FLIP FLOP

Fig 5.7 shows the simulation results of 16 bit CSA as shown. It consists two inputs A and A0 along with output A1

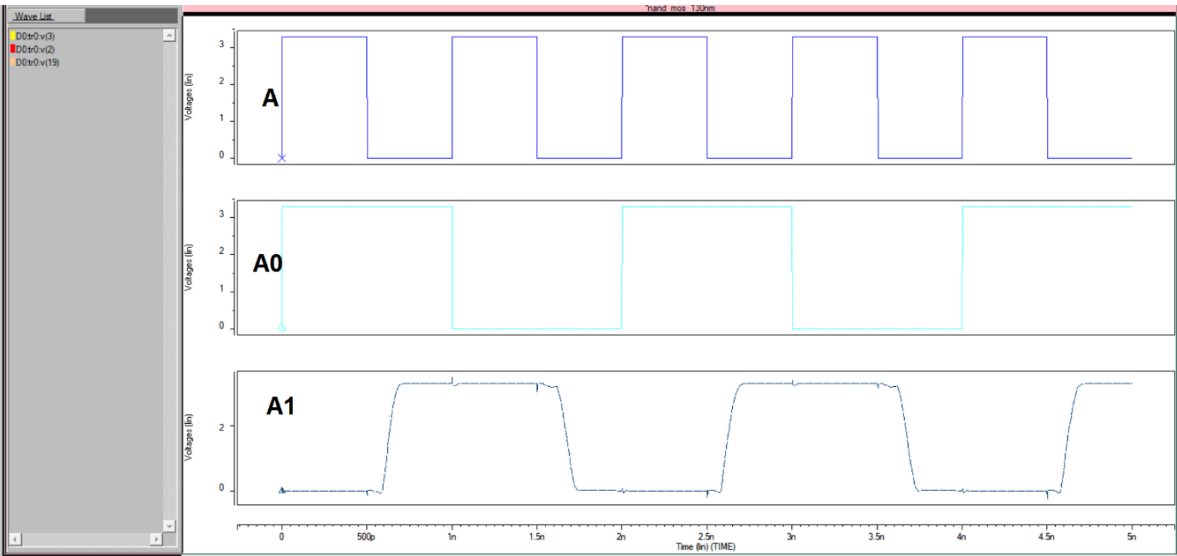


Figure 5.8 Simulation of modified flip flop

5.9 SIMULATION RESULTS OF MODIFIED LFSR

Fig 5.7 shows the simulation results of modified LFSR as shown. It consists A, B inputs along with output C0,C1,C2,C3.

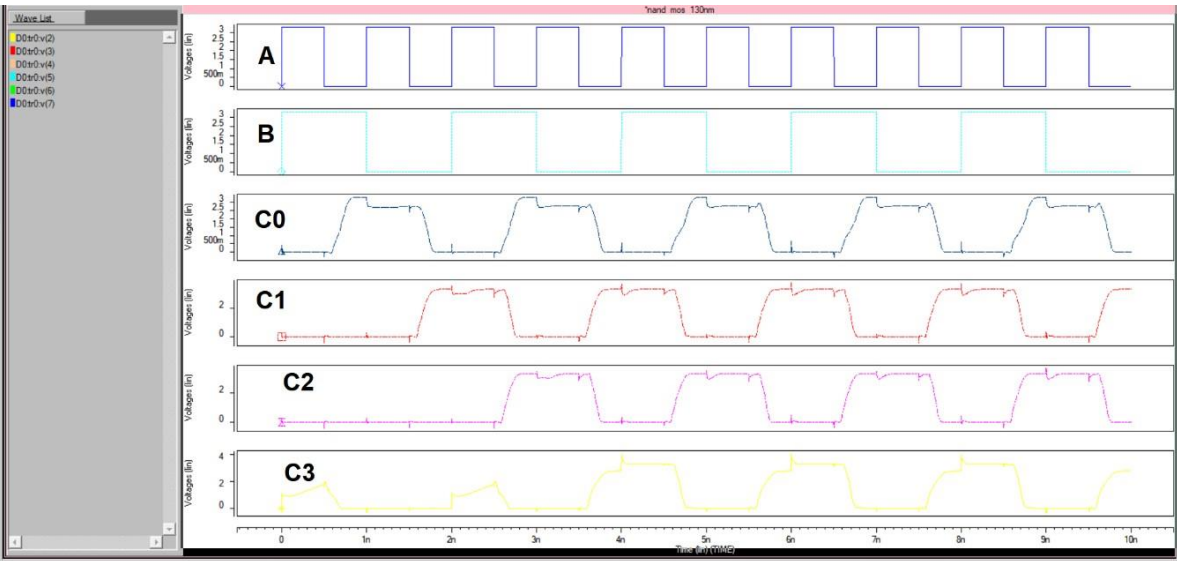


Figure 5.9 Simulation of modified LFSR

5.10 PERFORMANCE ANALYSIS

The performance analysis of Flip Flop, thermocode shift register in terms of power, delay, power delay product has been given below.

Device	130nm		
	Power	Delay	PDP
Flip-Flop	80.46u	236.52p	19.03f
Conventional Thermocode Shift Register	287.25u	522.22p	150.001f
Unidirectional Thermocode Shift Register	645.28u	458.26p	295.706f
Proposed Low Power Flip-flop	58.26u	198.56p	115.64f
Proposed Unidirectional Thermocode Shift Register	528.55u	395.25p	208.90f
Proposed Bidirectional Thermocode shift register	455.22u	498.66p	226.96f

Device	32nm		
	Power	Delay	PDP
Flip-Flop	65.22u	202.51p	13.207f
Conventional Thermocode Shift Register	202.54u	511.6p	103.619f

Unidirectional Thermocode Shift Register	601.58u	425.45p	255.97f
Proposed Low Power Flip-flop	48.78u	125.78p	61.35f
Proposed Unidirectional Thermocode Shift Register	505.22u	314.98p	159.09f
Proposed Bidirectional Thermocode shift register	395.23u	402.56p	165.10f

Table 5.10.1 Performance analysis of MOSFET Technology

The performance analysis of Flip flop, thermocode shift register in terms of power has been given below.

Device	15nm		
	Power	Delay	PDP
Flip-Flop	11.22u	148.11p	1661.79f
Conventional Thermocode Shift Register	145.12u	312.4p	4533.48f
Unidirectional Thermocode Shift Register	428.6u	279.11p	119626.54f
Proposed Flip-flop	9.11u	91.28p	831.56f
Proposed Unidirectional Thermocode Shift Register	312.4u	198.12p	61892.66f

Proposed Bidirectional Thermocode shift register	214.11u	201.46p	43182.37f
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Table 5.10.2 Performance analysis of GNRFET Technology

The power delay product which is known as PDP is also calculated.

CHAPTER 6

CONCLUSION

It has been proposed a new technique to design Thermometer Code shift register using modified flip flop gives better response in terms of power and delay in comparison to the conventional Thermometer Code shift register. We have achieved a design of a Thermometer Code shift register using a modified Flip flop which is faster and has reduced the delay of the carry select considerably. Since our objective was to reduce the delay and power of the Thermometer Code shift register and it has been reduced by 1.532mw, 0.21545 hence we achieved our objective. the path from V_{DD} to ground, leading to significant decrease in leakage currents. The gate-level netlist of the given circuit is first converted into a static CMOS complex gate implementation and then STACK techniques are introduced to obtain a leakage-controlled circuit. Further, the proposed technique overcomes the limitations posed by other existing methods for leakage reduction. From the results obtained it can be verified that there is a significant amount of reduction in power dissipation of the circuits when STACK technique was used. Low power consumption in turn increases the efficiency of the overall system when compared to the existing systems. The significant feature of stack is that it works effectively in both active and idle states of the circuit, resulting in better leakage reduction compared to other techniques. Further, the proposed technique overcomes the limitations posed by other existing methods for leakage reduction. An analysis of a High area-efficient 4:2 dual stage compressor has been designed using stack 130nm and 32nm MOSFET technology. So, we practically saw that the Thermometer Code shift register with modified Flip flop is much more efficient. Thermometer code Shift register are the key module of any pseudo random generator. So, improving its performance can improve the overall efficiency of the system. Future work can be concentrated on area efficiency of the Thermometer Code shift register and flip-flop and can obtain better efficiency in terms of area, power, delay and power delay product.

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