

ANALYSIS OF AN EFFICIENT WALLACE TREE ENCODER FOR HIGH-SPEED APPLICATIONS

A Project Report Phase – II

Submitted in partial fulfillment of requirements for the award of
Bachelor of Engineering in Electronics and Communication Engineering

by

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DEPERTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

SCHOOL OF ELECTRICAL AND ELECTRONICS

SATHYABAMA

**INSTITUTE OF SCIENCE AND TECHNOLOGY
(DEEMED TO BE UNIVERSITY)**

Accredited with Grade "A" by NAAC

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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the Bonafide work of **PARISA MAHENDRA NADH** (39130339) and **PATTA SAI KUMAR REDDY** (39130341) who carried out the project entitled "**ANALYSIS OF AN EFFICIENT WALLACE TREE ENCODER FOR HIGH-SPEED APPLICATIONS**" under our supervision from November 2022 to April 2023.

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DECLARATION

We, PARISA MAHENDRA NADH and PATTA SAIKUMAR REDDY hereby declare that the Project Report entitled “**ANALYSIS OF AN EFFICIENT WALLACE TREE ENCODER FOR HIGH-SPEED APPLICATIONS**” done by us under the guidance of Mr.M.A.MUTHIAH.,M.Tech Assistant Professor is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.

1. 
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PLACE:

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ABSTRACT

In this project, the analysis of an efficient Wallace tree encoder is proposed for high-speed applications. In changing analog to digital signal process, energy usage of analog and digital circuit design will play a major role in the world. Wallace tree encoder is to make use in the process of changing the unary code to binary. A Unary code is an output of a thermometer-to-binary encoder which is mainly making use of a component called flash ADC Analog to digital converter, also called as parallel Analog to digital converter. This can be termed to be a high-speed application and a flash type of flash Analog to digital converter. The major purpose of the Wallace tree encoder approve analysis is to formulate the less amount of enthusiasm, less optimal speed and less complexity Wallace tree encoder that is used in both the conventional and present conversion procedure. The Wallace tree is an alternative of extended product. The 1st process is to product by each bit of 1 factor by each digit of the other. Each of these multiplications has weight identical to the product of its factors. The final multiplication is finding by the weighted addition of all these multiplications. The main aim of the analysis of an efficient Wallace tree encoder is for high-speed applications, project is to make analysis because Wallace tree encoder is used in high-speed applications, and using less adders and less transistors, from this less area enough and high-speed performance occurred, from this we must implement an efficient Wallace tree encoder for high-speed applications.

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LIST OF SYMBOLS AND ABBREVIATIONS

ADC	ANALOG TO DIGITAL CONVERTER
NMOS	N – CHANNEL METALOXIDE SEMICONDUCTOR
PMOS	P – CHANNEL METALOXIDE SEMICONDUCTOR
CMOS	COMPLEMENTARY METALOXIDE SEMICONDUCTOR
VLSI	VERY LARGE-SCALE INTEGRATION
CPL	CURRENT-MODE LOGIC
MOSFET	METALOXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR
SPICE	SIMULATION PROGRAM WITH INTEGRATED CIRCUITS
LPF	LOW PASS FILTER
FET	FIELD EFFECT TRANSISTOR
AVR	AUTOMOTIVE VOLTAGE REGULATOR
FPGA	FIELD PROGRAMMABLE GATE ARRAY
GND	GROUND
PDP	PRODUCT DELAY PRODUCT

CHAPTER 1

INTRODUCTION

Wallace tree encoder is a well-organized hardware performance in VLSI which is used for analog to digital conversion process. Wallace tree encoder is used in the conversion of unary code to Binary code in analog to digital code converter circuit. Wallace tree encoder reduces the errors present due to presence of zeros in successive occurrence of one's at the comparator side. A Wallace tree encoder contains of full adder circuits by which they add the number of one's generated out of $2n - 1$ comparator.

Unary code or thermometer code is an output of a thermometer to binary encoder which is mainly use of a component called Flash ADC. The flash ADC also known as parallel ADC. Thermometer code is also called as unary code. This code can be obtained by following rules. If the given natural number is represented as N. Then the code can be represented with N length of 1's followed by a 0. The code can also be represented with N length of 0's followed by a 1. There will be $2N$ resistors along with $2N-1$ comparators in a N bit Flash ADC In thermometer code, the lowermost N bits of a byte encoding a number 'N' are '1', while the rest are '0'

Mainly the Wallace tree encoder is used for the performance of Digital Signal Processing DSP structures, Arithmetic Logical Units ALU's and several low power and high-speed arithmetic applications. To add partial products in phases until two numbers are left. Used in the process of converting the unary code to binary.

1.1 Wallace tree encoder

Wallace tree encoder is used in the conversion of unary code to Binary code in analog to digital code converter circuit. The important difference between the Wallace tree and others is that Wallace tree encoder has an inbuilt bubble error corrector circuit. In the sense inbuilt means in Wallace tree itself already have integrated the bubble error corrector in Wallace tree encoder. Due to this advantage, the architecture uses hybrid full adder circuit to make it more efficient in high-speed performances this was an VLSI based system, speed, area and power consumption are the factors effecting efficiency of Wallace tree encoder.

Wallace tree encoder does not require any XOR gates because it receives thermometer code as input.

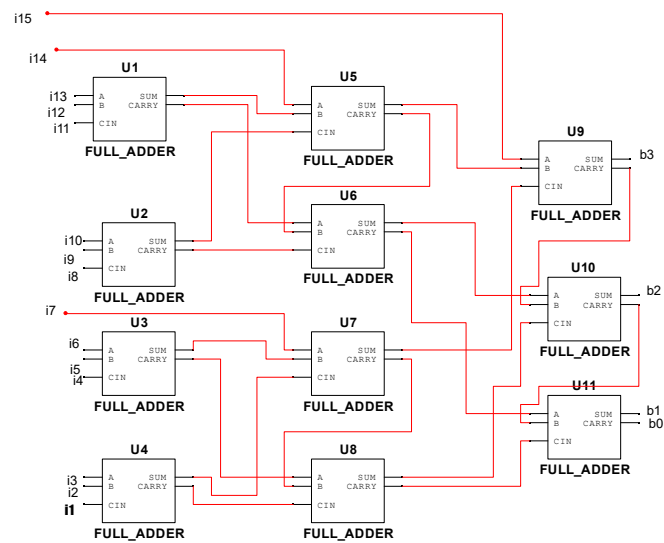


Fig.1.1 Wallace Tree Diagram

From this fig 1.1 it represents eleven full adders with fifteen thermometer code inputs and four binary outputs. Thermometer code inputs are labelled from i1 to i15. Binary outputs are labelled as b0, b1, b2 and b3. In this design conventional full adder is used and each of the full adder consists of 28 transistors. As there were eleven full adders in this design, 308 transistors are required to build Wallace tree encoder. In this design energy consumption of the Wallace tree encoder is corrected by using a complete adder in the circuit

Wallace tree encoder is implementing by using with the help of Xilinx software for the process of implementing Wallace tree with reduce in number of adders and transistor we have to enhance the performance of Wallace tree encoder for high-speed application its help full in various VLSI technologies.

A Wallace tree encoder is a digital circuit used for high-speed multiplication of large data sets. It uses a combination of multiplication and addition operations to efficiently compute the product of two binary numbers. The Wallace tree encoding algorithm reduces the number of partial products generated during the multiplication process, thereby reducing the overall computational complexity and power consumption of the circuit.

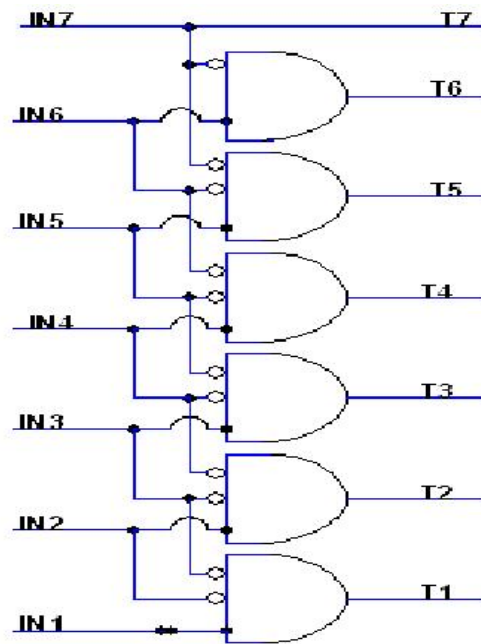


Fig.1.2 Wallace tree bubble error correction circuit

The presence of bubble error corrector in Wallace tree encoder the performance of Wallace tree will be very speed or work active in any applications. Wallace tree encoder is a type of digital circuit that is used to compress a large amount of data into a smaller set of bits. It is particularly useful in situations where data needs to be transmitted or stored efficiently, such as in computer networks, telecommunications, and data storage systems. The main advantage of Wallace tree encoder is that it can significantly reduce the amount of data that needs to be transmitted or stored. This can lead to faster data transmission rates, lower storage requirements, and reduced power consumption. In addition to its use in digital circuits, Wallace tree encoding has applications in various areas of daily life. For example, it can be used in image and video compression, where large amounts of data need to be compressed into smaller file sizes.

1.2 Thermometer code (Unary code)

Unary code takes after the output produced by a thermometer. The thermometer code process occurred in Wallace tree because of we need output for any work after completion we need result for that purpose, we use thermometer

code or unary code we call thermometer code as unary because the process done one by one so we call it as unary code.

In unary code, a value representing number 'N' has the bottommost 'N' bits as one (1), others as zero (0). So, to proceed from N to 'N+1', just change the rightmost 'zero' to 'one'. The diagram below shows graphically the unary codes for values from '0' to '7'. As is clear, each value noted a reading in thermometer. This is how, thermometer code got its name as thermometer code or unary code. Flash Analog to digital conversion ADCs, time-to-digital converters (TDC) are some of the circuits that uses thermometer code for getting outputs.

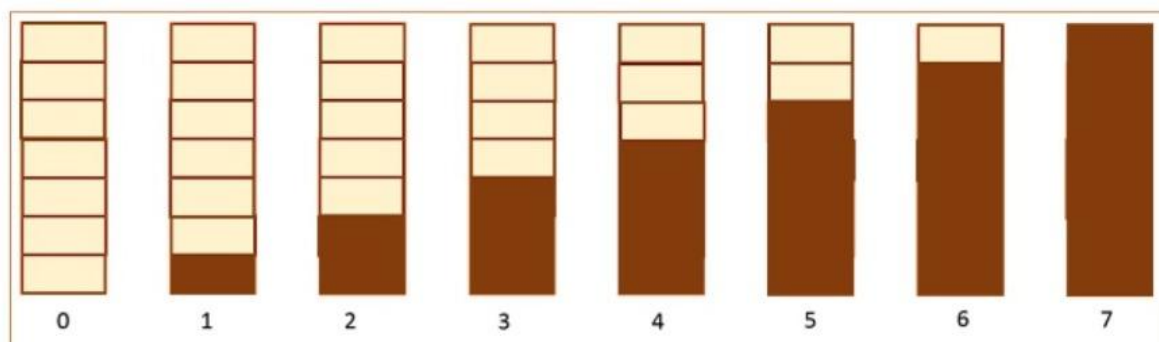


Fig1.3 The figure shows thermometer code with 7 values

In this fig how the conversion will occur is initially its zero there is no values then one by one the values inserted in that, like that data will be work one by one we call it as unary code that's why we got the name as unary code. Thermometer code is more commonly used than unary code in digital signal processing and communication systems because it provides a more compact representation of signals with a wide dynamic range. Unary code, on the other hand, is rarely used because it requires a large number of bits to represent even moderately large values. Unary code and thermometer code are two different methods of representing an analog signal as a digital sequence. Unary code represents a signal as a sequence of 1's, where the number of 1's in the sequence corresponds to the value of the analog signal. For example, the number 5 could be represented in unary code as "11111". Thermometer code is more commonly used than unary code in digital signal processing and communication systems because it provides a more compact representation of signals with a wide dynamic range.

Table 1.1 Thermometer code or Unary code

N	Unary code	Alternative Code
0	0	0
1	10	01
2	110	001
3	1110	0001
4	11110	00001
5	111110	000001
6	1111110	0000001
7	11111110	00000001
8	111111110	000000001
9	1111111110	0000000001
10	11111111110	00000000001

Thermometer code or unary code is an output of a thermometer to binary encoder which is mainly use of a component called Flash ADC Thermometer code is also called as unary code. This code can be obtained by following rules. If the given natural number is represented as N. Then the code can be represented with N length of 1's followed by a 0. The thermometer code is work like where 0 there placed by 1's vice versa like this the process will happened till we got the output for the given or proposed methods. Each symbol in thermometer code is a sequence of zeros (0's) followed by a sequence of ones (1's). There cannot be 0s in-between two 1s. For sample, a symbol 01011 is invalid in thermometer code for an n-bit binary code, the matching thermometer code will have $2n - 1$ symbol hence, as many bits will be needed to represent unary code for the same.

1.3 Flash ADC

Flash analog-to-digital converters, also known as parallel Analog to Digital Converters, are the speeds way to convert an analog signal to a digital signal. Flash ADCs are ideal for applications requiring very large bandwidth, but they use more power and much bigger in size than other ADC architectures. A Flash converter requires a large number of comparators compared to other analog to digital converters ADCs, mainly as the determination increases. A Flash converter requires $2^n - 1$ comparators for an n -bit conversion.

One of the important advantages of ADC converter is the high data acquisition rate even at multiplexed inputs. With the invention of a wide variety of ADC (IC's), A different of applications of the ADCs are calculations and control systems, industrial instrumentation, communication systems, and all other sensory based systems. Classification of analog to digital converters ADCs based on factors like presentation, bit rates, power, cost, etc.

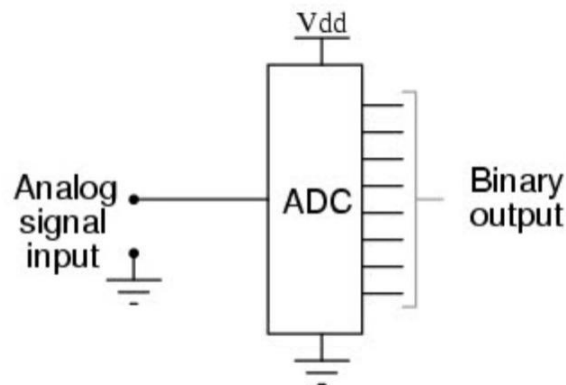


Fig 1.4 Analog to Digital Converter

The block diagram of ADC is shown in figure which includes sample, hold, quantize, and encoder. The procedure of ADC can be done like the following ADCs are used in a wide range of applications, including communication systems, control systems, data acquisition systems, and measurement instruments. The main function of an ADC is to sample the analog input signal and then quantize it into a discrete set of levels. The process of quantization introduces some error, known as quantization noise, which is usually modeled as a random signal.

CHAPTER 2

LITERATURE SURVEY

This chapter discusses about the literature survey and summary. It also gives idea about analysis of an efficient Wallace tree encoder.

2.1 LITERATURE SURVEY

Daegoule, Jincheolyoo, Kyuysunchoai, Ghaznzavi, all these researchers in 2002 proposed that In this project that the fat tree thermometer code to binary code encoder that is highly suitable for the ultra-high-speed flash ADC's. the speed will increase by almost a factor of two when using the fat tree encoder. For a more efficient implementation in CMOS. We can change OR gates with NOR and NAND gates using Demorgan's theorem. For calculating the performance of fat tree encoder, author's designed ultra-high-performance thresholding inverter ADC IN 0.18 CMOS technology. The Tc to BC. encoding is carried out in two stages in the fat tree encoder the first stage converts the thermometer code to one out of encode, the one out of encode is equal as a decoder output.

The second stage converts the one out of encode to binary code using the multiple trees of OR gate. Here the advantages and disadvantages In fat tree encoder bubble error correction is very easy bubble error correction is a very common term associated to flash ADC's where in output produced by comparators stage is expected to be a thermometer code. Fat tree encoder consumes more power and has more delay than the recent encoders. The output of the flash ADC is then processed by a Wallace tree encoder to reduce the number of output bits. The Wallace tree encoder in this case combines the intermediate samples in parallel to generate a smaller number of digits, thereby reducing the complexity of the interpolation circuit. In general, the choice of counter-based Wallace multiplier architecture depends on the specific requirements of the application, such as speed, area, and power consumption. Hybrid counter-based Wallace multiplier: This architecture combines the features of both serial and parallel counter-based Wallace multipliers.

Shahzad Asif, Yinankong both of the researchers in 2015 proposed about that Multiplication is one of the commonly used operations in the signal processing algorithms. So many numbers of modifications are proposed in this literature for optimizing the speed and area of Wallace multiplier. Now a days electronics related authors proved that counter-based Wallace multipliers faster operations as compared to the Wallace multipliers. The proposed counter-based Wallace multipliers are compared with the traditional Wallace multiplier for calculating then operations of both designs. Multiplication is also used in image processing and cryptography. The partial product is in the original Wallace tree multiplier is divided into groups which consists of three rows then the addition is performed in every column with the help of full adder and half adder. This process is repeated until the tree is reduced to two rows. So many papers have been published in the literature surveys for improving the performance of the Wallace multiplier.

In power consumption power is improved by five percent and latency is improved by fourty three percent this is one of advantage of the high-speed counter-based Wallace tree multiplier. Improvement in signed bit multiplications these are disadvantages of the Wallace multiplier. A Wallace multiplier is a type of multiplier used in digital circuits to perform multiplication of two binary numbers. It is based on the principle of dividing the operands into groups of bits and performing partial products on these groups. A counter-based Wallace multiplier is one of the variations of the Wallace multiplier, where a counter is used to count the number of 1's in the partial products. This helps to reduce the number of adders required to compute the final product. The output of the flash ADC is then processed by a Wallace tree encoder to reduce the number of output bits. The Wallace tree encoder in this case combines the intermediate samples in parallel to generate a smaller number of digits, thereby reducing the complexity of the interpolation circuit. In a folding ADC, the input analog signal is folded over a range of voltage levels, and the folded signal is converted into digital form using a flash ADC. The output of the flash ADC is then processed by a Wallace tree encoder to reduce the number of output bits.

P. Pereira, J.R. Fernandes, M.M. Silva these researchers in 2002 proposed about that the Wallace tree encoder has been used successfully in full-flash ADC's to convert the unary code to binary code, while performing error correction in this project author shows the how Wallace tree encoder convert to the binary circular code in folding and interpolation ADC's. Parallel type analog to digital converters can operate with high sampling frequency and this component are high cost and consumes high-power high-power consumption occurs because of using comparators. Comparator output is a circular code which is used to convert binary by the digital part of ADC's, by using this error correction can be implemented. Compare the Wallace tree encoder with the basic encoder and with an encoder with first order error correction. The most important error due to mismatches is the offset voltage in the folding circuits zero's and comparators input voltages and bit to bit of the corresponding three output codes those causing a large error at the output.

Then using three input XOR gates instead of two XOR gates a first order correcting encoder is obtained large errors are avoided, but LSB error is still possible. The Wallace tree encoder for circular to binary encoding in folding and interpolation ADC's. for medium resolution ADC's the Wallace tree encoder provides very effective error correction and also improve noise performance. The advantages and disadvantages are Low power consumption and complexity also very less optimum delay Wallace tree encoder, inefficiency of the circuit when isolated one's are encountered. In a folding ADC, the input analog signal is folded over a range of voltage levels, and the folded signal is converted into digital form using a flash ADC. The output of the flash ADC is then processed by a Wallace tree encoder to reduce the number of output bits. The Wallace tree encoder combines multiple binary digits in parallel to generate a smaller number of digits, thereby reducing the number of comparators and latches required in the folding ADC. o design a high-performance Wallace tree encoder, several VLSI architectures have been proposed in the literature. These architectures optimize different parameters. Designers need to carefully evaluate the different architectures and select the one that best meets their needs. Additionally, various techniques such as folding and parallelism can be used to further optimize the performance of the Wallace tree encoder.

J.M.Mathana, R.Dhanagopal, R.Menaka all these researchers in 2020 proposed that the power consumption of analog and digital circuit design is will play a major role in the world, many reachers are participated in this design low power analog and digital circuits, the nature of the signal is analog. now a day's signal analyzers are done in digital for only to achieve low power high accuracy speed and less area. The conversion of analog to digital is very important and also it is implemented in all real time signal processing. The main purpose of the recommended research is to formulate the minimal energy less optimal speed and minimal complexity Wallace tree encoder with both additional and modern conversion procedure. While the design of flash analog to digital converter need to consider the speed and power they introduced Wallace tree counter that counts the one a value to the comparator bubble errors can be default the higher input nand gates.

The proposed model describes about the low power less complexity and optimum delay. Wallace tree encoder by suitable design of full adder. The Wallace tree have advantages of low power, less complexity and optimum delay and having suitable design. Reducing power consumption of the encoder and it is a large concern for reducing power this is main disadvantage of the analysis of high-speed Wallace tree encode. To design a high-performance Wallace tree encoder, several VLSI architectures have been proposed in the literature. These architectures optimize different parameters such as area, speed, and power consumption, and can be classified as follows parallel-prefix adder-based Wallace tree encoder This architecture uses a parallel-prefix adder to compute the partial sums and then feeds them to the Wallace tree encoder for reduction. This architecture provides high-speed operation with low power consumption. A high-speed and area-efficient Booth recorded Wallace tree multiplier can be designed using various techniques. One such technique is the use of a hybrid Wallace tree encoder, which combines the features of both parallel-prefix and carry-save adder-based architectures. The partial products are first processed using a carry-save adder to reduce the number of bits, and then fed to a parallel-prefix adder to

generate the final sum. This architecture provides a good balance between speed and area efficiency.

M.Jagadeshwae Rao, Sanjay Duby these researchers in 2012 proposed that The multiplier is one of the key hardware blocks in most of the digital and high-performance systems such as digital signal processor and microprocessor. They aim offering higher speed and low power consumption even while occupying reduced silicon area this makes them compatible for various complex and portable VLSI circuit implementation. In the proposed architecture, partial product generation and reduction is accomplished by the use of booth recoding algorithm. The Wallace tree architecture aims to reduce the overall latency. This leads to increased speed and reduced power consumption. The design makes use of compressors in place of full adders, and the final carry propagate stage is replaced by a Carry select adder. The individual full adder blocks in the original structure are grouped and implemented using compressors.

The proposed 32×32-bit Booth recoded Wallace tree multiplier has been implemented on FPGA and the delay comparison with existing Wallace tree multiplier, multiplier designed using Vedic mathematics, Booth multiplier both radix-8 and radix-16, default multiplier present in Xilinx FPGA vertex-6 low power. In this booth recorded Wallace multiplier have to implement the reduction in latency and reduce area of the Wallace tree this is because for high performance of the Wallace tree this is the advantage of this booth recorded Wallace multiplier. And it can't do in with other gates only adders are used this is the disadvantage of the system. A Booth recorded Wallace tree multiplier is a type of multiplier used in digital circuits to perform multiplication of two binary numbers. It is based on the principles of Booth's algorithm and Wallace tree encoding. Booth's algorithm is used to convert one of the operands of the multiplication into a signed-digit form, which reduces the number of partial products required in the multiplication process. The signed-digit form is then processed using a Wallace tree encoder, which reduces the number of output bits from the multiplication operation.

C.Vinoth,V.S.Kanchana Bhaaskaran,B.Brindha all these researchers in 2011 proposed that The multiplier is one of the key hardware blocks in most of the digital and high-performance systems such as digital signal processors and microprocessors. They aim at offering higher speed and lower power consumption even while occupying reduced silicon area. In this paper, they arrive a better trade-off between the two, by realizing a marginally increased speed performance through a small rise in the number of transistors. The proposed architecture aims at partial product reduction by the use of 4:2, 5:2 compressor structures and the final stage of addition is performed by a Sharansky adder. The multiplier architecture comprises of a partial product generation stage, partial product reduction stage and the final addition stage. The latency in the Wallace tree multiplier can be reduced by decreasing the number of adders in the partial products reduction stage.

The proposed architecture is compared to conventional. The transistor count comparison and the latency comparison. The latency of existing Wallace tree multiplier which is found to be 27 has been reduced to 15th the comparison result also shows that a significant reduction of power is achieved. At an operating frequency of 50 MHz at 3.3Volts. Efficient in power, area and delay will happened in this is the advantage of novel Wallace tree, and the disadvantage of the system is in this chip multipliers can be implemented. One technique to reduce power consumption is the use of clock gating, which involves disabling the clock signal to certain parts of the multiplier when they are not in use. This reduces the power consumption of the multiplier while still maintaining its functionality. Another technique is the use of low power logic gates such as pass-transistor logic or static CMOS logic instead of dynamic CMOS logic. This reduces the power consumption of the multiplier while maintaining its speed. Another technique is the use of low power logic gates such as pass-transistor logic or static CMOS logic instead of dynamic CMOS logic. This reduces the power consumption of the multiplier while maintaining its speed. To improve the speed of the Wallace tree multiplier, pipelining can be used to break the multiplier into multiple stages, each processing a portion of the inputs in parallel. This provides high-speed operation with low power consumption

M.P. Anjaney, George Tom Varghese all these researchers in 2018 proposed that Flash ADC is the fastest analog to digital converter, also referred to as parallel ADC. It is right for packages requiring huge bandwidth. It is composed of a resistor ladder, comparator and an encoder circuit. Output of the comparator is a thermometer code. It needs to be transformed to corresponding binary code the usage of suitable encoder. Decreasing strength dissipation of an encoder is a major challenge even as designing low strength Flash ADC. Advancements in electronics require data converters for interfacing real world alerts for numerous programs. An ADC is a blended signal device with analog the front end and digital lower back end. Speed and accuracy of the converters are the predominant problem. Flash analog to digital converter (ADC) is the fastest analog to digital converter. suggests the shape of Flash ADC.

Thermometer code consists of collection of zeros accompanied by means of series of 1s i.e. There should be most effective one transition. Due to more than one non-ideality and mismatches inside the comparators, surprising zeros in series of ones and ones in collection of zeros appear. This makes the unary code invalid. This situation is called as bubble mistakes. Speed of operation of the existing design is reasonably good these are advantages of the project. Difficulty in designing parallel multipliers as number of shift and add operations vary these are the disadvantages of thermometer code to binary code converter. A thermometer code to binary code converter is a crucial component in Flash ADCs (Analog-to-Digital Converters). Flash ADCs are high-speed converters used to convert analog signals into digital signals. They use a bank of comparators to compare the input signal to a set of reference voltages, and the output of each comparator is a binary decision indicating whether the input voltage is higher or lower than the reference voltage. In a Flash ADC, the output of the comparators is in the form of a thermometer code, which is a one-hot code indicating the highest comparator that has its output set to "1". The thermometer code needs to be converted into binary code to obtain the digital output of the ADC.

M.kiranmai,V.Y.S.Sudir patnaikuni,K.Mouli all these researchers in 2017 proposed that the parallel structure of flash ADC in reduce the delay of ADC while compared with traditional ADC. Multipliers and their associated circuits like half adders, full adders and accumulators eat a extensive portion of maximum excessive-speed packages. The Reduced complexity discount approach substantially reduces the number of half adders with 75-80% reduction in an area of half adders than well-known Wallace multipliers. In each multiplier, at the final stage Carry Propagating Adder (CPA) is used. CMOS complete adder in reduced complexity Wallace Multiplier at the location of Conventional Full adder a good way to reduce region, energy and development in velocity.

In digital signal processing (DSP) and photograph processing multiplier play an vital function. In image processing speedy Fourier rework (FFT) is one of the most vital transforms regularly used. A computational method of fast Fourier rework calls for big variety of multiplication and addition operation. The execution of those algorithms requires dedicated MAC and Arithmetic and Logic Unit (ALU) architectures. Proposed structure has same degrees as RCW Multiplier. At the level where, traditional full adder is gift, Energy Efficient Full Adder is used. The advantages of CMOS full adder and multiplier are Low power techniques are applied to prolong the battery life of a system and disadvantages are analog to digital converter also required a low power technique in the design to reduce the total power consumption of ADC. The CMOS full adder is a digital circuit that performs binary addition. It takes three input signals (two operands and a carry-in signal) and produces two output signals (the sum and carry-out signals). The CMOS full adder can be implemented using complementary MOS (CMOS) technology, which is a low-power digital logic design technique. The CMOS full adder and multiplexer-based encoder is a low-power and area-efficient technique for implementing the thermometer code to binary code conversion. It is well-suited for low-resolution Flash ADCs, where a small number of comparators are used. However, the performance of the encoder can be affected by the accuracy and linearity of the comparators used in the Flash ADC.

Kokila Bharti Jiswal, Nitish Kumar V, Pavithra Seshadri, Lakshminarayanan G all these researchers in 2015 proposed that The electricity intake, postpone and region are always been an critical layout issues for any chip designer. Many DSP systems include multipliers in their layout. Delay of the circuit unavoidably changes with the delay of the multiplier. Wallace proposed the column compression technique for instant multiplication operations in which the overall put off is proportional to the logarithm of the word duration of multiplier operand. The Wallace tree multiplier with column compression approach is quicker than array. In order to reduce the electricity and, the traditional full adder in Wallace tree multiplier is changed with a modified full adder In MUX based totally complete adder the whole adder is carried out using four:1 multiplexer Wallace tree multiplier energy discount has been finished. It is obvious that, one four:1 MUX may be made using 3 2:1 MUX.

The energy dissipation because of quick circuit can be deterred. Also, all the inner nodes are directly excited by way of the primary inputs, consequently switching activity is likewise reduced. But this reduction in power can be acquired on the price of area increment. As can be seen from fig. 4, the essential path postpone includes 3 MUX. Wallace tree multiplier is suitable for low power and small area applications these are the advantages. For implementing high power and large area also possible for that purpose Wallace tree will be proposed for high speed these all about the disadvantages of low power Wallace tree multiplier. To reduce the power consumption of the Wallace tree multiplier, a modified full adder can be used. The modified full adder is a low-power version of the conventional full adder that uses fewer transistors and reduces the power consumption while maintaining the same functionality. The modified full adder can be implemented using techniques such as transmission gate logic, pass-transistor logic, or dynamic logic. In a low-power Wallace tree multiplier using a modified full adder, the partial products are generated as in a conventional Wallace tree multiplier. However, the full adders used to add the partial products are replaced with modified full adders. The modified full adders consume less power than the conventional full adders, resulting in lower power consumption for the overall multiplier.

S.Nagaraja,k.Thyagarajarajan,D.Srihari,K.Gopi all these people in 2018 proposed that the Wallace Tree Multiplier for CMOS and CPL Logics. CPL Logic is low electricity good judgment. This paper pursuits at comparing the vicinity, electricity and delay of Wallace Tree Multiplier for CMOS and CPL Logics. The Multipliers are one of the key factors in most of excessive overall performance stems like Digital Signal Processing and Microprocessors. CMOS Logic is most famous MOSFET era. CMOS generation has the principle advantage of a whole lot smaller power dissipation and additionally CMOS has nearly no static electricity dissipation. When there may be switching then simplest electricity is dissipated. This allows us to integrate extra CMOS gates on IC than bipolar or NMOS generation and resulting in higher overall performance. Complementary Pass Transistor Logic (CPL) uses best NMOS transistors for good judgment business enterprise.

Complementary Pass Transistor Logic (CPL) consists complementary inputs/outputs and NMOS skip transistor community and CMOS output inverters. Inverted and non-inverted inputs are required to pressure gates of bypass transistor. In CMOS method the primary gates AND, XOR and OR gates designed first. Using those fundamental good judgment gates Half Adder, Full Adder this is three:2 Compressor Complementary Pass Transistor Logic in comparison to the traditional CMOS Logic Analysis of Wallace tree multiplier advantages are CPL logic is a low power logic, we can compare the area power and delay of Wallace tree multiplier for CMOS and Cpl logics. Wallace tree multiplier is a commonly used multiplier architecture that can perform high-speed multiplication with a reduced number of partial products. The Wallace tree multiplier can be implemented using different logic families such as CMOS and CPL. The implementation of the Wallace tree multiplier using CPL logic involves the use of Current-Mode Logic. CPL logic is a type of digital logic that uses the current rather than the voltage to represent digital signals. The CPL logic provides high-speed operation and low power consumption, but it is less immune to noise than CMOS logic. In conclusion, the design and analysis of the Wallace tree multiplier for CMOS and CPL logics involve generating partial products, grouping partial products, and reducing partial products. The implementation of the multiplier using CMOS logic provides high noise immunity.

Yamini devi yukata, Katta Pavani, Krishi Saladin all these people in 2020 proposed that the Five Wallace tree multiplier systems the use of five exceptional PA's (Sklansky adder, Kogge stone adder, BrentKung adder, Han Carlson adder and Ladner Fischer adder are designed for input length of sixteen-bits in this paper using Verilog HDL. All the designed multipliers are simulated and synthesized using Xilinx ISE — Major operation block in any processing unit is a multiplier. There are many multiplication algorithms are proposed, with the aid of the usage of which multiplier shape can be designed. Among diverse multiplication algorithms, Wallace tree multiplication algorithm is useful in phrases of speed of operation. With the development of generation, call for circuits with high speed and low vicinity is increasing at present, the generation is advancing very unexpectedly in very short duration of time.

The circuits being layout have some billions of components with low place, excessive velocity and low electricity intake. Hence location pace and strength play important position within the design of any circuit. The design analysis of high-speed Wallace tree multiplier using parallel prefix adders for VLSI circuit designs have Used multiplier design in many processors and memory units is Wallace tree structure Wallace tree multiplier using Kogge stone adder can be used but costing little bit more area when compared to other proposed structures is the disadvantage of high-speed Wallace tree multiplier. A Wallace tree multiplier is a commonly used multiplier architecture that can perform high-speed multiplication with a reduced number of partial products. The partial products are grouped and added using full adders and half adders to obtain the final product. Parallel prefix adders are adder architectures that can perform addition of multiple operands in parallel, which results in a reduced delay and increased speed compared to a conventional adder. The analysis of the high-speed Wallace tree multiplier involves the evaluation of the performance parameters such as power consumption, area, and delay. The power consumption of the multiplier depends on the number of partial products, the number of adders used, and the supply voltage. The area of the multiplier depends on the number of partial products, the number of adders used, and the implementation of the logic gates.

F. Kaess, R. Karan, B. Hochet and M. DeClercq all these people in 1997 proposed that the new encoding scheme for excessive-pace flash analog to digital converters using a Wallace tree is defined. It presents a global blunders filtering and its normal topology optimizes the signal propagation designing a high-pace A-to-D Converter, considered one of the most important worries consist in imparting an encoder that suits first-class the high velocity necessities .High-speed converters typically include a flash shape Considering the “Bit swapping” technique, we can study that its set of rules is mathematically equivalent to counting the quantity of logical ONEs, present on the outputs of the comparator’s new encoder scheme for flash analog-to-digital conversion the usage of a Wallace tree has been defined. its particular hobby is that it cannot lead to huge range mistakes (system faults), which makes it ideal for packages where errors fee is of an essential importance.

The new coding scheme high-speed ADC’s advantages are having low power, less complexity and optimum delay Wallace tree encoder and the drawbacks of new coding schema have inefficiency of the circuit when isolated one’s are encountered. Flash ADCs (Analog to Digital Converters) are widely used in high-speed data acquisition systems due to their high sampling rates and low latency. However, traditional flash ADCs suffer from various drawbacks such as large area, high power consumption, and high sensitivity to process variation. A new encoding scheme for high-speed flash ADCs is proposed to overcome these limitations. This encoding scheme is based on the use of a thermometer-to-binary encoder, which enables the use of low-resolution flash ADCs without compromising the conversion accuracy. The main advantage of this new encoding scheme is its ability to achieve high-speed operation with reduced power consumption and area. The proposed thermometer-to-binary encoder requires fewer comparators compared to traditional flash ADCs, which results in reduced power consumption and area. The segmented DAC architecture enables the use of low-resolution DACs, which also reduces the power consumption and area of the ADC. In conclusion, the new encoding scheme for high-speed flash ADCs based on the thermometer-to-binary encoder and segmented DAC architecture offers a promising solution for high-speed data acquisition systems.

Ashima Gupta, Anil Singh, Alpana Agarwal all these people in 2018 proposed that This have a look at describes the fantastically-digital 4-bit two hundred MS flash analogue to digital converter (ADC) whose main element may be digitally synthesized for that reason attaining low power, reducing the time-to-marketplace and is scalable with technology. The comparators used in the ADC consist of complementary metallic–oxide–semiconductor and NAND-NOR. Analogue to virtual converters (ADCs) for interfacing the actual-global analogue signal to the digital device. Different ADCs had been advanced by means of altering the architecture of ADCs like pipelined, integrating, binary seek, delta sigma, successive approximation and flash ADC. Medium- to excessive-speed facts conversions may be performed by means of using pipelined ADCs at medium to high resolution.

The most vital block of flash ADC is the comparator. The existing comparators are analogue in nature, and consume high electricity, huge area and require high design effort. With era scaling the digital circuits achieve better performance in phrases of location, pace and strength density, on the other hand, the analogue circuit face hassle to keep the same. Alternative to that, the virtual circuits amplify the sign to rails and also less touchy to the noise, automatize the synthesis, and bodily format. The highly digital voltage scalable four-bit ADC's advantages are it is for high-speed applications, a greater number of full adders are used size also increases these are the disadvantage of digital voltage scalable ADC's. The Highly-Digital Voltage Scalable 4-Bit Flash ADC is a type of Analog-to-Digital Converter that is designed to achieve high resolution, low power consumption, and high scalability. The highly digital architecture of this ADC allows for low power consumption, as the comparators are designed to operate in a low-voltage regime. Additionally, the use of a voltage scaling technique allows for high resolution with fewer comparators, reducing the area and power consumption of the ADC. The voltage-scaling technique also enables the ADC to operate over a wide range of input voltages. The voltage scaling technique and highly digital architecture make this ADC a promising solution for high-resolution, low-power ADCs in battery-powered applications and wireless sensor networks.

Y.Sravanakumar,Ch.suresh,P.SwarnamalaB.S.V.Sathyanarayana,S.Gayat hri all these people in 2022 proposed that which is a resistor ladder, encoder and comparator circuit. Wallace tree encoder with Wallace tree encoder performs a essential position and it based on changing thermometer code into binary code in ADC. The proposed MGDl approach offer Less Delay, Less Power Consumption, Better Power Delay Product and a smaller quantity of transistors compared to present strategies. The proposed designs are designed and simulated using Mentor Graphics Tool with 90nm CMOS era. This can be termed to be a excessive-velocity software and a flash form of flash Incomplete adder as its primary mobile. The complete adders remember the variety of logics “1” at them enter to provide final binary output. The full adders are organized to sum the inputs with the intention to shape Wallace tree. The Wallace tree encoder also referred to as one’s counter is built with full adder cells.

In various Wallace tree encoders had been supplied in this project inclusive of MGDl Based 32-Bit Wallace tree encoder has the gain of low power, less computing complexity. It consumes the Power approximately 28.38pW which is less as compared to different encoder and has a minimal delay of about 30.1501ns. The number of transistors is 260 required for designing Wallace tree encoder. Full adder-based Wallace tree encoder is having advantages are Less delay, less power consumption, better power delay product by using less transistors, it will correct bubble errors without the need of extra bubbles and a greater number of transistors used is the disadvantage of full adder Wallace tree encoder. Various full adder-based 32-bit Wallace tree encoders have been proposed in literature to improve the performance and reduce the area and power consumption of the encoder. These encoders differ in terms of the type of full adder used in their design. These full adder-based 32-bit Wallace tree encoders have been extensively analysed and compared in terms of performance parameters such as delay, power consumption, and area. The choice of the full adder used in the design of a Wallace tree encoder depends on the specific application requirements and design constraints. The performance comparison of different full adder-based Wallace tree encoders provides useful insights for selecting the appropriate adder circuit for a particular application.

G. Challah Ram, D. Sudha Rani, R. Balasaikesava all these people in 2022 proposed that the Dadda multiplier algorithm is similar to Wallace algorithm with few modifications. The algorithm depends upon the weights of the partial products. Firstly, the partial products are obtained as in normal multiplication. These partial products are obtained as in normal multiplication. These partial products are arranged in rows and column are equal. After the arrangement of partial products, the column these are reduced by using some formulas. Normal Wallace multiplier occupies more memory when compared with array and Dadda Multipliers but consumes less delay. The delay consumption is based on the type of adders used in the multipliers. In order to achieve very low delay, the conventional half and full adders can be replaced delays the conventional half and full adders can be replaced with new techniques In the paper carry select adder and binary to excess codes converter are used in the implementation of Wallace multiplier and the adders are explained.

Binary to Excess code converter is used in CSLA when the carry input is one. BEC increments the input bits by one so it is chosen in the case of where carry input is given as 1 in CSLA. By using BEC gates. In order to obtain efficient memory can be minimized as BEC structure consist of some gates. If there are four elements in maximum height of the column these elements should be reduced to three so that the maximum height of the columns will be three this reduction process is continued for three elements the reduction of these partial products is done by using full adders and the carry should be continued till the maximum height of the column researches to two the final result is obtained by adding above two rows carry select adder is similar to ripple carry adder. In CSLA the total number of bits are partitioned into equal sizes and the carry in for second group is taken as both the cases for carry zero and one at once so that the delay can be greatly reduced. the desired outputs are selected line multipliers using adder can have better delays but it consumes more area as no of gates increased. The choice of the encoding scheme and full adder used in the design of a Wallace tree encoder plays a significant role in determining the performance of the circuit. Various encoding schemes, full adders, and multiplier architectures have been proposed in literature to improve the performance and reduce the power consumption and area of the circuit.

Thottempudi pardhu, Manusha.S, Katakam Sirisha all these people in 2022 proposed that The Wallace tree is built only with elementary adder cells. At the first logical level, each cell counts the number of logical ones at its entire and outputs a 2-bit binary coded output. After this first stage, in order to get a topologically regular structure, a good practice consists in adding the two bit words of adjacent cells two by two, giving 3-bit binary outputs as shown in the figure and so on in order to obtain the final binary output coder for converter. The intrinsic structure of the encoder, the hierarchy between the comparator is eliminated, allowing no wide range errors as it can be the case with other encoders. For instance, simple bubble far away from the transition area that means the few comparators that are situated around the exact one to zero transition point can only generate a maximal error of one will be addressed in ROM encoder thereby generation erroneous code. But that is not the case in Wallace encoder where in error is reduced to a very large extent.

Our design of the 3bit flash ADC requires 7 comparators and a Wallace tree encoder. Comparator were design using TQI technology as shown in figure and the Wallace tree encoder for 3-bit ADC is initially DC analysis need to be performed as it is take into account parasitic capacitances the desired comparator outputs were not obtained in transient analysis hence widths of the comparator transistors were adjusted to get desired comparator values. Also in built sample and hold device from eldo tool was added before the comparator is eliminated other allowing no wide range errors as it can be the case with other encoders for instance, a simple bubble far away from the transition area device from eldo tool was added before the comparator in order to increase the range of input frequency that our design supports for ramp input with maximum sampling rate range frequency comparators tool to increase for ramp output there are so many waveforms comparators for instance generate a maximum can only generate a maximal error of one also in bulit sample and hold service can only generate to increase a one to zero maximal error of one also inbuilt ramp input wave form and sine wave form is applied.

2.2 LITERATURE SUMMARY

Wallace tree encoder, multiplier, thermometer code, flash ADC's, fat tree encoder. Especially these are the matters we learn in this literature survey from those the things what we learn are the speed is advanced by using almost a component of two when the use of the fat tree encoder, which in truth demonstrates the fat tree encoder is a powerful solution for the bottleneck trouble in extremely-high velocity and the reality that there are three OR gate delays from any leaf node to any root node. The sign postpone from the $N-1$ inputs to the n outputs is uniform within the fat tree encoder. This is a vital asset permitting excessive speed wave pipelining without the pipeline registers. In counter-primarily based encoder we're carried out research and examine that their commended layout strength consumption of the Wallace tree encoder that is diminished by means of the corrected layout of the entire adder.

The adapted complete adder comprises of approximately thirteen transistors. By reducing the number of the transistors, the electricity intake of the entire adder can be decreased and it shows a greater changed complete adder. Wallace tree encoder in interpolation ADC's we find that the parallel structure of flash ADC will lessen the postpone of the ADC's where as compared to conventional ADC's It ends in higher yield and to advanced noise performance with the help of Acceptable brought circuitry. High performance Wallace tree encoder the comparator compares and produces the output inside the type of modern zero's and 1's whilst reference ladder generates the reference voltage. Then the binary cost is transformed into thermometer code. The binary conversion is finished with the aid of Wallace Tree encoder utilising bubble mistakes common sense a low strength Wallace tree encoder is designed using skip transistor logic (PTL) full adder. The Wallace tree architecture booth encoder is aims to reduce the overall latency. This thing leads to increased high speed and reduced power consumption. The design makes use of compressors in place of full adders, and the final carry propagate stage is replaced by a Carry select adder. If we replace XOR gates with multiplier gate the critical path delay is minimized. The novel low strength and high velocity Wallace tree is having the Sklansky kind of tree adder is

preferred due to its decrease electricity consumption than that incurred by means of other tree adder systems.

Furthermore, the latency of Sklansky adder is decreased to 6, that is much less than that found out by way of Brent Kung, Han Carlson and Ladner-Fischer tree adder circuits. Sklansky adder, the binary trees of cells first generate all the carry input bits concurrently. This structure follows a normal pattern. In conversion of thermometer code binary code, the thermometer code consists of series of zeros followed by series of 1s i.e. There need to be most effective one transition. Due to the multiple non-idealities and mismatches inside the comparators, unexpected zeros in collection of ones and ones in collection of zeros appear.

This makes the thermometer code invalid. This circumstance is called as bubble errors. So, whilst designing a Flash ADC, bubble mistakes correction must additionally be considered together with Wallace tree encoder. From this literature survey finally, we understood that the Wallace tree, Wallace tree multiplier, thermometer code, and what are the proposed methods they proposed and Wallace tree is the simplest and the most in your price range in phrases of chip location manner to implement this encoding algorithm. Its blessings over greater classical encoders so that the Wallace tree works with very high speed and for good performance the general encoder is normally worked that means speed is little bit low as compared to Wallace tree encoder this suitable for working with any type of logic gates or any type of circuits and transistors. Wallace tree encoder is a widely used encoding technique in digital signal processing and communication systems. It is used to convert a parallel binary data stream into a more compact and efficient representation. In a Wallace tree encoder, the input binary data is first divided into groups of 3 bits. Each group is then processed using a full adder to generate a partial sum and a carry bit. The partial sums are then combined using another level of full adders to generate the final encoded output. Several research papers have been published on the topic of Wallace tree encoder, which includes the following A High-Speed Wallace-Tree Encoder Design by Y. Jin and J. Wang: This paper presents a high-speed Wallace tree encoder design using a pipelined architecture. The proposed design achieves a high encoding speed and low power consumption compared to conventional Wallace tree encoder designs.

A novel design of Wallace tree encoder for low power and high-speed applications by H. Thakur and M. S. Yadav: This paper proposes a novel design of the Wallace tree encoder that reduces power consumption and increases the encoding speed by reducing the number of full adders used in the encoding process. Design of high-speed Wallace tree encoders for multipliers by K. M. Kavi and V. K. Jain: This paper presents a design of high-speed Wallace tree encoders for use in multipliers. The proposed design uses a pipelined architecture with carry look-ahead adders to achieve a high encoding speed. Low-Power and High-Speed Wallace Tree Encoder for Digital Signal Processing Applications by S. S. S. Karthikeyan and S. Manikandan: This paper proposes a low-power and high-speed Wallace tree encoder design for digital signal processing applications. The proposed design uses a modified Wallace tree architecture with a reduced number of full adders to achieve low power consumption and high encoding speed. Overall, the research on Wallace tree encoder is focused on improving its speed, power consumption, and efficiency for various applications in digital signal processing and communication systems.

ADCs are used in a wide range of applications, including communication systems, control systems, data acquisition systems, and measurement instruments. The main function of an ADC is to sample the analog input signal and then quantize it into a discrete set of levels. The process of quantization introduces some error, known as quantization noise, which is usually modeled as a random signal. ADCs can be classified based on their architecture, resolution, sampling rate, and input signal range. The choice of the encoding scheme and full adder used in the design of a Wallace tree encoder plays a significant role in determining the performance of the circuit. Various encoding schemes, full adders, and multiplier architectures have been proposed in literature to improve the performance and reduce the power consumption and area of the circuit. The performance comparison of different full adder-based Wallace tree encoders provides useful insights for selecting the appropriate adder circuit for a particular application.

2.3 PROBLEM DEFINITION

In This analysis of an efficient Wallace tree encoder for high-speed applications on this what we should implement before that We discover that in previous initiatives all are inform about that simplest pace and overall performance of an Wallace tree encoder, For this we need put into effect a Wallace tree encoder that's having occupies less space meaning small quantity of vicinity and performance might be high Without changing the performance we want to enforce an efficient Wallace tree encoder for excessive-pace applications with the assist of full adders reducing. Primarily based on the base papers of the preceding projects we want to reduce adders or transistor from that we need to implement a Wallace tree encoder for high-pace applications.

Wallace tree encoder where we use why we need this about all these types of questions we define the results about the Wallace tree encoder for high-speed applications after long research we conclude that Wallace tree encoder is used to reduce the number of partial products that need to be generated during binary multiplication. In a standard multiplication process, each bit of the multiplier is multiplied with each bit of the multiplicand, resulting in a large number of partial products that need to be added together. This process can be time-consuming and resource-intensives, used in digital signal processing for filtering the signals.in this proposed process can we use mosfet or logic gates to implement the Wallace tree encoder which is very efficient in speed as compared to the normal encoder and we are used full adders to produce the Wallace tree encoder for high-speed applications for signal processing, image processing to transfer data without interruption this Wallace tree encoder is more useful. The main difference between an encoder and a Wallace tree encoder is the encoding scheme used. An encoder uses a simple mapping between the input data and the output code, while a Wallace tree encoder uses a more complex algorithm that involves adding together multiple groups of input bits. while both an encoder and a Wallace tree encoder are used to convert a binary code into a more compressed form, a Wallace tree encoder is a specific type of encoder that uses a more complex algorithm to achieve greater compression.

CHAPTER 3

PROCEDURES OF EXISTING SYSTEM

3.1 EXISTING METHODOLOGY

In this existing methodology what we learned is in all Wallace tree projects they concluded that it's a high speed and best performance done because of bubble sorting error inbuilt in Wallace tree and many number of adders and transistors are used for this more area is occupied and performance is same for that improving this existing method we learned from all the above literature surveys ,and it consists of eleven (11) full adders with 15 thermometers as code inputs and four binary outputs labeled as b3, b2, b1, b0. In the existing type of Wallace tree encoder, all the 15 thermometer code inputs starting from i1 to i15 are channeling via equal number of complete adders. Hence the propagation delays between each input and the corresponding output is effectively controlled and also identical. So, speed of operation of the existing design is reasonably good. In this design conventional full adder is used and each of the full adders consists of 28 transistors.

Totally 308 transistors are required for full adder Wallace design tree encoder and hence the prevailing circuit takes up more energy. The recent advancement of technology most of the signal processing tasks have been transferred from the analog to the digital domain. The ADCs (Analog to Digital Converter) provide a liaison between the real-world analog signals and the digital processors. Circuit realization for low power and low area has become an important issue with the growth of integrated circuit towards very high integration density and high operating frequencies. The full adder circuit adds three one-bit binary number inputs (Cin, A, B) and outputs two one-bit binary numbers, a sum (SUM) and a carry (COUT). Due to the important role played by Full adder in various arithmetic units, optimized design of Full adder to achieve low power, small size and delay is needed.

The relations between the inputs and the outputs are expressed as:

$$\text{SUM} = A \oplus (B \oplus C) \text{ -----(1)}$$

$$\text{COUT} = AB + BC + AC \text{ -----(2)}$$

The above shown Conventional full adder is a combination of PMOS pull up transistor and NMOS pull down transistor. It is well known for its robustness and scalability at low supply voltages. But the use of substantial number of transistors results in high input loads, more power consumption and larger silicon area.

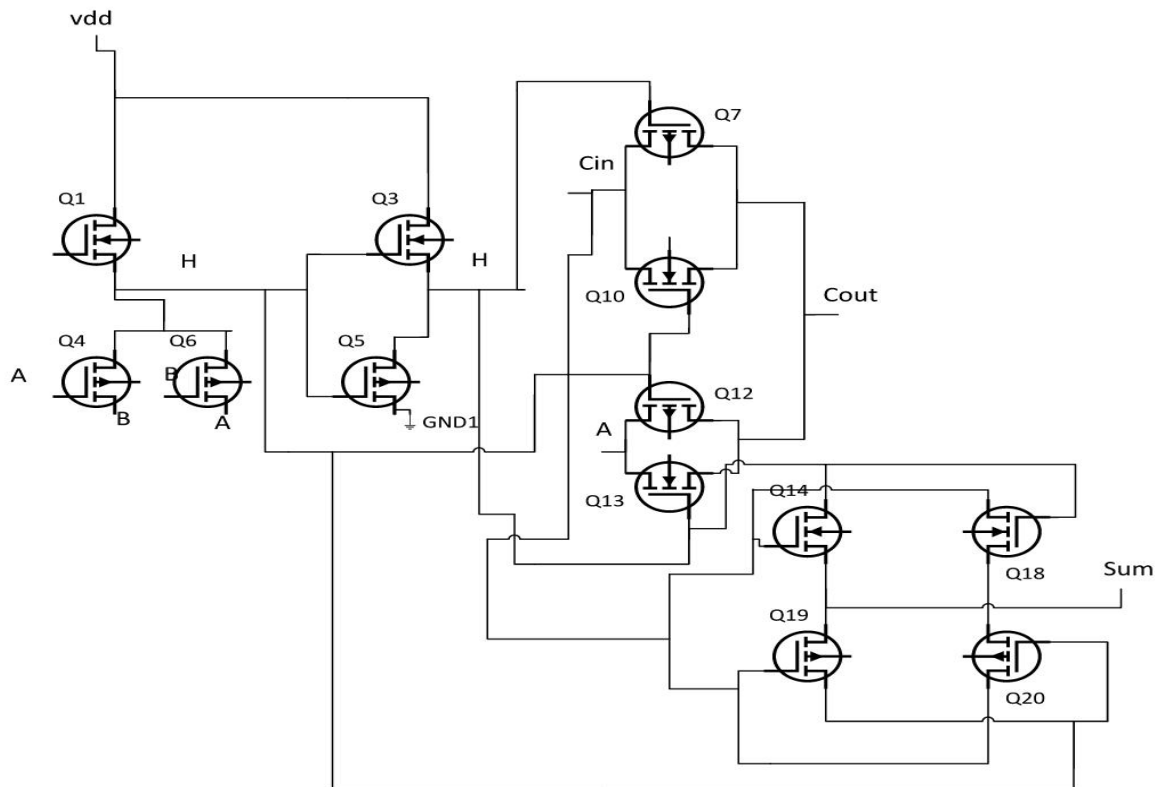


Fig 3.1: Existing full adder circuit diagram

In this they were concluded that using full adders proposed a Wallace tree encoder with using cadence software tool which was used for design and implement different types of new technologies researches this project was adopted complete adder comprises of about 13 transistors, by reducing the number of transistors the energy consumption of the complete adder can be reduced, in this process how the they designed is they naming the number of transistors using the format as Q1, Q2,...up to Q13.

3.2 DRAWBACKS IN PREVIOUS SYSTEM

Larger transistor counts the additional circuitry required by the Wallace tree encoder typically results in a larger number of transistors being used, which can increase the static power consumption. More clock cycles the multiplication operation using the Wallace tree encoder typically takes more clock cycles than a regular multiplication operation. This can result in a longer overall processing time and hence a higher dynamic power consumption. The power consumption of the Wallace tree encoder can be a concern in some applications, particularly those that are power-constrained or battery-powered. The high-power consumption is mainly due to the following factors. Increased circuit complexity The Wallace tree encoder adds additional circuitry to the multiplication operation, which can increase the total circuit complexity and, consequently.

The power consumption Low-power circuit design The circuit design can be optimized for low power consumption, using techniques such as clock gating, power gating, and voltage scaling. Use of low-power components: Low-power components, such as low-power transistors and memory cells, can be used to reduce power consumption. Parallelization the Wallace tree encoder can be parallelized to reduce the number of clock cycles required for the multiplication operation, thereby reducing dynamic power consumption. Energy-efficient algorithms Energy-efficient multiplication algorithms can be used, such as Booth's algorithm or Montgomery multiplication, which are known to be more energy-efficient than the Wallace tree encoder for certain operand size. Increased circuit complexity The Wallace tree encoder introduces additional complexity to the multiplication process, which can make it more difficult to implement and debug. This complexity can also increase the area and power consumption of the circuit. Reduced accuracy The Wallace tree encoder is known to introduce some errors into the multiplication process due to rounding and truncation. While these errors may be negligible in some applications, they can be significant in others where high precision is required. Limited scalability The Wallace tree encoder is not well-suited for very large multiplication operations, since the number of partial products can grow exponentially with the size of the operands.

While there are techniques for mitigating this problem, such as multi-level Wallace trees, they can add additional complexity and latency to the algorithm. Dependent on input values the performance of the Wallace tree encoder can be highly dependent on the values of the input operands. In some cases, the algorithm may perform poorly or introduce significant errors if the input values have certain properties, such as a large number of leading or trailing zeros. Overhead The additional logic required to implement the Wallace tree encoder can result in increased overhead in terms of area, power consumption, and design time. This overhead may be a concern in some applications where resources are limited.

Additional circuitry: The Wallace tree encoder adds additional circuitry to the multiplication operation, which can increase the total circuit area. Larger transistor count The additional circuitry required by the Wallace tree encoder typically results in a larger number of transistors being used, which can increase the static power consumption and also increase the area. Multi-level implementation For large operand sizes, the Wallace tree encoder may need to be implemented using multiple levels of Wallace trees, which can significantly increase the area. Circuit optimization The circuit design can be optimized for area, using techniques such as gate sizing, transistor sizing, and logic simplification. Area-efficient components: Area-efficient components, such as low-power transistors and memory cells, can be used to reduce the overall circuit area. Algorithmic optimization: Algorithmic optimizations, such as using Booth's algorithm or Montgomery multiplication, can reduce the number of partial products and hence the area overhead of the Wallace tree encoder.

Customized implementations Customized implementations of the Wallace tree encoder, tailored for specific applications or operands, can be designed to reduce the area overhead. Additional circuitry. The Wallace tree encoder adds additional circuitry to the multiplication operation, which can increase the propagation delay of the circuit. Multi-level implementation For large operand sizes, the Wallace tree encoder may need to be implemented using multiple levels of Wallace trees, which can significantly increase the delay.

Longer critical path The multiplication operation using the Wallace tree encoder typically has a longer critical path than a regular multiplication operation. This can result in longer overall processing time and hence a higher delay.

Circuit optimization The circuit design can be optimized for speed, using techniques such as gate sizing, transistor sizing, and logic simplification.

High-speed components High-speed components, such as high-speed transistors and memory cells, can be used to reduce the overall circuit delay.

Algorithmic optimization Algorithmic optimizations, such as using Booth's algorithm or Montgomery multiplication, can reduce the number of partial products and hence the delay overhead of the Wallace tree encoder.

Parallelization the Wallace tree encoder can be parallelized to reduce the number of clock cycles required for the multiplication operation, thereby reducing the delay.

Modular design The Wallace tree encoder can be designed using a modular approach, where each stage of the Wallace tree is designed separately and then integrated into the overall design. This can simplify the layout and reduce the complexity of interconnections.

Design reuse Design reuse can be used to simplify the layout by reusing previously designed and optimized components.

3.3 APPLICATIONS FOR WALLACE TREE ENCODER

Wallace tree used in digital signal processing DSP structures, arithmetic logical units ALU's and several low power and high-speed arithmetic applications. To sum partial products in step by step until two numbers are left. Used in the process of converting the thermometer or unary code to binary. Wallace tree encoder is well efficient in reducing all the bubble errors. High speed application for the flash type of ADC. Encoders are very common electronic circuits used in all digital systems. Encoders are used to translate the decimal values to the binary in order to perform the binary functions such as addition, subtraction, multiplication, etc. Other applications especially for Priority Encoders may include detecting interrupts in microprocessor applications. Wallace tree encoders can have several roles in automotive applications, particularly in the design of digital signal processing circuits used in advanced driver assistance systems (ADAS) and autonomous driving systems.

One role of Wallace tree encoders in automotive is to perform high-speed and efficient multiplication of large data sets. This can be important for implementing algorithms used in ADAS and autonomous driving systems, such as object detection and recognition, image and video processing, and sensor fusion. Another role of Wallace tree encoder in automotive is to reduce power consumption and chip area. This is important for designing circuits that can operate reliably and efficiently in the harsh environments of automotive applications. By reducing power consumption and chip area, Wallace tree encoders can help improve the overall reliability, performance, and cost-effectiveness of automotive systems. Overall, Wallace tree encoders can play a key role in the design and implementation of digital signal processing circuits used in automotive applications. They can provide efficient and high-speed multiplication, which can improve the overall performance of algorithms used in ADAS and autonomous driving systems, while also reducing power consumption and chip area for improved reliability and cost-effectiveness.

An encoder is a digital circuit that converts a binary code into a more compact and efficient representation, typically using fewer bits. The output of an encoder is a code that represents the input data in a more compressed form. Encoders are commonly used in digital communication systems, data compression, and error correction. A Wallace tree encoder is a specific type of encoder that uses a tree-like structure of full adders to encode a binary code. It is designed to operate on groups of binary digits, typically 3 or 4 bits, and generates a more compressed output code than a simple encoder. The main difference between an encoder and a Wallace tree encoder is the encoding scheme used. An encoder uses a simple mapping between the input data and the output code, while a Wallace tree encoder uses a more complex algorithm that involves adding together multiple groups of input bits. Another difference is that a Wallace tree encoder is more complex and requires more circuitry than a simple encoder, but it can generate a more compressed output code. This makes it useful in applications where space and power consumption are important factors, such as in digital signal processing and communication systems.

CHAPTER 4

PROPOSED SYSTEM

We find out that during preceding tasks all are inform approximately that simplest tempo and overall performance of a Wallace tree encoder, for this we want positioned into effect a Wallace tree encoder it is having occupies much less space that means small amount of region and performance might be high Without converting the performance we want to put into effect Wallace tree encoder for excessive-place applications with the help of full adders reducing. Primarily based on the base papers of the preceding tasks we want to reduce adders or transistor from that we want to enforce a Wallace tree encoder for high-tempo packages. Finally, we want to propose a Wallace tree encoder for high-speed applications with less area and high performance.

The difference between existing methodology and proposed methodology is that size of the Wallace tree is large in existing methodology from this we have to develop with the small Wallace tree with high-speed performance in proposed methodology. And in existing methodology the area occupies large amount and in proposed methodology with less amount of area we want implement. In the existing method power consumption as over high and we have to check whether the power consumption is less or high, we have to develop Wallace tree encoder. The number of transistors we are used that are twelve those are all in a Wallace tree in this Wallace tree we have fifteen is to four ratio that means fifteen inputs and four outputs based on full adders or logic gates using only we are implementing the Wallace tree encoder for high speed applications. One proposed system for a Wallace tree encoder using fewer transistors is to use a modified Wallace tree structure that reduces the number of full adders required in the encoding process. This modified structure is called a carry-select adder (CSLA) Wallace tree encoder. The CSLA Wallace tree encoder also includes a carry-select adder circuit that is used to combine the encoded outputs of each group into a single output code. This circuit further reduces the number of full adders required in the overall encoding process.

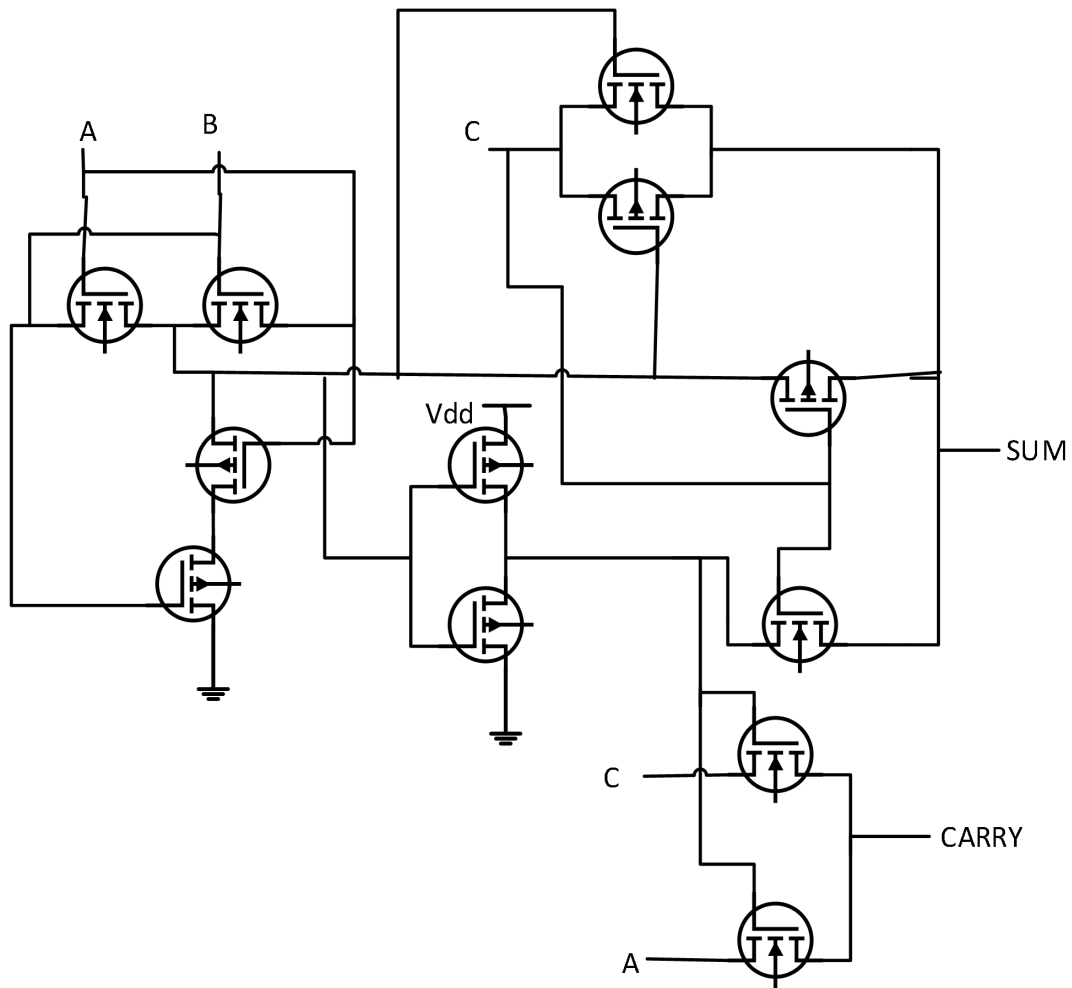


Fig 4.1: Proposed full adder circuit

In this proposed system we have reduced that thirteen transistors into twelve transistors using we implemented this circuit using HSPUI software. In this A, B, Cin are inputs and SUM and Cout or CARRY these are outputs. And we got the appropriate output with average power and delay and from these two we calculated the PDP values and all using the power formula and all the main applications of this Wallace tree encoder is to perform the signals without interrupts it acts as a filter and bubble corrector, it was used in digital circuits, in daily life we are used in image and video compression that means reduce the size of the file without changing the resolution and also used in speech recognition systems ,where audio signals need to be compressed and transmitted efficiently.

4.1 HSPICE SOFTWARE

Hewlett Simulation Program with integrated circuit is the full name of HSPICE. Unlike board-level designs made up of individual components, integrated circuits cannot be breadboarded before being manufactured. Furthermore, due to the high cost of photolithographic masks and other manufacturing requirements, it is critical to design the circuit to be as close to perfect as possible before it is designed until committing to producing an integrated circuit, the industry-standard method of verifying circuit operation at the transistor level is to simulate the circuit with SPICE.

4.2 COSMOSCOPE

Cosmos cope is a software which is used to calculate the delay value.

4.2.1 Power

power refers to the rate at which energy is consumed or produced. In physics, power is defined as the amount of work done per unit of time. Power can also be thought of as the rate of energy transfer or conversion. It is measured in units of watts (W) or joules per second (J/s). Electric power is the rate at which electrical energy is transmitted by an electric circuit per unit of time. It is the pace at which work is completed. Electrical power is the rate at which electrical energy is transmitted by an electric circuit per unit time in terms of an electric circuit.

The unit of the Electric power = Watt

$$\text{Power} = V \cdot I (\text{W})$$

$$I = Q/t$$

Where:

W = power in watts

V = Potential in Volts.

I = Current in amps

Q = charge in coulombs

t = Time in seconds

4.2.2 Potential

potential is a scalar quantity that represents the potential energy per unit charge at a given point in space. It is typically denoted by the letter "V" and is measured in units of volts (V).

4.2.3 DELAY

The time taken for a signal to reach its destination is referred to as delay. The time it takes for the consequence for a shift in input to be noticeable at the output is known as the delay of a logic gate. Power delay product is the product of the power and delay.

$$\text{PDP} = \text{power} * \text{Delay}$$

4.2.4 TIME

Time is a concept used to describe the progression of events in a measurable and quantifiable manner. It is often thought of as a continuous and linear dimension in which events occur in a sequence from past to present to future. In electronics and digital circuits, time plays a crucial role in determining the speed and performance of the system. The time it takes for signals to propagate through the circuitry is an important factor in determining the overall performance of the system. This propagation time is influenced by factors such as the distance between components, the capacitance and resistance of the components, and the clock frequency of the system. Timing analysis is a crucial aspect of digital circuit design, as it involves analyzing the propagation times of signals through the circuit to ensure that they meet the required timing specifications. Techniques such as clock skew correction, buffering, and pipelining can be used to improve timing performance in digital circuits.

4.2.5 FREQUENCY

In electronics, frequency refers to the number of cycles of a periodic waveform that occur in one second. It is typically measured in Hertz (Hz), which represents one cycle per second.

4.2.6 CURRENT

In electronics, current refers to the flow of electric charge through a circuit. It is typically measured in amperes (A), which represents the rate of flow of electric charge in coulombs per seconds.

CHAPTER 5

RESULTS AND DISCUSSION

The existing and proposed architecture are simulated by using AvanWaves simulator. In this paper two types of the whole adder designs are supplied. The operation is finished as separate module. Each module has 12 transistors when those modules are combined, it results in an exclusive performance than the conventional design. we are able to design an N bit adder in order to deliver suitable performance than the conventional design. In this design inverted transistor and multiplexer is used, this inverter will provide high drivability and full swing essential route signal deliver.

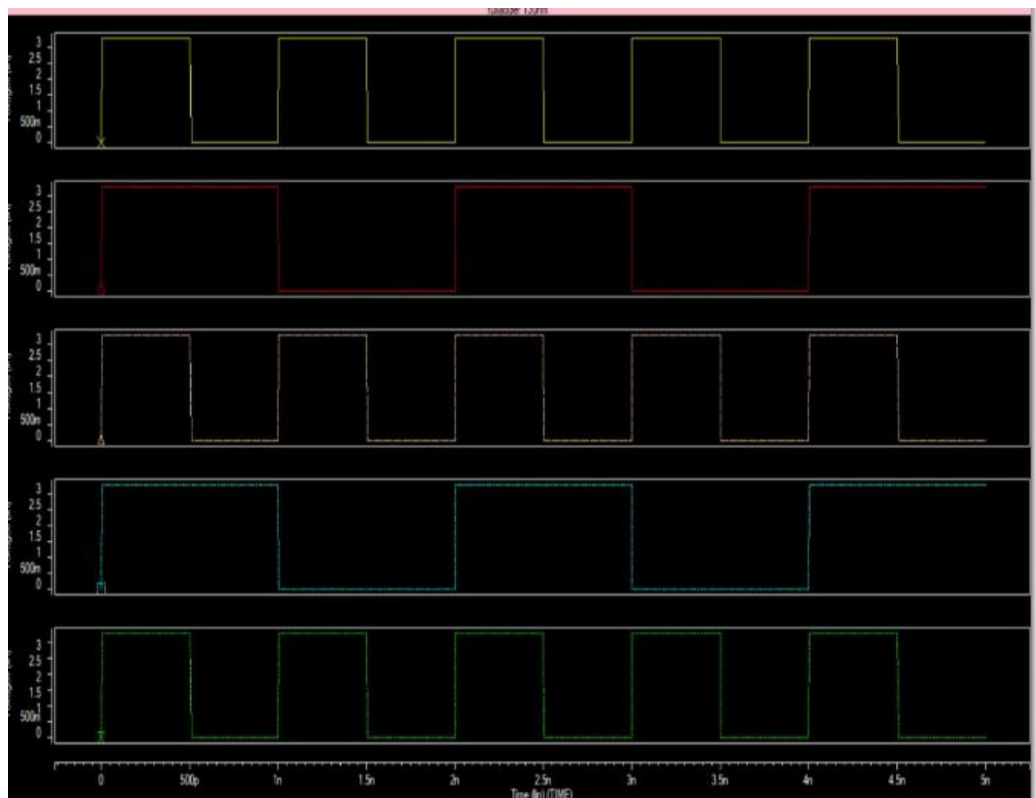


Fig 5.1 Proposed system simulation result

The figure 5.1 shows the simulation output of proposed full adder FA. the inputs are given as A, B and outputs are SUM, CARRY.

Table 5.1 PERFORMANCE ANALYSIS

Device	Average power(W)	Delay(s)	PDP(J)
NAND	$2.193 \times 10^{-4} \text{W}$	$47.85 \times 10^{-12} \text{s}$	$1.0493 \times 10^{-14} \text{J}$
NOT	$7.878 \times 10^{-6} \text{W}$	$2.789 \times 10^{-12} \text{s}$	$2.1971 \times 10^{-17} \text{J}$
Existing Full Adder	$8.4496 \times 10^{-5} \text{W}$	$380.87 \times 10^{-12} \text{s}$	$3.2181 \times 10^{-14} \text{J}$
Existing Wallace Tree Encoder	$1.8380 \times 10^{-3} \text{W}$	$999.76 \times 10^{-12} \text{s}$	$1.837 \times 10^{-12} \text{J}$
Proposed Full Adder	$4.628 \times 10^{-5} \text{W}$	$201.146 \times 10^{-12} \text{s}$	$9.3090 \times 10^{-15} \text{J}$
Proposed Wallace Tree Encoder	$1.289 \times 10^{-3} \text{W}$	$785.7 \times 10^{-12} \text{s}$	$1.0127 \times 10^{-12} \text{J}$

In this analysis table device, average power, delay, PDP these are the parameters we calculated through this research about Wallace tree encoder and we used this cosmos scope software for calculating the delay values , average power was calculated or getting from the HSPUI software after simulating the circuit we got the output results in that average power for each and every calculation is related with other parameter ,we find that the PDP value from the delay and the average power product we got the value of PDP for different types of devices like existing adder, proposed adder, Nand ,not for all these devices we done all the delay ,average power and PDP values are find out by the this calculations.

Finding the average power, delay, and power-delay-product (PDP) for a device is important for a number of reasons, including. The average power consumption of a device is an important consideration in many applications, especially those where power consumption is a critical factor, such as in mobile devices, wearables, or battery-powered devices. By knowing the average power consumption and external battery life.

The delay of a device is a measure of how long it takes for the device to respond to an input signal. In many applications, such as in digital signal processing, the delay of a device can be critical to its overall performance. By measuring the delay of a device, designers can optimize the device to reduce the delay and improve performance. The power-delay-product (PDP) is a measure for energy consumed by a device over a given period of time. It is calculated by multiplying the average power consumption by the delay of the device. The PDP is an important metric in many applications, especially those where energy efficiency is a critical factor, such as in wireless communication systems or data centers.

By optimizing the PDP, designers can reduce the energy consumption of the device and improve its overall efficiency. In summary, finding the average power, delay, and power-delay-product for a device is important for optimizing its power consumption, performance, and energy efficiency, which are critical factors in many applications. Additionally, the existing methodology requires a larger area, whereas the proposed methodology aims to occupy less area. Moreover, the existing method consumes a significant amount of power. Here are some possible avenues for future work.

Optimizing for different number representations The Wallace tree encoder was originally developed for use with binary numbers, but it can also be adapted for use with other number systems, such as ternary or quaternary. Further work could explore how to optimize the algorithm for these representations.

Improving accuracy The Wallace tree encoder is known to introduce some errors into the multiplication process due to rounding and truncation. The main advantage of the Wallace tree encoder is that it can significantly reduce the number of bits required to represent binary data, which can save storage space and reduce the complexity of digital circuits. This makes it useful in applications such as digital signal processing, image processing, and data compression. The Wallace tree encoder is a powerful tool for reducing the storage and processing requirements of digital data, and its performance can be optimized through careful design and analysis. However, like all digital circuits, the performance of the Wallace tree encoder is limited by physical factors such as the speed of electronic signals and the properties of the materials used to construct the circuit.

CHAPTER 6

FUTURE WORK AND CONCLUSION

In this project we are reduce the transistors and done a circuit which was having very speed and average power and Delay values compared with the previous ones and concluded that the Wallace tree encoder is used in Images processing, digital signal processing for filter the signals and helpful for error corrections and also used in telecommunications and in many applications we are using this PROJECT .In VLSI based on the coms technology we are using to design the circuit and now a days the role of VLSI is very precious how means it was using in all automobile industrial, automotive, many more things there placing number of transistors, resistor's, capacitor on a single chip to do multiple tasks only it's because of VLSI.

The main difference between the existing methodology and proposed methodology lies in the size of the Wallace tree. In the existing methodology, the tree is larger which affects the speed performance, whereas the proposed methodology aims to develop a smaller Wallace tree that would improve the speed performance. Additionally, the existing methodology requires a larger area, whereas the proposed methodology aims to occupy less area. Moreover, the existing method consumes a significant amount of power, and we need to develop a Wallace tree encoder to check whether the power consumption is high or low in the proposed methodology. The Wallace tree is a specific type of circuit designed for multiplication, and it has some unique advantages and disadvantages. However, there are other types of circuits that can be used for multiplication as well, depending on the specific requirement of the system.

One alternative to the Wallace tree is the Dadda multiplier, which is another type of binary multiplication operation more efficiently than a traditional ripple-carry adder. The Dadda multiplier also uses a tree-like structure, but it uses a different method for grouping and adding te partial products. Another alternative is Booth multiplier, which is a circuit that uses a combination of shifts and additions to perform multiplication more efficiently than a traditional ripple-carry adder. The booth multiplier is also more efficient than the Wallace tree in terms of hardware

requirements, but it can be slower for smaller operand sizes. There are also other multiplication circuits, such as the array multiplier, the carry-save multiplier, among others, each with their own advantages and disadvantages. Ultimately, the choice of multiplication circuit depends on the specific requirements of the system, such as the desired speed, accuracy, and hardware constraints.

Wallace tree encoder is a commonly used technique for products generated in a multiplication operation. although the basic algorithm is well established, there are still several areas where further research could be done to improve its performance or extended its capabilities. Here some possible avenues for future work. Optimizing for different number representations The Wallace tree encoder was originally developed for use with binary numbers, but it can also be adapted for use with other number systems, such as ternary or quaternary. Further work could explore how to optimize the algorithm for these representations Improving accuracy The Wallace tree encoder is known to introduce some errors into the multiplication process due to rounding and truncation. Researchers could investigate ways to reduce or eliminate these errors, potentially by using more advanced error-correction techniques.

Parallelizing the algorithm, The Wallace tree encoder can be easily parallelized, since each column of the tree operates independently of the others. Further work could be explored how to optimize the algorithm for use with multi-core processors or specialized hardware such as FPGA. Developing more efficient variations Although the basic Wallace tree encoder is widely used, there are several variations that have been proposed in the literature that may offer better performance or other advantages. Researchers could investigate these variations in more detail, potentially developing new techniques that improve on the original algorithm. Exploring new applications The Wallace tree encoder was originally developed for use in digital signal processing applications, but it has since found use in a wide variety of other areas, such as cryptography and image processing. Future work could explore how the algorithm can be adapted for use in these and other applications.

In conclusion, the design and implementation of high-performance digital circuits require careful consideration of various factors such as speed, power

consumption, and area. The Wallace tree encoder is an essential component of arithmetic circuits, especially in the design of multipliers. The choice of the encoding scheme and full adder used in the design of a Wallace tree encoder plays a significant role in determining the performance of the circuit. Various encoding schemes, full adders, and multiplier architectures have been proposed in literature to improve the performance and reduce the power consumption and area of the circuit. The selection of the appropriate encoding scheme and full adder depends on the specific application requirements and design constraints.

Extensive analysis and comparison of different encoding schemes and full adder-based Wallace tree encoders provide useful insights for designing high-performance digital circuits. Several studies have been conducted to analyze and optimize the performance of the Wallace tree encoder in various contexts. These studies have focused on factors such as circuit area, power consumption, speed, and accuracy, and have proposed various modifications to the basic Wallace tree algorithm to improve its performance in different scenarios. In conclusion, the design and implementation of high-performance digital circuits require careful consideration of various factors such as speed, power consumption, and area. The Wallace tree encoder is an essential component of arithmetic circuits, especially in the design of multipliers. The choice of the encoding scheme and full adder used in the design of a Wallace tree encoder plays a significant role in determining the performance of the circuit. Various encoding schemes, full adders, and multiplier architectures have been proposed in literature to improve the performance and reduce the power consumption and area of the circuit. The selection of the appropriate encoding scheme and full adder depends on the specific application requirements and design constraints. Extensive analysis and comparison of different encoding schemes and full adder-based Wallace tree encoders provide useful insights for designing high-performance digital circuits.

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