

HIGH SPEED SERIAL DIVIDER FOR VLSI APPLICATIONS

Submitted in partial fulfilment of requirements for the award of
Bachelor of Engineering in
Electronics and Communication Engineering

by

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SATHYABAMA

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(DEEMED TO BE UNIVERSITY)**

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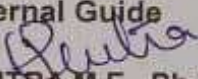
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BONAFIDE CERTIFICATE

This is to certify that this Project Report is the bona fide work of **ABIRAMI M (39130007)** and **SHAHITHA BANU A (39130412)** who carried out the project entitled "HIGH SPEED DIGITAL ARCHITECHTURE FOR VLSI APPLICATIONS" under our supervision from January 2023 to April 2023.

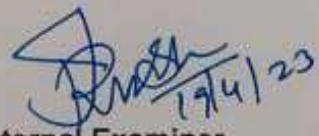
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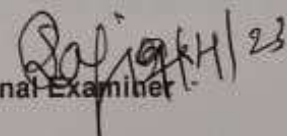

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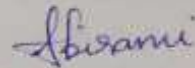
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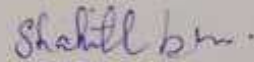

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DECLARATION

We, ABIRAMI M (39130007) and SHAHITHA BANU A (39130412) hereby declare that the Project Report entitled "HIGH SPEED SERIAL DIVIDER FOR VLSI APPLICATIONS" done by us under the guidance of Dr.P.CHITRA M.E., Ph.D. Associate Professor is submitted in partial fulfillment of the requirements for the award of Bachelor of Engineering degree in Electronics and Communication Engineering.



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ABSTRACT

VLSI (Very Large Scale Integration) is the process of creating an integrated circuit by combining thousands of transistors into a single chip. This project describes the architecture of an arithmetic serial divider. Processors play a very crucial role in every digital system. The divider circuit increases the performance, accuracy and functionality of a processor. It consists of both combinational and sequential components. The major block of this consists of arithmetic logic units where arithmetic divider modules are frequently required for digital signal and image processing applications. Adders and multipliers are mostly used as building blocks for implementing the divider block. In order to increase the accuracy, functionality and performance of processor designers are working on increase the efficiency of dividers. In previous architecture of serial divider was done using cadence 90nm technology. But in this project, the dividers designed using 130 nm, 32 nm in HSPICE and cosmos Scope. The average power, delay, fall time, rise time, and power delay product will be determined.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION OF ARITHMETIC SERIAL DIVIDER:

The division operations in a system requiring a processor can be performed by approaching through a software environment or by using hardware based approach. Serial divider designed based on repeated one's compliment binary subtraction algorithm. It consists of several combinational and sequential components such as, 4 bit ripple carry adder, 2:1 multiplexers, D flip flops, 4 bit synchronous up counter. Serial divider plays a very important role in many digital systems such as calculators, microprocessor, digital filters, and digital signal processor. SOC designers have to focus on the design of these dividers to increase the performance, accuracy and functionality of the processors.

Division operation consumes more time when compared to addition, subtraction or multiplication as surveyed from the people who work in the area of architecture designing and implementation of processors.

1.2 INTRODUCTION OF HIGH SPEED BINARY DIVIDER:

The binary divider is one of the most complicated arithmetic circuits due to the numerous subtractors and registers for managing the parallel dividend inputs. In many applications, however, the data is serially transferred to reduce the interconnection overheads. Before activating the division, in the conventional parallel-in/parallel-out divider architecture, all the bits of dividend are received first, requiring a large size of buffers. Targeting the serial data interfaces, present in this project an area-efficient serial-in/serial-out binary divider based on the linear feedback shift register (LFSR). As the proposed architecture splits the division operation into several steps, in addition, the critical delay is greatly reduced.

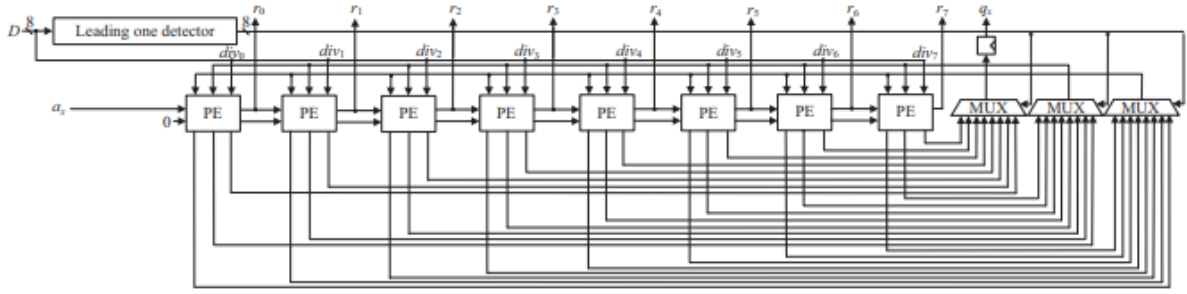


Figure1.1 8 Bit Binary divider

Implement two different binary dividers the parallel structure and the proposed serial one. Both architectures are equally synthesized in 130nm CMOS process compared to the conventional architecture. It is noticeable that the proposed divider always enhances the area costs as well as the critical delay. For the case of 32-bit division, for example, the proposed divider reduces the silicon area and the critical delay by 29 and 2.6 times.

1.3 INTRODUCTION OF FLOATING POINT DIVIDER BASED ON GOLDSCHMIT'S ALGORITHM:

Goldschmidt's single flux quantum (SFQ) floating-point divider that is suitable for the implementation using the bit-serial pipelined SFQ circuit. Thus design the bit-serial SFQ divider that outputs the 11-bit quotient. The simulation results show correct operation at the frequency of 50-GHz and bias margin of 80%–125%. This project estimated dependence of latency and the number of Josephson junctions on accuracy of outputs. According to the estimation, double-precision SFQ divider can be designed using 27 000 Josephson junctions, which can be implemented on one chip using the current SFQ circuit fabrication technology because of the small circuit area and multiplier-based hardware architecture. A Josephson junction is made by sandwiching a thin layer of a non superconducting material between two layers of superconducting materials.

There are two major hardware architecture approaches to implement the divider, subtractive and multiplicative approaches. The subtractive approach, which is similar to the manual division calculation, uses subtraction and shift operations to calculate quotient. The calculation time of the subtractive method is relatively slow because the subtraction and shift sequence has to be repeated

many times, at least the bit-length of the dividend. Owing to simplicity of the calculation and implementation, the subtractive approach has been widely used in commercial microprocessors. The multiplicative approach uses multiplication to calculate the quotient on the basis of mathematical algorithm. In this approach, the input dividend converges to the quotient quadratically by iterating multiplication. The multiplicative approach also has been implemented in various microprocessors such as the IBM RS/6000 and AMD K7 processor. Because the multiplier in the divider based on the multiplicative approach can be also used as the floating-point multiplier, the GPU, which has to perform both multiplication and division, can be implemented efficiently.

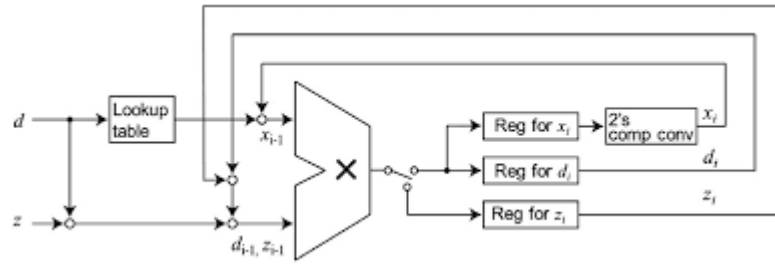


Figure1.2 Bit-serial Goldschmidt's SFQ divider

1.4 INTRODUCTION OF DIVIDER WITH QUOTIENT WITH FRACTIONS:

A new scalable architecture for Paravartya division have been proposed in which 8 partial quotient terms are generated parallelly in each stage and produces a quotient that is accurate up to one decimal place. A 16-bit by 16-bit divider based on this architecture is found to be 4.5ns faster than the conventional serial implementation of Paravartya sutra. It is also found to have 62 percent reduction in delay when compared with the existing dividers like SRT, Newton-Raphson and Nikhilam dividers that produces quotient and remainder.

1.5 INTRODUCTION OF FREQUENCY DIVIDER:

With the emerging of millimeter-wave frequency applications such as wireless personal area networks and image sensing, high-performance millimeter-wave phase locked loops (PLL) are highly demanded. The injection locked frequency divider (ILFD) with the high-division ratio is a promising solution for the

first frequency divider of a millimeter-wave PLL because of the merits of high-operation frequency and low-power consumption.

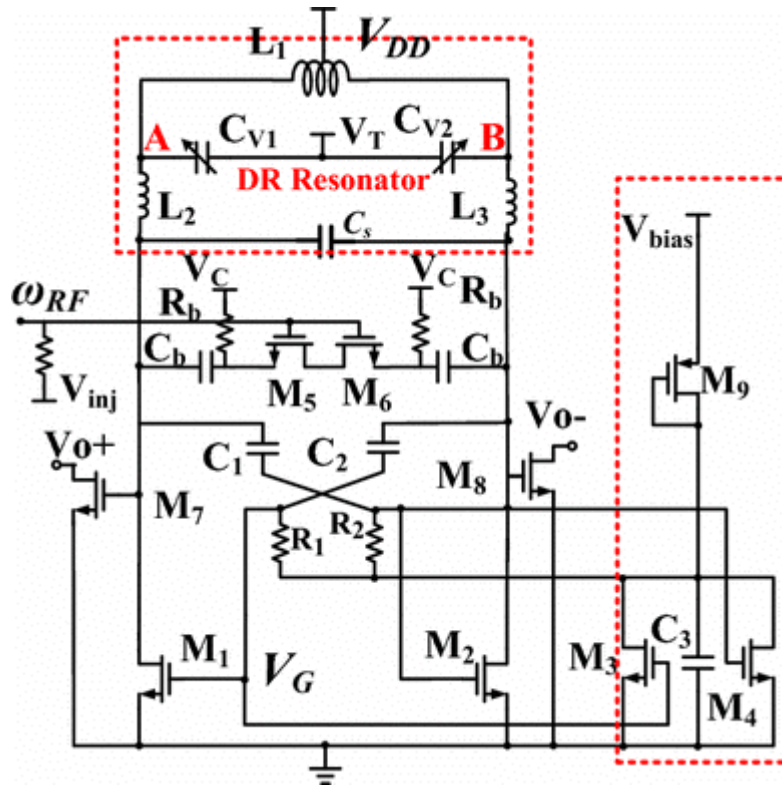


Figure 1.3 Divider by 4 ILFD

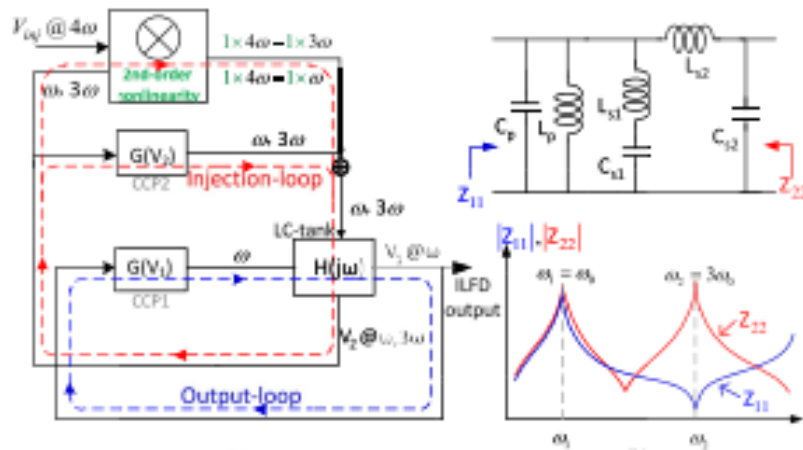


Figure 1.4 (a) Block diagram of the divide-by-4 ILFD

(b) Half LC-tank network and impedance plots

CHAPTER 2

LITERATURE SURVEY AND OBJECTIVES

2.1 LITERATURE SURVEY:

Mishra et.al.,(2017) determines that processors play a very crucial role in every digital systems. The major blocks include the arithmetic logic units where arithmetic divider modules are frequently required for digital signal and image processing applications. SOC designers have to focus on the design of these dividers to increase the performance, accuracy and functionality of the processors. The division operation completes after several clock cycles which is more as compared to other modules in the arithmetic logic unit. This project describes the architecture of an arithmetic serial divider. The divider circuit is designed using an adder/subtractor cell and non-restoring algorithm is used to evaluate the result. CADENCE 90nm technology library is used for designing the architecture of the divider module. For image and computer vision applications thus the arithmetic divider is the primary block in VLSI design of the architecture. The transistor level is implemented in CADENCE environment. Non-restoring type division is used here. The adder/subtractor cell is the basic building block of the architecture. The results are obtained for many division examples such as $11/23$, $-12/15$ and $11/16$ and are illustrated in this project. The answer for $-12/15$ presented here was determined to be correct as per the given example. The quotient values are $Q=q_0q_1q_2q_3q_4q_5q_6q_7q_8=100110011$ and remainder value, $R=000011=3d$. Now 2's complement of $Q = 11001101 = -205$. Thus $(2^8) \cdot -12 = (-205) \cdot 15 + 3$ is proved correct. After sign correction $Q = -205 + 1 = -204$ and $R = 3 - 15 = -12$. Hence $(2^8) \cdot -12 = (-204) \cdot 15 + (-12)$ is proved correct. The power dissipation for the divider was determined to be 0.875 mW.

Vikasini et.al.,(2021) determines that high Speed DSP applications are influenced by the efficiency of the arithmetic modules used. Division is a bulky and computational complex operation with high latency than the other arithmetic operations. Vedic Mathematics provides a better method of computation as they are based on the principles on which the human mind works. In this project, a new scalable architecture for Paravartya division have been proposed in which 8 partial quotient terms are generated with that in each stage and produces a quotient that

is accurate up to one decimal place. A 16-bit by 16-bit divider based on this architecture is found to be 4.5ns faster than the conventional serial implementation of Paravartya sutra. It is also found to have 62 percent reduction in delay when compared with the existing dividers like SRT, Newton-Raphson and Nikhilam dividers that produces quotient and remainder. A scalable architecture for Paravartya sutra have been designed and implemented for 8-bit and 16-bit division which produces a quotient that is accurate up to 1 decimal place. The 16-bit proposed divider is found to be 4.5 ns faster than the conventional implementation of Paravartya sutra. It is also found to have at least 62 % improvement in delay when compared with the Newton-Raphson, SRT and Nikhilam dividers. The increase in the number of slice LUTs is justified by the advantages provided by the proposed divider. The future scope of this research work would be to build higher order dividers using this architecture and also to reduce the LUT utilization. ASIC implementation can also be done in order to see the actual speedup offered by the proposed divider.

Ibrahim et.al.,(2020) determines a new unified and scalable digit-serial systolic array structure to implement the unified Stein's multiplication and division algorithm. The proposed structure is flexible enough to help the designer select the required number of processing elements and manage the latency of the multiplication/division operations. Thus, the proposed design can realize the required time performance with minimum space complexity. The implementation results of the proposed design and the previously reported digit-serial competitor designs display that the proposed scalable architecture has better performance for 32-bit embedded cryptographic processors that need reasonable performance with a small footprint. In this brief, this module exhibited a new scalable and unified digit-serial systolic array architecture to implement division and multiplication operations over $GF(2^m)$. The proposed structure has the advantage of selecting the required number of PEs and managing the latency. This makes the designer have enough flexibility to realize the required time performance with a minimum space complexity. The implementation results display that the proposed design has better performance for bus sizes ≥ 28 compared to the other competitor designs. This makes the proposed design more suitable for 32-bit embedded cryptographic processors that need reasonable performance with a small footprint.

Yoshikawa et.al.,(2019) determines that Goldschmidt's single flux quantum (SFQ) floating-point divider that is suitable for the implementation using the bit-serial pipelined SFQ circuit. Project used to design the bit-serial SFQ divider that outputs the 11-bit quotient. The simulation results show correct operation at the frequency of 50-GHz and bias margin of 80%–125%. This module estimated dependence of latency and the number of Josephson junctions on accuracy of outputs. According to the estimation, double-precision SFQ divider can be designed using 27 000 Josephson junctions, which can be implemented on one chip using the current SFQ circuit fabrication technology. Because of the small circuit area and multiplier-based hardware architecture, the investigated divider can be applied to build an SFQ graphical processing unit. They investigated the floating-point bit-serial divider for SFQ logic based on Goldschmidt's division algorithm. They designed the 4-bit SFQ divider composed of one pipelined multiplier using the AIST 10 kA/cm² Nb advanced process. When the bit-length of the dividend and divisor are 4, accuracy of 2–11 can be obtained by iterating multiplication by three cycles. Estimated latency and the number of JJs of the designed 4-bit SFQ divider are 87 clocks and 8091, respectively. According to estimation based on the circuit design of the 4-bit divider, the double-precision divider can be implemented with 26,518 JJs by following this architecture, which can be implemented on one chip using the current SFQ circuit fabrication technology.

Park, et.al.,(2016) determines a low-complexity binary divider for high-speed serial interfaces. In contrast that the previous parallel dividers require a large amount of hardware costs, the divider achieves a low-complexity division by targeting the serial interface that is widely used for the recent digital communications. By modifying the linear feedback shift register (LFSR) architecture for polynomial division, the high-speed processing element is newly introduced to handle the serialized dividend input. As a result, the serialized architecture reduced the area-time complexity by 75 times compared to the previous slow parallel divider. In digital systems, the binary divider is one of the most complicated arithmetic circuits due to the numerous subtractors and registers for managing the parallel dividend inputs. Before activating the division, in the conventional parallel-in/parallel-out divider architecture, all the bits of dividend are

received first, requiring a large size of buffers. Consider a serial data communication. Note that there is only a single input port for the dividend, which is denoted as ax , so that all the bits of n -bit dividend are serially issued to the divider in descending order, Targeting the serial data interfaces, Module present in this project an area-efficient serial-in/serial-out binary divider based on the linear feedback shift register (LFSR). In this project, they have presented a cost-effective binary divider, which targets the high-speed serial interfaces. Based on the proposed serialized PE-based architecture, the divider relaxes both the hardware complexity and the critical delay compared to the conventional parallel structures.

IC design can be divided into two main broad categories of Analog and Digital. The analog block includes receiver (RX) and transmitter (TX) for data transmission which works on different frequency ranges. The digital block consists of FSM's which has an operating frequency in the range of Mega Hz. It is not easy to design a PLL for each block to provide particular frequency to work. This project reports a Design of multi-modulus Clock divider which will take the PLL output and give the divided output with respect to the division ratio. The design is for 9GHz wide band Programmable multi-modulus clock divider using latch-based static CMOS logic. Clock divider circuit gives a wide range of frequencies from 2-255. The divider is designed using 45nm CMOS technology at supply voltage of 1V. The design is implemented in Cadence Virtuoso and the results are reported. In this project, a multi-modulus clock divider for a high speed application is proposed along with a new architecture of positive edge triggered D-flip-flop based MOD-256 counter. The clock divider structure is implemented for 8-bit, which provides wide range of frequency division ratio from 2-255. Simulation results shows that the divider has an operating frequency of 9G Hz and 1.567mW of power dissipation using the 45nm CMOS technology.

The electronics world is very well described in two distinct but dependent interdisciplinary areas, namely hardware and software. An algorithm is a systematic arrangement that helps develop a sophisticated electronic system, including hardware and software aspects. Addition, subtraction, multiplication, and division are critical elements of arithmetic implementation in the electronic system, but fewer efforts have been made to implement division than other arithmetic operations, even though the number of transistors on a chip is increasing beyond

the Moore's law prediction. Technological upgrades are leading to a new paradigm of applications, where the performance of a division circuit or block is a vital and critical feature of a successful system. The lexicon of algorithms used in the implementation of the division operation in electronics systems is discussed in detail in the present article, which indicates the mathematical formulation, criticality, conversion pattern, hardware requirements, and logic used for conversion. The study indicated the possibility of improving the presently available algorithms or creating a new algorithm to enhance practical implementation. Based on the review, it is found out that the digit recurrence division algorithm is most likely preferred for implementation in different applications considering its ease in conversion logic and considerable area and latency constraints. Area and latency constraints are very important for embedded systems and ASIC design, where fast action in a considerably less area is of great importance. They put efforts into developing a new digit recurrence algorithm, which has simple conversion logic and benefits in the area and variable conversion time constraints of the divider circuit.

Yamada et.al.,(2021) determines that a design method for wideband resistive voltage dividers (WRVDs), working in the range of power frequencies to a few megahertz, with serial-parallel construction. It introduces an extended concept of the Hamon method into the WRVDs, not in a conventional way like balancing a bridge, but in a new way that involves impedance matching with optimal solution methods. With this method, average resistance matching and stray capacitance matching are simultaneously realized by an optimal arrangement of two element resistor groups as the input and output resistors. The surrounding stray capacitances between the resistors and chassis are also considered. The performance has been confirmed to improve by about 50 times, compared with that without the method. The stray capacitances contributing to the phase error have been divided into two categories. One is around its input resistor, which can be quasi-uniform through applying an electrostatic shielding. The shielding comprises of two parts and the performance has been confirmed by a simulation, but the effect of some field distortions needs further investigation. Finally, the voltage ratio error given the resistance and capacitance matching errors has been evaluated with the equation derived from our study. In conclusion, the WRVD

design method based on the matching method has been confirmed to give our WRVD a better performance by about 50 times. However, the result has not considered the effects of the stray impedances of sockets and buffer amplifiers connected at the output, as well as the effect of the field distortions by the electrostatic shield.

Shi et.al.,(2018) determines that the design and self calibration in phase angle errors of the RVD with serial-parallel connection and IVD with cascade structure. Resistive voltage dividers (RVDs) and inductive voltage dividers (IVDs) are two frequently-used voltage dividers (VDs) in the ac power standard system and several VDs have been designed and calibrated by national metrology. For ac power measurement under low power factor, the phase angle errors of VDs are a main error source and need to be calibrated accurately, especially at high frequencies. They have compared the self-calibration results between the two VDs with ratio of 64:1 at 32 V. However, the VDs are usually used at high voltages up to hundreds of volts in the ac power standard. In this project they have presented the VDs with high ratios and verified the accuracy of self-calibration results. The self-calibration results have been verified with a comparison experiment at frequencies up to 100 kHz. The voltage dependence in phase angle errors of the two voltage dividers has also been calibrated from 64 V to 300 V and the measurement results are presented. Resistive voltage divider, inductive voltage divider, self-calibration, phase angle errors, verification. The structure and self-calibration in phase angle errors of 257:1 RVD and 256:1 IVD have been described. The accuracy of the self-calibration results has also been verified to be reliable at frequencies up to 100 kHz with a comparison experiment. The voltage dependence of the two VDs has been determined from 64 V to 300 V at frequencies up to 100 kHz.

Gupta et.al.,(2020) determines that a universal asynchronous receiver and transmitter (UART) are described, which is basically a serial data transmission protocol used in digital circuit applications. UART receiver has a baud rate generator, negative edge detector, parity checker, receiver finite state machine (FSM) and serial in parallel out (SIPO) register. The baud rate generator of both transmitter and receiver is the same, so the baud rate of transmitter/receiver is the same. Baud rate generator is the same as the frequency divider circuit. The data

frame of the UART transmitter is 1 start bit, 8 transmits data bits, 1 parity bit and 1 stop bit. The baud rate of the transmitter and receiver is 4 Mbps using the system clock of 64 MHz's. implementation of high-speed Universal Asynchronous Receiver and Transmitter (UART) is successfully and verified using Verilog hardware descriptive language (HDL language).The high-speed serial data transfer at 4 Mbps rate with a clock frequency of 64 Mbps. UART is used for serial data transfer and the speed of UART is depending upon the transmission media of transmitter and receiver. The baud rate of the UART transmitter and receiver is the same. The verification of UART is verified using the simulation waveform of transmitter and receiver and the synthesis result is verified at the FPGA Zed board.

2.2 LITERATURE SUMMARY:

Arithmetic divider modules are frequently required for digital signal and image processing applications. Dividers are used to increase the performance, accuracy and functionality of the processors. The adder/ subtractor cell is the basic building block of the architecture.

2.3 PROBLEM DEFINITION:

Analyze the performance of the high speed serial divider for VLSI applications.

2.4 OBJECTIVES OF THE PROJECT:

In terms of increasing the efficiency and speed of the serial divider for digital applications this project is developed. In order to increase the speed the division algorithms and many power techniques will be applied in all circuits. Identify the pros and cons in existing serial divider.

CHAPTER 3

EXISTING METHODOLOGY

3.1 DIVISION ALGORITHMS AND TECHNIQUES USED IN SERIAL DIVIDER:

Different existing algorithms are used for design of divider blocks. Adders and multipliers are mostly used as the building blocks for implementing the divider block. Basically there are two categories of division algorithm i.e. a) subtraction followed by shifting operation b) multiplication operation. Decimal division uses the method which they do normally. The usual pencil and project method and includes the first category. In this method A and B are the binary dividend and divisor respectively. A and B have values are either 0 or 1. The quotient can be of any base and is generally a power of 2. Here the subtraction and shifting operation is iterated for certain steps and thus called digit recurrence division algorithms.

In this digit recurrence algorithm, one bit of the quotient is calculated for a single iteration. Partial remainder which is obtained by shifting is compared with multiples of the divisor for determining quotient bit. Adder/subtractor modules are used in the control unit and that makes easy implementation of the algorithm with high level of accuracy. But the disadvantage of this algorithm is, it has more timing complexity when compared with multiplicative division algorithm. Digit recurrence algorithm is of three types like restoring, non-restoring and SRT. In base-2 restoring division algorithm, quotient bit q_i is taken from the set {0, 1}. In this algorithm Y is '1' when $2^{-1} - Y \geq 0$ else it is '0', here is the partial remainder and Y is divisor. For $Y=0$, Y is again added with. The algorithm undergoes an iteration of n -bit accuracy.

For the non-restoring algorithm, there is no back addition of the divisor with the partial remainder. The quotient bit Y belongs to the set {-1, 0, 1} in case of radix-2 SRT algorithm. If $2^{-1} < 0.5$, '-1' is selected, again if $-0.5 \leq 2^{-1} < 0.5$, '0' is selected and if $0.5 \leq 2^{-1}$, '1' is selected. But when $Y=0$, neither addition or subtraction operation is performed. SRT division is named so, as Sweeney, Robertson and Tocher had introduced this algorithm.

3.2 SERIAL DIVISION ALGORITHM:

Digit recurrence algorithm is the most common algorithm. This algorithm is again divided into SRT type, restoring and non restoring algorithm. The basic algorithm is digit recurrence, which is a non-restoring algorithm and is used to design a digital serial divider whereas recurrence algorithm mentioned above uses addition, subtraction and shifting operations iteratively to carry out the division process. Digital serial division architecture is designed using the non-restoring type of division technique. If "0100" has undergone one bit left shifting, then "1000" is the result which is two times of the shifted binary number. For non-restoring type of division algorithm twice of R_{i-1} (partial remainder) is determined using the above principle.

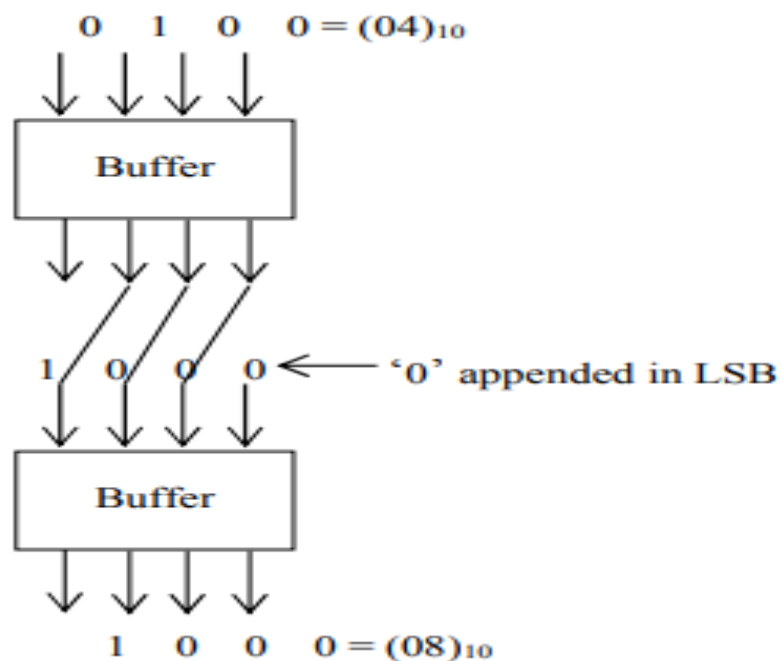


Figure 3.1 Blocks for retrieving twice of an n-bit number

The modules used an unit of adder and subtractor, registers and shift register. The type of adder (ripple carry adder (RCA) or carry look ahead adder (CLA)) to be included depends on the base of the number system. RCA is suitable for lower radices. CLA or carry select adder is preferred when the system has higher radices. The quotient determined in the previous step controls the

adder/subtractor cell to perform the addition or subtraction. The partial remainder R_{i-1} is shifted with the help of shift register to get $2R_{i-1}$.

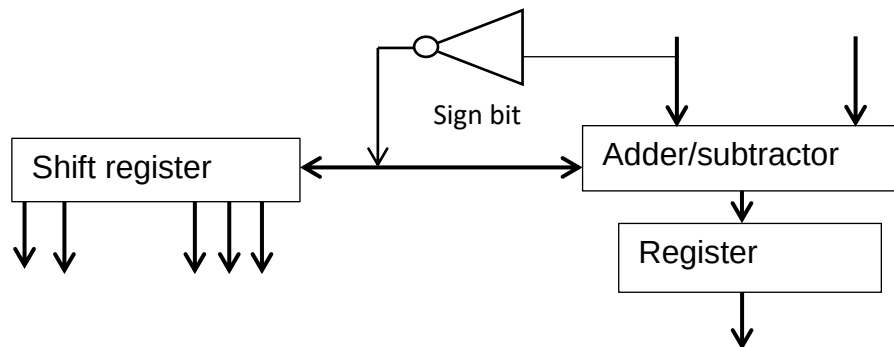


Figure 3.2 Architecture for non-restoring type divider

3.3 ARCHITECHTURE OF SERIAL DIVIDER:

The architecture for a serial division is shown in Fig.3.3. The logic for the block shown here is given in but in this project there is a modification done by the addition of an extra adder/subtractor unit at the beginning. This is done to obtain the value of initial remainder $R(0)=A$. Here the architecture shown is for a 6-bit divider which has controlled adder/subtractor unit that can be extended for 'n' bits.

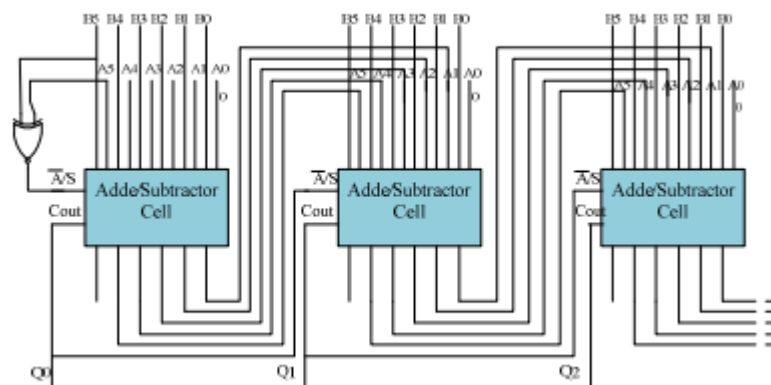


Figure 3.3 Serial divider architecture

There are six each full adders and XOR gates in the adder/subtractor block. A (dividend) and B (divisor) are the operands of the cell where A is the direct input and B is one of the input of XOR gate and the select bit $\bar{A}/S$ is the another input. The adder/subtractor cell is controlled by the select bit $\bar{A}/S$. Addition is performed when $\bar{A}/S$ is '0' whereas subtraction is performed if $\bar{A}/S$ is '1'. the

A bar/S bit has a connection with the output pin of XNOR gate with its two input pins connected to the MSB or sign bit of A and B. A bar/S is equal to 1 if both A and B are positive, resulting in subtraction operation in the 1st adder/subtractor block.

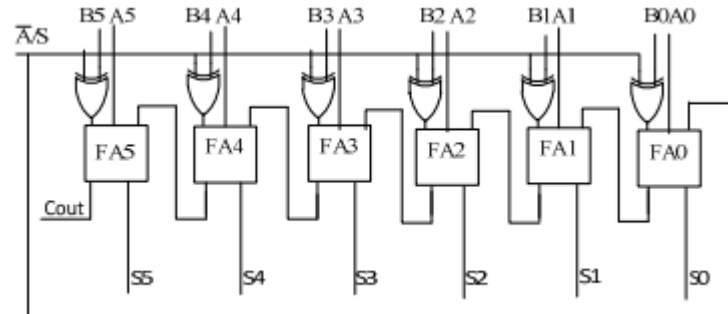


Figure 3.4 Adder/ subtractor unit

So subtraction operation is performed if the quotient bit is '1' whereas addition is performed if the quotient bit is '0'. Thus quotient is connected to A bar/S bit of adder/subtractor block of the preceding cell which is the carry out bit of the first unit. The carry output is then served to be the quotient bit in the computation because A bar/S bit of i th adder/subtractor block has a connection with quotient bit of $(i-1)$ th block. In the hardware connection, $R(0)$ which is the partial remainder of the 1st block is one bit left shifted. It also serves as one of the input bit to 2nd stage of adder/subtractor block and the LSB of the next block is appended with a '0'. The next partial remainder $R(1)$ is determined by the addition/subtraction of $2R(0)$ generated in the process with the divisor B. The quotient bit $Q(1)$ is the carry out bit of the cell. In the further stages of serial divider architecture the above connection is repeated. So for $-12/15$, $p=8$ and nine stages are used. The final value of quotient is calculated using a correction circuit for non-restoring division. But in this divider architecture correction circuit is not used for non-restoring division. In the next section, the architecture for the divider circuit implemented using cadence 90nm technology libraries is described and also the description for functional simulation of the circuit is stated.

3.4 IMPLEMENTATION:

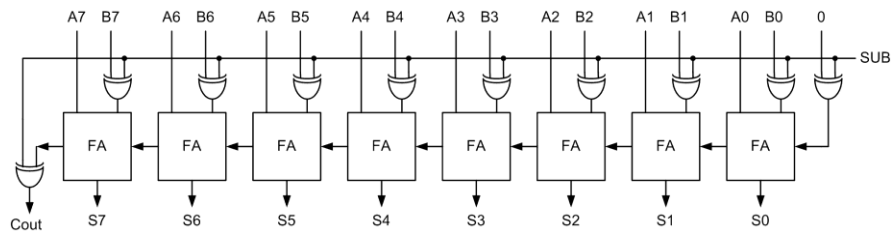


Figure 3.5 Adder Schematic diagram of adder /subtractor cell

For image and computer vision applications thus the arithmetic divider is the primary block in VLSI design of the architecture. The transistor level is implemented in CADENCE environment. Non-restoring type division is used here. The adder/subtractor cell is the basic building block of the architecture. The results are obtained for many division examples such as 11/23, -12/15 and 11/16 and are illustrated in this project. The answer for -12/15 presented here was determined to be correct as per the given example. The quotient values are $Q = q_0q_1q_2q_3q_4q_5q_6q_7q_8 = 100110011$ and remainder value, $R_8 = 000011 = 3d$. Now 2's complement of $Q = 11001101 = -205$. Thus $(2^8) \cdot -12 = (-205) \cdot 15 + 3$ is proved correct.

CHAPTER 4

PROPOSED SYSTEM

In order to improve efficiency, existing system serial divider will be analyzed using 130 nm, 32 nm CMOS technology. Further, serial divider code shift register will be modified and analyzed using 130 nm, 32 nm CMOS technology. In terms of power, speed, and power delay product. This out performs an efficient Serial divider shift register for high speed applications.

A full adder circuit is central to most digital circuits that perform addition or subtraction. It is so called because it adds together two binary digits plus a carry in digit to produce a sum and carry out digit. Full adder is written in CMOS technology MOSFET under 130nm. Figure 4.1 shows the existing CMOS technology Full adder which have high power, high delay and high PDP. In the below Full adder fourteen transistors are taken (seven PMOS transistors and seven NMOS transistors).

This Full adder is taken in the Serial divider circuit diagram to measure the power, delay, fall time, rise time and PDP. The serial divider circuit diagram has Full adder, XNOR and XOR. To measure the power, delay and PDP, first code have to write for each device in the Serial divider block diagram in HSPICE. Coming to the full adder, the code have written for each transistor as A=2, B=3, Cin=6. Stimulation is done in the HSPICE software.

After stimulation the power is nearly 0.00004944% which is high other than other full adder in 130 nm. And the delay is 12.991ps in MOSFET under 130nm. Finally, the product of power and delay will be the PDP (Power -Delay product).

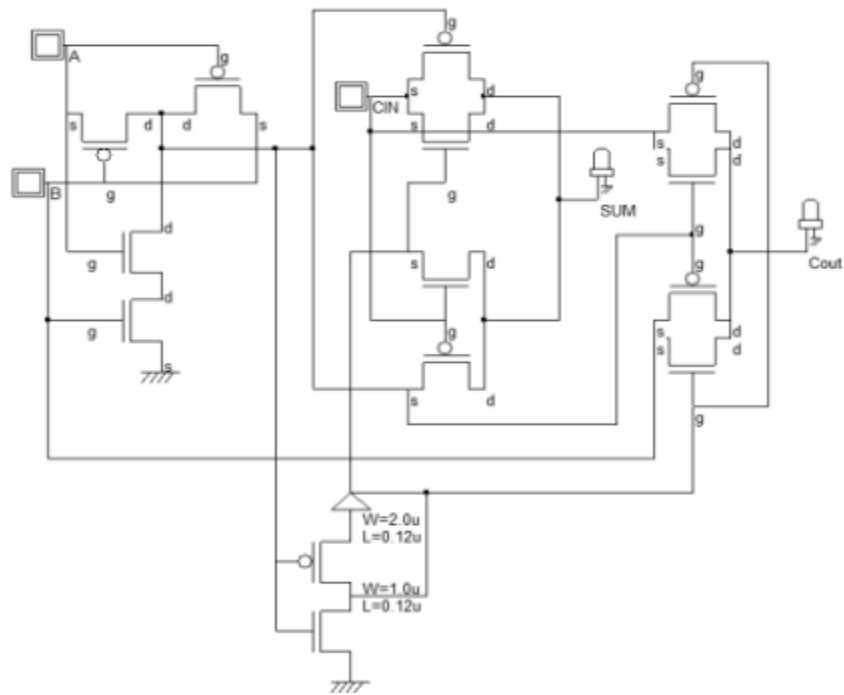


Figure 4.1 CMOS technology Full adder

4.1. MODIFIED FULL ADDER:

Capacitance of a diode is directly proportional to its size. This enhances its speed in turn.

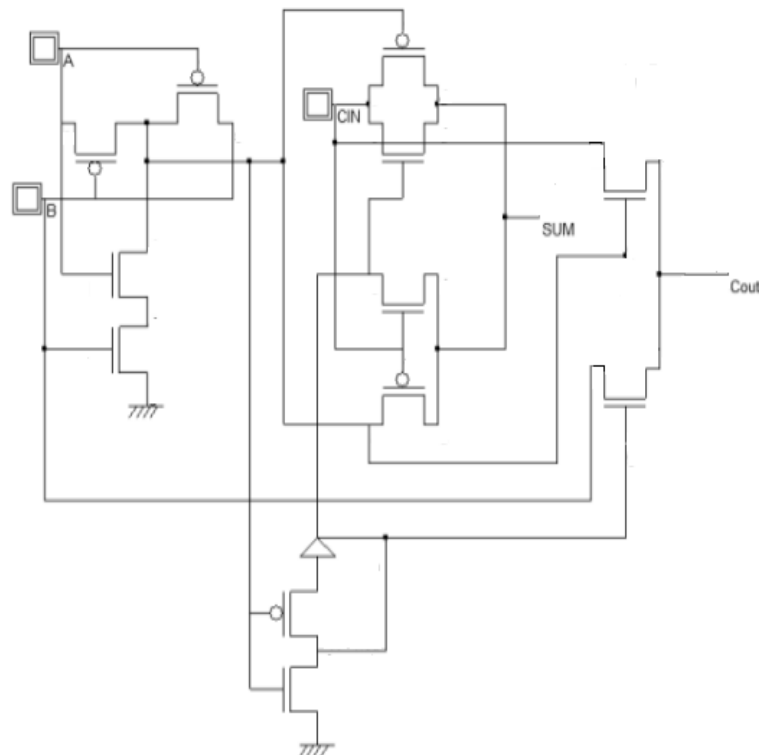


Figure 4.2 Modified full adder

The modified Full adder has twelve transistors (five PMOS transistor and seven NMOS transistor) which have low power, low delay, low PDP, high fall time and high rise time than existing full adder. The existing full adder is replaced the modified full adder from existing in serial divider circuit diagram to measure the power, delay, PDP, fall time and rise time. After replacement, Code was written and stimulation is done in HSPICE software. The power, delay, fall time, rise time and PDP will reduce in MOSFET under 32nm, 130nm.

The power is reduced to 0.00145% and 0.0000242% in MOSFET under 32nm, 130nm

4.2 HSPICE SOFTWARE:

Hewlett Simulation Program with Integrated Circuit is the full name of the HPICE. Unlike board-level designs made up of individual components, integrated circuits cannot be bread boarded before being manufactured. Furthermore, due to the high cost of photolithographic masks and other manufacturing requirements, it is critical to design the circuit to be as close to perfect as possible before it is designed. Until committing to producing an integrated circuit, the industry-standard method of verifying circuit operation at the transistor level is to simulate the circuit with HSPICE.

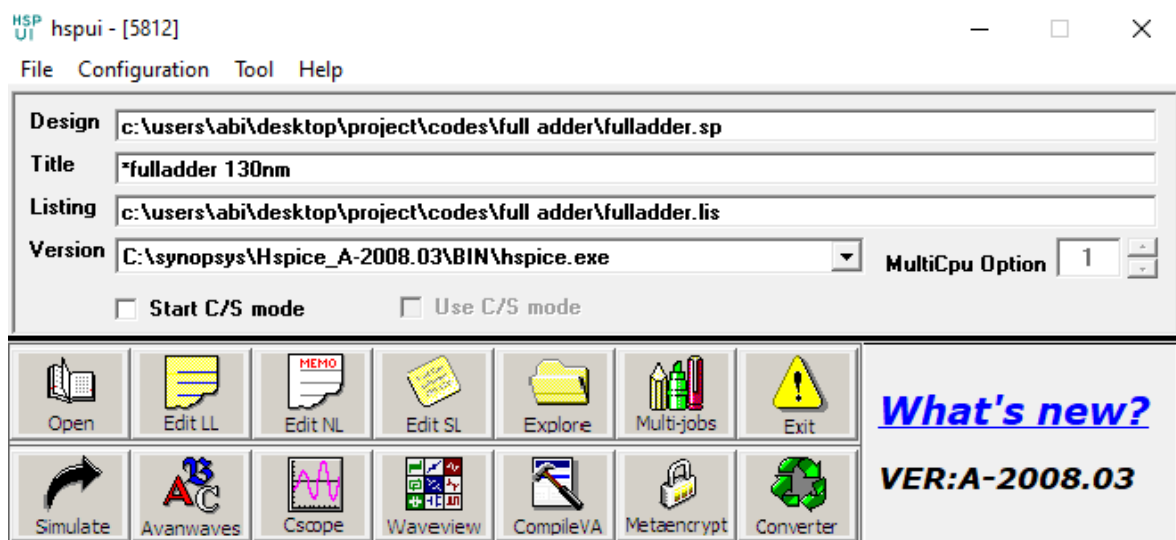


Figure 4.3 HSPICE software

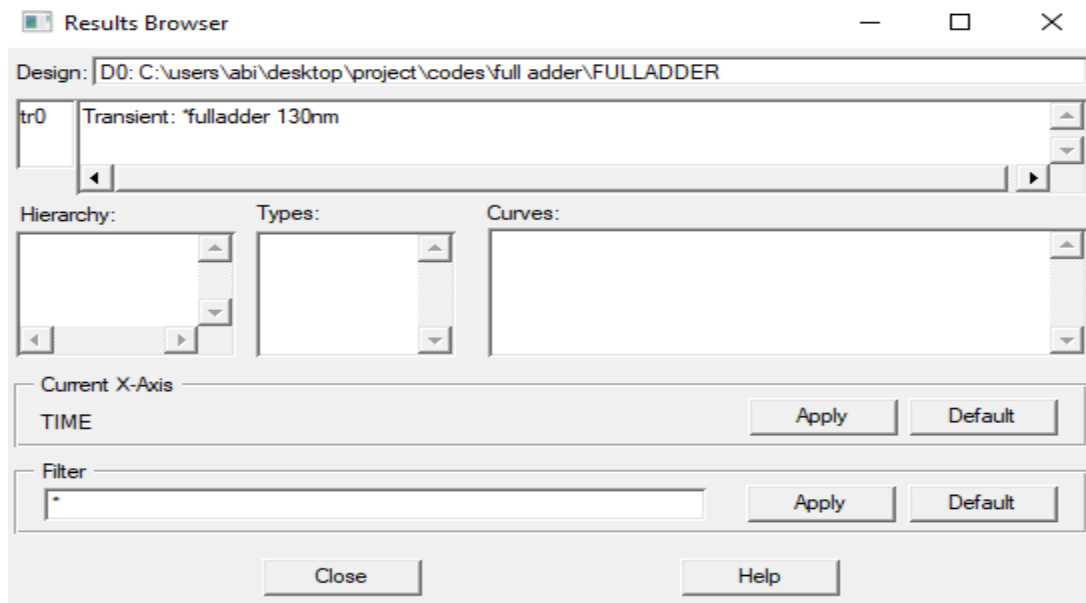


Figure 4.4 Results browser

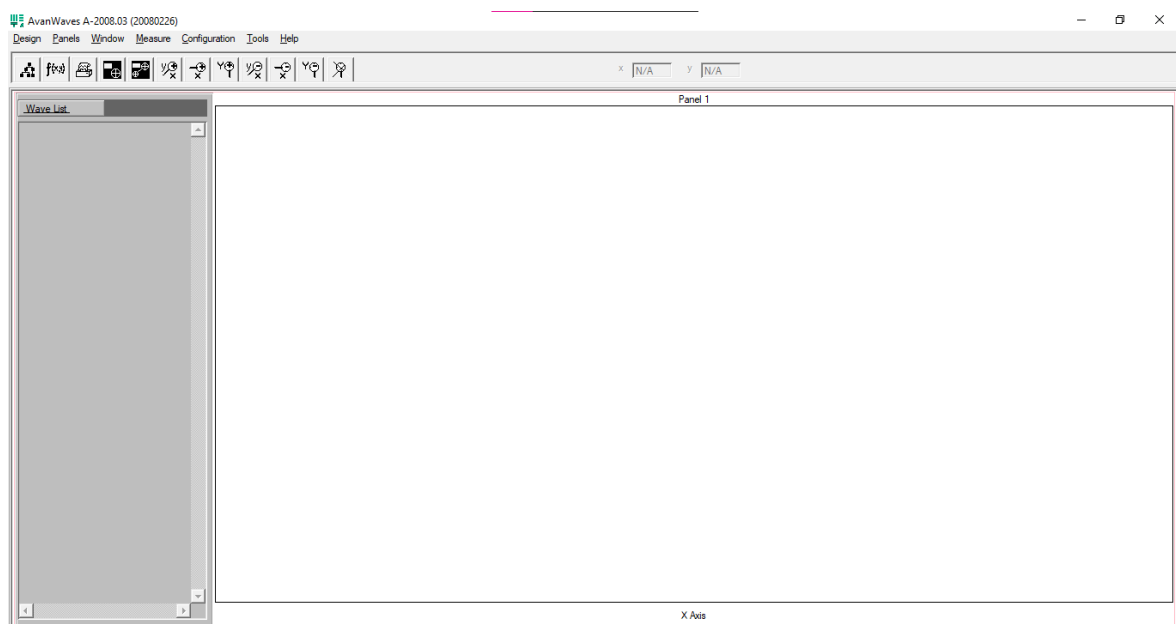


Figure 4.5 Simulated screen

Figure 4.4 represent the results browser where the nodes are chose. This is make sure that how many graphs going to display in simulated screen.

Figure 4.5 represent the simulated screen where the selected were shown. By using this graph were verified for further process.

4.3. COSMOSSCOPE:

CosmosScope is an software which is used to calculate the delay, rise time and fall time.

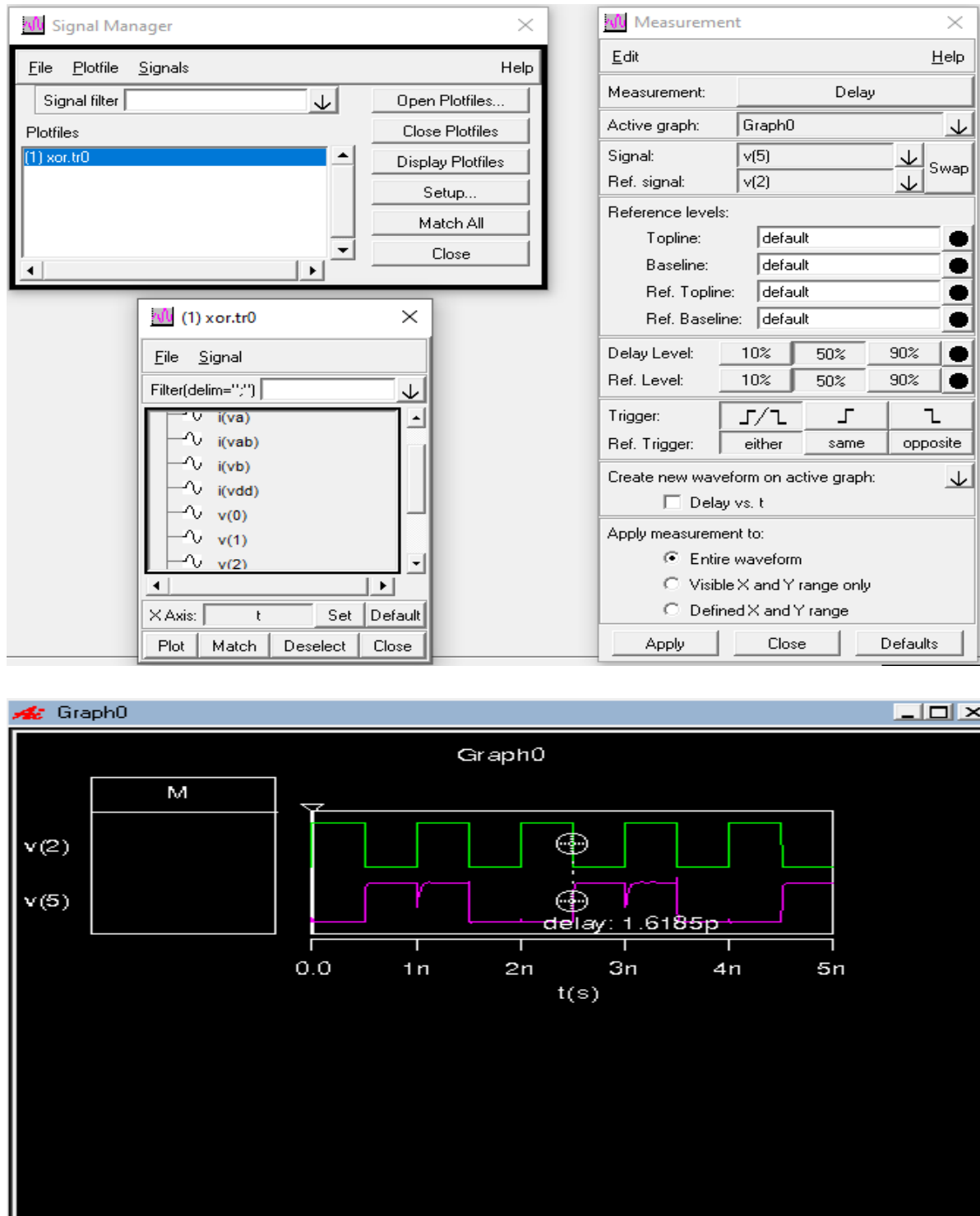


Figure 4.6 CosmosScope software

This is the figures of cosmos scope software, which have the signal manager, waveform selector, measurements and graph screen. By using measurement, the parameters were selected to measure the values in the waveform. After select the parameters, the waveforms should select to calculate the delay, rise time, fall time.

4.4. PARAMETERS:

4.4.1. POWER:

Electric power is the rate at which electrical energy is transmitted by an Electric circuit per unit of time .it is he pace at which work is completed. Electric power is the rate at which electrical energy is transmitted by an electric circuit per unit time in terms of an electric circuit.

The unit of the Electric power = Watt

$$\text{Power} = V \cdot I (W)$$

$$I = Q/t$$

Where

W = power in watts

V = Potential in volts

I = Current in amps

Q=charge in coulombs

T = time in seconds

4.4.2 DELAY:

The time it take for a signal to reach its destination is referred as delay. The time it takes for the consequence of a shift in input to be noticeable at the output is known as the delay of a logic gate.

4.4.3 POWER DELAY PRODUCT:

Power Delay Product is the product of the power and delay

$$\text{PDP} = \text{Power} * \text{Delay}$$

4.4.4 FALL TIME:

The fall time is calculated by finding a crossing with the middle level of the waveform. Looking forward from this point, the time when the waveform falls to the lower level is found. Looking backward, the time when the waveform rises to the upper level is also found. You set the upper and lower levels as 0-100%, 10-90%, or 20-80% of the Topline/Baseline levels

4.4.5 RISE TIME:

Displays the rise time between default or selected upper and lower levels of a waveform. You can also compute the rise time based on manually-set upper/lower levels as described in the topic titled "Manually Set a Custom Topline/Baseline".

CHAPTER 5

RESULTS AND DISCUSSIONS

The existing and proposed architecture are simulated by using Avan waves simulator. Output of the existing radix 4 booth multipliers and proposed radix 4 booth multipliers are analyzed from the results and it is concluded that the proposed architecture reduces the power consumption compared with the existing system. The synthesis is done using HSPICE.

These are the output waveforms of XOR, XNOR, full adder and serial adder circuit diagram in MOSFET under 32nm and 130nm.

5.1 SIMULATION RESULTS IN MOSFET UNDER 130 nm:

The below figures are the output waveforms of XOR, XNOR, full adder and serial adder circuit diagram in MOSFET under 130nm. In every waveform x axis will be time in secs and y axis will be voltages.

5.1.1 SIMULATION RESULT OF XOR:

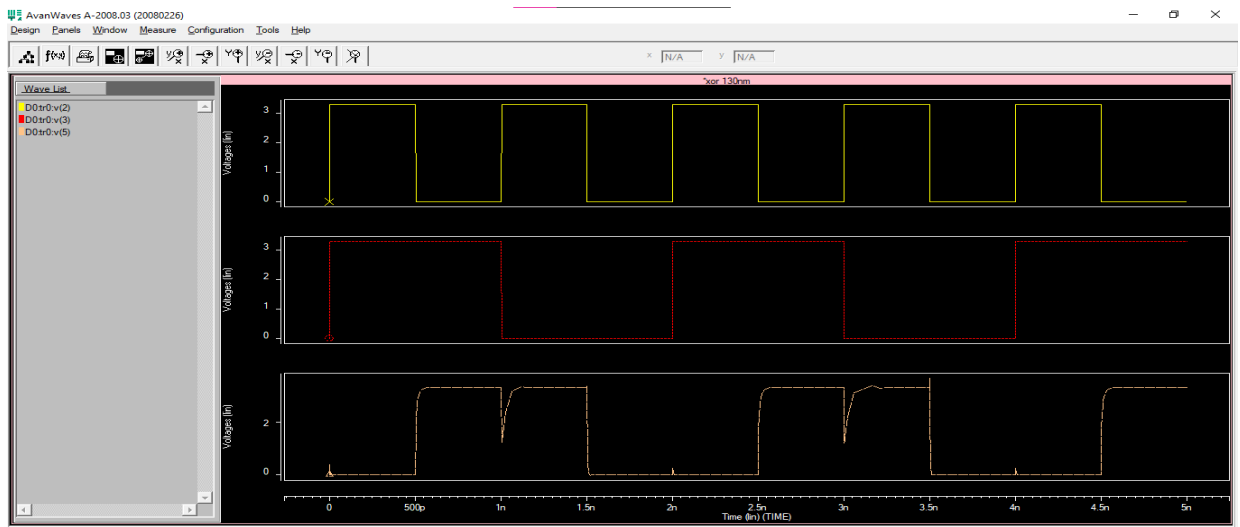


Figure 5.1.Simulation result of XOR under 130 nm

Figure 5.1 represent the simulation result of XOR. This graph taken from the avan waves which is plotted to confirm the output of the source code of XOR gate. From XOR gate, the measurements were taken. The consumed power is 1.599×10^{-5} watt, delay is 1.6185 ps.

5.1.2 SIMULATION RESULT OF XNOR:

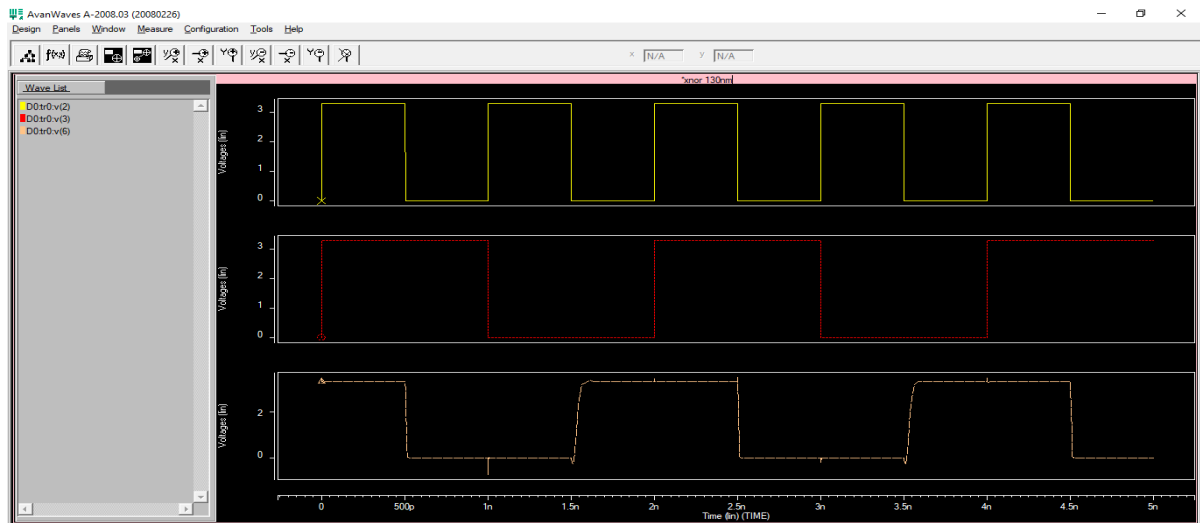


Figure 5.2.Simulation result of XNOR under 130 nm

Figure 5.2 represent the simulation result of XNOR. This graph taken from the avan waves which is plotted to confirm the output of the source code of XNOR gate. From XNOR gate, the measurements were taken. The consumed power is 1.142×10^{-5} watt, delay is 5.9328 ps.

5.1.3 SIMULATION RESULT OF FULL ADDER:

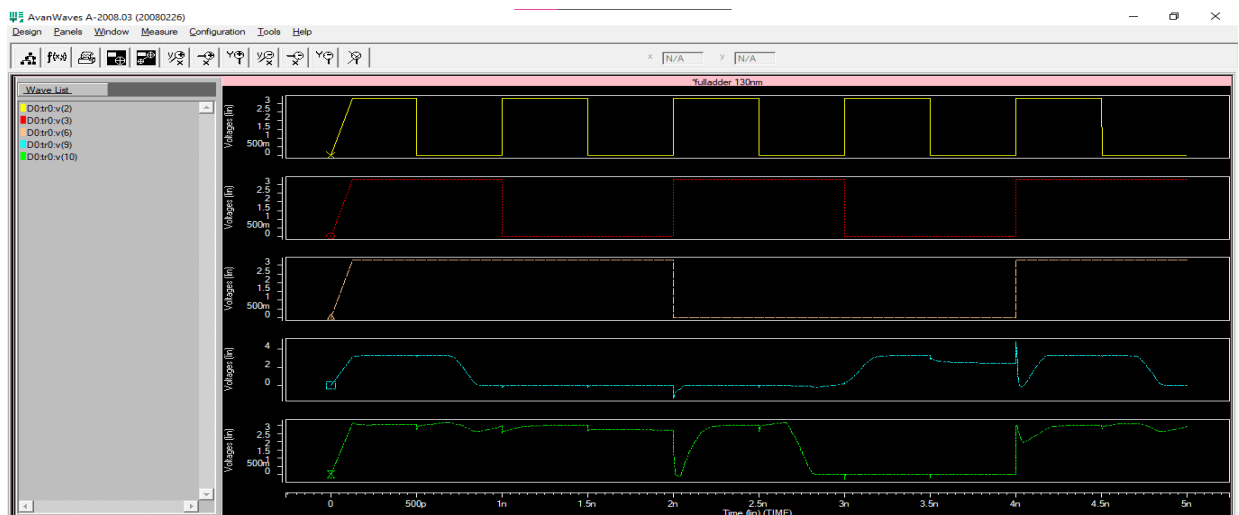


Figure 5.3.Simulation result of full adder under 130 nm

Figure 5.3 represent the simulation result of full adder. This graph taken from the avan waves which is plotted to confirm the output of the source code of

full adder gate. From full adder gate, the measurements were taken. The consumed power is 25.10×10^{-5} watt, delay is 12.991 ps.

5.1.4 SIMULATION RESULT OF ADDER UNIT:

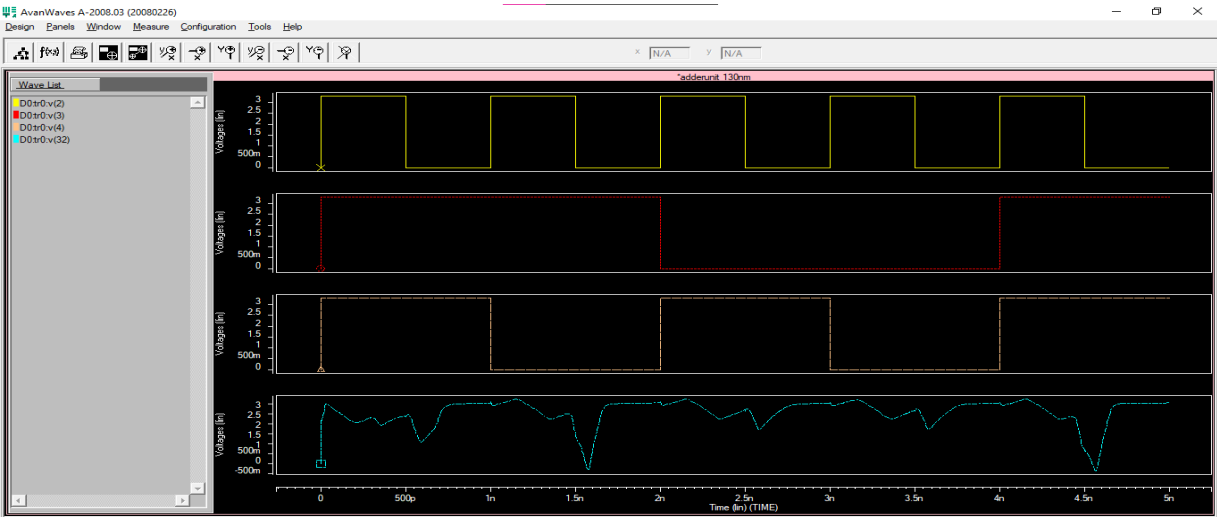


Figure 5.4.Simulation result of adder unit under 130 nm

Figure 5.4 represent the simulation result of adder unit. This graph taken from the avan waves which is plotted to confirm the output of the source code of adder unit. From adder unit, the measurements were taken. The consumed power is 83.37×10^{-5} watt, delay is 105.96 ps.

5.1.5 SIMULATION RESULT OF SERIAL DIVIDER:

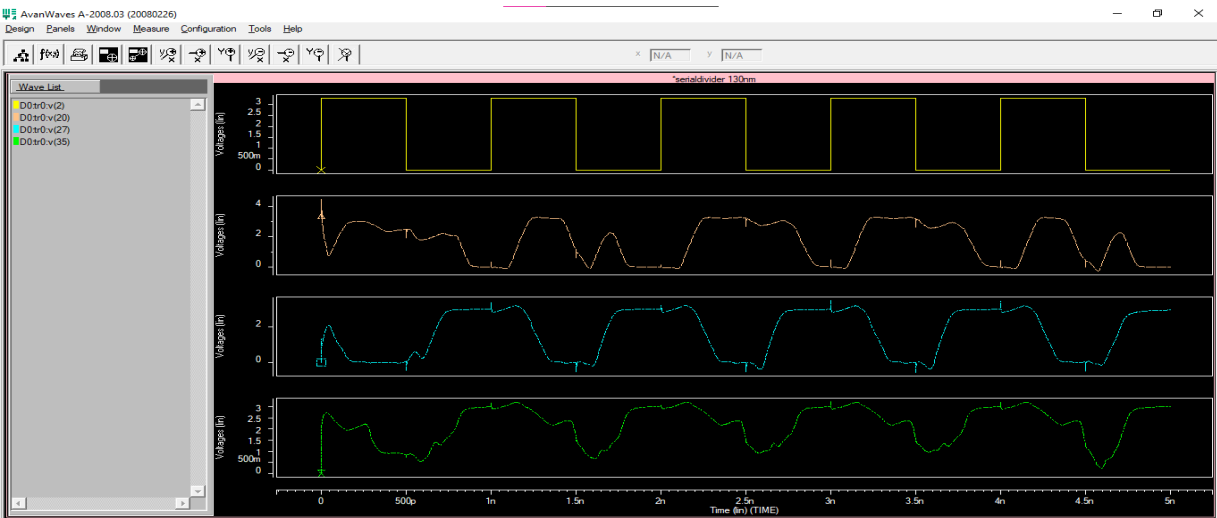


Figure 5.5.Simulation result of serial divider under 130nm

Figure 5.5 represent the simulation result of serial divider. This graph taken from the avan waves which is plotted to confirm the output of the source code of serial divider. From serial divider, the measurements were taken. The consumed power is 260.5×10^{-5} watt, delay is 179.19 ps.

5.2. SIMULATION RESULTS IN MOSFET UNDER 32 nm:

The below figures are the output waveforms of XOR, XNOR, full adder and serial adder circuit diagram in MOSFET under 32 nm. In every waveform x axis will be time in sec and y axis will be voltages.

5.2.1 SIMULATION RESULT OF XOR:

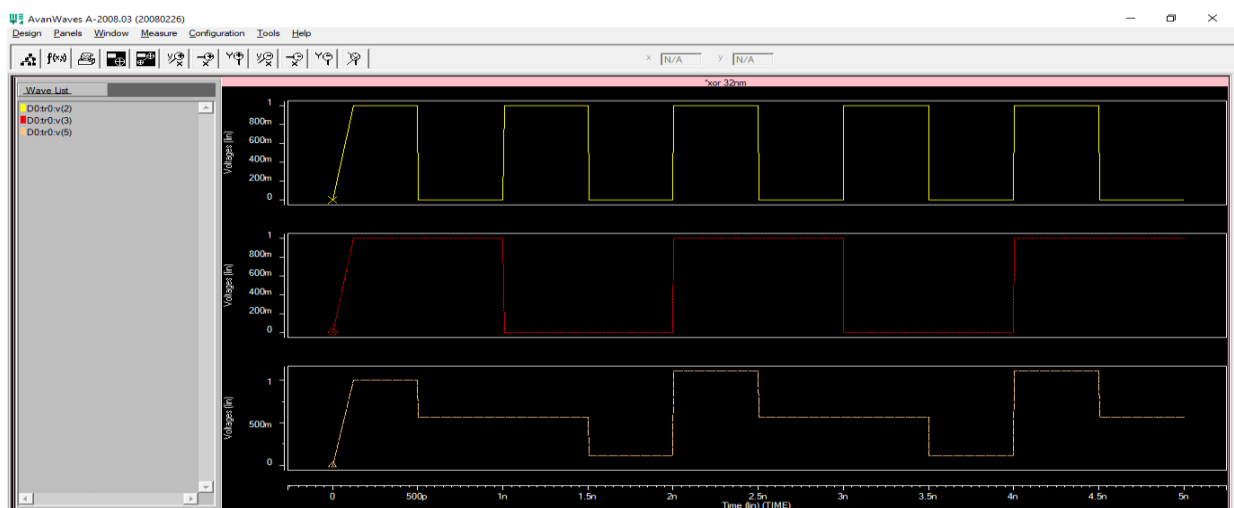


Figure 5.6.Simulation result of XOR under 32nm

Figure 5.6 represent the simulation result of XOR. This graph taken from the avan waves which is plotted to confirm the output of the source code of XOR gate. From XOR gate, the measurements were taken. The consumed power is 3.707×10^{-5} watt, delay is 1.628 ps.

5.2.2 SIMULATION RESULT OF XNOR:

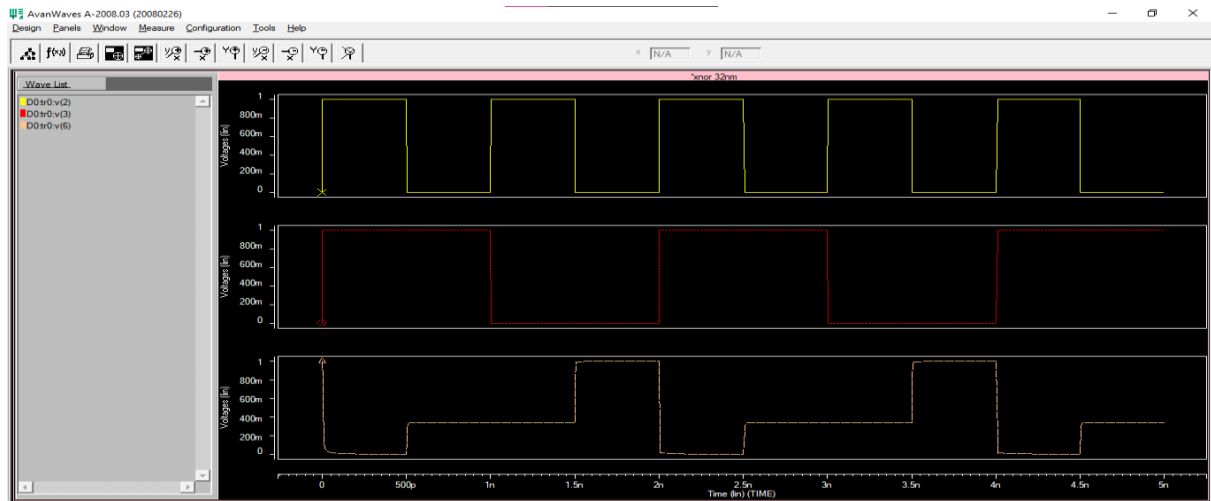


Figure 5.7 Simulation result of XNOR under 32nm

Figure 5.7 represent the simulation result of XNOR. This graph taken from the avan waves which is plotted to confirm the output of the source code of XNOR gate. From XNOR gate, the measurements were taken. The consumed power is 3.976×10^{-5} watt, delay is 495.9 ps.

5.2.3 SIMULATION RESULT OF FULL ADDER:

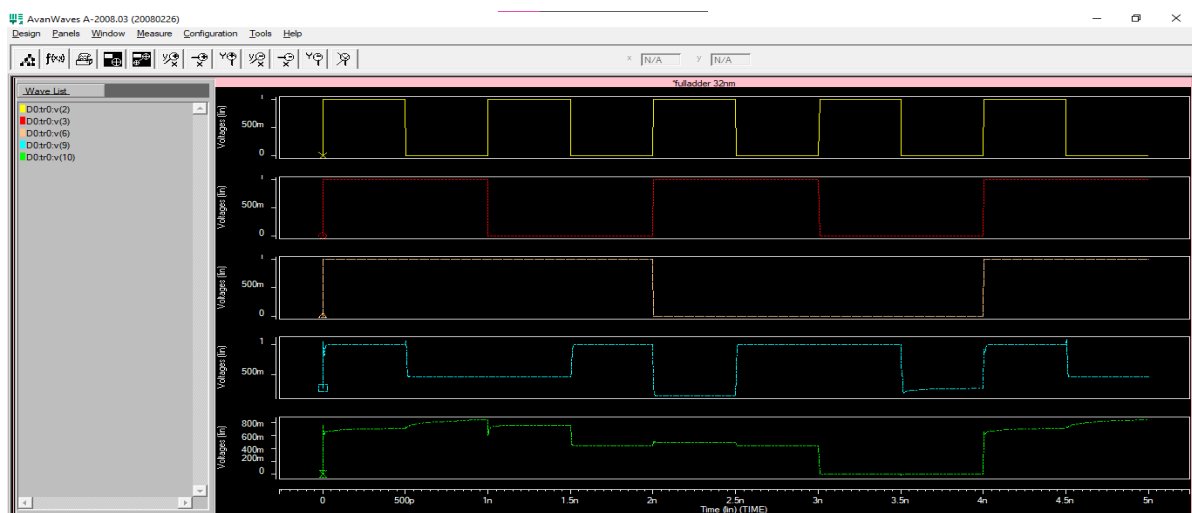


Figure 5.8.Simulation result of full adder under 32 nm

Figure 5.8 represent the simulation result of full adder. This graph taken from the avan waves which is plotted to confirm the output of the source code of

full adder gate. From full adder gate, the measurements were taken. The consumed power is 6.640×10^{-5} watt, delay is 0.008 ps.

5.2.4 SIMULATION RESULT OF ADDER UNIT:

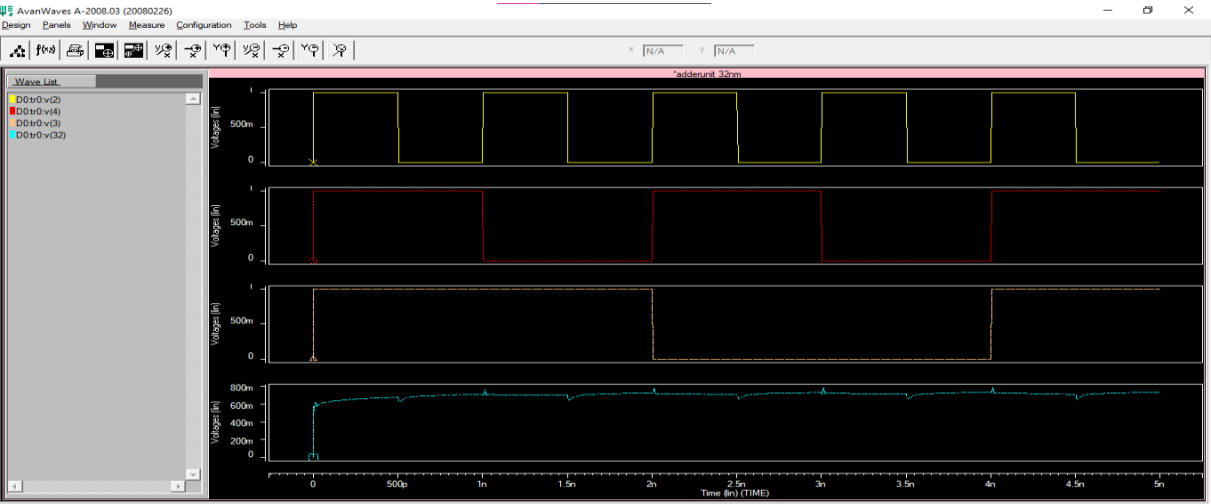


Figure 5.9.Simulation result of full adder under 32 nm

Figure 5.9 represent the simulation result of adder unit. This graph is taken from the avan waves, which is plotted to confirm output of the source code of adder unit. From adder unit, the measurements were taken. The consumed power is 83.37×10^{-5} watt, delay is 23.14 ps.

5.2.5 SIMULATION RESULT OF SERIAL DIVIDER:

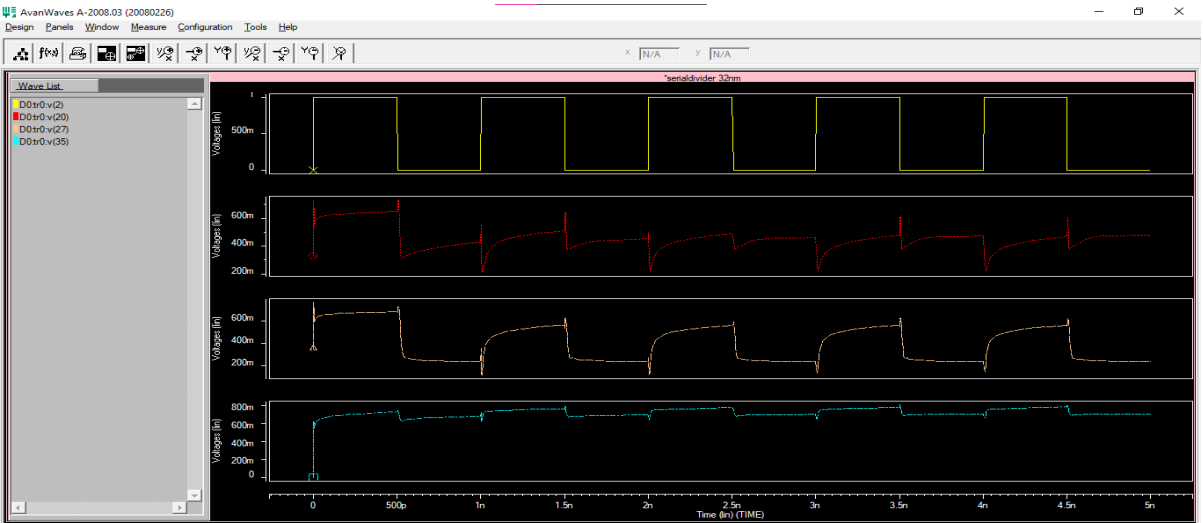


Figure 5.10 Simulation result of full adder under 32 nm

Figure 5.10 represent the simulation result of serial divider. This graph taken from the avan waves which is plotted to confirm the output of the source code of serial divider gate. From serial divider, the measurements were taken. The consumed power is 74.85×10^{-5} watt, delay is 404.2 ps.

5.3 PERFORMANCE ANALYSIS:

The below tables are the readings of power, delay and PDP in MOSFET under 130nm of XNOR, and, XOR, full adder, serial adder.

130 nm: Operating Voltage: 3.3v, Operating frequency: 1 Ghz

32nm: Operating Voltage: 1v, Operating frequency: 1 Ghz

5.3.1 PERFORMANCE ANALYSIS OF XOR:

PARAMETERS	130 nm	32 nm
Power(watt) (10^{-5})	1.599	3.707
Delay(Ps)	1.6185	1.628
Power delay product(Jule) (10^{-17})	2.587	6.034
Fall time(Ps)	0.239	2.872
Rise time(Ps)	1.562	2.16

Table 5.1 Design analysis of XOR

5.3.2 PERFORMANCE ANALYSIS OF XNOR:

PARAMETERS	130 nm	32 nm
Power(watt) (10^{-5})	1.142	3.970
Delay(Ps)	5.9328	495.9
Power delay product(jule) (10^{-17})	6.775	1968
Fall time(Ps)	0.880	1.36
Rise time(Ps)	0.400	1.439

Table 5.2. Design analysis of XNOR

5.3.3 PERFORMANCE ANALYSIS OF FULLADDER:

PARAMETERS	130 nm	32 nm
Power(watt) (10^{-5})	25.10	6.640
Delay(Ps)	12.991	0.008
Power delay product(jule) (10^{-17})	326.07	0.990
Fall time(Ps)	0.240	1.76
Rise time(Ps)	0.400	1.562

Table 5.3 Design analysis of full adder

5.3.4 PERFORMANCE ANALYSIS OF MODIFIED FULL ADDER:

PARAMETERS	130 nm	32nm
Power(watt) (10^{-5})	4.307	2.416
Delay(Ps)	0.026	0.410
Power delay product(jule) (10^{-17})	0.111	0.990
Fall time(Ps)	0.8	1.76
Rise time(Ps)	0.720	1.562

Table 5.4 Design analysis of modified full adder

5.3.5 PERFORMANCE ANALYSIS OF ADDER UNIT:

PARAMETERS	130 nm	32 nm
Power(watt) (10^{-5})	83.37	83.37
Delay(Ps)	105.96	23.14
Power delay product(jule) (10^{-17})	8833.8	1929
Fall time(Ps)	0.079	0.032
Rise time(Ps)	0.720	0

Table 5.5 Design analysis of adder unit

5.3.6 PERFORMANCE ANALYSIS OF MODIFIED ADDER UNIT:

PARAMETERS	130 nm	32 nm
Power(watt) (10^{-5})	60.42	36.71
Delay(Ps)	16.91	0.219
Power delay product(jule) (10^{-17})	1021.7	8.039
Fall time(Ps)	0.079	1.544
Rise time(Ps)	0.960	0.559

Table 5.6 Design analysis of modified adder unit

5.3.7 PERFORMANCE ANALYSIS OF SERIAL DIVIDER:

PARAMETERS	130 nm	32 nm
Power(watt) (10^{-5})	260.5	74.85
Delay(Ps)	179.19	404.2
Power delay product(jule) (10^{-17})	46593.7	30239
Fall time(Ps)	0.079	0.479
Rise time(Ps)	0.079	0.239

Table 5.7 Design analysis of serial divider

5.3.8 PERFORMANCE ANALYSIS OF MODIFIED SERIAL DIVIDER:

PARAMETERS	130 nm	32 nm
Power(watt) (10 ⁻⁵)	175.9	63.53
Delay(Ps)	260.33	0.686
Power delay product(jule) (10 ⁻¹⁷)	45792.0	43.58
Fall time(Ps)	0.056	0.799
Rise time(Ps)	0.079	0.400

Table 5.8 Design analysis of modified serial divider

CHAPTER 6

CONCLUSION

Division and addition are the important operations in DSP processors. The full adders have been designed using various logic styles following a unique pattern of structure to improve their performance in various means like less transistors, low power, minimal delay, reduced area, rise time, fall time and increased power delay product. This project explores and analyses serial divider for high speed VLSI applications. The simulation is carried out at 130nm, 32nm CMOS technology under MOSFET using various voltages. The power, delay, rise time, fall time and power delay product analysis are compared. It is noted that, on an average power of existing serial divider is efficient than the proposed serial divider. In existing full adder, there are 7 pmos transistors present. In proposed there are only 5 pmos transistors. So this design consumes less power than the existing one. Because pmos transistors consumed area more than nmos transistors. The proposed serial divider obtaining a high speed, low area, less power dissipation and low propagation delay. The devices were designed and their performance were analysed using HSpice tool. In order to reduce power and delay furthermore, the proposed full adder developed and compared with existing full adder.

The performance of proposed full adder is improved by 83.85 % and 64.72% than the existing full adder respectively in MOSFET under 130nm, 32nm. The performance of proposed serial divider is improved by 33.5 % and 16.2% than the existing full adder respectively in MOSFET under 130nm, 32nm.

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