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SCHOOL OF ELECTRICAL AND ELECTRONICS
DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

UNIT - I
Electronic Circuits-SECA1305

1.1 INTRODUCTION

For the operation of most of the electronics devices and circuits, a d.c. source is required. So it is advantageous to convert domestic a.c. supply into d.c.voltages. The process of converting a.c. voltage into d.c. voltage is called as rectification. This is achieved with i) Step-down Transformer, ii) Rectifier,iii) Filter and iv) Voltage regulator circuits.These elements constitute d.c. regulated power supply shown in the Fig 1 below

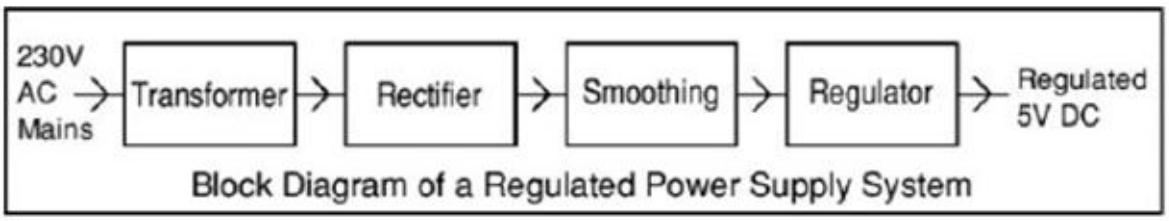


Fig 1.1Block Diagram of regulated D.C Power Supply

- ✓ Transformer – steps down 230V AC mains to low voltage AC.
- ✓ Rectifier – converts AC to DC, but the DC output is varying.
- ✓ Smoothing – smooth the DC from varying greatly to a small ripple.
- ✓ Regulator – eliminates ripple by setting DC output to a fixed voltage.

The block diagram of a regulated D.C. power supply consists of step-down transformer, rectifier, filter, voltage regulator and load. An ideal regulated power supply is an electronics circuit designed to provide a predetermined d.c. voltage Vo which is independent of the load current and variations in the input voltage ad temperature. If the output of a regulator circuit is a AC voltage then it is termed as voltage stabilizer, whereas if the output is a DC voltage then it is termed as voltage regulator.

1.2 RECTIFIER

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional Waveform, with a nonzero average component. A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c. voltage (Unidirectional).

1.2.1 Characteristics of a Rectifier Circuit:

Any electrical device which offers a low resistance to the current in one direction but a high resistance to the current in the opposite direction is called rectifier. Such a device is capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform, with a nonzero average component.

A rectifier is a device, which converts a.c. voltage (bi-directional) to pulsating d.c..Load currents: They are two types of output current. They are average or d.c. current and RMS currents.

Average or DC current: The average current of a periodic function is defined as the area of one cycle of the curve divided by the base. It is expressed mathematically as

i) Average value/dc value/mean value= Total time period/Area over one period

$$V_{dc} = \frac{1}{T}\int_0^T V d(wt)$$

Effective (or) R.M.S current: The effective (or) R.M.S. current squared ofa periodic function of time is given by the area of one cycle of the curve, which represents the square of the function divided by the base.

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

Peak factor: It is the ratio of peak value to RMS value

Form factor: It is the ratio of RMS value to average value

Ripple Factor: It is defined as ratio of R.M.S. value of a.c. component to the d.c. component in the output is known as "Ripple Factor".

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

Efficiency: It is the ratio of d.c output power to the a.c. input power. It signifies, how efficiently the rectifier circuit converts a.c. power into d.c. power.

$$\eta = \frac{o/p\ power}{i/p\ power}$$

Peak Inverse Voltage (PIV): It is defined as the maximum reverse voltage that a diode can withstand without destroyingthe junction.

Transformer Utilization Factor (UTF): The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the Transformer used in the circuit. So, transformer utilization factor is defined as

$$TUF = \frac{P_{dc}}{P_{ac(rated)}}$$

% Regulation: The variation of the d.c. output voltage as a function of d.c. load current is called regulation. The percentage regulation is defined as

$$\%\,\mathrm{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} * 100$$

1.3 CLASSIFICATION OF RECTIFIERS

Using one or more diodes in the circuit, following rectifier circuits can be designed.

1) Half - Wave Rectifier

2) Full – Wave Rectifier

3) Bridge Rectifier

1.3.1 HALF-WAVE RECTIFIER:

A Half – wave rectifier as shown in **fig 1.2** is one, which converts a.c. voltage into a pulsating voltage using only one half cycle of the applied a.c. voltage.

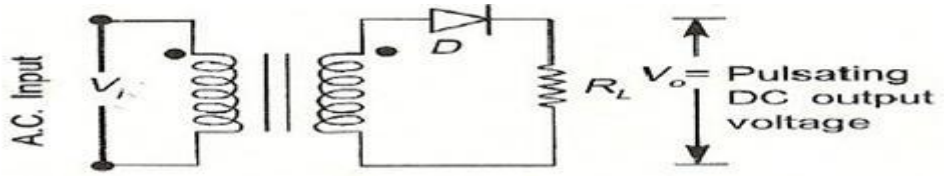


Fig 1.2 Half wave rectifier

The a.c. voltage is applied to the rectifier circuit using step-down transformer-rectifying element i.e., pn junction diode and the source of a.c. voltage, all connected is series. The a.c. voltage is applied to the rectifier circuit using step-down transformer

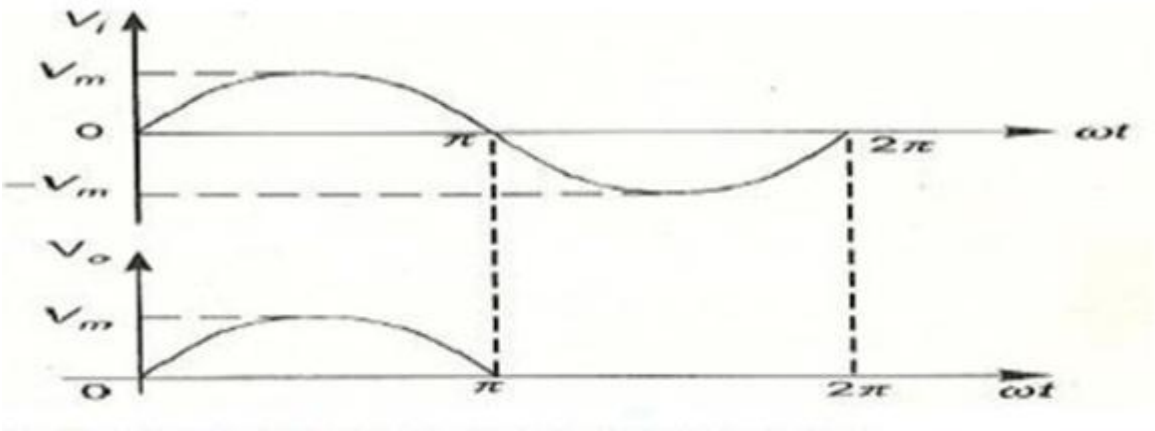


Fig 1.3 Waveform of Half wave rectifier

Let V=Vm sin (wt) The input to the rectifier circuit, Where Vm is the peak value of secondary a.c. voltage.

1.3.1.1 Operation:

For the positive half-cycle of input a.c. voltage, the diode D is forward biased and hence it conducts. Now a current flows in the circuit and there is a voltage drop across RL. The waveform of the diode current (or) load current is shown in fig 3. For the negative half-cycle of input, the diode D is reverse biased and hence it does not Conduct. Now no current flows in the circuit i.e., i=0 and Vo=0. Thus for the negative half- cycle no power is delivered to the load.

1.3.1.2 Analysis:

In the analysis of a HWR, the following parameters are to be analyzed.

1. DC output current
2. DC Output voltage
3. R.M.S. Current
4. R.M.S. voltage
5. Rectifier Efficiency (η)
6. Ripple factor (γ) 7. Peak Factor
8. % Regulation
9. Transformer Utilization Factor (TUF)
10. form factor
11. o/p frequency

Let a sinusoidal voltage Vi be applied to the input of the rectifier.

Then V=Vm sin (wt) Where Vm is the maximum value of the secondary voltage. Let the diode be idealized to piece-wise linear approximation with resistance Rf in the forward direction i.e., in the ON state and Rr (=∞) in the reverse direction i.e., in the OFF state. Now the current 'i' in the diode (or) in the load resistance RL is given by V=Vm sin (wt)

i) AVERAGE VOLTAGE

$$V_{dc} = \frac{1}{T}\int_0^T V d(wt)$$

$$V_{dc} = \frac{1}{T}\int_0^{2\Pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_{\Pi}^{2\Pi} V(\alpha) d\alpha$$

$$V_{dc} = \frac{1}{2\Pi}\int_0 V_m \sin(wt)$$

$$V_{dc} = \frac{V_m}{\Pi}$$

ii).AVERAGE CURRENT:

$$I_{dc} = \frac{I_m}{\Pi}$$

iii) RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{2}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{I_m}{\Pi}}$$

V) PEAK FACTOR

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m/2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rmsvalue}{averagevalue}$$

$$\text{Form factor} = \frac{(V_m/2)}{V_m/\Pi}$$

Form Factor =1.57

vii) Ripple Factor:

$$\Gamma = \frac{V_{ac}}{V_{dc}}$$

$$V_{ac} = \sqrt{V_{rms}^2 - V_{dc}^2}$$

$$\Gamma = \frac{\sqrt{V_{rms}^2 - V_{dc}^2}}{V_{ac}}$$

$$\Gamma = \sqrt{\frac{V_{rms}^2}{V_{dc}^2} - 1}$$

$$\Gamma = 1.21$$

viii) Efficiency (η):

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{p_{ac}}{P_{dc}} * 100$$

η =40.8

Ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. Therefore, transformer utilization factor is given as *TUF* =0.286. The value of TUF is low which shows that in half-wave circuit, the transformer is not fully utilized. If the transformer rating is 1 KVA (1000VA) then the half-wave rectifier can deliver 1000 X 0.287 = 287 watts to resistance load.

x) Peak Inverse Voltage (PIV): It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half-wave rectifier, PIV is Vm.

1.3.1.3 DISADVANTAGES OF HALF-WAVE RECTIFIER:

1. The ripple factor is high.
2. The efficiency is low.
3. The Transformer Utilization factor is low.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

1.3.2.1 FULL WAVE RECTIFIER:

A full-wave rectifier converts an ac voltage into a pulsating dc voltage using both half cycles of the applied ac voltage. In order to rectify both the half cycles of ac input, two diodes are used in this circuit. The diodes feed a common load RL with the help of a center-tap transformer. A center-tap transformer is the one, which produces two sinusoidal waveforms of same magnitude and frequency but out of phase with respect to the ground in the secondary winding of the transformer. The full wave rectifier is shown in the **Fig 1.4** below

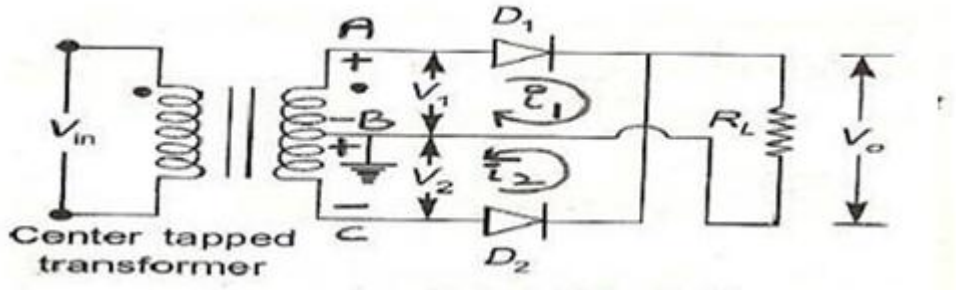


Fig 1.4 Full wave rectifier

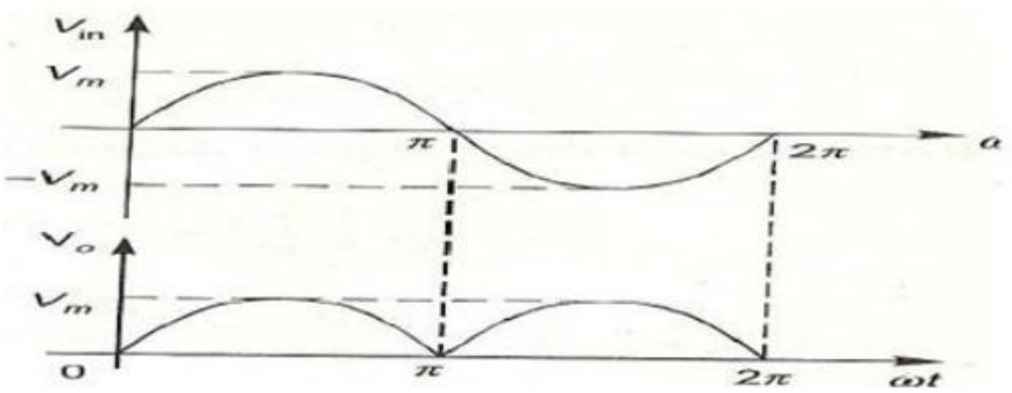


Fig 1.5 Input and output waveform of Full wave rectifier

Fig. 1.5 shows the input and output wave forms of the ckt. During positive half of the input signal, anode of diode D1 becomes positive and at the same time the anode of diode D2 becomes negative. Hence D1 conducts and D2 does not conduct. The load current flows through D1 and the voltage drop across RL will be equal to the input voltage.

During the negative half cycle of the input, the anode of D1 becomes negative and the anode of D2 becomes positive. Hence, D1 does not conduct and D2 conducts. The load current flows through D2 and the voltage drop across RL will be equal to the input voltage. It is noted that the load current flows in the both the half cycles of ac voltage and in the same direction through the load resistance.

a. AVERAGE VOLTAGE

$$V_{dc} = I_{dc}.R_L. = \frac{2I_m}{\pi}.R_L \quad \text{We know } I_m = \frac{V_m}{R_S + R_f + R_L}$$

$$\therefore V_{dc} = \frac{2.V_m.R_L}{\pi(R_S + R_f + R_L}$$

$$If\,(R_s + R_f) << R_L$$

$$V_{dc} = \frac{2V_m}{\pi} = 0.637V_{m.}$$

b. AVERAGE CURRENT

$$\frac{1}{2\pi}\int_0^{2\pi} id\theta = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin\theta dt$$

$$I_{dc} = \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\theta d\theta - \int_{\pi}^{2\pi} \sin\theta d\theta\right]$$

$$= \frac{I_m}{2\pi}[(-2)(-2)]$$

$$= \frac{I_m}{2\pi}.4 = \frac{2I_m}{\pi} = 0.637\,I_m.$$

$$\boxed{I_{dc} = 0.637 I_{m.}}$$

$$\therefore I_{DC}\ FWR = 2\ I_{DC}\ HWR.$$

RMS VOLTAGE:

$$V_{rms} = \sqrt{\frac{1}{T}\int_0^T V^2 d(wt)}$$

$$V_{rms} = \sqrt{\frac{1}{2\Pi}\int_0^{2\Pi} (V_m sim(wt))^2 d(wt)}$$

$$\boxed{V_{rms} = \frac{V_m}{\sqrt{2}}}$$

IV) RMS CURRENT

$$\boxed{I_{rms} = \frac{2I_m}{\Pi}}$$

V) PEAK FACTOR

$$\text{Peak factor} = \frac{peakvalue}{rmsvalue}$$

$$\text{Peak Factor} = \frac{V_m}{(V_m/2)}$$

Peak Factor =2

vi) FORM FACTOR

$$\text{Form factor} = \frac{Rms\ value}{average\ value}$$

$$\text{Form factor} = \frac{(V_m/\sqrt{2})}{2V_m/\Pi}$$

Form Factor =1.11

vii) Ripple Factor:

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

for FWR.

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \& \quad I_{DC} = \frac{2I_m}{\pi}$$

$$\therefore \gamma_{FWR} = \sqrt{\left(\frac{I_m}{\sqrt{2}} / \frac{2I_m}{\pi}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

$$= \sqrt{\left(\frac{3.1416}{2\times 1.414}\right)^2 - 1} = 0.483$$

viii) Efficiency (η):

$$\eta = \frac{o/ppower}{i/ppower} * 100$$

$$\eta = \frac{P_{dc}}{P_{ac}} \times 100\%$$

For FWR, $p_{dc} = I_{dc}^2 . R_L = \left(\frac{2}{\pi} . I_m\right)^2 . R_L$

$P_{ac} = I^2_{rms} (R_f + R_S + R_L)$

$$\left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_S + R_L)$$

$$\eta = \frac{\frac{I^2_m 4}{\pi^2} . R_L}{\frac{I^2 m^2}{2} . (R_f + R_s + R_L)}$$

$$If\ (R_f + R_S) << R_L$$

$$\eta = \frac{4}{\pi^2} . \frac{2}{1} = \frac{8}{\pi^2} = 0.812 = 81.2\%$$

ix) Transformer Utilization Factor (TUF):

The d.c. power to be delivered to the load in a rectifier circuit decides the rating of the transformer used in the circuit. So,

a) $\text{TUF (Secondary)} = \frac{P_{dc}\ delivered\ to\ load}{AC\ power\ rating\ of\ transformer\ secondary}$

b) Since both the windings are used $\text{TUF}_{FWR} = 2\ \text{TUF}_{HWR}$

$= 2 \times 0.287 = 0.574$

c) TUF primary = Rated efficiency $= \frac{P_{dc}}{P_{ac}} \times 100 = 81.2\%$

d) Average $= \frac{0.812 + 0.574}{2} = 0.693$

x) Peak Inverse Voltage (PIV):

It is defined as the maximum reverse voltage that a diode can withstand without destroying the junction. The peak inverse voltage across a diode is the peak of the negative half- cycle. For half- wave rectifier, PIV is 2Vm

xi) % Regulation

$$\textbf{Voltage regulation} = \frac{I_{dc}(R_s + R_f)}{\frac{2V_m}{\pi} - I_{DC}(R_f + R_S)}$$

Advantages

1) Ripple factor = 0.482 (against 1.21 for HWR)

2) Rectification efficiency is 0.812 (against 0.405 for HWR)

3) Better TUF (secondary) is 0.574 (0.287 for HWR)

4) No core saturation problem

Disadvantages:

1) Requires center tapped transformer.

1.3.3 BRIDGE RECTIFIER.

Another type of circuit that produces the same output waveform as the full wave rectifier circuit above, is that of the Full Wave Bridge Rectifier. This type of single phase rectifier uses four individual rectifying diodes connected in a closed loop "bridge" configuration to produce the desired output. The main advantage of this bridge circuit is that it does not require a special centre tapped transformer, thereby reducing its size and cost. The single secondary winding is connected to one side of the diode bridge network and the load to the other side as shown below.

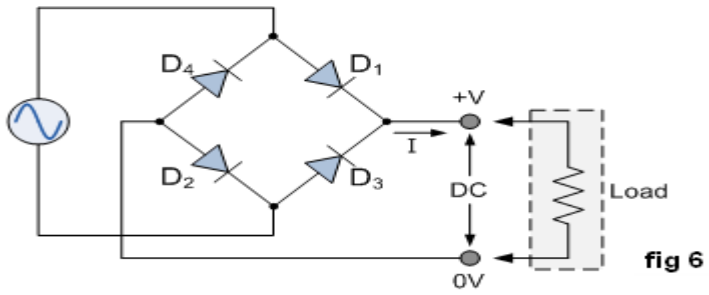


Fig 1.6 Bridge rectifier

The four diodes labelled D1 to D4 are arranged in "series pairs" with only two diodes conducting current during each half cycle. During the positive half cycle of the supply, diodes D1 and D2 conduct in series while diodes D3 and D4 are reverse biased and the current flows through the load as shown below (fig 7).

The Positive Half-cycle

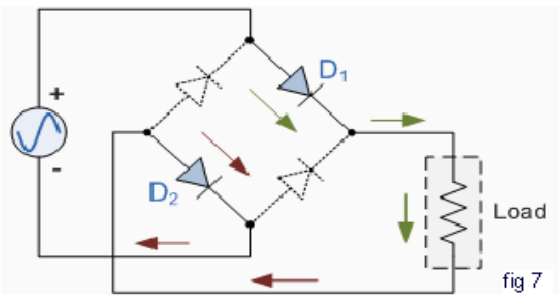


Fig 1.7 Bridge rectifier-positive half cycle

The Negative Half-cycle

During the negative half cycle of the supply, diodes D3 and D4 conduct in series (fig 8), but diodes D1 and D2 switch "OFF" as they are now reverse biased. The current flowing through the load is the same direction as before.

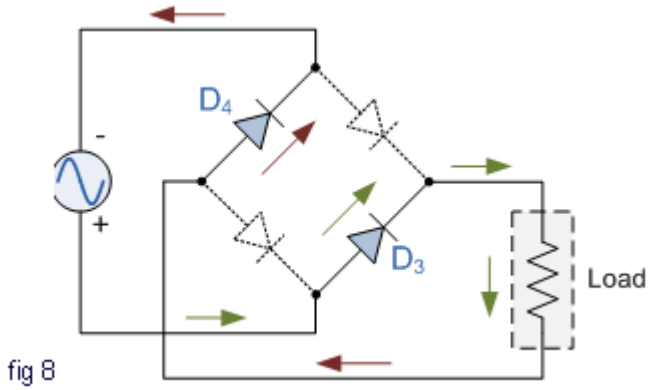


Fig 1.8 Bridge rectifier-positive half cycle

As the current flowing through the load is unidirectional, so the voltage developed across the load is also unidirectional the same as for the previous two diode full-wave rectifier, therefore the average DC voltage across the load is 0.637Vmax. However in reality, during each half cycle the current flows through two diodes instead of just one so the amplitude of the output voltage is two voltage drops (2 x 0.7 = 1.4V) less than the input VMAX amplitude. The ripple frequency is now twice the supply frequency (e.g. 100Hz for a 50Hz supply) **2.3**

Therefore, the following expressions are same as that of full wave rectifier.

a) Average current $I_{dc} = \frac{2I_m}{\pi}$

b) RMS current $I_{rms} = \frac{I_m}{\sqrt{2}}$

c) DC output voltage (no.load) V_{DC} $\frac{2V_m}{\pi}$

d) Ripple factor γ=0.482

e) Rectification efficiency = $\eta = 0.812$

f) DC output voltage full load.

= $V_{DCFL} = \frac{2V_m}{\pi} - I_{dc}(R_S + 2R_f)$; i.e., less by one diode loss.

TUF of both primary & secondary are 0.812 therefore TUF overall is 0.812 (better than FWR with 0.693)

Comparison:

Sl. No.	Parameter	HWR	FWR	BR
1	No. of diodes	1	2	4
2	PIV of diodes	V_m	2 V_m	V_m
3	Secondary voltage (rms)	V	V-0-V	V
4	DC output voltage at no load	$\frac{V_m}{\pi}$ =0.318 V_m	$\frac{2V_m}{\pi}$ =0.636 V_m	$\frac{2V_m}{\pi}$ =0.636 V_m
5	Ripple factor γ	1.21	0.482	0.482
6	Ripple frequency	f	2f	2f
7	Rectification efficiency η	0.406	0.812	0.812
8	TUF	0.287	0.693	0.812

1.4 FILTERS

The output of a rectifier contains dc component as well as ac component. Filters are used to minimize the undesirable ac i.e., ripple leaving only the dc component to appear at the output. Some important filters are:

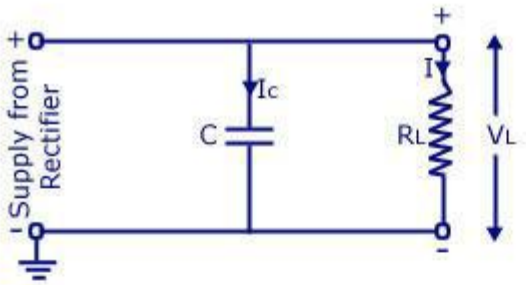
1. Inductor filter
2. Capacitor filter
3. LC or L section filter
4. CLC or Π-type filter

1.4.1 CAPACITOR FILTER

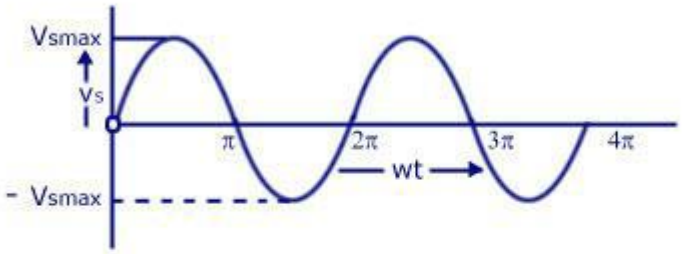
This is the most simple form of the **filter circuit** and in this arrangement a high value capacitor C is placed directly across the output terminals, as shown in figure. During the conduction period it gets charged and stores up energy to it during non-conduction period. Through this process, the time duration during which Ft is to be noted here that the capacitor C gets charged to the peak because there is no resistance (except the negligible forward resistance of diode) in the charging path. But the discharging time is quite large (roughly 100 times more than the charging time depending upon the value of RL) because it discharges through load resistance RL.

The function of the capacitor filter may be viewed in terms of impedances. The large value capacitor C offers a low impedance shunt path to the ac components or ripples but offers high impedance to the dc component. Thus ripples get bypassed through capacitor C and only dc component flows through the load resistance RL

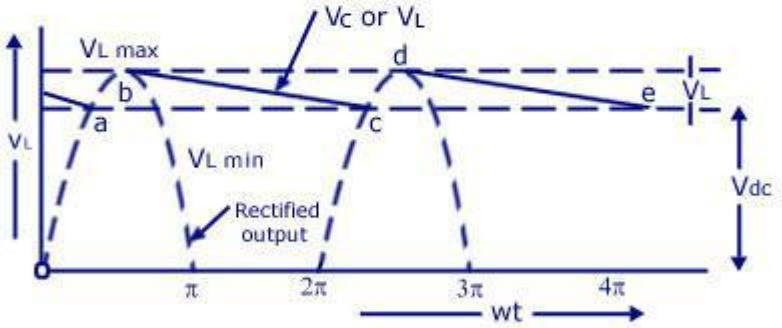
Capacitor filter is very popular because of its low cost, small size, light weight and good characteristics.



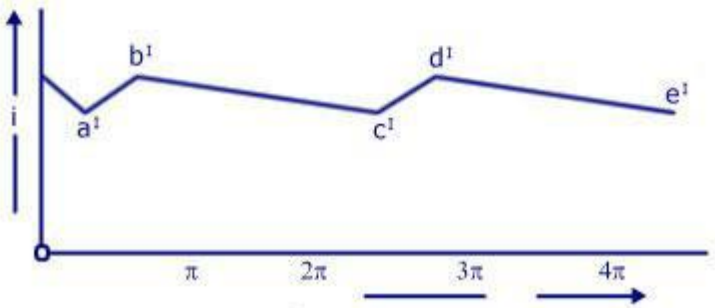
Circuit Diagram



Input voltage Waveform to Rectifier

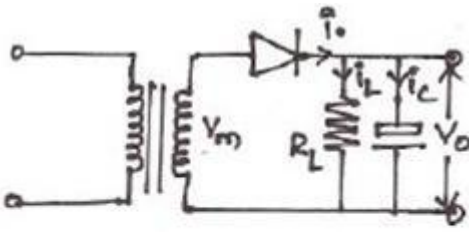


Rectified and filtered Output Voltage Waveform



Load Current Waveform
Half-wave Rectifier With Shunt Capacitor Filter

Fig 1.9 Capacitor filter in Rectifiers

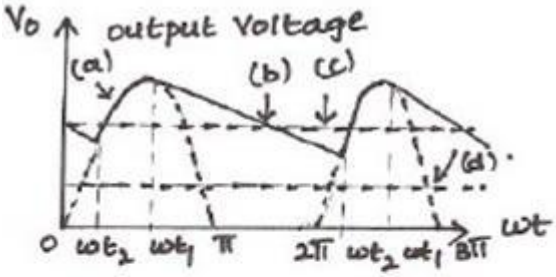


Cut In angle – wt_2

Cut out angle = Wt_1

$Wt_1 = \pi - \tan^{-1} WCR_L$

Fig 1.10 Capacitor Filter With HWR



(a) Capacitor charging through diode ($Wt_2 - Wt_1$)

(b) Capacitor discharging through R_L (Wt_1 to Wt_2)

(c) Average (DC) voltage with fitter

(d) Average (DC) voltage without fitter.

CAPACITOR FILTER WITH FWR

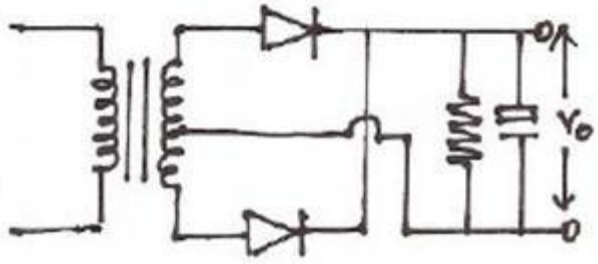
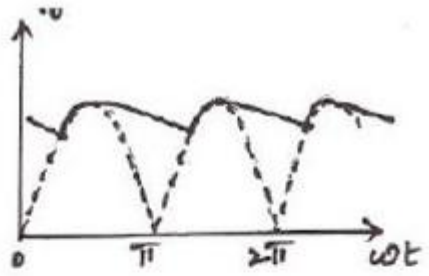
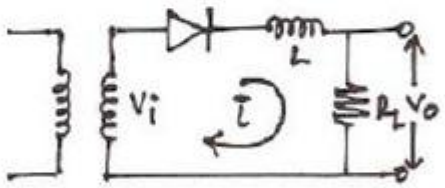


Fig 1.11 Capacitor Filter With FWR



$$\text{Ripple factor } r = \frac{1}{4\sqrt{3}fCR_L}$$

Ripple freq $_{FWR}$ = 2 ripple freq $_{HWR}$.



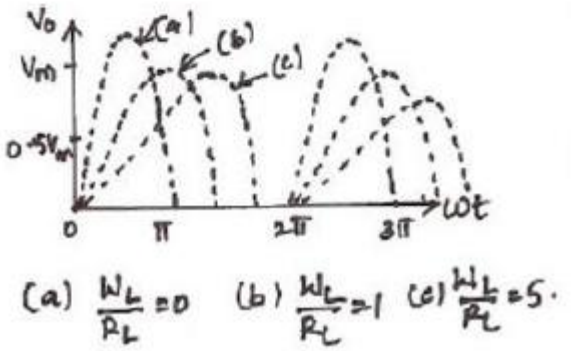


Fig 1.12 Ripple factor of Capacitor Filter With HWR and FWR

Concluding:

1.For a fixed-value filter capacitance larger the load resistance RL larger will be the discharge time constant CRL and therefore, lower the ripples and more the output voltage. On the other hand lower the load resistance (or more the load current), lower will be the output voltage.

2.Similarly smaller the filter capacitor, the less charge it can hold and more it will discharge. Thus the peak-to-peak value of the ripple will increase, and the average dc level will decrease. Larger the filter capacitor, the more charge it can hold and the less it will discharge. Hence the peak-to-peak value of the ripple will be less, and the average dc level will increase. But, the

maximum value of the capacitance that can be employed is limited by another factor. The larger the capacitance value, the greater is the current required to charge the capacitor to a given voltage. The maximum current that can be handled by a diode is limited by the figure quoted by the manufacturer. Thus the maximum value of the capacitance, that can be used in the shunt filter capacitor is limited.

1.4. 2 Series Inductor Filter.

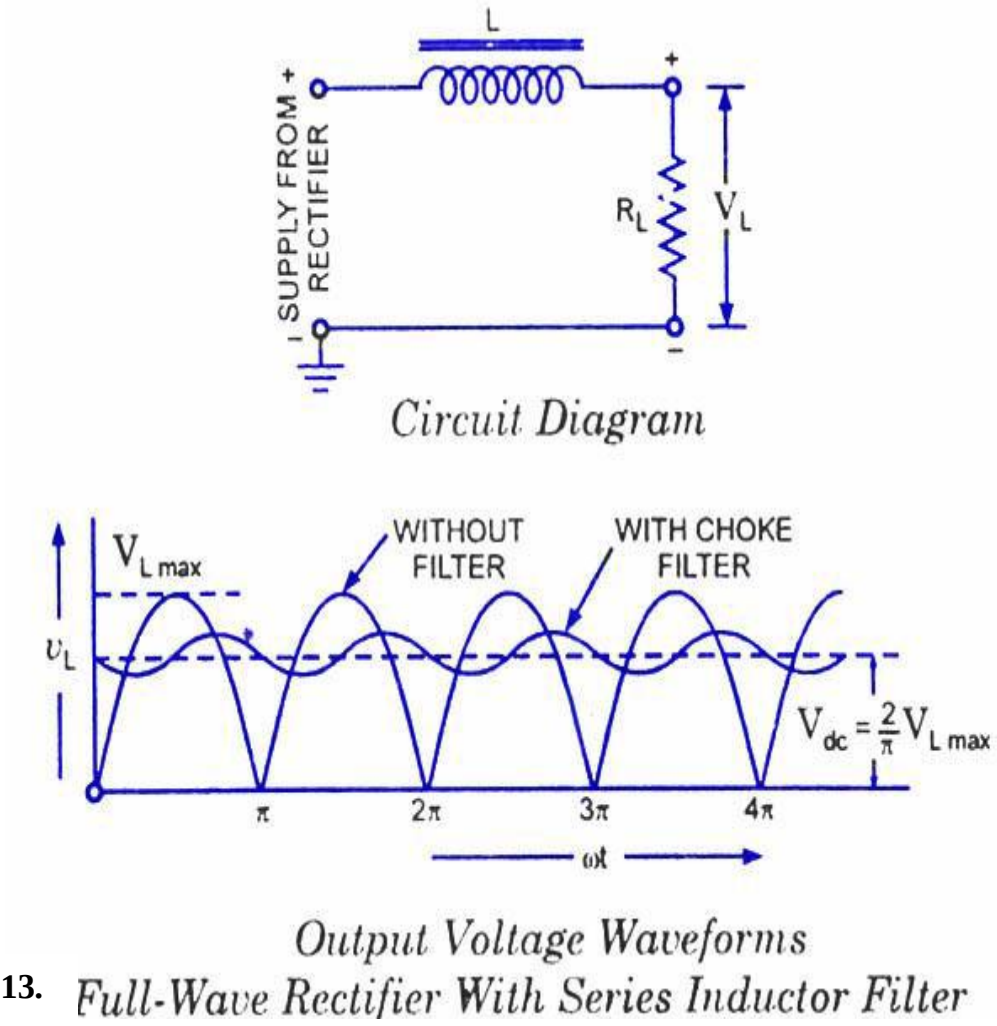


Fig 1.13. *Full-Wave Rectifier With Series Inductor Filter*

In this arrangement a high value inductor or choke L is connected in series with the rectifier element and the load, as illustrated in figure. The filtering action of an inductor filter depends upon its property of opposing any change in the current flowing through it. When the output current of the rectifier increases above a certain value, energy is stored in it in the form of magnetic field and this energy is given up when the output current falls below the average value. Thus by placing a choke coil in series with the rectifier output and load, any sudden change in current that might have occurred in the circuit without an inductor is smoothed out by the presence of the inductor L.

The function of the inductor filter may be viewed in terms of impedances. The choke offers high impedance to the ac components but offers almost zero resistance to the desired dc components. Thus ripples are removed to a large extent. Nature of the output voltage without filter and with choke filter is shown in figure.

For dc (zero frequency), the choke resistance Rc in series with the load resistance RL forms a voltage divider and dc voltage across the load is given as

where Vdc is dc voltage output from a full-wave rectifier. Usually choke coil resistance Rc, is much small than RL and, therefore, almost entire of the dc voltage is available across the load resistance RL.

Since the reactance of inductor increases with the increase in frequency, better filtering of the higher harmonic components takes place, so effect of third and higher harmonic voltages can be neglected.

As obvious from equation , if choke coil resistance Rc is negligible in comparison to load resistance RL, then the entire dc component of rectifier output is available across 2 RL and is equal to — VL max. The ac voltage partly drops across XL and partly over RL.

1.4 .3 L-SECTION FILTER:

A simple series inductor reduces both the peakand effective values of the output current and output voltage. On the other hand a simple **shunt capacitor filter** reduces the ripple voltage but increases the diode current. The diode may get damaged due to large current and at the same time it causes greater heating of supply transformer resulting in reduced efficiency.

In an inductor filter, ripple factor increases with the increase in load resistance RL while in a capacitor filter it varies inversely with load resistance RL. From economical point of view also, neither series inductor nor shunt capacitor type filters are suitable. Practical **filter-circuits** are derived by combining the voltage stabilizing action of shunt capacitor with the current smoothing action of series choke coil. By using combination of inductor and capacitor ripple factor can be lowered, diode current can be restricted and simultaneously ripple factor can be made almost independent of load resistance (or load current). Two types of most commonly used combinations are choke-input or L-section filter-and capacitor-input or Pi-Filter.

Choke-input filter is explained below:

Choke-input filter consists of a choke L connected in series with the rectifier and a capacitor C connected across the load . This is also sometimes called the L-section filter because in this arrangement inductor and capacitor are connected, as an inverted L. ln figure only one filter

section is shown. But several identical sections are often employed to improve the smoothing action. (The choke L on the input side of the filter readily allows dc to pass but opposes the flow of ac components because its dc resistance is negligibly small but ac impedance is large. Any fluctuation that remains in the current even after passing through the choke are largely by-passed around the load by the shunt capacitor because Xc is much smaller than RL. Ripples can be reduced effectively by making XL greater than Xc at ripple frequency. However, a small ripple still remains in the filtered output and this is considered negligible if it than l%. The rectified and filtered output voltage waveforms from a full-wave re with choke-input filter are shown in figure.

1.4.5 II-SECTION FILTER:

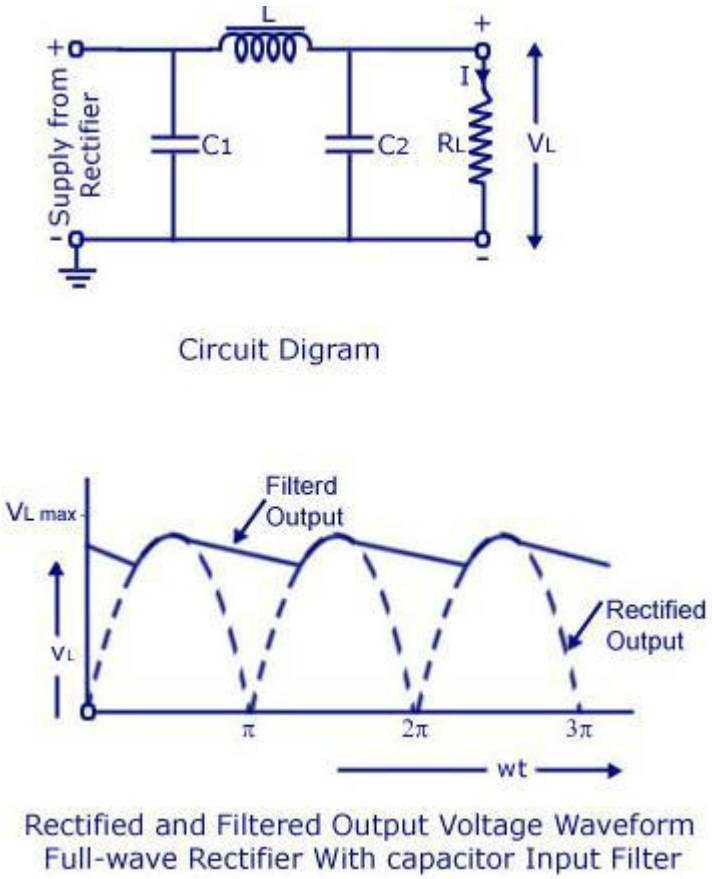


Fig 1.15 Capacitor-Input or Pi-Filter.

Such a filter consists of a shunt capacitor C1 at the input followed by an L-section filter formed by series inductor L and shunt capacitor C2. This is also called the *n-filter* because the shape of the circuit diagram for this filter appears like Greek letter *n (pi)*. Since the rectifier feeds directly into the capacitor so it is also called *capacitor input filter*. As the rectified output is fed directly into a capacitor C1. Such a filter can be used with a half-wave rectifier (series inductor and L-section filters cannot be used with half-wave rectifiers). Usually electrolytic capacitors are used even though their capacitances are large but they

occupy minimum space. Usually both capacitors C1 and C2 are enclosed in one metal container. The metal container serves as, the common ground for the two capacitors.

A capacitor-input or *pi*- filter is characterized by a high voltage output at low current drains. Such a filter is used, if, for a given transformer, higher voltage than that can be obtained from an L-section filter is required and if low ripple than that can be obtained from a shunt capacitor filter or L-section filter is desired. In this filter, the input capacitor C1 is selected to offer very low reactance to the ripple frequency. Hence major part of filtering is accomplished by the input capacitor *C1*. Most of the remaining ripple is removed by the L-section filter consisting of a choke L and capacitor C2.) The action of this filter can *best* be understood by considering the action of L-section filter, formed by L and C2, upon the triangular output voltage wave from the input capacitor C1 The charging and discharging action of input capacitor C1 has already been discussed. The output voltage is roughly the same as across input capacitor C1 less the dc voltage drop in inductor. The ripples contained in this output are reduced further by L-section filter. The output voltage of pi-filter falls off rapidly with the increase in load-current and, therefore, the voltage regulation with this filter is very poor.

SALIENT FEATURES OF L-SECTION AND PI-FILTERS.

1. In pi-filter the dc output voltage is much larger than that can be had from an L-section filter with the same input voltage.

2.In pi-filter ripples are less in comparison to those in shunt capacitor or L-section filter. So smaller valued choke is required in a pi-filter in comparison to that required in L-section filter.

3.In pi-filter, the capacitor is to be charged to the peak value hence the rms current in supply transformer is larger as compared in case of L-section filter.

4.Voltage regulation in case of pi-filter is very poor, as already mentioned. So n-filters are suitable for fixed loads whereas L-section filters can work satisfactorily with varying loads provided a minimum current is maintained.

5.In case of a pi-filter PIV is larger than that in case of an L-section filter.

COMPARISON OF FILTERS

1) A capacitor filter provides Vm volts at less load current. But regulation is poor.

2) An Inductor filter gives high ripple voltage for low load currents. It is used for high load currents

3) L – Section filter gives a ripple factor independent of load current. Voltage

Regulation can be improved by use of bleeder resistance

4) Multiple L – Section filter or π filters give much less ripple than the single L – Section Filter.

1.5 **Voltage Regulator :**

A **voltage regulator** is such a device that maintains constant output voltage, instead of any kind of fluctuations in the input voltage being applied or any variations in current, drawn by the load.

Types of Regulators

Regulators can be classified into different categories, depending upon their working and type of connection.

Depending upon the type of regulation, the regulators are mainly divided into two types namely, line and load regulators.

 Line Regulator − The regulator which regulates the output voltage to be constant, in spite of input line variations, it is called as **Line regulator**.

 Load Regulator − The regulator which regulates the output voltage to be constant, in spite of the variations in load at the output, it is called as **Load regulator**.

Depending upon the type of connection, there are two type of voltage regulators. They are 1.Series voltage regulator 2.Shunt voltage regulator. The arrangement of them in a circuit will be just as in the following figures.

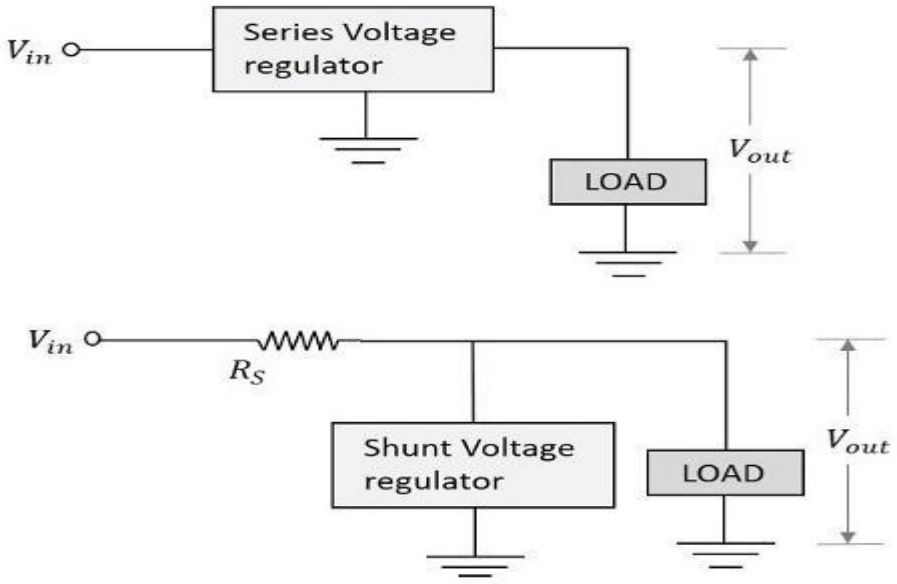


Fig 1.16 Voltage regulator with arrangement

1.5.1 Zener Voltage Regulator

A Zener voltage regulator is one which uses Zener diode for regulating the output voltage. We have already discussed the details regarding Zener diode in BASIC ELECTRONICS tutorial. When the Zener diode is operated in the breakdown or **Zener region**, the voltage across it is substantially **constant** for a **large change of current** through it. This characteristic makes Zener diode a **good voltage regulator**.

The following figure shows an image of a simple Zener regulator.

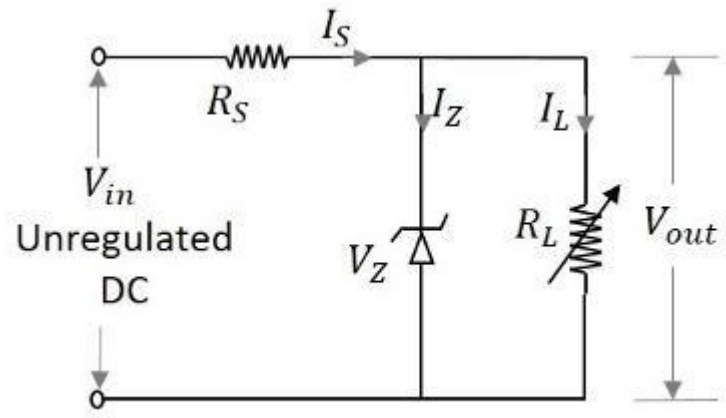


Fig 1.17 Zener Voltage Regulator

The applied input voltage ViVi when increased beyond the Zener voltage VzVz, then the Zener diode operates in the breakdown region and maintains constant voltage across the load. The series limiting resistor RsRs limits the input current.

Working of Zener Voltage Regulator

The Zener diode maintains the voltage across it constant in spite of load variations and input voltage fluctuations. Hence we can consider 4 cases to understand the working of a Zener voltage regulator.

Case 1 − If the load current ILIL increases, then the current through the Zener diode IZIZ decreases in order to maintain the current through the series resistor RSRS constant. The output voltage Vo depends upon the input voltage Vi and voltage across the series resistor RSRS. This is can be written as

Vo=Vin−IRsVo=Vin−IRs Where II is constant. Therefore, VoVo also remains constant.

Case 2 − If the load current ILIL decreases, then the current through the Zener diode IZIZ increases, as the current ISIS through RS series resistor remains constant. Though the current IZIZ through Zener diode increases it maintains a constant output voltage VZVZ, which maintains the load voltage constant.

Case 3 − If the input voltage ViVi increases, then the current ISIS through the series resistor RS increases. This increases the voltage drop across the resistor, i.e. VSVS increases. Though the current through Zener diode IZIZ increases with this, the voltage across Zener diode VZVZ remains constant, keeping the output load voltage constant.

Case 4 − If the input voltage decreases, the current through the series resistor decreases which makes the current through Zener diode IZIZ decreases. But the Zener diode maintains output voltage constant due to its property.

Limitations of Zener Voltage Regulator

There are a few limitations for a Zener voltage regulator. They are −

- It is less efficient for heavy load currents.
- The Zener impedance slightly affects the output voltage.

Hence a Zener voltage regulator is considered effective for low voltage applications. Now, let us go through the other types of voltage regulators, which are made using transistors.

1.5.2 Transistor Series Voltage Regulator

This regulator has a transistor in series to the Zener regulator and both in parallel to the load. The transistor works as a variable resistor regulating its collector emitter voltage in order to maintain the output voltage constant. The figure below shows the transistor series voltage regulator.

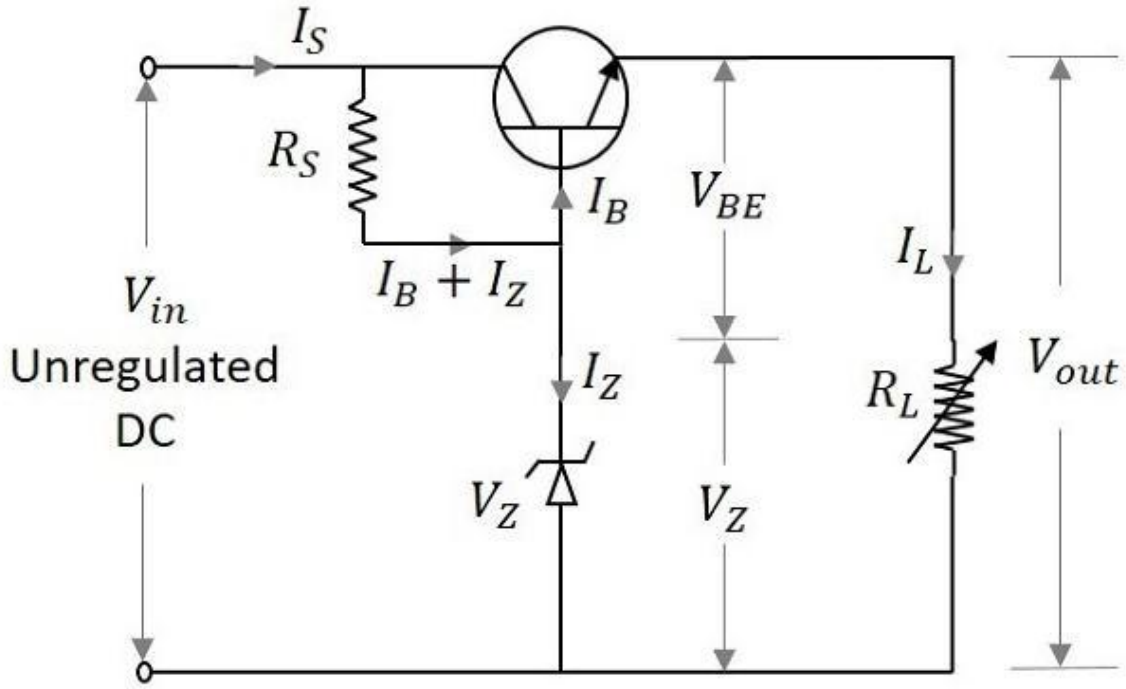


Fig 1.18 Transistor Series Voltage Regulator

With the input operating conditions, the current through the base of the transistor changes. This effects the voltage across the base emitter junction of the transistor VBEVBE. The output voltage is maintained by the Zener voltage VZVZ which is constant. As both of them are maintained equal, any change in the input supply is indicated by the change in emitter base voltage VBEVBE.

Hence the output voltage Vo can be understood as

$V_O=V_Z+V_{BE}V_O=V_Z+V_{BE}$

Working of Transistor Series Voltage Regulator

The working of a series voltage regulator shall be considered for input and load variations. If the input voltage is increased, the output voltage also increases. But this in turn makes the voltage across the collector base junction $V_{BE}V_{BE}$ to decrease, as the Zener voltage remains constant. The conduction decreases as the resistance across emitter collector region increases. This further increases the voltage across collector emitter junction VCE thus reducing the output voltage V_O. This will be similar when the input voltage decreases.

When the load changes occur, which means if the resistance of the load decreases, increasing the load current I_L, the output voltage V_O decreases, increasing the emitter base voltage V_{BE}. With the increase in the emitter base voltage the conduction increases reducing the emitter collector resistance. This in turn increases the input current which compensates the decrease in the load resistance. This will be similar when the load current increases.

Limitations of Transistor Series Voltage Regulator

Transistor Series Voltage Regulators have the following limitations −

- The voltagesV_{BE} and V_ZV_Z are affected by the rise in temperature.
- No good regulation for high currents is possible.
- Power dissipation is high.
- Power dissipation is high.
- Less efficient.

To minimize these limitations, transistor shunt regulator is used.

1.5.3 Transistor Shunt Voltage Regulator

A transistor shunt regulator circuit is formed by connecting a resistor in series with the input and a transistor whose base and collector are connected by a Zener diode that regulates, both in parallel with the load. The figure below shows the circuit diagram of a transistor shunt regulator.

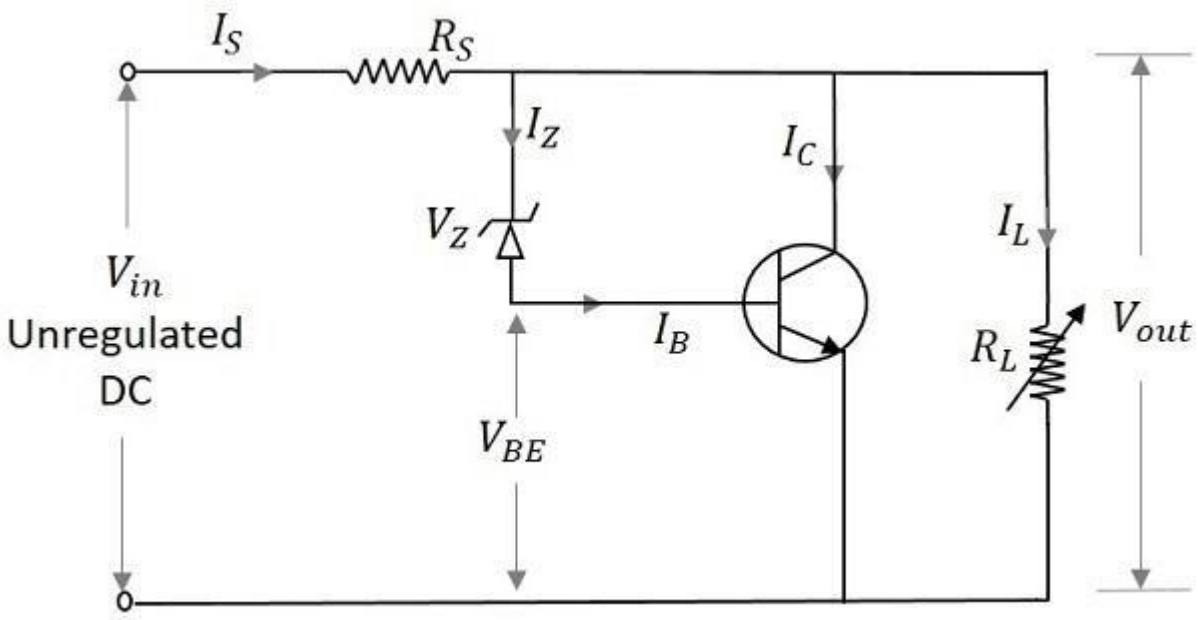


Fig 1.19 Transistor Shunt Voltage Regulator

1.5.4 Working of Transistor Shunt Voltage Regulator

If the input voltage increases, the V_{BE} and V_O also gets increased. But this happens initially. Actually when V_{in} increases, the current also increases. This current when flows through RS, causes a voltage drop V_SVS across the series resistor, which also gets increased with V_{in}. But this makes V_O to decrease. Now this decrease in Vo compensates the initial increase maintaining it to be constant. Hence Vo is maintained constant. If the output voltage decreases instead, the reverse happens.

If the load resistance decreases, there should be decrease in the output voltage Vo. The current through the load increases. This makes the base current and collector current of the transistor to decrease. The voltage across the series resistor becomes low, as the current flows heavily. The input current will be constant.

The output voltage appears will be the difference between the applied voltage ViVi and the series voltage drop Vs. Hence the output voltage will be increased to compensate the initial decrease and hence maintained constant. The reverse happens if the load resistance increases.

1.6 SWITCHED-MODE POWER SUPPLY

A switched-mode power supply (SMPS) is an electronic circuit that converts power using switching devices that are turned on and off at high frequencies, and storage components such as inductors or capacitors to supply power when the switching device is in its non-conduction state. Switching power supplies have high efficiency and are widely used in a

variety of electronic equipment, including computers and other sensitive equipment requiring stable and efficient power supply.

A switched-mode power supply is also known as a switch-mode power supply or switching-mode power supply. Switched-mode power supplies are classified according to the type of input and output voltages. The four major categories are:

- AC to DC
- DC to DC
- DC to AC
- AC to AC

A basic isolated AC to DC switched-mode power supply consists of:

- Input rectifier and filter
- Inverter consisting of switching devices such as MOSFETs
- Transformer
- Output rectifier and filter
- Feedback and control circuit

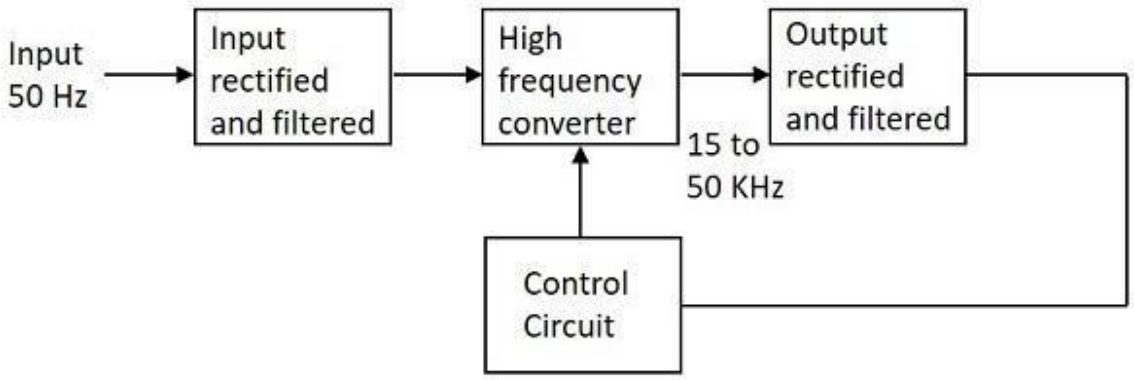


Fig 1.20 Switched-Mode Power Supply

Input Stage

The AC input supply signal 50 Hz is given directly to the rectifier and filter circuit combination without using any transformer. This output will have many variations and the capacitance value of the capacitor should be higher to handle the input fluctuations. This unregulated dc is given to the central switching section of SMPS.

Switching Section

A fast switching device such as a Power transistor or a MOSFET is employed in this section, which switches ON and OFF according to the variations and this output is given to the primary of the transformer present in this section. The transformer used here are much

smaller and lighter ones unlike the ones used for 60 Hz supply. These are much efficient and hence the power conversion ratio is higher.

Output Stage The output signal from the switching section is again rectified and filtered, to get the required DC voltage. This is a regulated output voltage which is then given to the control circuit, which is a feedback circuit. The final output is obtained after considering the feedback signal.

Control Unit This unit is the feedback circuit which has many sections. Let us have a clear understanding about this from The following figure.

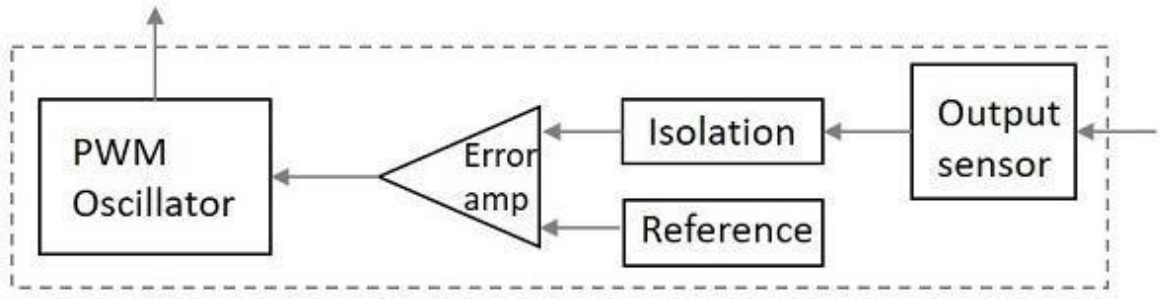


Fig 1.21 Control Unit

The above figure explains the inner parts of a control unit. The output sensor senses the signal and joins it to the control unit. The signal is isolated from the other section so that any sudden spikes should not affect the circuitry. A reference voltage is given as one input along with the signal to the error amplifier which is a comparator that compares the signal with the required signal level. By controlling the chopping frequency the final voltage level is maintained. This is controlled by comparing the inputs given to the error amplifier, whose output helps to decide whether to increase or decrease the chopping frequency. The PWM oscillator produces a standard PWM wave fixed frequency.

We can get a better idea on the complete functioning of SMPS by having a look at the following

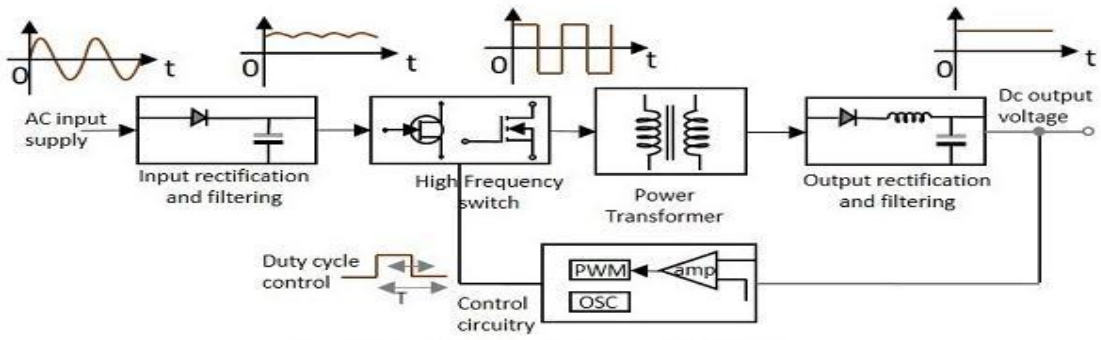


Fig 1.22 Functional Block Diagram of SMPS

The input DC supply from a rectifier or battery is fed to the inverter where it is turned on and off at high frequencies of between 20 KHz and 200 KHz by the switching MOSFET or power transistors. The high-frequency voltage pulses from the inverter are fed to the transformer primary winding, and the secondary AC output is rectified and smoothed to produce the required DC voltages. A feedback circuit monitors the output voltage and instructs the control circuit to adjust the duty cycle to maintain the output at the desired level.

The SMPS is mostly used where switching of voltages is not at all a problem and where efficiency of the system really matters. There are few points which are to be noted regarding SMPS. They are

- SMPS circuit is operated by switching and hence the voltages vary continuously.
- The switching device is operated in saturation or cut off mode.
- The output voltage is controlled by the switching time of the feedback circuitry.
- Switching time is adjusted by adjusting the duty cycle.
- The efficiency of SMPS is high because, instead of dissipating excess power as heat, it continuously switches its input to control the output.

Disadvantages

There are few disadvantages in SMPS, such as

- The noise is present due to high frequency switching.
- The circuit is complex.
- It produces electromagnetic interference.

Advantages

The advantages of SMPS include,

- The efficiency is as high as 80 to 90%
- Less heat generation; less power wastage.
- Reduced harmonic feedback into the supply mains.
- The device is compact and small in size.
- The manufacturing cost is reduced.
- Provision for providing the required number of voltages.

Applications There are many applications of SMPS. They are used in the motherboard of computers, mobile phone chargers, HVDC measurements, battery chargers, central power distribution, motor vehicles, consumer electronics, laptops, security systems, space stations, etc.

Types of SMPS

SMPS is the Switched Mode Power Supply circuit which is designed for obtaining the regulated DC output voltage from an unregulated DC or AC voltage. There are four main types of SMPS such as

- DC to DC Converter
- AC to DC Converter
- Fly back Converter
- Forward Converter

The AC to DC conversion part in the input section makes the difference between AC to DC converter and DC to DC converter. The Fly back converter is used for Low power applications. Also there are Buck Converter and Boost converter in the SMPS types which decrease or increase the output voltage depending upon the requirements. The other type of SMPS include Self-oscillating fly-back converter, Buck-boost converter, Cuk, Sepic, etc.

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UNIT - 2
Electronic Circuits-SECA1305

2.1 NEED FOR TRANSISTOR BIASING

If the o/p signal must be a faithful reproduction of the i/p signal, the transistor must be operated in active region. That means an operating point has to be established in this region . To establish an operating point (proper values of collector current Ic and collector to emitter voltage VCE) appropriate supply voltages and resistances must be suitably chosen in the ckt. This process of selecting proper supply voltages and resistance for obtaining desired operating point or Q point is called as biasing and the ckt used for transistor biasing is called as biasing ckt.

There are four conditions to be met by a transistor so that it acts as a faithful ampr:

1) Emitter base junction must be forward biased (VBE=0.7Vfor Si, 0.2V for Ge) and collector base junction must be reverse biased for all levels of i/p signal.

2) Vce voltage should not fall below VCE (sat) (0.3V for Si, 0.1V for Ge) for any part of the i/p signal. For VCE less than VCE (sat) the collector base junction is not probably reverse biased.

3) The value of the signal Ic when no signal is applied should be at least equal to the max. collector current t due to signal alone.

4) Max. rating of the transistor Ic(max), VCE (max) and PD(max) should not be exceeded at any value of i/p signal.

Consider the fig shown in fig1. If operating point is selected at A, A represents a condition when no bias is applied to the transistor i.e, Ic=0, VCE =0. It does not satisfy the above said conditions necessary for faithful amplification.

Point C is too close to PD(max) curve of the transistor. Therefore the o/p voltage swing in the positive direction is limited.

Point B is located in the middle of active region .It will allow both positive and negative half cycles in the o/p signal. It also provides linear gain and larger possible o/p voltages and currents. Hence operating point for a transistor amplifier is selected to be in the middle of active region.

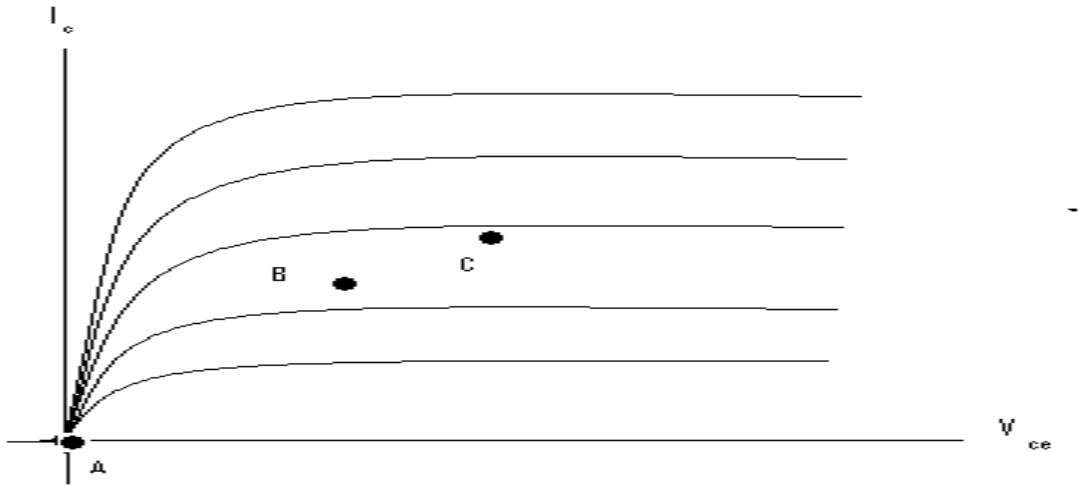
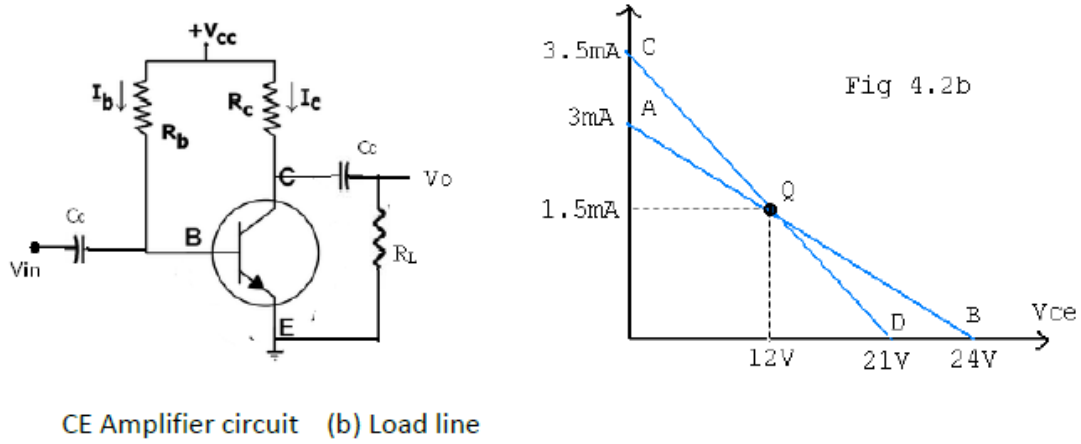


Fig 2.1 Transistor output characteristics

2.2 DC LOAD LINE

Referring to the biasing circuit of fig 4.2a, the values of VCC and RC are fixed and Ic and VCE are dependent on RB. Applying Kirchhoff's voltage law to the collector circuit in fig. 4.2a, we get

$$Vcc = IcRc + Vce$$



CE Amplifier circuit (b) Load line

Fig 2.2 DC load line

The straight line represented by AB in fig4.2b is called the dc load line. The coordinates of the end point A are obtained by substituting VCE =0 in the above equation. Therefore The coordinates of A are VCE =0 and the coordinates of B are obtained by substituting Ic=0 in the above equation. Then Vce = Vcc. Therefore the coordinates of B are VCE =Vcc and Ic=0. Thus the dc load line AB can be drawn if the values of Rc and Vcc are known.

As shown in the fig4.2b, the optimum POINT IS LOCATED AT THE MID POINT OF THE MIDWAY BETWEEN a AND b. In order to get faithful amplification, the Q point must be well within the active region of the transistor.

Even though the Q point is fixed properly, it is very important to ensure that the operating point remains stable where it is originally fixed. If the Q point shifts nearer to either A or B, the output voltage and current get clipped, thereby o/p signal is distorted.

In practice, the Q-point tends to shift its position due to any or all of the following three main factors.

1) Reverse saturation current, Ico, which doubles for every 10oC raise in temperature

2) Base emitter Voltage ,VBE, which decreases by 2.5 mV per oC

3) Transistor current gain, hFE or β which increases with temperature.

If base current IB is kept constant since IB is approximately equal to Vcc/RB. If the transistor is replaced by another one of the same type, one cannot ensure that the new transistor will have identical parameters as that of the first one. Parameters such as β vary over a range. This results in the variation of collector current Ic for a given IB. Hence , in the o/p characteristics, the spacing between the curves might increase or decrease which leads to the shifting of the Q-point to a location which might be completely unsatisfactory.

2.3 AC LOAD LINE

After drawing the dc load line, the operating point Q is properly located at the center of the dc load line. This operating point is chosen under zero input signal condition of the circuit. Hence the ac load line should also pas through the operating point Q. The effective ac load resistance Rac, is a combination of RC parallel to RL i.e. So the slope of the ac load line CQD. To draw the ac load line, two end points, I.e. VCE(max) and IC(max) when the signal is applied are required

$V_{CE(\max)} = V_{CEQ} + I_{CQ} R_{ac}$, which locates point D on the Vce axis.

$I_{c(\max))} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$, which locates the point C on the I_C axis.

By joining points c and D, ac load line CD is constructed. As RC > Rac, The dc load line is less steep than ac load line.

2.4 STABILITY FACTOR (S):

The rise of temperature results in increase in the value of transistor gain β and the leakage current Ico. So, IC also increases which results in a shift in operating point. Therefore, The biasing network should be provided with thermal stability. Maintenance of the operating

point is specified by S, which indicates the degree of change in operating point due to change in temperature.

The extent to which IC is stabilized with varying IC is measured by a stability factor S

$$S = \frac{\partial I_c}{\partial I_{co}} \approx \frac{dI_c}{dI_{co}} \approx \frac{\Delta I_c}{\Delta I_{co}} \beta \text{ and } I_B \text{ constant}$$

For CE configuration $I_C = \beta I_B + (1+\beta) I_{CO}$

Differentiate the above equation w.r.t I_C, We get

$$1 = \beta \frac{dI_B}{dI_C} + (1+\beta) \frac{dI_{co}}{dI_c}$$

$$\therefore \left(1 - \beta \frac{dI_B}{dI_C}\right) = \frac{(\beta+1)}{S}$$

$$\therefore S = \frac{1+\beta}{1-\beta \frac{dI_B}{dI_C}}$$

S should be small to have better thermal stability.

Stability factor S' and S'':

S' is defined as the rate of change of I_C with V_{BE}, keeping I_C and V_{BE} constant.

$$S' = \frac{\partial I_c}{\partial V_{BE}}$$

S'' is defined as the rate of change of I_C with β, keeping I_{CO} and V_{BE} constant.

$$S'' = \frac{\partial I_c}{\partial \beta}$$

2.5 METHODS OF TRANSISTOR BIASING

2.5.1 Fixed bias (base bias)

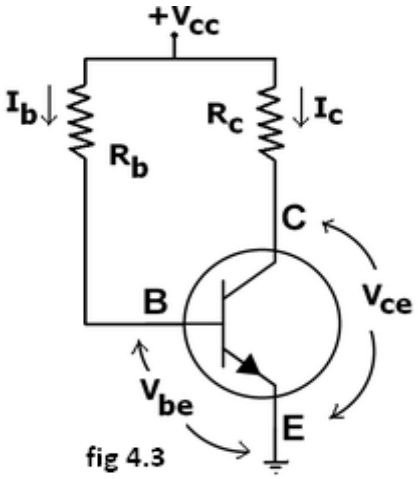


Fig 2.3 Fixed Biasing Circuit

This form of biasing is also called *base bias*. In the fig 4.3 shown, the single power source (for example, a battery) is used for both collector and base of a transistor, although separate batteries can also be used. In the given circuit, Vcc = IBRB + Vbe . Therefore, IB = (Vcc - Vbe)/RB Since the equation is independent of current ICR, dIB//dICR =0 and the stability

factor is given by the equation….. reduces to S=1+β .Since β is a large quantity, this is very poor biasing circuit. Therefore in practice the circuit is not used for biasing. For a given transistor, Vbe does not vary significantly during use. As Vcc is of fixed value, on selection of Rthe base current IB is fixed. Therefore this type is called *fixed bias* type of circuit. Also for given circuit, Vcc = ICRC + Vce Therefore, Vce = Vcc - ICRC

Merits:

It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (RB).

A very small number of components are required.

Demerits:

The collector current does not remain constant with variation in temperature or power supply voltage. Therefore the operating point is unstable.

Changes in Vbe will change IB and thus cause RE to change. This in turn will alter the gain of the stage.

When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.

2.5.2 EMITTER-FEEDBACK BIAS:

The emitter feedback bias circuit is shown in the fig 4.4. The fixed bias circuit is modified by attaching an external resistor to the emitter. This resistor introduces negative feedback that stabilizes the Q-point. From Kirchhoff's voltage law, the voltage across the base resistor is VRb = VCC - IeRe - Vbe. From Ohm's law, the base current is Ib = VRb / Rb.

The way feedback controls the bias point is as follows. If Vbe is held constant and temperature increases, emitter current increases. However, a larger Ie increases the emitter voltage Ve = IeRe, which in turn reduces the voltage VRb across the base resistor. A lower base-resistor voltage drop reduces the base current, which results in less collector current because Ic = ß IB. Collector current and emitter current are related by Ic = α Ie with α ≈ 1, so increase in emitter current with temperature is opposed, and operating point is kept stable. Similarly, if the transistor is replaced by another, there may be a change in IC (corresponding to change in β-value, for example). By similar process as above, the change is negated and operating point kept stable. For the given circuit, IB = (VCC - Vbe)/(RB + (β+1)RE).

Merits:

The circuit has the tendency to stabilize operating point against changes in temperature and β-value.

Demerits:

In this circuit, to keep IC independent of β the following condition must be met:

$$I_C = \beta I_B = \frac{\beta(V_{CC} - V_{be})}{R_B + (\beta + 1)R_E} \approx \frac{(V_{CC} - V_{be})}{R_E}$$

which is approximately the case if (β + 1)R_E >> R_B.

large, or making RB very low. If RE is of large value, high VCC is necessary. This increases cost as well as precautions necessary while handling. If RB is low, a separate low voltage supply should be used in the base circuit. Using two supplies of different voltages is impractical. In addition to the above, RE causes ac feedback which reduces the voltage gain of the amplifier.

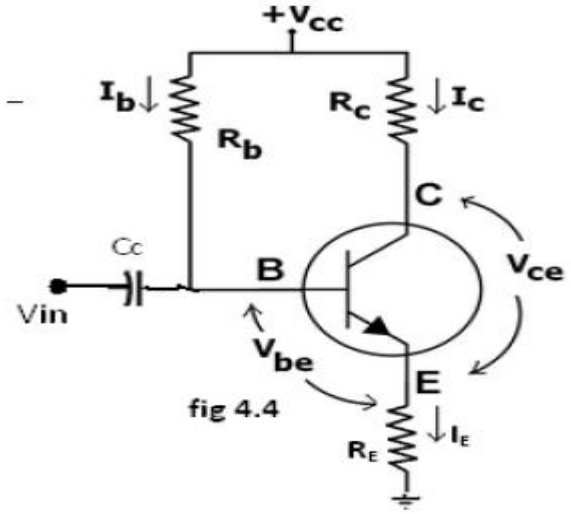


Fig 2.4 Self Biasing Circuit

2.5.3 COLLECTOR TO BASE BIAS OR COLLECTOR FEED-BACK BIAS:

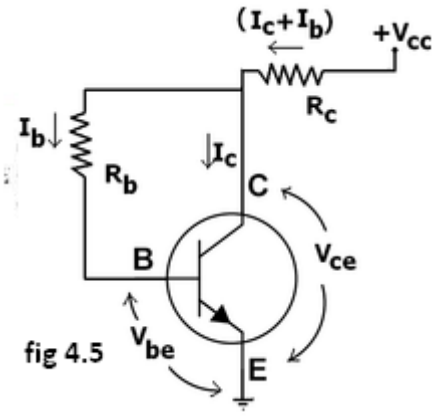


Fig 2.5 Collector to Base Biasing Circuit

This configuration shown in fig 4.5 employs negative feedback to prevent thermal runaway and stabilize the operating point. In this form of biasing, the base resistor R_B is connected to the collector instead of connecting it to the DC source V_{cc}. So any thermal runaway will induce a voltage drop across the R_C resistor that will throttle the transistor's base current

From Kirchhoff's voltage law, the voltage V_{R_b} across the base resistor R_b is

$$V_{R_b} = V_{cc} - \overbrace{(I_c + I_b)R_c}^{\text{Voltage drop across } R_c} - \overbrace{V_{be}}^{\text{Voltage at base}}.$$

By the Ebers–Moll model, $I_c = \beta I_b$, and so

$$V_{R_b} = V_{cc} - (\overbrace{\beta I_b}^{I_c} + I_b)R_c - V_{be} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

From Ohm's law, the base current $I_b = V_{R_b}/R_b$, and so

$$\overbrace{I_b R_b}^{V_{R_b}} = V_{cc} - I_b(\beta + 1)R_c - V_{be}.$$

Hence, the base current I_b is

$$I_b = \frac{V_{cc} - V_{be}}{R_b + (\beta + 1)R_c}$$

If *V*be is held constant and temperature increases, then the collector current *I*c increases. However, a larger *I*c causes the voltage drop across resistor *R*c to increase, which in turn reduces the voltage

across the base resistor *R*b. A lower base-resistor voltage drop reduces the base current *I*b, which results in less collector current *I*c. Because an increase in collector current with temperature is opposed, the operating point is kept stable.

Merits:

Circuit stabilizes the operating point against variations in temperature and β (i.e. replacement of transistor)

Demerits:

In this circuit, to keep *I*c independent of β, the following condition must be met:

$$I_c = \beta I_b = \frac{\beta(V_{cc} - V_{be})}{R_b + R_c + \beta R_c} \approx \frac{(V_{cc} - V_{be})}{R_c}$$

which is the case when

$$\beta R_c \gg R_b.$$

As β-value is fixed (and generally unknown) for a given transistor, this relation can be satisfied either by keeping *R*c fairly large or making *R*b very low.

If *R*c is large, a high *V*cc is necessary, which increases cost as well as precautions necessary while handling.

If *R*b is low, the reverse bias of the collector–base region is small, which limits the range of collector voltage swing that leaves the transistor in active mode.

The resistor *R*b causes an AC feedback, reducing the voltage gain of the amplifier. This undesirable effect is a trade-off for greater Q-point stability.

Usage: The feedback also decreases the input impedance of the amplifier as seen from the base, which can be advantageous. Due to the gain reduction from feedback, this biasing form is used only when the trade-off for stability is warranted.

2.2.4 COLLECTOR –EMITTER FEEDBACK BIAS

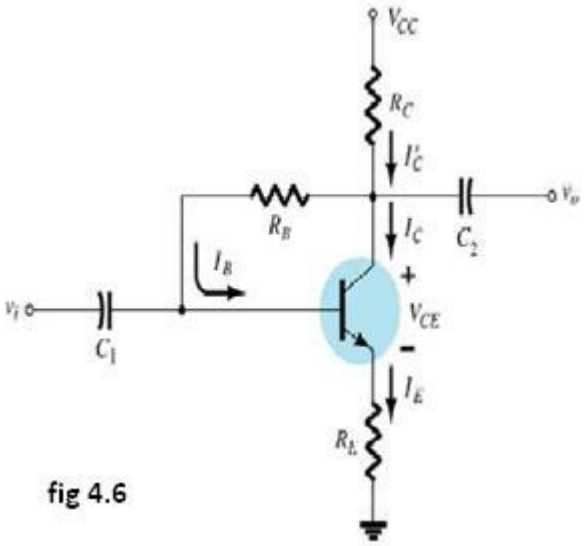


fig 4.6

Fig 2.6 Collector –Emitter Feedback Bias

The above fig2.2.4 shows the collector –emitter feedback bias circuit that can be obtained by applying both the collector feedback and emitter feedback. Here the collector feedback is provided by connecting a resistance RB from the collector to the base and emitter feedback is

provided by connecting an emitter Re from emitter to ground. Both feed backs are used to control collector current and base current IB in the opposite direction to increase the stability as compared to the previous biasing circuits.

2.2.5 VOLTAGE DIVIDER BIAS OR SELF BIAS OR EMITTER BIAS

The voltage divider as shown in the fig 4.7 is formed using external resistors R1 and R2. The voltage across R2 forward biases the emitter junction. By proper selection of resistors R1 and R2, the operating point of the transistor can be made independent of β. In this circuit, the voltage divider holds the base voltage fixed independent of base current provided the divider current is large compared to the base current. However, even with a fixed base voltage, collector current varies with temperature (for example) so an emitter resistor is added to stabilize the Q-point, similar to the above circuits with emitter resistor.

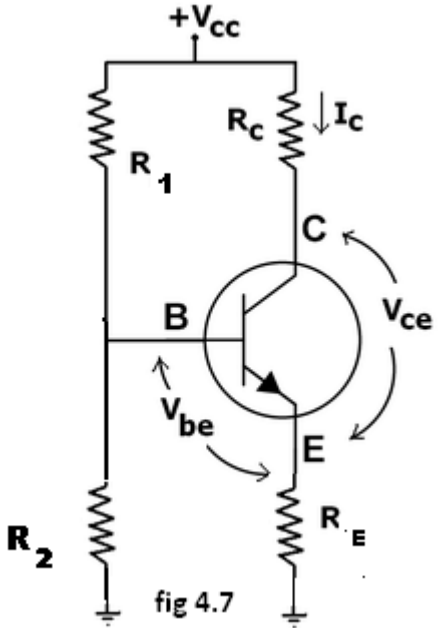


Fig 2.7 Voltage Divider Biasing Circuit

In this circuit the base voltage is given by:

$$V_B = \text{voltage across } R_2 = V_{cc}\frac{R_2}{(R_1+R_2)} - I_B\frac{R_1R_2}{(R_1+R_2)}$$

$$\approx V_{cc}\frac{R_2}{(R_1+R_2)} \text{ provided } I_B << I_2 = V_B/R_2.$$

Also $V_B = V_{be} + I_E R_E$

For the given circuit,

$$I_B = \frac{\frac{V_{CC}}{1+R_1/R_2} - V_{be}}{(\beta+1)R_E + R_1 \parallel R_2}.$$

Let the current in resistor R1 is I1 and this is divided into two parts – current through base and resistor R2. Since the base current is very small so for all practical purpose it is assumed that I1 also flows through R2, so we have

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$$V_2 = \frac{V_{CC}}{R_1 + R_2} \cdot R_2$$

Applying KVL in the circuit, we have

$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

$$I_C = \frac{V_2 - V_{BE}}{R_E} \quad \because I_C \cong I_E$$

$$I_C = \frac{\frac{V_{CC}}{R_1 + R_2} \cdot R_2 - V_{BE}}{R_E}$$

It is apparent from above expression that the collector current is independent of ? thus the stability is excellent. In all practical cases the value of VBE is quite small in comparison to the V2, so it can be ignored in the above expression so the collector current is almost independent of the transistor parameters thus this arrangement provides excellent stability.

Again applying KVL in collector circuit, we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$\because I_C \cong I_E$$

$$\therefore V_{CC} = I_C R_C + V_{CE} + I_C R_E$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

The resistor RE provides stability to the circuit. If the current through the collector rises, the voltage across the resistor RE also rises. This will cause VCE to increase as the voltage V2 is independent of collector current. This decreases the base current, thus collector current increases to its former value.

Stability factor for such circuit arrangement is given by

$$S = \frac{(1+\beta)(R_{eq} + R_E)}{R_{eq} + R_E(1+\beta)}$$

$$R_{eq} = R_1 || R_2$$

$$S = \frac{(1+\beta)\left(1 + \frac{R_{eq}}{R_E}\right)}{\frac{R_{eq}}{R_E} + 1 + \beta}$$

If Req/RE is very small compared to 1, it can be ignored in the above expression thus we have

$$S = \frac{1+\beta}{1+\beta} = 1$$

Which is excellent since it is the smallest possible value for the stability. In actual practice the value of stability factor is around 8-10, since Req/RE cannot be ignored as compared to 1.

Merits:

Unlike above circuits, only one dc supply is necessary.

Operating point is almost independent of β variation.

Operating point stabilized against shift in temperature. Demerits:

In this circuit, to keep IC independent of β the following condition must be met:

which is approximately the case if where R1 || R2 denotes the equivalent resistance of R1 and R2 connected in parallel.

As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE fairly large, or making R1||R2 very low.

If RE is of large value, high VCC is necessary. This increases cost as well as precautions necessary while handling.

If R1 || R2 is low, either R1 is low, or R2 is low, or both are low. A low R1 raises VB closer to VC, reducing the available swing in collector voltage, and limiting how large RC can be made without driving the transistor out of active mode. A low R2 lowers Vbe, reducing the allowed collector current. Lowering both resistor values draws more current from the power supply and lowers the input resistance of the amplifier as seen from the base.

AC as well as DC feedback is caused by RE, which reduces the AC voltage gain of the amplifier. A method to avoid AC feedback while retaining DC feedback is discussed below.

Usage: The circuit's stability and merits as above make it widely used for linear circuits.

2.3 BIAS COMPENSATION USING DIODE AND TRANSISTOR

The various biasing circuits considered use some type of negative feedback to stabilize the operation point. Also, diodes, thermistors and sensistors can be used to compensate for **variations in current.**

2.3.1 DIODE COMPENSATION: The following fig4.8 shows a transistor amplifier with a diode D connected across the baseemitter The following fig4.8 shows a transistor amplifier with a diode D connected across the base-emitter junction for compensation of change in collector saturation current ICO. The diode is of the same material as the transistor and it is reverse biased by e the emitter-base junction voltage VBE, allowing the diode reverse saturation current IO to flow through diode D. The base current IB=I-IO.

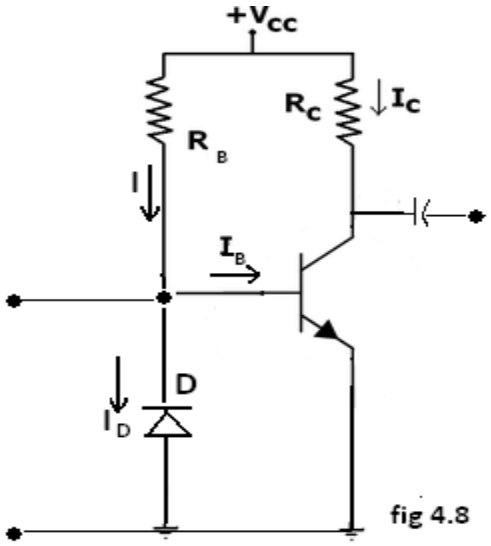


Fig 2.8 Diode Compensation circuit

As long as temperature is constant, diode D operates as a resistor. As the temperature increases, ICO of the transistor increases. Hence, to compensate for this, the base current IB should be decreased. The increase in temperature will also cause the leakage current IO through D to increase and thereby decrease the base current IB. This is the required action to keep Ic constant. This type of bias compensation does not need a change in Ic to effect the change in IC, as both IO and ICO can track almost equally according to the change in temperature.

2.3.2 THERMISTOR COMPENSATION:

The following fig 2.9 a thermistor R_T, having a negative temperature coefficient is connected in parallel with R_2. The resistance of thermistor decreases exponentially with increase of temperature. An increase of temperature will decrease the base voltage V_{BE}, reducing I_B and I_C. Fig

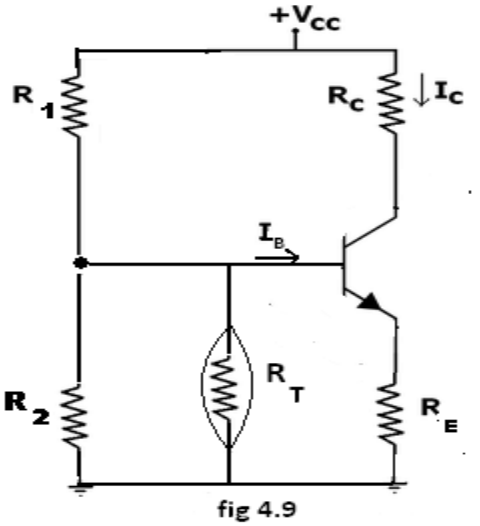


Fig 2.9 Thermistor Compensation

2.3.3 SENSISTOR COMPENSATION:

In the following fig4.10 shown a sensistor Rs having a positive temperature coefficient is connected across R_1 or R_E. Rs increases with temperature. As the temperature increases, the equivalent resistance of the parallel combination of R1 and Rs also increases and hence V_{BE} decreases, reducing I_B and Ic. This reduced Ic compensates for increased Ic caused by the increase in V_{BE}, I_{CO} and β due to temperature.

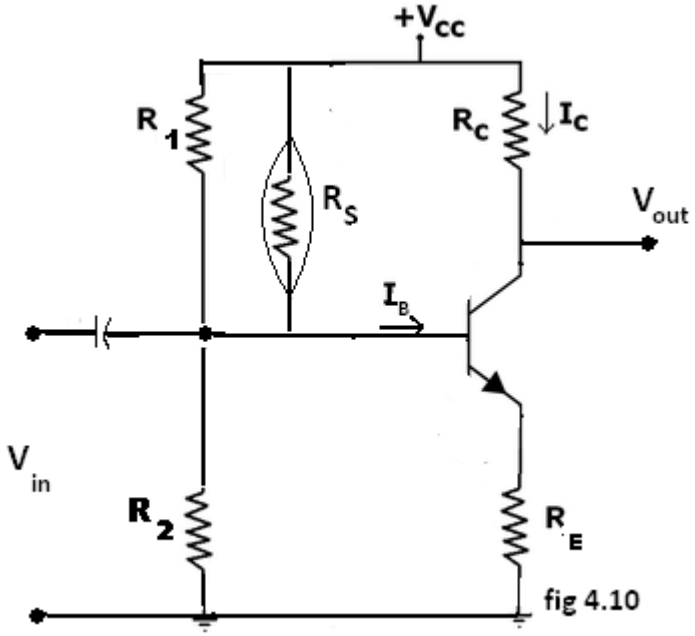


Fig 2.10 Thermistor Compensation

2.4 THERMAL RUNAWAY AND THERMAL STABILITY

The collector current for the CE circuit is given by The three variables in the equation, β, , and increases with rise in temperature. In particular, the reverse saturation current or leakage current changes greatly with temperature. Specifically it doubles for every 10oC rise in temperature. The collector current causes the collector base junction temperature to rise which in turn, increase , as a result will increase still further, which will further rise the temperature at the collector base junction. This process will become cumulative leading at the collector base junction. This process will become cumulative leading to *"thermal runaway"*. Consequently, the ratings of the transistor are exceeded which may destroy the transistor itself.

The collector is made larger in size than the emitter in order to help the heat developed at the collector junction. However if the circuit is designed such that the base current is made to decrease automatically with rise in temperature, then the decrease in will compensate for increase in the

, keeping

almost constant.

2.4.1 THERMAL RESISTANCE

Consider transistor used in a circuit where the ambient temperature of the air around the transistor is TAoC and the temperature of the collector-base junction of the transistor is TJoC. Due to heating within the transistor TJ is higher than TA. As the temperature difference TJ- TA is greater, the power dissipated in the transistor, PD will be greater, i.e, TJ- TA PD The equation can be written as TJ- TA PD. , where is the constant of proportionality and is called the Thermal resistance. Rearranging the above equation = TJ- TA /PD. Hence is measured in oC/W which may be as small as 0.2 oC/W for a high power transistor that has an efficient heat sink or up to 1000oC/W for small signal, low power transistor which have no cooling provision. As Θ represents total thermal resistance from a transistor junction to the ambient temperature, it is referred to as ΘJ-A. However, for power transistors, thermal resistance is given form junction to case, ΘJ-C.

The amount resistance from junction to ambience is considered to consist of 2 parts. ΘJ-A = ΘJ-C - ΘC-A.

Which indicates the heat dissipated in the junction must make its way to the surrounding air through two series paths from junction to case and from case to air. Hence the power dissipated.

If the effective surface area of the transistor case could be increased, the resistance to heat flows, or could be increased ΘC-A, could be decreased. This can be achieved by the use of a heat sink.

The heat sink is a relatively large, finned, usually black metallic heat conducting device in close contact with transistor case or flange. Many versions of heat sink exist depending upon the shape and size of the transistor. Larger the heat sink smaller is the thermal resistance ΘHS-A.

This thermal resistance is not added to ΘC-A in series, but is instead in parallel with it and if ΘHS-A is much less than ΘC-A, then ΘC-A will be reduced significantly, thereby improving the dissipation capability of the transistor. Thus

Θ J-A

=Θ J-C + Θ C-A|| ΘHS-A.

2.4.2 CONDITION FOR THERMAL STABILITY

For preventing thermal runaway, the required condition I the rate at which the heat is released at the collector junction should not exceed the rate at which the heat can be dissipated under steady state condition. Hence the condition to be satisfied to avoid thermal runaway is given

$$\frac{\partial P_C}{\partial T_j} < \frac{1}{\theta}$$

If the circuit is properly designed, then the transistor cannot runaway below a specified ambient temperature or even under any conditions.

In the self biased circuit the transistor is biased in the active region. The power generated at the junction without any signal is

$P_C = I_C V_{CB} \approx I_C V_{CE}$

Let us assume that the quiescent collector and the emitter currents are equal. Then

$$P_C = I_C V_{CC} - I_C^2 (R_E + R_C) \ldots\ldots\ldots\ldots$$

The condition to prevent thermal runaway can be written as

$$\frac{\partial P_C}{\partial I_C} \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta} \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

As Θ and $\frac{\partial I_C}{\partial T_j}$ are positive, $\frac{\partial P_C}{\partial I_C}$ should be negative in order to satisfy the above condition.

Differentiating equation (1) w.r.t I_C we get

$$\frac{\partial P_C}{\partial I_C} = V_{CC} - 2I_C (R_E + R_C) \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

Hence to avoid thermal runaway it is necessary that

$$I_C > \frac{V_{CC}}{2(R_E + R_C)} \ldots\ldots\ldots\ldots\ldots\ldots\ldots (4)$$

SinceVCE=VCC-IC(RE+RC) then eq(4) implies that VCE<VCC/2. IF the inequality of eq(4) is not satisfied and VCE<VCC/2, then from eq(3), $\frac{\partial P_C}{\partial I_C}$ is positive., and the corresponding eq(2) should be satisfied. Otherwise thermal runaway will occur.

2.5 BJT HYBRID MODEL

Small signal low frequency transistor Models:

All the transistor amplifiers are two port networks having two voltages and two currents. The positive directions of voltages and currents are shown in

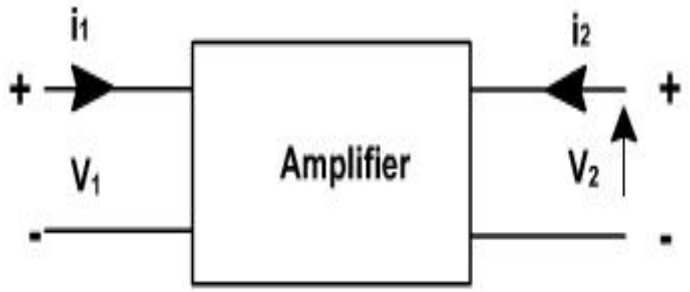


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Fig 2.11 Two port network

A two - port network is represented by four external variables: voltage V1 and current I1 at the input port, and voltage V2 and current I2 at the output port, so that the two -port network can be treated as a black box modeled by the relationships between the four variables,V1,V2, I1,I2 . Out of four variables two can be selected as are independent variables and two are dependent variables.The dependent variables can be expressed interns of independent variables. This leads to various two port parameters out of which the following three are important:

1. Impedance parameters (z - parameters)
2. Admittance parameters (y - parameters)
3. Hybrid parameters (h - parameters)

z-parameters

A two -port network can be described by z-parameters as

$$V_1 = Z_{11}I_1 + Z_{12}I_2$$
$$V_2 = Z_{21}I_1 + Z_{22}I_2$$

In matrix form, the above equation can be rewritten as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

Where

$$z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0}$$

Input impedance with output port open circuited

$$z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0}$$

Reverse transfer impedance with input port open circuited

$$z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0}$$

Forward transfer impedance with output port open circuited

$$z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0}$$

Output impedance with input port open circuited

Y -parameters

A two -port network can be described by Y-parameters as

$$I_1 = Y_{11}V_1 + Y_{12}V_2$$
$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$y_{11} = \left. \frac{I_1}{V_1} \right|_{V_2=0}$$

Input admittance with output port short circuited

$$y_{12} = \left. \frac{I_1}{V_2} \right|_{V_1=0}$$

Reverse transfer admittance with input port short circuited

$$y_{21} = \left. \frac{I_2}{V_1} \right|_{V_2=0}$$

Forward transfer admittance with output port short circuited

$$y_{22} = \left. \frac{I_2}{V_2} \right|_{V_1=0}$$

Output admittance with input port short circuited

Hybrid parameters (h-parameters)

If the input current I1 and output voltage V2 are taken as independent variables, the dependent variables V1 and I2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Where h_{11}, h_{12}, h_{21}, h_{22} are called as hybrid parameters.

$$h_{11} = \left. \frac{V_1}{I_1} \right|_{V_2=0}$$

Input impedence with o/p port short circuited

$$h_{12} = \left.\frac{V_1}{V_2}\right|_{I_1=0}$$

Reverse voltage transfer ratio with i/p port open circuited

$$h_{21} = \left.\frac{I_2}{I_1}\right|_{V_2=0}$$

Forward voltage transfer ratio with o/p port short circuited

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

output impedence with i/p port open circuited

THE HYBRID MODEL FOR TWO PORT NETWORK:

Based on the definition of hybrid parameters the mathematical model for two pert networks known as h-parameter model can be developed. The hybrid equations can be written as:

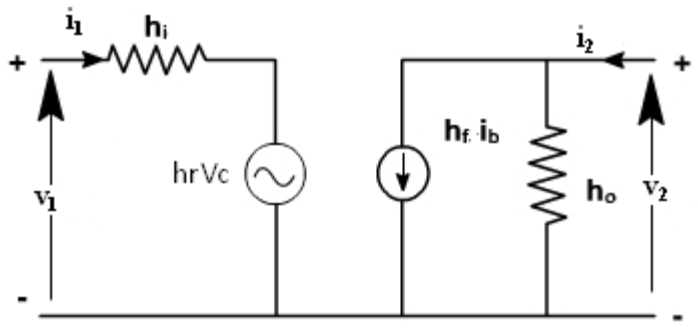
$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

(The following convenient alternative subscript notation is recommended
by the **IEEE Standards**:
***i*=11= input** ***o* = 22 = output**

***f* =21 = forward transfer *r* = 12 = reverse transfer)**

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff'svoltage and current laws for input and output ports.



If these parameters are specified for a particular configuration, then suffixes e,b or c are also included, e.g. h_{fe} ,h_{ib} are h parameters of common emitter and common collector amplifiers

Using two equations the generalized model of the amplifier can be drawn as shown in fig. 2.

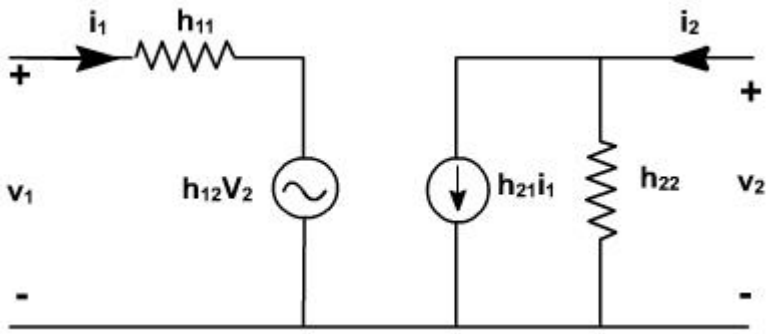


Fig. 2

TRANSISTOR HYBRID MODEL:

The hybrid model for a transistor amplifier can be derived as follow:

Let us consider CE configuration as show in fig. 3. The variables, i_B, i_C ,v_C, and v_B represent total instantaneous currents and voltages i_B and v_C can be taken as independent variables and v_B, I_C as dependent variables.

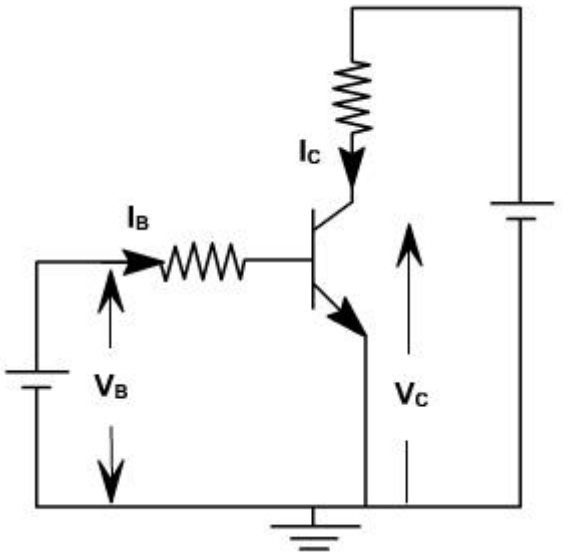


Fig. 3

$V_B = f1\ (i_B, v_C)$

$I_C = f2\ (i_B, v_C)$.

Using Taylor 's series expression, and neglecting higher order terms we obtain.

$$\Delta v_B = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} \Delta v_C$$

$$\Delta i_C = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_C} \Delta i_B + \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} \Delta v_C$$

The partial derivatives are taken keeping the collector voltage or base current constant. The Δv_B, Δv_C, Δi_B, Δi_C represent the small signal (incremental) base and collector current and voltage and can be represented as v_B, i_C, i_B, v_C

$$\therefore v_b = h_{ie}\, i_B + h_{re}\, v_C$$
$$i_C = h_{fe}\, i_B + h_{oe}\, v_b$$

where

$$h_{ie} = \left.\frac{\partial f_1}{\partial i_B}\right|_{v_c} = \left.\frac{\partial v_B}{\partial i_B}\right|_{v_c}; \qquad h_{re} = \left.\frac{\partial f_1}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

$$h_{fe} = \left.\frac{\partial f_2}{\partial i_B}\right|_{v_c} = \left.\frac{\partial i_C}{\partial i_B}\right|_{v_c}; \qquad h_{oe} = \left.\frac{\partial f_2}{\partial v_C}\right|_{i_B} = \left.\frac{\partial v_B}{\partial v_C}\right|_{i_B}$$

The model for CE configuration is shown in fig. 4.

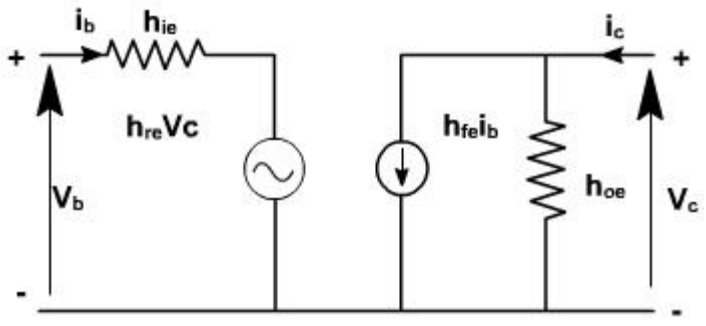


Fig. 4

To determine the four h-parameters of transistor amplifier, input and output characteristic are used. Input characteristic depicts the relationship between input voltage and input current with output voltage as parameter. The output characteristic depicts the relationship between output voltage and output current with input current as parameter. Fig. 5, shows the output characteristics of CE amplifier.

$$h_{fe} = \left.\frac{\partial i_C}{\partial i_B}\right|_{V_C} = \frac{i_{C2} - i_{C1}}{i_{b2} - i_{b1}}$$

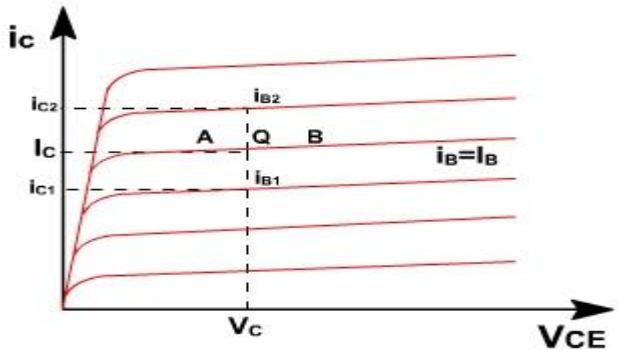


Fig. 5

The current increments are taken around the quiescent point Q which corresponds to $i_B = I_B$ and to the collector voltage $V_{CE} = V_C$

$$h_{oe} = \left.\frac{\partial i_C}{\partial V_C}\right|_{i_B}$$

The value of h_{oe} at the quiescent operating point is given by the slope of the output characteristic at the operating point (i.e. slope of tangent AB).

$$h_{ie} = \frac{\partial V_B}{\partial i_B} \approx \left.\frac{\Delta V_B}{\Delta i_B}\right|_{V_C}$$

h_{ie} is the slope of the appropriate input on fig. 6, at the operating point (slope of tangent EF at Q).

$$h_{re} = \frac{\partial V_B}{\partial V_C} = \left.\frac{\Delta V_B}{\Delta V_C}\right|_{I_B} = \frac{V_{B2} - V_{B1}}{V_{C2} - V_{C1}}$$

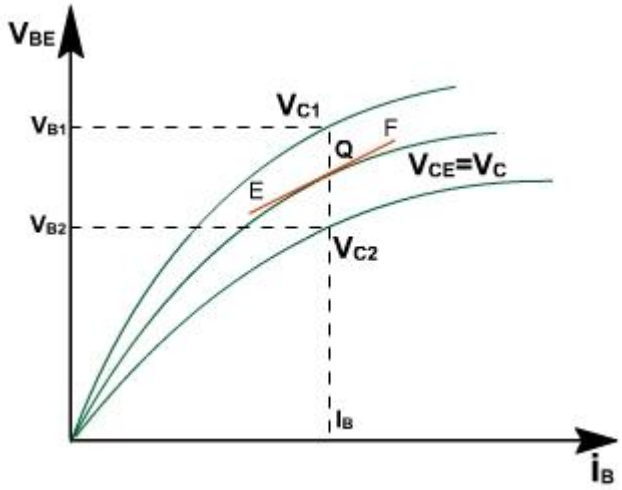


Fig. 6

A vertical line on the input characteristic represents constant base current. The parameter hre can be obtained from the ratio (V_{B2}– V_{B1}) and (V_{C2}– V_{C1}) for at Q.

Typical CE h-parametersof transistor 2N1573 are given below:

h_{ie} = 1000 ohm.
h_{re} = 2.5 * 10 –4
h_{fe} = 50
h_{oe} = 25 ??A / V

ANALYSIS OF A TRANSISTOR AMPLIFIER USING H-PARAMETERS:

To form a transistor amplifier it is only necessary to connect an external load and signal source as indicated in **fig. 1** and to bias the transistor properly.

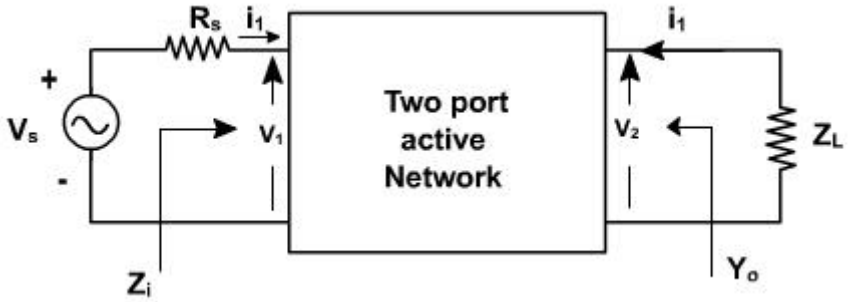
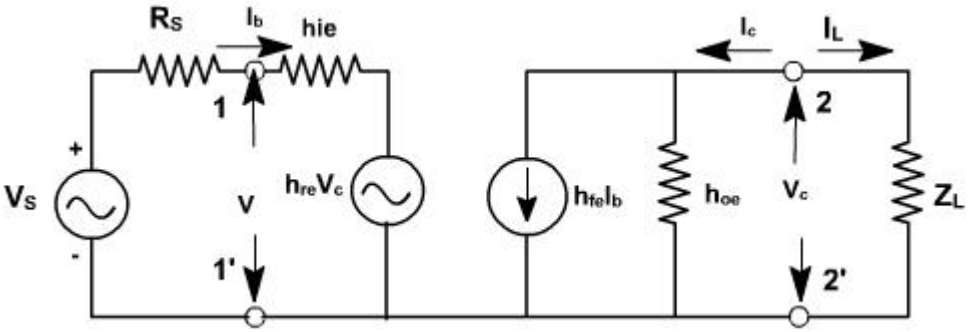


Fig. 1

Consider the two-port network of CE amplifier. R_S is the source resistance and Z_L is the load impedence h-parameters are assumed to be constant over the operating range. The ac equivalent circuit is shown in fig. 2. (Phasor notations are used assuming sinusoidal voltage input). The quantities of interest are the current gain, input impedence, voltage gain, and output impedence.



Current gain:

For the transistor amplifier stage, A_i is defined as the ratio of output to input currents.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1}$$

Input impedence:

The impedence looking into the amplifier input terminals (1,1') is the input impedance Z_i

$$Z_i = \frac{V_b}{I_b}$$

$$V_b = h_{ie} I_b + h_{re} V_c$$

$$\frac{V_b}{I_b} = h_{ie} + h_{re} \frac{V_c}{I_b}$$

$$= h_{ie} - \frac{h_{re} I_c Z_L}{I_b}$$

$$\therefore Z_i = h_{ie} + h_{re} A_I Z_L$$

$$= h_{ie} - \frac{h_{re} h_{fe} Z_L}{1 + h_{oe} Z_L}$$

$$\therefore Z_i = h_{ie} - \frac{h_{re} h_{fe}}{Y_L + h_{oe}} \qquad (\text{since } Y_L = \frac{1}{Z_L})$$

Voltage gain:

The ratio of output voltage to input voltage gives the gain of the transistors.

$$A_v = \frac{V_C}{V_b} = -\frac{I_C Z_L}{V_b}$$

$$\therefore A_v = \frac{I_B A_i Z_L}{V_b} = \frac{A_i Z_L}{Z_i}$$

Output Admittance:

$$Y_O = \left.\frac{I_c}{V_c}\right|_{V_s} = 0$$

$$I_c = h_{fe} I_b + h_{oe} V_c$$

$$\frac{I_c}{V_c} = h_{fe}\frac{I_b}{V_c} + h_{oe}$$

when $V_s = 0$, $\quad R_s . I_b + h_{ie} . I_b + h_{re} V_c = 0.$

$$\frac{I_b}{V_c} = -\frac{h_{re}}{R_s + h_{ie}}$$

$$\therefore Y_O = h_{oe} - \frac{h_{re}\, h_{fe}}{R_s + h_{ie}}$$

Voltage amplification taking into account source impedance (R_S) is given by

$$A_{VS} = \frac{V_c}{V_s} = \frac{V_c}{V_b} * \frac{V_b}{V_S} \qquad \left(V_b = \frac{V_s}{R_s + Z_i} * Z_i\right)$$

$$= A_V \cdot \frac{Z_i}{Z_i + R_s}$$

$$= \frac{A_i Z_L}{Z_i + R_s}$$

It is defined as

A_v is the voltage gain for an ideal voltage source ($R_v = 0$).

Consider input source to be a current source I_S in parallel with a resistance R_S as shown in fig. 3.

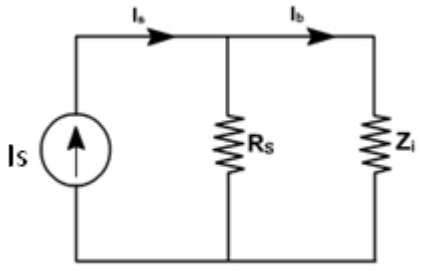


Fig. 3

In this case, overall current gain A_{IS} is defined as

$$A_{I_s} = \frac{I_L}{I_s}$$

$$= -\frac{I_c}{I_s}$$

$$= -\frac{I_c}{I_b} * \frac{I_b}{I_s} \qquad \left(I_b = \frac{I_s * R_s}{R_s + Z_i}\right)$$

$$= A_I * \frac{R_s}{R_s + Z_i}$$

If $R_s \to \infty$, $A_{Is} \to A_I$

h-parameters

To analyze multistage amplifier the h-parameters of the transistor used are obtained from manufacture data sheet. The manufacture data sheet usually provides h-parameter in CE configuration. These parameters may be converted into CC and CB values. For example fig. 4 hrc in terms of CE parameter can be obtained as follows.

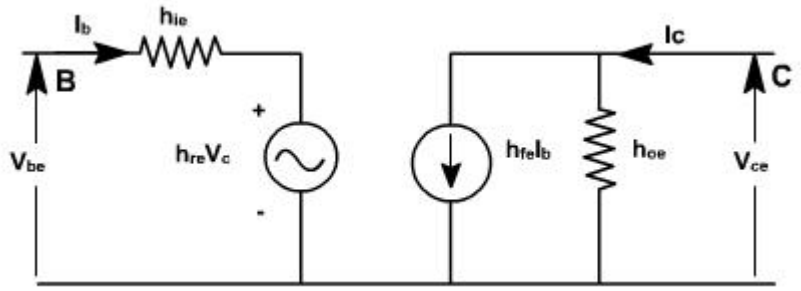


Fig. 4

For CE transistor configuaration

Vbe = hie Ib + hre Vce

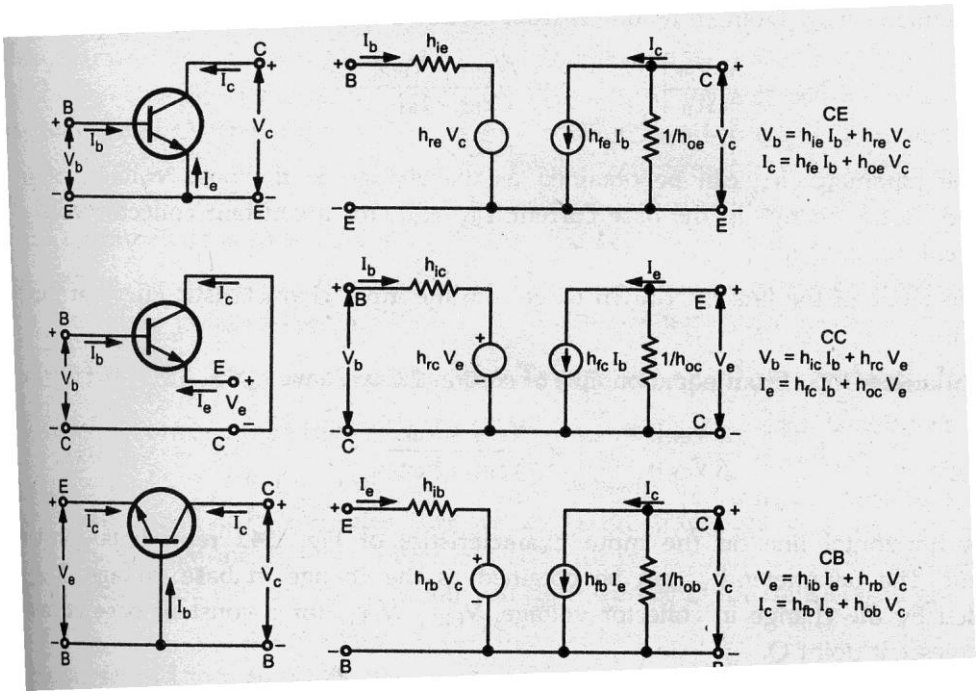
Ic = h fe Ib + hoe Vce

The circuit can be redrawn like CC transistor configuration as shown in fig. 5.

Vbc = hie Ib + hrc Vec

Ic = hfe Ib + hoe Vec

hybrid model for transistor in three different configurations



Typical h-parameter values for a transistor

Parameter	CE	CC	CB
h_i	1100 Ω	1100 Ω	22 Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	-51	-0.98
h_o	25 µA/V	25 µA/V	0.49 µA/V

Analysis of a Transistor amplifier circuit using h-parameters

A transistor amplifier can be constructed by connecting an external load and signal source and biasing the transistor properly.

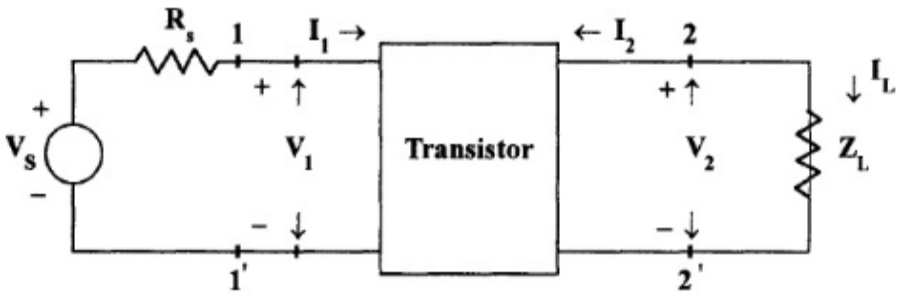


Fig.1.4 Basic Amplifier Circuit

The two port network of Fig. 1.4 represents a transistor in any one of its configuration. It is assumed that h-parameters remain constant over the operating range.The input is sinusoidal and I_1,V_1,I_2 and V_2 are phase quantities

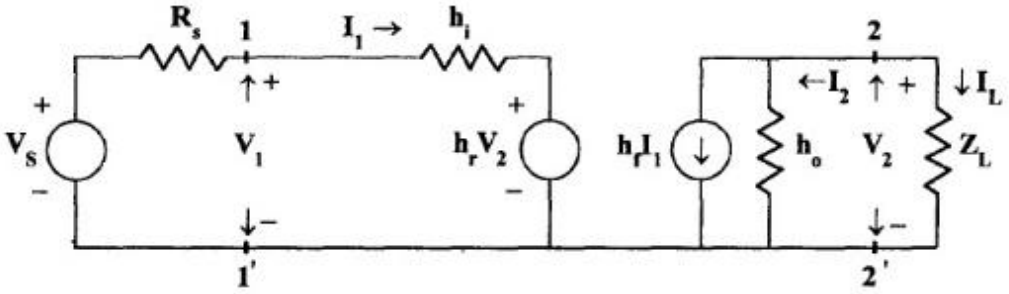


Fig. 1.5 Transistor replaced by its Hybrid Model

Current Gain or Current Amplification (A_i)

For transistor amplifier the current gain A_i is defined as the ratio of output current to input current,i.e,

$$A_i = I_L / I_1 = -I_2 / I_1$$

From the circuit of Fig

$$I_2 = h_f I_1 + h_o V_2$$

Substituting $V_2 = I_L Z_L = -I_2 Z_L$

$$I_2 = h_f I_1 - I_2 Z_L h_o$$

$I_2 + I_2 Z_L h_o = h_f I_1$

$I_2(1+ Z_L h_o) = h_f I_1$

$A_i = -I_2 / I_1 = - h_f / (1+ Z_L h_o)$

Therefore,

$A_i = - h_f / (1+ Z_L h_o)$

Input Impedence (Z_i)

In the circuit of Fig , R_S is the signal source resistance .The impedence seen when looking into the amplifier terminals (1,1′) is the amplifier input impedence Z_i,

$Z_i = V_1 / I_1$

From the input circuit of Fig $V_1 = h_i I_1 + h_r V_2$

$Z_i = (h_i I_1 + h_r V_2) / I_1$

$= h_i + h_r V_2 / I_1$

Substituting

$V_2 = -I_2 Z_L = A_1 I_1 Z_L$

$Z_i = h_i + h_r A_1 I_1 Z_L / I_1$

$= h_i + h_r A_1 Z_L$

Substituting for A_i

$Z_i = h_i - h_f h_r Z_L / (1+ h_o Z_L)$

$= h_i - h_f h_r Z_L / Z_L(1/Z_L+ h_o)$

Taking the Load admittance as $Y_L = 1/ Z_L$

$Z_i = h_i - h_f h_r / (Y_L + h_o)$

Voltage Gain or Voltage Gain Amplification Factor(A_v)

The ratio of output voltage V_2 to input voltage V_1 give the voltage gain of the transistor i.e,

$$A_v = V_2 / V_1$$

Substituting

$$V_2 = -I_2 Z_L = A_1 I_1 Z_L$$

$$A_v = A_1 I_1 Z_L / V_1 = A_i Z_L / Z_i$$

Output Admittance (Y_o)

Y_o is obtained by setting V_S to zero, Z_L to infinity and by driving the output terminals from a generator V_2. If the current V_2 is I_2 then $Y_o = I_2/V_2$ with $V_S=0$ and $R_L = \infty$.

From the circuit of fig

$$I_2 = h_f I_1 + h_o V_2$$

Dividing by V_2,

$$I_2 / V_2 = h_f I_1 / V_2 + h_o$$

With $V_2 = 0$, by KVL in input circuit,

$$R_S I_1 + h_i I_1 + h_r V_2 = 0$$

$$(R_S + h_i) I_1 + h_r V_2 = 0$$

Hence, $I_2 / V_2 = -h_r / (R_S + h_i)$

$$= h_f (-h_r / (R_S + h_i) + h_o$$

$$Y_o = h_o - h_f h_r / (R_S + h_i)$$

The output admittance is a function of source resistance. If the source impedence is resistive then Y_o is real.

Voltage Amplification Factor(A_{vs}) taking into account the resistance (R_s) of the source

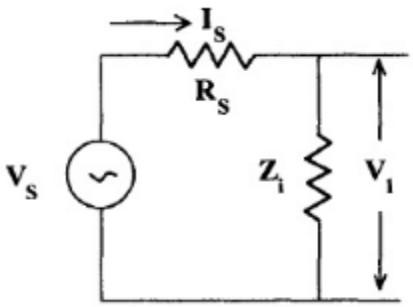


Fig. 5.6 Thevenin's Equivalent Input Circuit

This overall voltage gain A_{vs} is given by

$$A_{vs} = V_2 / V_S = V_2V_1 / V_1V_S = A_v V_1 / V_S$$

From the equivalent input circuit using Thevenin's equivalent for the source shown in Fig. 5.6

$V_1 = V_S Z_i / (Z_i + R_S)$

$V_1 / V_S = Z_i / (Z_i + R_S)$

Then, $A_{vs} = A_v Z_i / (Z_i + R_S)$

Substituting $A_v = A_i Z_L / Z_i$

$A_{vs} = A_i Z_L / (Z_i + R_S)$

$A_{vs} = A_i Z_L R_S / (Z_i + R_S) R_S$

$A_{vs} = A_{is} Z_L / R_S$

Current Amplification (A_{is}) taking into account the sourse Resistance(R_S)

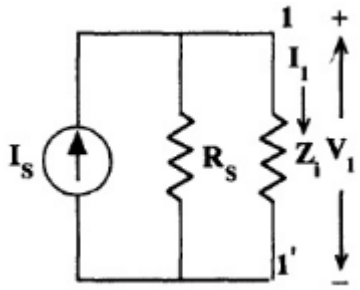


Fig. 1.7 Norton's Equivalent Input Circuit

The modified input circuit using Norton's equivalent circuit for the calculation of A_{is} is shown in Fig. 1.7

Overall Current Gain, $A_{is} = -I_2 / I_S = - I_2 I_1 / I_1 I_S = A_i I_1 / I_S$

From Fig. 1.7 $I_1 = I_S R_S / (R_S + Z_i)$

$I_1 / I_S = R_S / (R_S + Z_i)$

and hence, $A_{is} = A_i R_S / (R_S + Z_i)$

Operating Power Gain (A_P)

The operating power gain A_P of the transistor is defined as

$A_P = P_2 / P_1 = -V_2 I_2 / V_1 I_1 = A_v A_i = A_i A_i Z_L / Z_i$

$A_P = A_i^2 (Z_L / Z_i)$

Small Signal analysis of a transistor amplifier

$A_i = - h_f / (1 + Z_L h_o)$	$A_v = A_i Z_L / Z_i$
$Z_i = h_i + h_r A_1 Z_L = h_i - h_f h_r / (Y_L + h_o)$	$A_{vs} = A_v Z_i / (Z_i + R_S) = A_i Z_L / (Z_i + R_S)$ $= A_{is} Z_L / R_S$
$Y_o = h_o - h_f h_r / (R_S + h_i) = 1 / Z_o$	$A_{is} = A_i R_S / (R_S + Z_i) = A_{vs} = A_{is} R_S / Z_L$

BIASING OF FET AMPLIFIERS

Fixed Bias

Unlike BJTs, thermal runaway does not occur with FETs. However, the wide differences in maximum and minimum **transfer characteristics** make I_D levels unpredictable with simple fixed-gate bias voltage. To obtain reasonable limits on quiescent drain currents I_D and drain-source voltage V_{DS}, source resistor and potential divider bias techniques must be used. With few exceptions, MOSFET bias circuits are similar to those used for **JFET**s. Various FET biasing circuits are discussed below:

Fixed Bias:

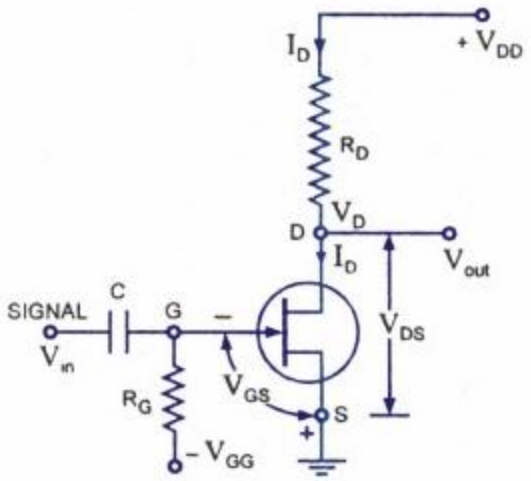


FIG.: Fixed biasing circuit for JFET

DC bias of a FET device needs setting of gate-source voltage V_{GS} to give desired drain current I_D . For a JFET drain current is limited by the saturation current I_{DS}. Since the FET has such a high input impedance that no gate current flows and the dc voltage of the gate set by a voltage divider or a fixed battery voltage is not affected or loaded by the FET.

Fixed dc bias is obtained using a battery V_{QG}. This battery ensures that the gate is always negative with respect to source and no current flows through resistor R_G and gate terminal that is I_G =0. The battery provides a voltage V_{GS} to bias the N-channel JFET, but no resulting current is drawn from the battery V_{GG}. Resistor R_G is included to allow any ac signal applied through capacitor C to develop across R_G. While any ac signal will develop across R_G, the dc voltage drop across R_G is equal to $I_G R_G$ = 0 volt.

The gate-source voltage V_{GS} is then

$V_{GS} = – v_G – v_s = – v_{GG} – 0 = – V_{GG}$

The drain to source current I_D is then fixed by the gate-source voltage as determined by equation. This current then causes a voltage drop across the drain resistor R_D and is given as $V_{RD} = I_D R_D$ and output voltage, $V_{out} = V_{DD} – I_D R_D$

Self bias:

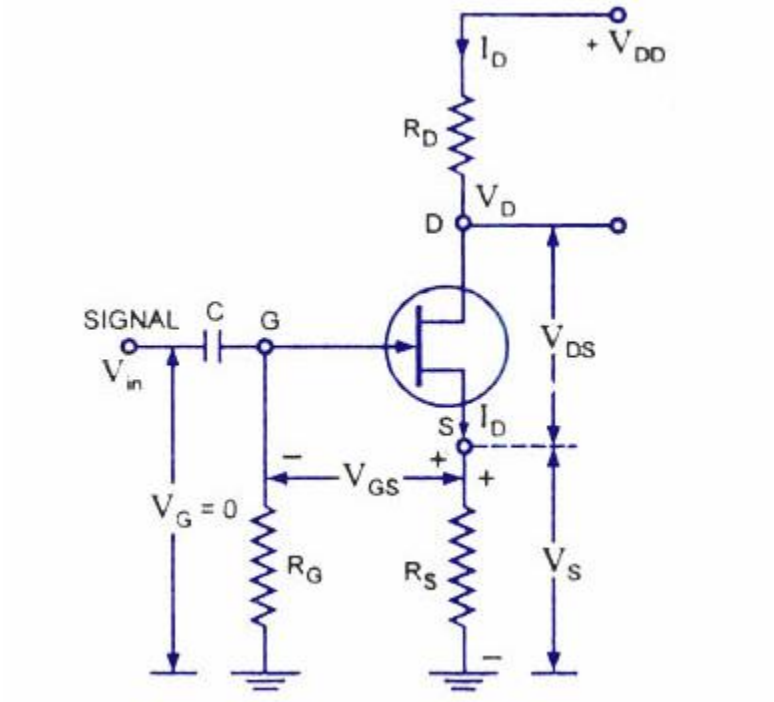


FIG.: Self bias circuit for JFET

This is the most common method for biasing a JFET. Self-bias circuit for N-channel JFET is shown in figure. Since no gate current flows through the reverse-biased gate-source, the gate current $I_G = 0$ and, therefore,$v_G = i_G R_G = 0$ With a drain current I_D the voltage at the S is, $V_s = I_D R_s$. The gate-source voltage is then,

$V_{GS} = V_G – V_s = 0 – I_D R_s = – I_D R_s$. So, voltage drop across resistance R_s provides the biasing voltage V_{Gg} and no external source is required for biasing and this is the reason that it is called self-biasing. The operating point *(*that is zero signal I_D and V_{DS}) can easily be determined from equation and equation given below :

$V_{DS} = V_{DD} – I_D (R_D + R_S)$

Thus dc conditions of JFET amplifier are fully specified. Self biasing of a JFET stabilizes its quiescent operating point against any change in its parameters like transconductance. Let the given JFET be replaced by another JFET having the double conductance then drain current will also try to be double

but since any increase in voltage drop across R_s, therefore, gate-source voltage, V_{GS} becomes more negative and thus increase in drain current is reduced.

Potential Divider Bias for JFET:

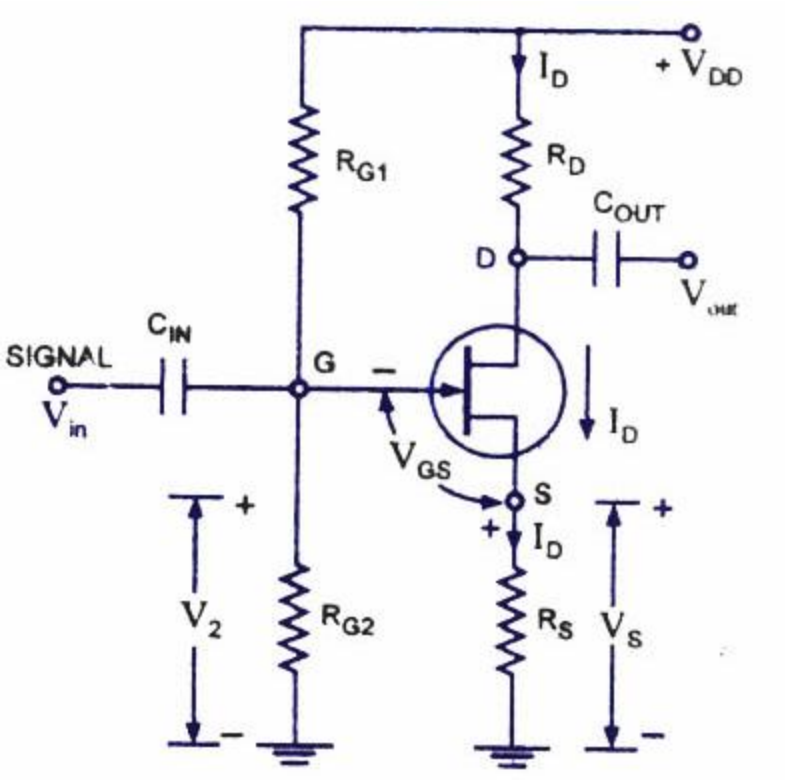


FIG.: Potential Divider Bias circuit for JFET

A slightly modified form of dc bias is provided by the circuit shown in figure. The resistors R_{GI} and R_{G2} form a potential divider across drain supply V_{DD}. The voltage V_2 across R_{G2} provides the necessary bias. The additional gate resistor R_{GI} from gate to supply voltage facilitates in larger adjustment of the dc bias point and permits use of larger valued R_S.

The gate is reverse biased so that $I_G = 0$ and gate voltage

$V_G = V_2 = (V_{DD}/R_{G1} + R_{G2}) * R_{G2}$

And

$V_{GS} = v_G - v_s = V_G - I_D R_s$

The circuit is so designed that $I_D R_s$ is greater than VG so that VGS is negative. This provides correct bias voltage.

The operating point can be determined as

$I_D = (V_2 - V_{GS})/ R_S$

And

$V_{DS} = V_{DD} - I_D (R_D + R_S)$

FET SMALL SIGNAL ANALYSIS

Introduction:

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a current-controlled device and the FET is a voltage-controlled device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a transconductance factor, g_m.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

While the common-source configuration is the most popular, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides a much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

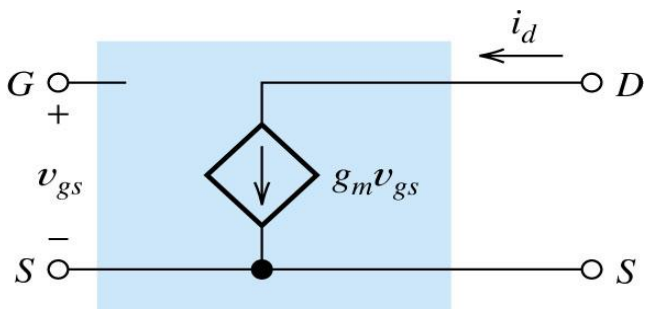


FIG.: Small signal model of FET

COMMON SOURCE AMPLIFIER

A common-source JFET amplifier is one in which the ac input signal is applied to the gate and the ac output signal is taken from the drain. The source terminal is common to both the input and output signal. A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to ac ground. A self-biased common-source n-channel JFET amplifier with an ac source capacitively coupled to the gate is shown in Figure below. The resistor, RG, serves two purposes: It keeps the gate at approximately 0 V dc (because IGSS is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. A bias voltage is produced by the drop across RS. The bypass capacitor, C2, keeps the source of the JFET at ac ground.

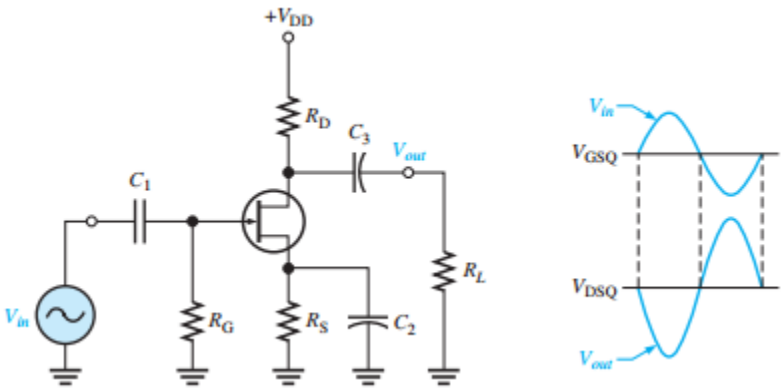


FIG.: Self biased Common source Amplifier

The input signal voltage causes the gate-to-source voltage to swing above and below its Q-point value (VGSQ), causing a corresponding swing in drain current. As the drain current increases, the voltage drop across RD also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in phase with the gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value (VDSQ) and is 180° out of phase with the gate-to-source voltage, as illustrated in Figure above. A Graphical Picture The operation just described for an n-channel JFET is illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure below. Part (a) shows how a sinusoidal variation, Vgs, produces a corresponding sinusoidal variation in Id. As Vgs swings from its Q-point value to a more negative value, Id decreases from its Q-point value. As Vgs swings to a less negative value, Id increases. The signal at the gate drives the drain

current above and below the Q-point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the ID axis and down to the VDS axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown. Because the transfer characteristic curve is nonlinear, the output will have some distortion. This can be minimized if the signal swings over a limited portion of the load line.

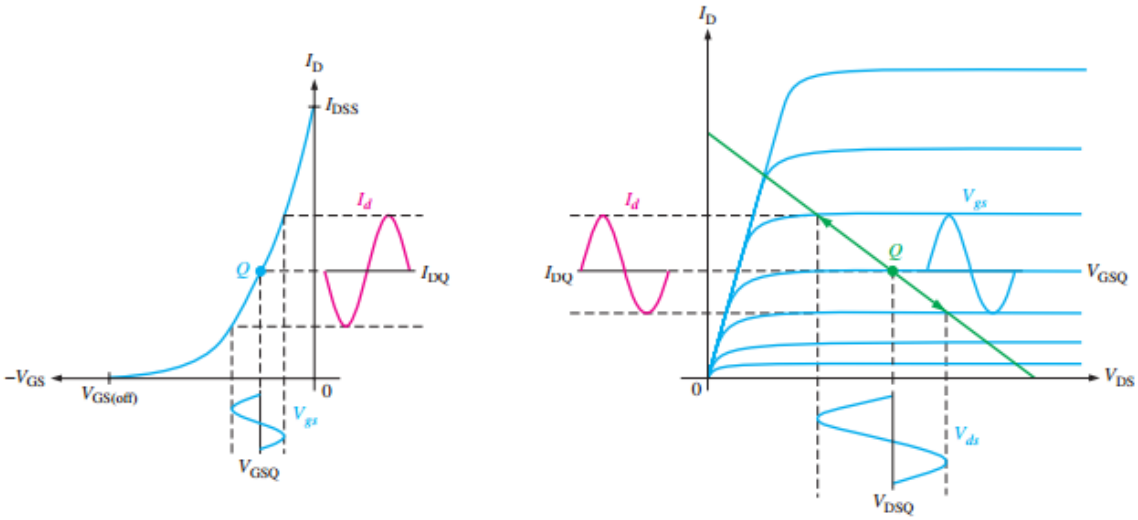


Fig. Transfer Characteristic curve and Drain curve for Common source JFET Amplifier

AC Equivalent Circuit to analyze the signal operation of the amplifier in Figure below ,an ac equivalent circuit is as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The VDD terminal is at a zero-volt ac potential and therefore acts as an ac ground. The ac equivalent circuit is shown in Figure below. Notice that the VDD end of Rd and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.

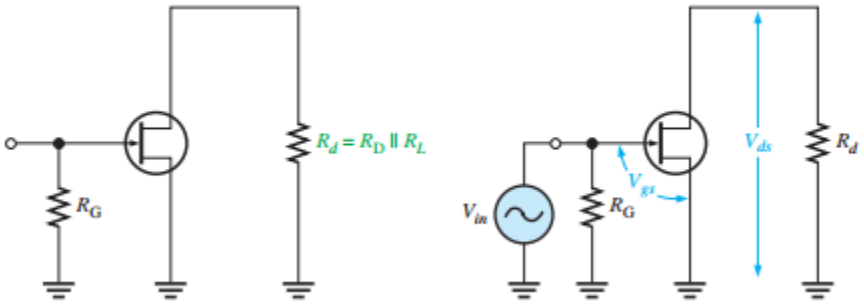


Fig: The AC equivalent circuit for Common source amplifier

An ac voltage source is shown connected to the input in Figure above. Since the input resistance to a JFET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance. Vgs = Vin

$$V_{gs} = V_{in}$$

Voltage Gain The expression for JFET voltage gain that was given in Equation below applies to the common-source amplifier.

$$A_v = g_m R_d$$

Phase Inversion The output voltage (at the drain) is out of phase with the input voltage (at the gate). The phase inversion can be designated by a negative voltage gain, Recall that the common-emitter BJT amplifier also exhibited a phase inversion.

Input Resistance is derived as follows, because the input to a common-source amplifier is at the gate, the input resistance is extremely high. Ideally, it approaches infinity and can be neglected. As you know, the high input resistance is produced by the reverse-biased PN junction in a JFET and by the insulated gate structure in a MOSFET. The actual input resistance seen by the signal source is, the gate-to-ground resistor, RG, in parallel with the FET's input resistance, VGS IGSS. The reverse leakage current, IGSS, is typically given on the datasheet for a specific value of VGS so that the input resistance of the device can be calculated.

$$R_{in} = R_G \,||\left(\frac{V_{GS}}{I_{GSS}}\right)$$

Common drain JFET amplifier

A common-drain JFET amplifier is one in which the input signal is applied to the gate and the output is taken from the source, making the drain common to both. Because it is common, there is no need for a drain resistor. A common-drain JFET amplifier is shown in Figure below. A common-drain amplifier is also called a source-follower. Self-biasing is used in this particular circuit. The input signal is applied to the gate through a coupling capacitor, C1, and the output signal is coupled to the load resistor through C2.

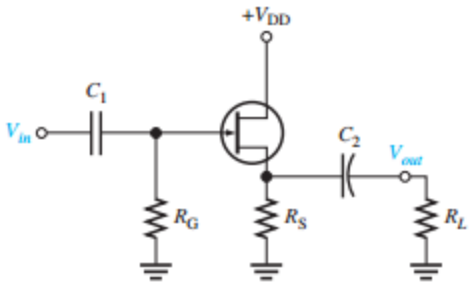


FIG.: Self biased Common Drain Amplifier

Voltage Gain as in all amplifiers, the voltage gain is Av Vout / Vin. For the source-follower, Vout is IdRs and Vin is Vgs IdRs as shown in above Figure. Therefore, the gate-to-source voltage gain is IdRs (Vgs IdRs). Substituting Id gmVgs into the expression gives the following result:

$$A_V = \frac{g_m v_{gs} R_s}{v_{gs} + g_m v_{gs} R_s}$$

The vgs term cancel so,

$$A_V = \frac{g_m R_s}{1 + g_m R_s}$$

Notice here that the gain is always slightly less than 1. If then a good approximation is Since the output voltage is at the source, it is in phase with the gate (input) voltage.

Input Resistance Because the input signal is applied to the gate, the input resistance seen by the input signal source is extremely high, just as in the common-source amplifier configuration. The gate resistor, RG, in parallel with the input resistance looking in at the gate is the total input resistance.

$$R_{in} = R_G \,||R_{IN(gate)}$$

Where

$R_{IN(gate)} = V_{GS} \,||I_{GSS}$

common gate amplifier

The common-gate FET amplifier configuration is comparable to the common-base BJT amplifier. Like the CB, the common-gate (CG) amplifier has a low input resistance. This is different from the CS and CD configurations, which have very high input resistances

Common-Gate Amplifier Operation A self-biased common-gate amplifier is shown in figure. The gate is connected directly to ground. The input signal is applied at the source terminal through C1. The output is coupled through C2 from the drain terminal.

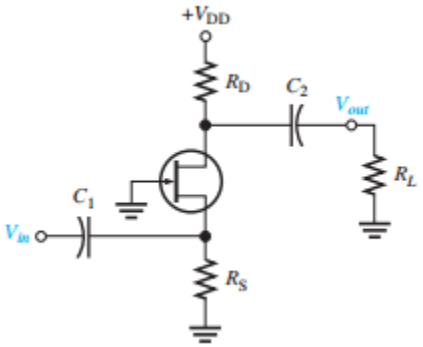


Fig: Common Gate Amplifier

Voltage Gain The voltage gain from source to drain is developed as follows:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_d}{V_{gs}} = \frac{I_d\, R_d}{V_{gs}} = \frac{g_m\, V_{gs}\, R_d}{V_{gs}}$$

$$A_v = g_m R_d$$

Where Rd = RD || RL. Notice that the gain expression is the same as for the common-source JFET amplifier.

Input Resistance As you have seen, both the common-source and common-drain configurations have extremely high input resistances because the gate is the input terminal. In contrast, the common-gate configuration where the source is the input terminal has a low input resistance. This is shown as follows. First, the input current is equal to the drain current

$$I_{in} = I_s = I_d = g_m\, V_{gs}$$

Second, the input voltage equals Vgs.

$$V_{in} = V_{gs}$$

Therefore, the input resistance at the source terminal is

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{gs}}{g_m V_{gs}}$$

$$R_{in} = \frac{1}{g_m}$$

MOSFET BIASING:

Biasing of Enhancement MOSFET:

Drain to Gate bias**:**

The following figure shows the drain to gate bias circuit for enhancement mode MOSFET.

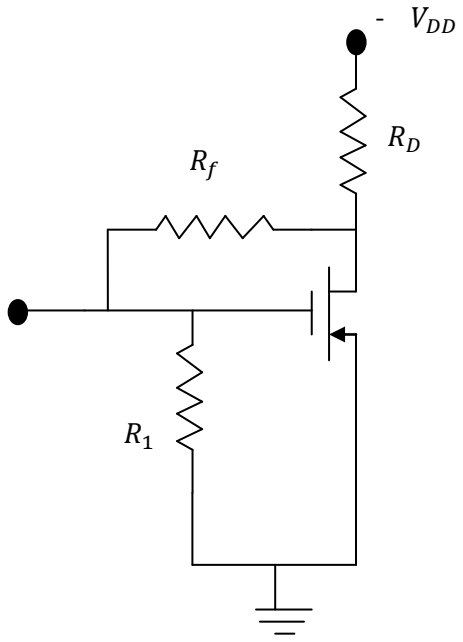


FIG. : Drain to Gate bias circuit for enhancement MOSFET.

Here, the bias voltage is $v_{GS} = \left[\frac{R_1}{R_1 + R_f}\right] V_{DS}$.

This circuit offers the DC stabilization through the feedback resistorR_f. However, the input resistance is reduced because of Miller effect. Also, the voltage divider biasing technique given for JFET can be used for the enhancement MOSFET. Here, the DC stability is accomplished by the DC feedback through R_s.

But the self- bias technique given for JFET cannot be used for establishing an operating point for the enhancement MOSFET because the voltage drop across R_s is in a direction to reverse-bias the gate and it actually needs forward gate bias.

Potential Divider Bias:

The following figure shows the circuit diagram. The MOSFET is a N- channel enhancement mode MOSFET common source circuit with source resistor.

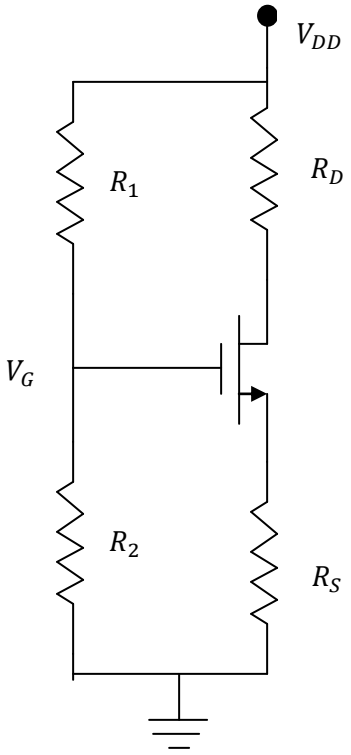


FIG.: N-Channel enhancement mode MOSFET common source circuit with source resistor.

The gate voltage is

$$V_G = V_{GS} = \left[\frac{R_1}{R_1 + R_2}\right] V_{DD}$$

And the gate to source voltage is

$$V_{GS} = V_{DD} - V_G$$

Assuming that $V_{GS} > V_{TN}$ and the MOSFET is biased in the saturation region, the drain current is

$$I_D = K_N (V_{GS} - V_{TN})^2$$

Here the threshold voltage V_{TN} and conduction parameter K_N are functions of temperature.

The drain to source voltage is $V_{DS} = V_{DD} - I_D R_D$

If $V_{DS} > V_{DS}(sat) = V_{GS} > V_{TN}$, then the MOSFET is biased in the saturation region. If

$V_{DS} < V_{DS}(sat) = V_{GS} > V_{TN}$, then the MOSFET is biased in the non -saturation region and the drain current is given by,

$$I_D = K_N (2(V_{GS} - V_{TN})V_{DS} - {V_{DS}}^2$$

Biasing of depletion MOSFET:

Both the self bias and voltage divider bias circuit given for JFET can be used to establish an operating point for the depletion mode MOSFET.

Small signal analysis of MOSFET:

Common source configuration of E- MOSFET with potential divider biasing:

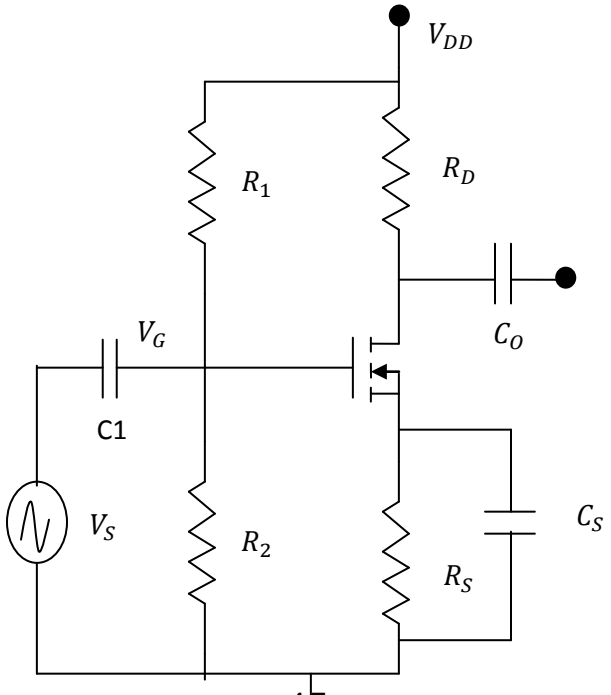


FIG.: Circuit Diagram of common source amplifier

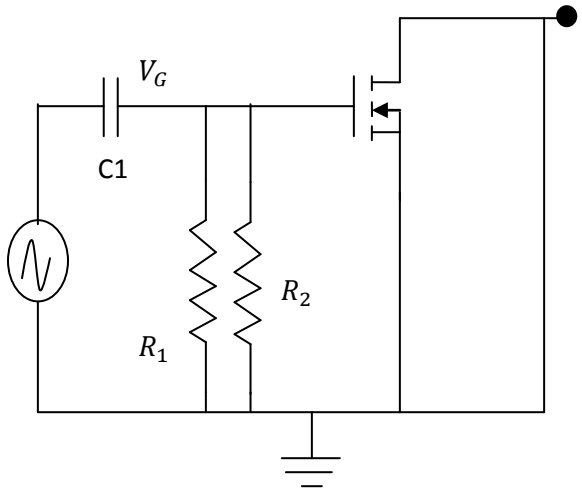


FIG.: AC Equivalent circuit

In common source configuration of E-MOSFET, the inputs is fed to the gate and output is taken at the drain. The resistor R1 and R2 acts as biasing resistors. For AC analysis the source is connected to ground and hence source terminal is connected to both input and output.

The circuit diagram of voltage-divider bias for E-MOSFET is shown in the above figure. The AC equivalent model of the voltage –divider bias circuit of E-MOSFET can be obtained by shorting the capacitors and grounding the biasing sources as shown in the above figure. Replacing the devices by its small signal model, We get the figure shown below.

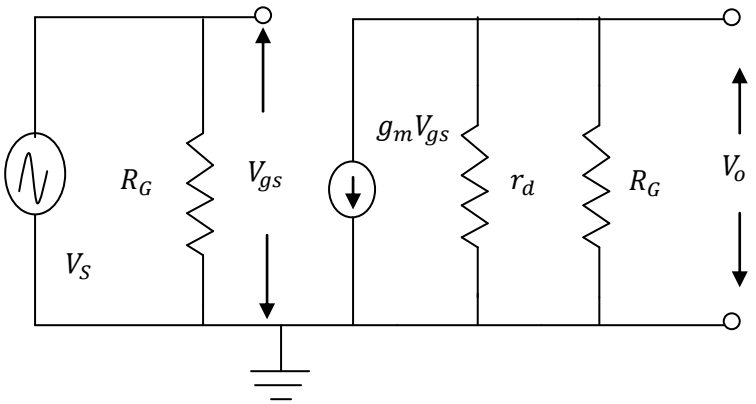


FIG.: Small signal equivalent circuit for common source amplifier

Input impedance:

Input impedance is the resistance looking back from the input terminal. From the small signal signal model of voltage divider configuration of E-MOSFET shown in the above figure, the input impedance can be calculated as

$$Z_i = R_1 \,||R_2$$

Output impedance:

Output impedance is the resistance looking back from the output terminal. From the small signal; model of MOSFET, The output impedance is calculated as follows,

$$Z_o = R_D \,||\, r_d$$

When Vi = 0, gate- source voltage, V_{gs} = 0 . Therefore, $g_m V_{gs}$ is an open circuit. Hence the output impedance is equal to drain resistance. Therefore, the output impedance is given by,

$$Z_o = R_D$$

Voltage gain:

Voltage gain is the ratio of output voltage to input voltage.

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_O(R_D \,||\, r_d) = I_D(R_D \,||\, r_d)$$

Where, $I_D = g_m V_{gs}$

Therefore, $A_V = \frac{V_o}{V_i} = -g_m R_D$

Common Drain Amplifier:

The circuit diagram and the small signal diagram are as follows

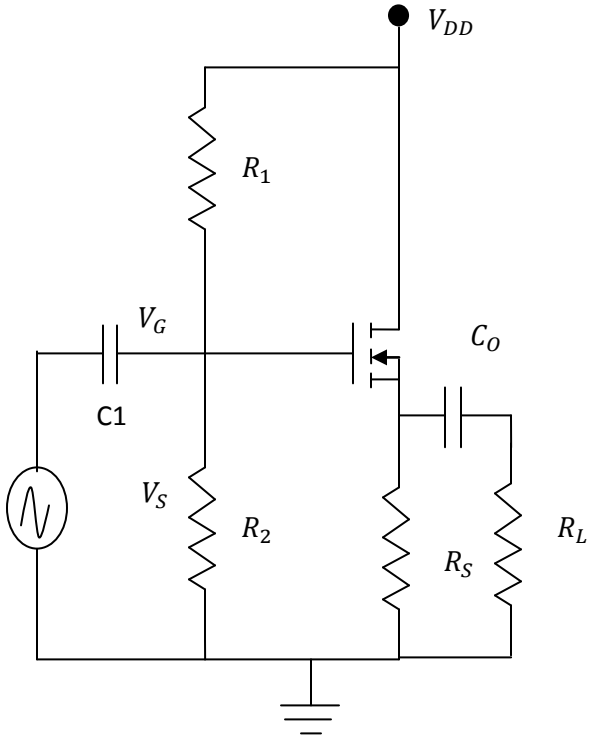


FIG.: Circuit Diagram of common drain Amplifier

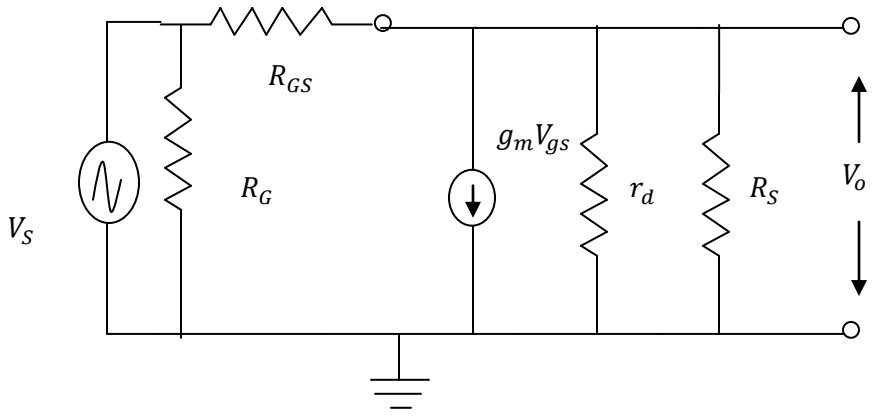


FIG.: Small signal model of common drain amplifier

Input Impedance is given by, $Z_g = R_{GS}[1 + g_m(R_S || R_L)]$;

Therefore,

$$Z_i = R_G || Z_g$$

The output impedance is

$$Z_O = R_S || (1/g_m)$$

Voltage Gain is,

$$A_v = 1$$

Common Gate Amplifier:

The circuit diagram and the small signal model are given below

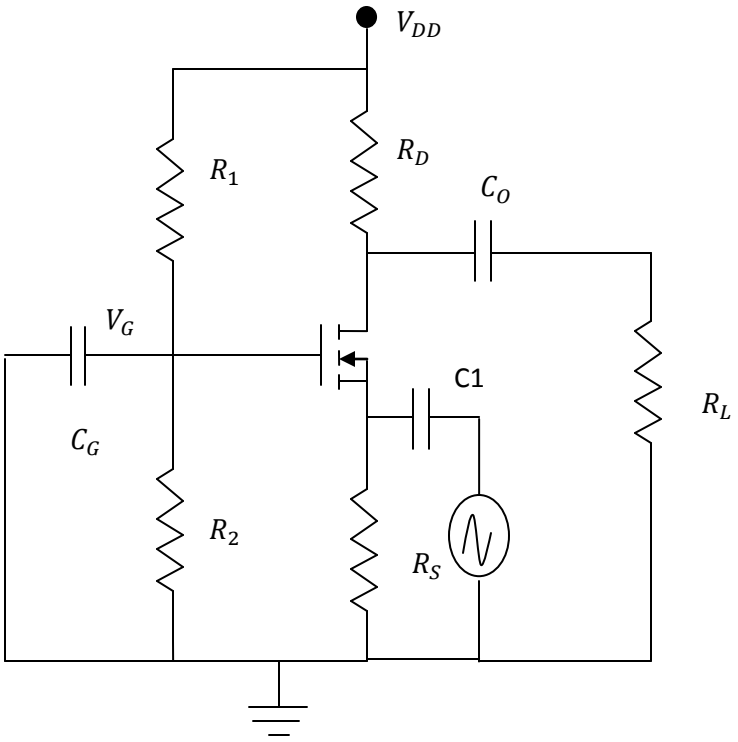


FIG.: Common gate amplifier

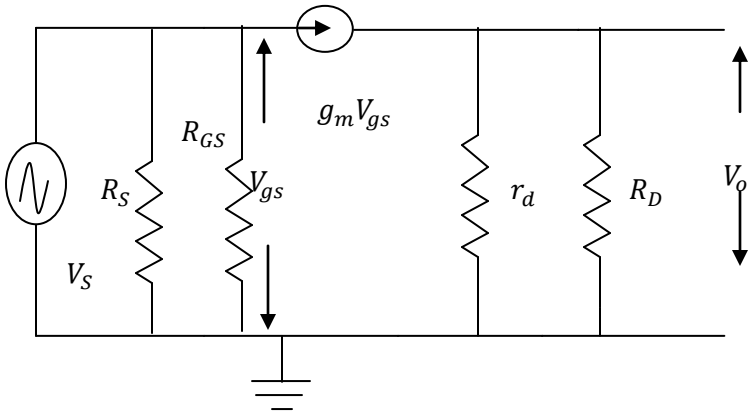


FIG.: Small signal model of common gate amplifier

Input Impedance, $Z_i = R_S || 1/g_m$

Output Impedance, $Z_O = R_D || r_d$

Voltage Gain, $A_V = \frac{V_o}{V_i} = g_m(R_D || r_d || R_L)$

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SCHOOL OF ELECTRICAL AND ELECTRONICS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

UNIT -3

Electronic Circuits-SECA1305

3.1 Frequency Response of Amplifiers

The gain factors such as voltage, current, trans conductance and trans resistance of amplifiers are functions of signal frequency. In the amplifier gain versus frequency plot, the gain factor is plotted in terms of decibels and frequency in terms of Hertz on logarithmic scales. The main purpose is to determine the frequency response of amplifier circuits due to circuit capacitors and transistor capacitances. The frequency response will be useful to determine bandwidth of the circuit. The transfer function is derived by using the complex frequencys, of several passive circuits. With the help of Bode plots of the transfer function, the magnitude response, phase response, time constant and 3 dB cutoff frequencies are calculated. In this chapter, the frequency responses of transistor circuits including BJTs and FETs are studied. The effects due to circuit capacitors including coupling, bypass,and load capacitors and internal transistor capacitances are analysed. The RF amplifier and video amplifier circuits used in high frequency applications are discussed.

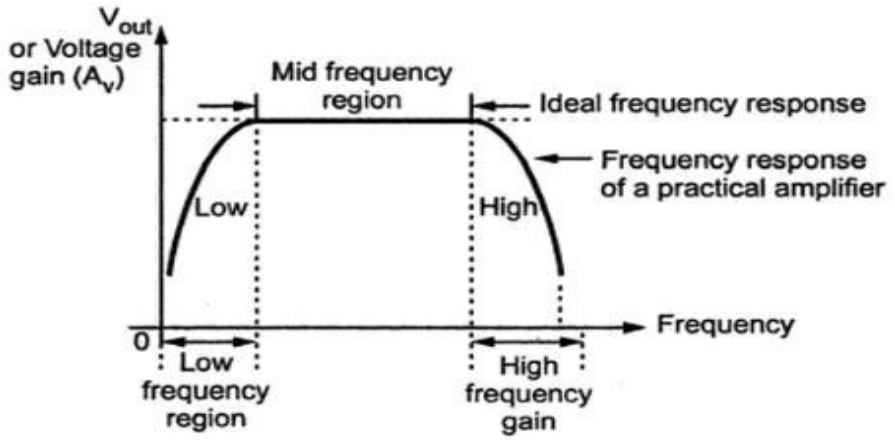


Fig. 4.1 A typical frequency response of an amplifier

Fig 3.1 Frequency Response of Amplifiers

The response of any single-stage (or) Multistage network is highly influenced by the frequency of the applied signal. At low frequencies, the effect of capacitors (coupling and bypass) cannot be neglected due to their high value of capacitive reactance under these conditions. Moreover, any fluctuations in the number of stages of a cascaded system will also affect the frequency response of that system. While plotting the frequency response of a circuit, it is conventional to use a logarithmic scale along the X-axis (horizontal axis), so as to permit a plot extending from low to the high frequency regions. In general, any frequency response curve can be splitted into three regions, namely.

(a) Low frequency region

(b) Mid frequency region and

(c) High frequency region

3.2 Low Frequency analysis of BJT

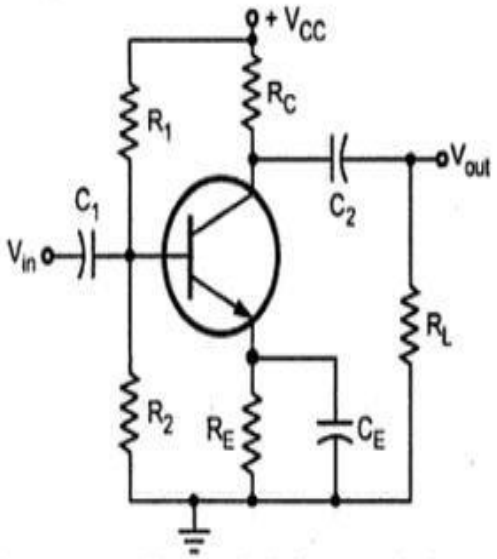


Fig 3.2 **Typical RC coupled common emitter amplifier**

Let us consider a typical common emitter amplifier as shown in Fig. 4.3.

The amplifier shown in Fig. 4.3 has three RC networks that affect its gain as the frequency is reduced below midrange. These are :

1) RC network formed by the input coupling capacitor C_1 and the input impedance of the amplifier.

2) RC network formed by the output coupling capacitor C_2, the resistance looking in at the collector, and the load resistance.

3) RC network formed by the emitter bypass capacitor C_E and the resistance looking in at the emitter.

Input RC Network

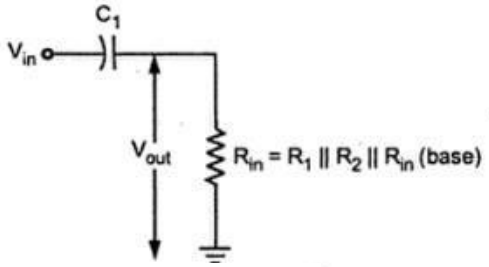


Fig 3.3

Fig. 4.4 shows input RC network formed by C_1 and the input impedance of the amplifier. Note that V_{out} shown in the Fig. 4.4 is the output voltage of the network.

Applying voltage divider theorem we can write

$$V_{out} = \left(\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} \right) V_{in}$$

We know that a critical point in the amplifier response is generally accepted to occur when the output voltage is 70.7 percent of the input ($V_{out} = 0.707\ V_{in}$) . Thus we can write, at critical point

$$\frac{R_{in}}{\sqrt{R_{in}^2 + X_{C1}^2}} = 0.707 = \frac{1}{\sqrt{2}}$$

$\therefore$ At this condition $R_{in} = X_{C1}$.

At this condition the overall gain is reduced due to the attenuation provided by the input RC network. The reduction in overall gain is given by

$$A_v = 20 \log \left(\frac{V_{out}}{V_{in}} \right) = 20 \log (0.707) = -3dB$$

The frequency f_c at this condition is called lower critical frequency and is given by

$$f_c = \frac{1}{2\pi R_{in} C_1}$$

where $R_{in} = R_1 \,||\, R_2 \,||\, h_{ie}$

$$\therefore \quad f_c = \frac{1}{2\pi (R_1 \,||\, R_2 \,||\, h_{ie}) C_1}$$

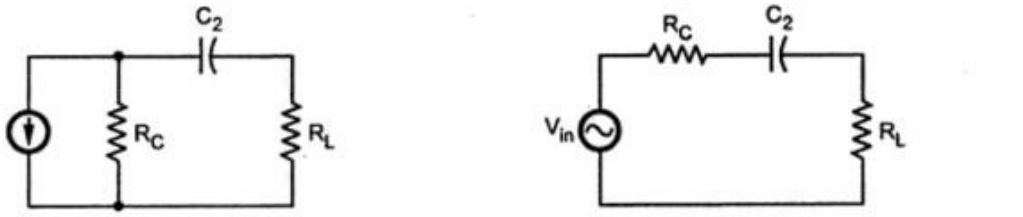
If the resistance of input source is taken into account the above equation becomes

$$f_c = \frac{1}{2\pi (R_s + R_{in}) C_1}$$

The phase angle in an input RC circuit is expressed as $\theta = \tan^{-1} \left(\frac{X_{C1}}{R_{in}} \right)$.

Output RC Network

Fig. 4.5 shows output RC network formed by C_2, resistance looking in at the collector and the load resistance.



(a) Current source (b) Current source replaced by voltage source

Fig 3.4

The critical frequency for this RC network is given by,

$$f_c = \frac{1}{2\pi(R_C + R_L)C_2}$$

The phase angle in the output RC circuit is expressed as $\theta = \tan^{-1}\left(\frac{X_{C2}}{R_C + R_L}\right)$.

Bypass Network

Fig. 4.6 (b) shows RC network formed by the emitter bypass capacitor C_E and the resistance looking in at the emitter.

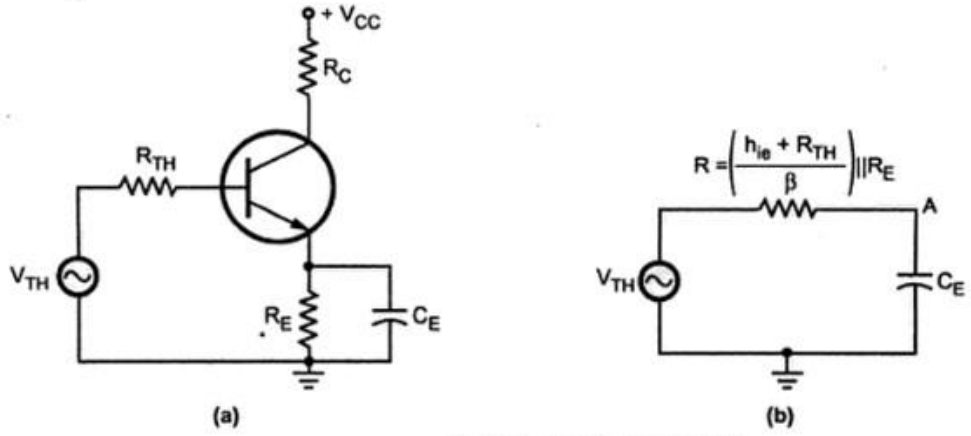


Fig 3.5 Bypass RC network

Here, $\frac{h_{ie} + R_{TH}}{\beta}$ is the resistance looking in at the emitter. It is derived as follows

$$R = \frac{V_e}{I_e} + \frac{h_{ie}}{\beta} \cong \frac{V_b}{\beta I_b} + \frac{h_{ie}}{\beta} = \frac{I_b R_{TH}}{\beta I_b} + \frac{h_{ie}}{\beta} = \frac{R_{TH} + h_{ie}}{\beta}$$

where $R_{TH} = R_1 \,||\, R_2 \,||\, R_s$. It is the thevenin's equivalent resistance looking from the base of the transistor towards the input as shown in the Fig. 4.6 (a)

The critical frequency for the bypass network is

$$f_c = \frac{1}{2\pi R C_E}$$

3.3 High Frequency analysis of BJT

Let us consider a typical common emitter amplifier as shown in Fig. 4.12.

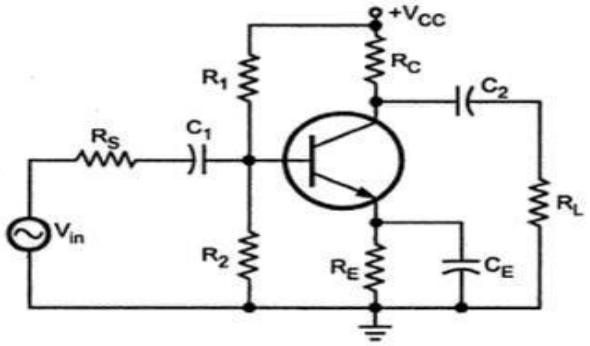


Fig 3.6 **Typical RC coupled common emitter amplifier**

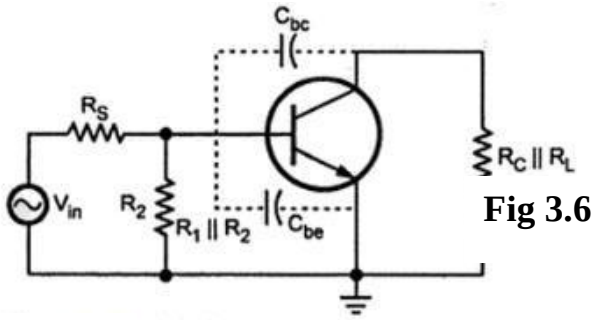


Fig 3.7 **High frequency equivalent circuit**

As mentioned earlier, at high frequencies, the coupling and bypass capacitors act as a short circuit and do not affect the amplifier frequency response. However, at higher frequencies the internal capacitances do come into play. Fig. 4.13 shows the high frequency equivalent circuit for the given amplifier circuit.

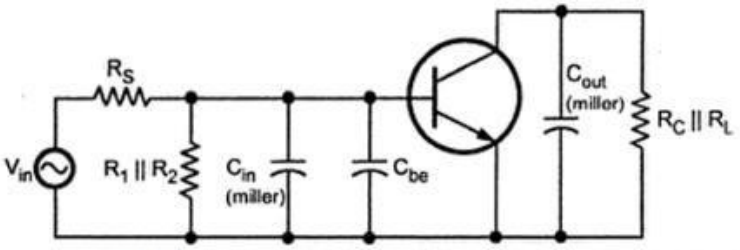


Fig 3.8 **Simplified high frequency equivalent circuit**

Using Miller theorem this high frequency equivalent circuit can be further simplified as follows.

The internal capacitance C_{bc} can be splitted into $C_{in\,(miller)}$ and $C_{out\,(miller)}$ as shown in the Fig. 4.14.

where $$C_{in\,(miller)} = C_{bc}\,(A_v + 1)$$

and $$C_{out\,(miller)} = C_{bc}\left(\frac{A_v + 1}{A_v}\right) \approx C_{bc}$$

Fig. 4.14 shows that there are two RC networks which affect the high frequency response of the amplifier. These are :

1) Input RC Network and

2) Output RC Network

Input RC Network

Fig. 4.15 shows input RC network.

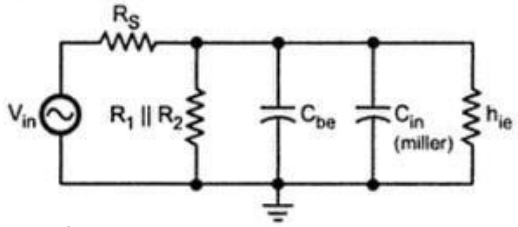


Fig 3.9 **Input RC network**

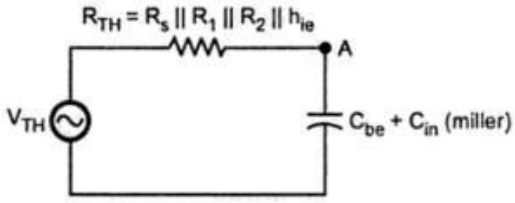


Fig 3.10 **Reduces input RC network**

This network is further reduced as shown in the Fig. 4.16. At high frequencies capacitive reactance becomes smaller. If we apply voltage divider theorem, voltage at point A in Fig. 4.16 reduces as capacitive reactance reduces with increase in frequency above midrange. This reduces the signal voltage applied to the base, reducing the circuit gain and hence the output voltage.

The critical frequency can be calculated at condition capacitive reactance is equal to the resistance, i.e. $X_{C1} = R_s \| R_1 \| R_2 \| h_{ie}$.

It is given as,

$$f_c\,(input) = \frac{1}{2\pi(R_s \| R_1 \| R_2 \| h_{ie})\,C_T}$$

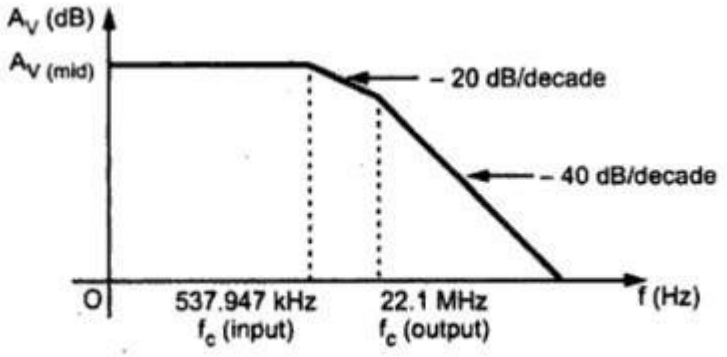


Fig 3.11 High frequency response of the amplifier

3.5 Miller's Effect

Miller effect is the increase in the equivalent input capacitance of a voltage amplifier due to a capacitance connected between two gain-related nodes, one on the input side of an amplifier and the other the output side.

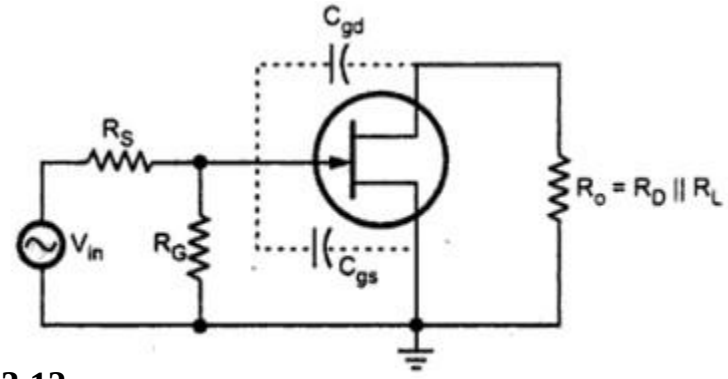


Fig 3.12 High frequency equivalent circuit

3.6 Miller Capacitance

Using Miller theorem this high frequency equivalent circuit can be further simplified as follows :

The internal capacitance C_{gd} can be splitted into $C_{in\ (miller)}$ and $C_{out\ (miller)}$ as shown in the Fig.

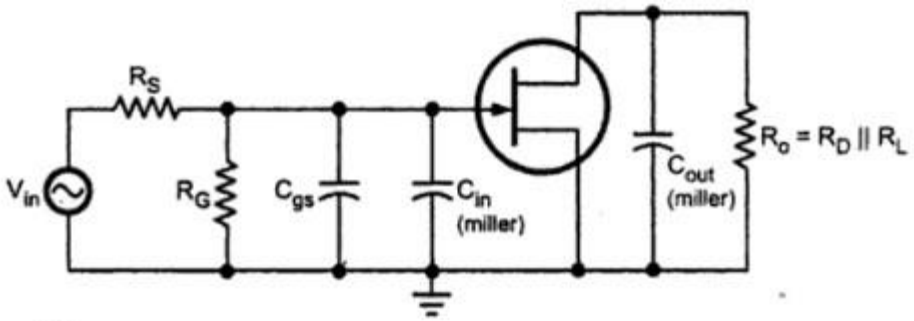


Fig 3.13 lified high frequency equivalent circuit

where

$$C_{in\ (miller)} = C_{gd}\,(A_v + 1)$$

$$C_{out\ (miller)} = C_{gd}\,\frac{(A_v + 1)}{(A_v)}$$

3.7 Multistage amplifiers

It has been observed that the voltage (or power) gain, obtained from a single stage small signal amplifier, is limited. Moreover, it is not sufficient for all practical applications. Therefore in order to achieve greater voltage and power gain, we have to use more than one stage of amplification. Such an amplifier is called a *multistage amplifier*. It will be interesting to know that when we use multistage amplifier, then we feed the output of one stage to the input of the next as shown in Figure 4.26. Such a connection of amplifiers is called *cascading*. The amplifier used in radio and television receivers is, usually, a multistage amplifier.

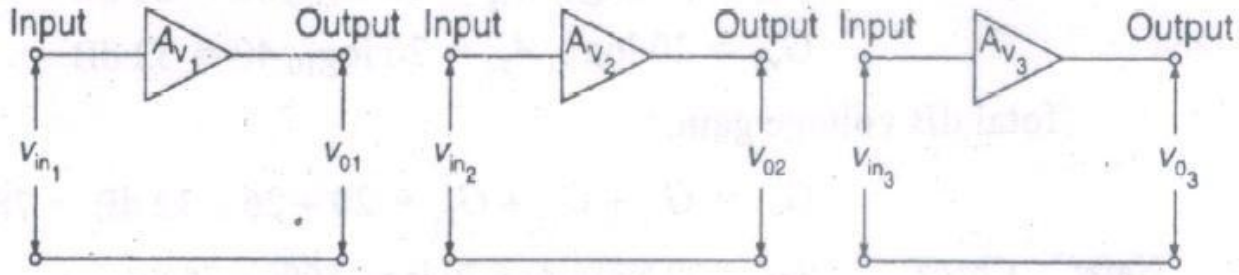


Fig 3.14 i. A general multistage amplifier.

3.7.1 Gain of a multistage amplifiers

We have already discussed in the last article that in a multistage amplifier the output voltage of the first stage acts as an input voltage to the second stage. And the output voltage of second stage as an input to the third stage and so on. *The voltage gain of a multistage amplifier is equal to the product of the gains of the individual stages*. Thus if A_{v_1}, A_{v_2} and A_{v_3} are the individual stage gains, then overall voltage gain,

$$A_v = A_{v_1} \times A_{v_2} \times A_{v_3}$$

The amplifier voltage gain may also be expressed in decibels (dB). However, in that case the overall decibel voltage gain is the sum of the decibel gains of the individual stages. Thus if G_{v_1}, G_{v2} and G_{v3} are the individual stage decibel gains, then overall decibel voltage gain,

$$\begin{aligned} G_v &= G_{v_1} + G_{v_2} + G_{v_3} \\ &= 20 \log_{10} A_{v_1} + 20 \log_{10} A_{v_2} + 20 \log_{10} A_{v_3} \\ &= 20 \log_{10} A_v \text{ (dB)} \end{aligned}$$

Similarly, the overall current amplification,

$$A_i = A_{i_1} \times A_{i_2} \times A_{i_3}$$

Then the overall power gain,

$$A_p = A_v \cdot A_i$$

and the overall decibel power gain,

$$G_p = 10 \log_{10} A_p$$

Example *A given amplifier arrangement has the following voltage gains. $A_{v1} = 10$, $A_{v2} = 20$ and $A_{v3} = 40$. What is the overall voltage gain? Also express each gain in dB and determine the total dB voltage gain.*

Solution. Given: $A_{v_1} = 10$; $A_{v_2} = 20$ and $A_{v_3} = 40$

Overall voltage gain

We know that the overall voltage gain,

$$A_v = A_{v1} \times A_{v2} \times A_{v3} = 10 \times 20 \times 40 = 8000 \textbf{ Ans.}$$

Total dB voltage gain

We know that dB voltage gain of the first stage

$$G_{v1} = 20 \log_{10} A_{v_1} = 20 \log_{10} 10 = 20 \text{ dB}$$

Similarly, $$G_{v2} = 20 \log_{10} A_{v_2} = 20 \log_{10} 20 = 26 \text{ dB}$$

and $$G_{v3} = 20 \log_{10} A_{v_3} = 20 \log_{10} 40 = 32 \text{ dB}$$

$\therefore$ Total dB voltage gain,

$$G_v = G_{v_1} + G_{v_2} + G_{v_3} = 20 + 26 + 32 \text{ dB} = 78 \text{ dB}$$ **Ans.**

Note: Check $G_v = 20 \log_{10} A_v = 20 \log_{10} 8000 = 78$ dB.

3.7.2 Need for multistage amplifiers

- **When the amplification of a single stage amplifier is not sufficient, or,**
- **When the input or output impedance is not of the correct magnitude, for a particular application two or more amplifier stages are connected, in cascade. Such amplifier, with two or more stages is also known as multistage amplifier.**

3.8 Methods of interconnecting multistage amplifiers

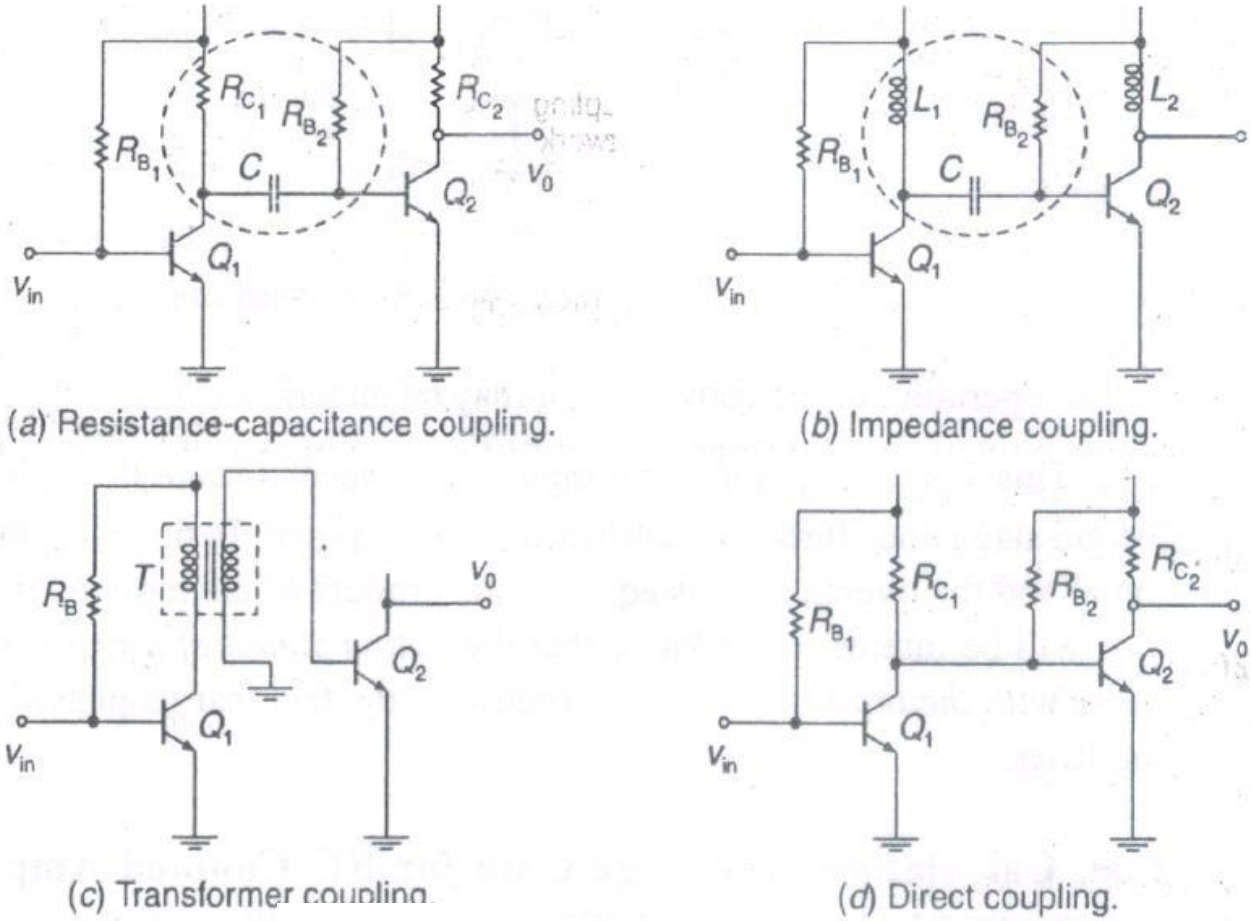
As a matter of fact, all amplifiers, need some kind of *coupling* network. Even a single stage amplifier, needs coupling to the input source and output load. The multistage amplifiers need coupling between their individual stages. This type of coupling is called interstage coupling. It serves the following two purposes:

1. It transfers a.c. output of one stage to the input of the next stage.
2. It isolates the d.c. conditions of one stage to the next. It is necessary to prevent the shifting of Q-points.

The coupling network (or coupling device) must ensure that both the above purposes are fulfilled, when an a.c. signal is to be amplified. Following are the four coupling schemes used in amplifiers.

1. *Resistance-capacitance (RC) coupling*. It is the most important method of coupling the signal from one stage to the next and is shown in Figure 4.27 (a). In this method, the signal developed across the collector resistor of each stage is coupled through capacitor into the base of the next stage. The cascaded stages amplify the signal and the overall gain is equal to the product of individual stage gains. The amplifiers, using this coupling scheme, are called *RC-coupled amplifiers*.

2. *Impedance coupling*. This coupling is shown in Figure 4.27 (*b*). It may be noted that the collector resistor (R_C) is replaced by an inductor (L). As the frequency increases, inductive reactance X_L (equal to $\omega \cdot L$) approaches infinity and each inductor appears open. In other words, the inductors pass direct current but block alternating current. The amplifiers, using this coupling scheme, are called *impedance-coupling amplifiers*.



(*a*) Resistance-capacitance coupling. (*b*) Impedance coupling.

(*c*) Transformer coupling (*d*) Direct coupling.

Fig 3.15 Coupling schemes in amplifiers.

3. *Transformer coupling*. This coupling is shown in Figure 4.27 (*c*). In this method, primary winding of the transistor acts as a collector load and the secondary winding conveys the a.c. output signal directly to the base of the next stage. It may be noted that there is no need of coupling capacitor in the transformer coupling. The amplifiers, using this coupling scheme, are called *transformer-coupled amplifiers*.

4. *Direct-coupling*. This coupling is shown in Figure 4.27 (*d*). In this method, the a.c. output signal is fed directly to the next stage. This type of coupling is used where low frequency signals are to be amplified. The coupling devices such as capacitors, inductors and transformers cannot be used at low frequencies because their size becomes very large. The amplifiers, using this coupling scheme, are called *direct coupled amplifiers or d.c. amplifiers*.

3.8.1 Comparison of different coupling methods

Parameter	RC Coupled	Transformer Coupled	Direct Coupled
Coupling Components	Resistor and Capacitor	Impedance matching transformer	–
Block DC	Yes	Yes	No
Frequency response	Flat at middle frequencies	Not uniform, high at resonant frequency and low at other frequencies	Flat at middle frequencies and improvement in the low frequency response
Impedance matching	Not achieved	Achieved	Not achieved
DC amplification	No	No	Yes
Weight	Light	Bulky and heavy	
Drift	Not present	Not present	Present
Hum	Not present	Present	Not present
Application	Used in all audio small signal amplifiers. Used in record players, tape recorders, public address systems, radio receivers and television receivers.	Used in amplifier where impedance matching is an important criteria. Used in the output stage of the pubic address system to match the impedance of loudspeaker. Used in the RF amplifier stage of the receiver as a tuned voltage amplifier.	Used in amplification of slow varying parameters and where DC amplification is required.

3.9 Types of Multistage amplifiers

- RC coupled Amplifiers (or) Cascade amplifier
- Direct Coupled Amplifiers
- Transformer Coupled Amplifiers
- Cascode amplifier
- Darlington Emitter Follower Amplifier

3.10 Two stage RC Coupled amplifiers (or) Cascade amplifier

Figure 4.28 shows a two-stage RC coupled transistor amplifier. The circuit consists of two single-stage common emitter transistor amplifiers. The resistors R_C, R_B and capacitor C_C form the coupling network. The capacitor C_1 is used to couple the input signal to the base of Q_1, while the capacitor C_2 is used to couple the output signal from the collector of Q_2 to the load. The capacitor C_E, connected at the emitters of Q_1 and Q_2, are needed because they *bypass* the emitter to the ground. Without these capacitors, the voltage gain of each stage will be lost.

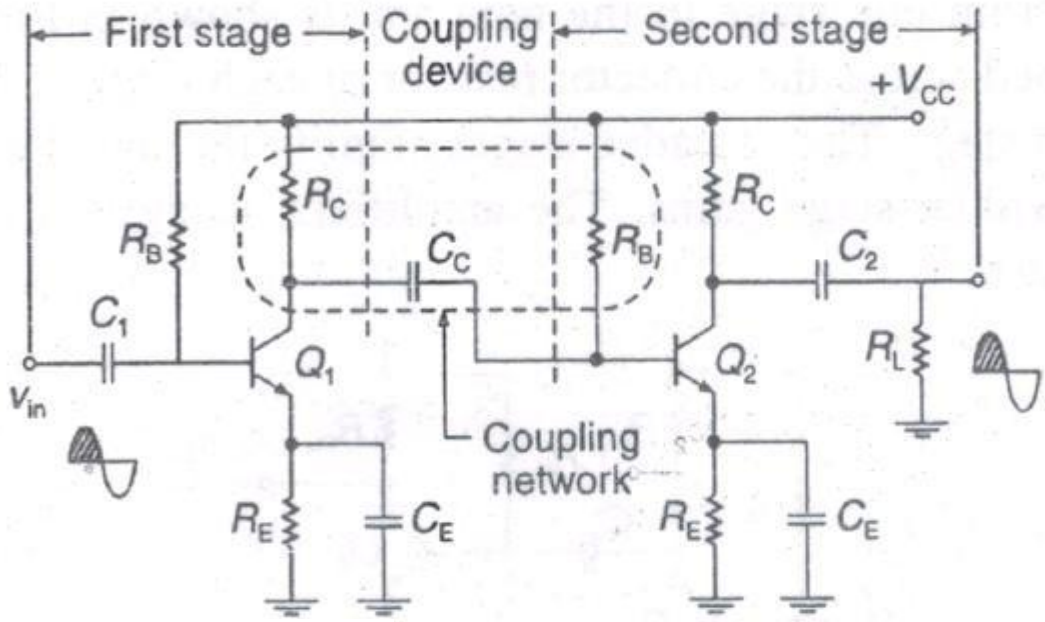
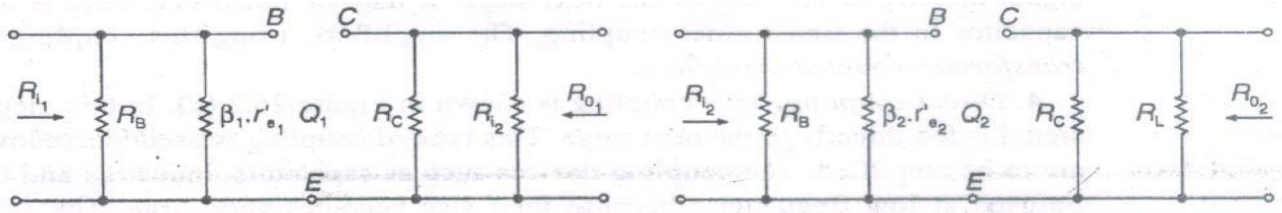


Fig 3.16 RC coupled amplifier.

The operation of the above circuit may be understood as follows: When an a.c. signal is applied to the input of the first stage, it is amplified by a transistor and appears across the collector resistor (R_C). This signal is given to the input of the second stage through a coupling capacitor C_C. The second stage does further amplification of the signal. In this way, the cascaded stages amplify the signal and the overall gain is equal to the product of the individual stage gains.

It will be interesting to know that the *output signal of a two-stage RC coupled amplifier is in phase with the input signal*. It is because of the fact that its phase has been reversed twice by the amplifier.

3.10.1 Calculation of Voltage Gain for RC Coupled Amplifier



(*a*) A.C. equivalent circuit for first stage. (*b*) A.C. equivalent circuit for second stage.

Fig 3.17 A.C. equivalent circuit of a two-stage RC coupled amplifier.

The parameters r'_{e1} and r'_{e2} represent the a.c. emitter diode resistances of the transistors Q_1 and Q_2 respectively. The values of r'_{e1} and r'_{e2} may be obtained from the relations,

$$r'_{e1} = \frac{25}{I_{E_1}} \quad \text{and} \quad r'_{e2} = \frac{25}{I_{E_2}}$$

where I_{E_1} and I_{E_2} are the values of emitter current in milliamperes. Now the input resistance of the first stage as seen from the Figure 26.4 (*a*),

$$R_{i_1} = R_B \parallel (\beta_1 \cdot r'_{e1}) = \beta_1 \cdot r'_{e1} \qquad \text{... (If } R_B >> \beta_1 \cdot r'_{e1})$$

and the output resistance,

$$R_{o_1} = R_C \parallel R_{i_2}$$

where R_{i_2} is the input resistance of the second stage and its value is given by the relation,

$$R_{i_2} = R_B \parallel (\beta_2 \cdot r'_{e2}) = \beta_2 \cdot r'e_2 \qquad \text{... (If } R_B >> \beta_2 \cdot r'_{e2})$$

The output resistance of the second stage,

$$R_{o_2} = R_C \parallel R_L$$

Now the voltage gain of the first stage,

$$A_{v_1} = \beta_1 \times \frac{R_{o_1}}{R_{i_1}} = \beta_1 \times \frac{R_{o1}}{\beta_1 \cdot r'_{e_1}} = \frac{R_{o_1}}{r'_{e_1}}$$

Similarly, voltage gain of the second stage,

$$A_{v_2} = \frac{R_{o_2}}{r'_{e_2}}$$

$\therefore$ Overall voltage gain of the amplifier,

$$A_v = A_{v_1} \cdot A_{v_2} = \frac{R_{o_1}}{r'_{o_1}} \times \frac{R_{o_2}}{r'_{o_2}}$$

If the transistors used in both the stages are identical, then current gain of the transistors Q_1 and Q_2 (*i.e.*, β_1 and β_2) will be equal. In that case, the emitter currents will also be equal. Thus $r'_{e_1} = r'_{e_2} = r_e$. Then overall voltage gain,

$$A_v = R_{o_1} \cdot R_{o_2} / r_e^2$$

3.10.2 Frequency Response of RC Coupled Amplifier

The frequency response of an amplifier is a graph, which indicates the relationship between the voltage gain as a function of frequency. Usually, the voltage gain (in decibels) is plotted along the vertical axis and the frequency (in hertz or kilohertz) along the horizontal axis of the frequency response graph. Figure 4.30 shows the frequency response of RC coupled amplifier.

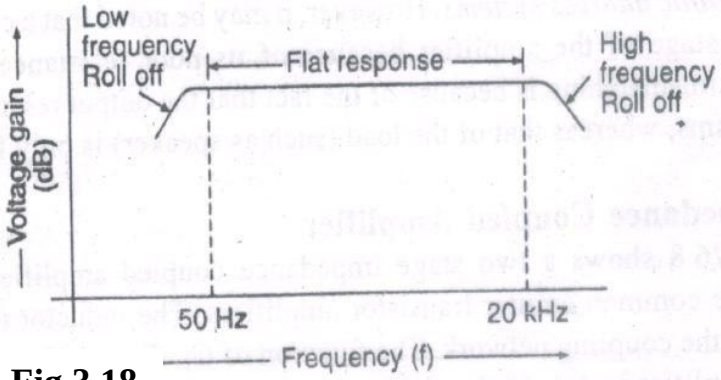


Fig 3.18 Frequency response of RC coupled amplifier.

It is evident from the graph that the voltage gain *drops off* (or rolls off) at low frequencies (*i.e.*, frequencies below 50 Hz) and at high frequencies (*i.e.*, frequencies above 20 kHz), while it remains *constant* in the mid-frequency range. The behaviour is discussed in more detail as follows:

1. *At low frequencies (i.e., below 50 Hz).* We know that the capacitive reactance (X_C) is inversely proportional to the frequency. Thus at low frequencies, the reactance of the capacitor C_C is quite large. Therefore it will allow only a small part of the signal to pass from one stage to the next stage. In addition to this, the emitter bypass capacitor (C_E) cannot shunt the emitter resistor effectively, because of its large reactance at low frequencies. As a result of these two factors, the voltage gain rolls off at low frequencies.

2. *At high frequencies (i.e., above 20 kHz).* In this frequency range, the reactance of capacitor C_C becomes quite small, therefore it behaves like a short-circuit. As a result of this, the loading effect of the next stage increases, which reduces the voltage gain. In addition to this, the capacitance of the emitter diode plays an important role at high frequencies. It increases the base current of the transistor due to which the *current gain (β) reduces*. Hence the voltage gain rolls off at high frequencies.

3. *At mid-frequencies (i.e., 50 Hz to 20 kHz).* The effect of coupling capacitor, in this frequency range, is such that it maintains a constant voltage gain. Thus as the frequency increases, the reactance of capacitor C_C decreases, which tends to increase the gain. However, at the same time, the lower capacitive reactance increases the loading effect of the next stage due to which the gain reduces. These two factors almost cancel each other. Thus a constant gain is maintained throughout this frequency range.

3.10.3 Advantages and Disadvantages of RC Coupled Amplifier

Advantages

1. It is the most convenient and least expensive multistage amplifier.
2. It has a wide frequency response *i.e.*, its gain versus frequency curve remains constant over a wide frequency range.
3. It provides less frequency distortion.

Disadvantages

1. The overall gain of the amplifier is comparatively small because of the loading effect of successive stages.
2. It has a tendency to become noisy with age, especially in moist climates.
3. It provides poor resistance (or impedance) matching between the stages.

3.11 Two stage Transformer Coupled Amplifiers

Figure 4.31 shows a two-stage transformer coupled amplifier. The circuit consists of two single-stage common emitter transistor amplifiers. The function of transformer (T_1) is to couple the a.c. output signal from the output of the first stage to the input of the second stage, while transformer (T_2) couples the output signal to the load. The input coupling capacitor is C_1, while the emitter bypass capacitor is C_E,

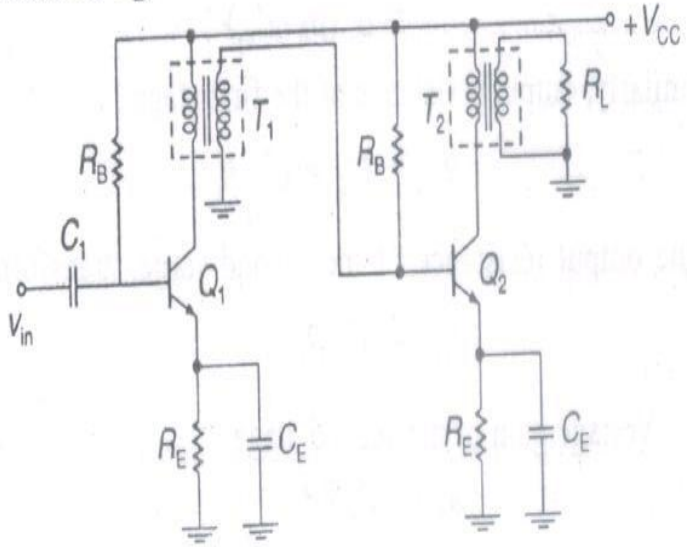
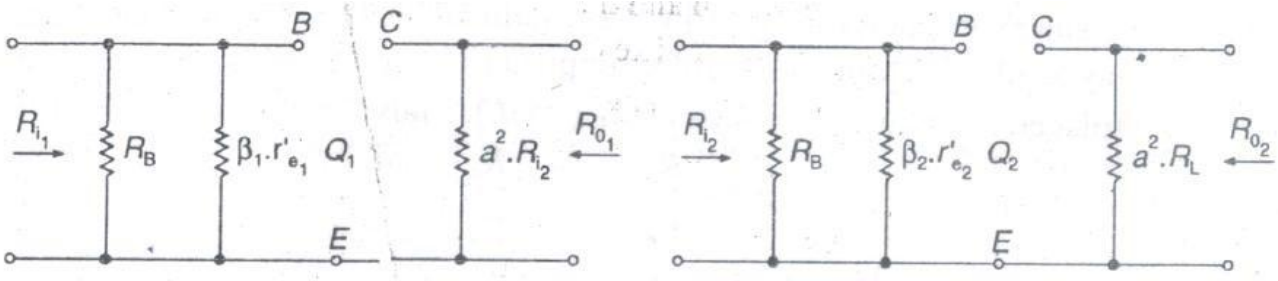


Fig 3.19 Two stage Transformer Coupled Amplifier

The operation of the above circuit may be understood from the condition that when an a.c. input signal is applied to the base transistor Q_1, it appears in the amplified form across primary winding of the transformer (T_1). The voltage developed across the primary winding is then transferred to the input of the next stage by the secondary winding of the transformer (T_1). The second stage does amplification in an exactly similar manner.

In actual practice, a by pass capacitor is used on the bottom of each primary winding to produce an a.c. ground. This avoids the load inductance of the connecting line that returns to the d.c. supply point. Similarly, a bypass capacitor is used on the bottom of each secondary winding to get an a.c. ground. This prevents the signal power loss in the biasing resistors.

3.11.1 Calculations of Voltage Gain for Transformer Coupled Amplifier



(*a*) For first stage. (*b*) For second stage.

A.C. equivalent circuit for two stage transformer coupled amplifier.

Fig 3.20

C ircuit of a two-stage transformer coupled amplifier shown in Figure 4.31. The a.c. equivalent circuit for the amplifier is shown in Figure 4.32 (*a*) and (*b*). In these figures, the a.c. equivalent circuit of the transistor is shown by the a.c. emitter diode resistance and three points marked *E*, *B* and *C*. Assuming the transformer to be an ideal (*i.e.*, neglecting its leakage current, winding resistance etc.), whatever be the load on its secondary winding side, it transforms the same on the primary side. The value of the transformed load,

$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = a^2 \cdot R_L \quad \ldots \left(\text{where a} = \frac{N_1}{N_2}\right)$$

where N_1 = Number of primary turns, and

N_2 = Number of secondary turns.

Similarly, if R_{i_2} is the input resistance of the second stage, then its value transformed to the primary side,

$$R'_{i_2} = a^2 \cdot R_{i_2}$$

We know that the input resistance of the first stage is given by the relation,

$$R_{i_1} = R_B \parallel (\beta_1 \cdot r'_{e_1}) \quad \ldots (\text{If } R_B >> \beta_1 \cdot r'_{e_1})$$

and the input resistance of the second stage, transformed to the primary side,

$$R'_{i_2} = a^2 \cdot R_{i_2} = a^2 \cdot R_B \parallel (\beta_2 \cdot r'_{e_2})$$

$$= a^2 (\beta_2 \cdot r'_{e_2}) \quad \ldots (\text{If } R_B >> \beta_2 \cdot r'_{e2})$$

Similarly, output resistance of the first stage,

$$R_{o_1} = R'_{i_2} = a^2 \cdot R_{i_2}$$

and the output resistance of the second stage, transformed to the primary side,

$$R_{o_2} = a^2 \cdot R_L$$

∴ Voltage gain of the second stage,

$$A_{v_1} = R_{o_1} / r'_{e_1}$$

and voltage gain of the second stage,

$$A_{v2} = \frac{R'_{o_2}}{r'_{e_2}} = \frac{a^2 \cdot R_L}{r'_{e_2}}$$

$\therefore$ Overall voltage gain,

$$A_v = A_{v1} \cdot A_{v2} = \frac{R_{o_1}}{r'_{e_1}} \times \frac{a^2 \cdot R_L}{r'_{e_2}}$$

3.11.2 Frequency Response of Transformer Coupled Amplifier

Figure 4.33 shows the frequency response graph (*i.e.*, a graph of voltage gain *versus* frequency) for a transformer coupled transistor amplifier.

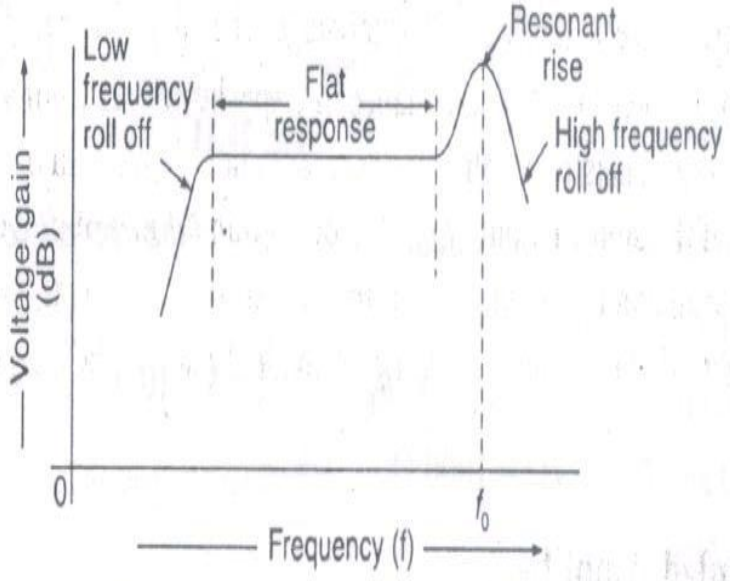


Fig 3.21 Frequency response of a transformer coupled amplifier.

It is evident from this figure, that the voltage gain drops off (or rolls off) at low as well as at high frequencies , whereas it remains constant in mid-frequency range. Another noticeable feature is that *at one particular frequency (f_0) the voltage gain increases and then rolls off continuously*. This typical behaviour may be explained as follow:

We know that output voltage of a transformer coupled amplifier is equal to the product of collector current and the reactance of the primary winding of coupling transformer. At low frequencies, the reactance of primary winding ($X_L = \omega \cdot L$) begins to decrease, and hence the voltage gain reduces. At high frequencies, the effect of leakage inductance and distributed capacitance (*i.e.*, the capacitance between the turns of the winding) becomes significant and hence the voltage gain reduces. *The peak gain results due to the resonance (or turning) effect of inductance and distributed capacitance, which forms a resonant circuit*. The frequency, at which the peak occurs, is called resonant frequency (f_0).

It has been found that flat part of frequency response curve of transformer coupled amplifiers is small as compared to that of RC coupled amplifiers. As a result of this, *these amplifiers can not be used over a wide range of frequencies*. Moreover, if they are used, *they produce frequency distortion*, which means that all frequency components in a complete input signal (such as music, speech signal) are not equally amplified. However, the transformers can be suitably designed to provide a fairly flat response curve and excellent fidelity over the entire audio frequency range (*i.e.*, 20 Hz to 20 kHz).

3.11.3 Advantages and Disadvantages of Transformer Coupled Amplifier

Advantages

1. No signal power is lost in the collector or base resistors, because of the low winding resistance of the transformer.
2. It provides a higher voltage gain than the RC coupled amplifier.
3. It provides an excellent resistance (or impedance) matching between the stages. The resistance matching is desirable for maximum power transfer.

Disadvantages

1. The coupling transformer is expensive and bulky, particularly when operated at audio frequencies.
2. At radio frequencies, the winding inductance and distributed capacitance produces reverse frequency distortion.
3. It tends to produce '*hum*' in the circuit.

Fig 3.22

3.12 Two stage Direct Coupled Amplifier

3.12.1 Calculation of Voltage Gain of Direct Coupled Amplifier

Consider the circuit diagram of a. direct coupled amplifier shown in Figure 4.34. The a.c equivalent circuit for such an amplifier is shown in Figure 4.35.

It is also called as *DC amplifier* and is used to *amplify very low frequency* (*i.e.*, below 10 Hz) signals including direct current or zero frequency. It may be noted that the capacitors, inductors and transformers can not be used as a coupling network at very low frequencies because the electrical size of these devices, at low frequencies, becomes very large.

Figure 4.34 shows a two-stage direct coupled transistor amplifier. It may be noted that the output of the first stage is directly connected to the base of the next transistor. Moreover, there are no input or output coupling capacitors. The operation of this circuit is discussed below:

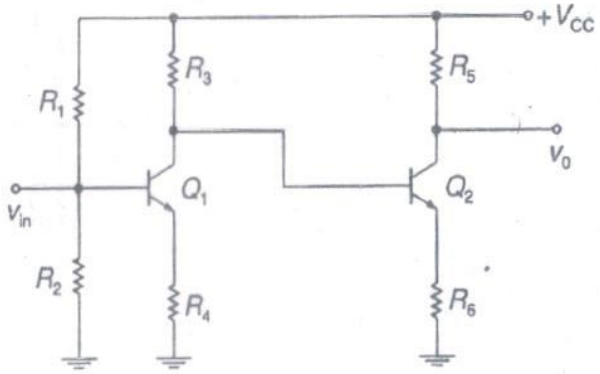


Fig 3.22 Two stage direct coupled amplifier.

The signal to be amplified is applied directly to the input of the first stage. Due to the transistor action, it appears in the amplified form across the collector resistor or transistor Q_1. This voltage then drives the base of the second transistor Q_2 and the amplified output is obtained across the collector resistor of transistor Q_2.

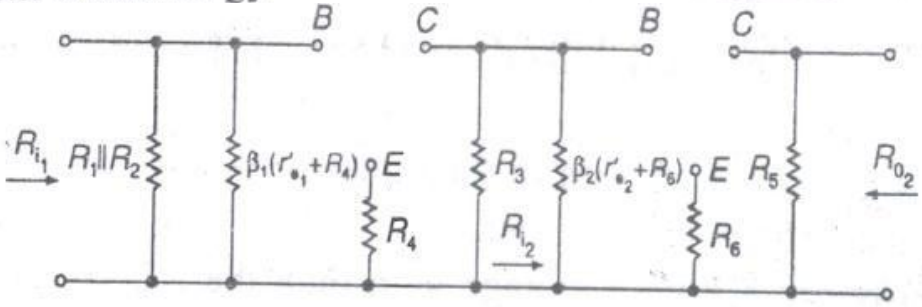


Fig 3.23 A.C. equivalent circuit of a two stage direct coupled amplifier.

It is evident from the figure shown above that the input resistancc of the first stage,

$$R_{i_1} = (R_1 \parallel R_2) \parallel \beta_1 (r'_{e_1} + R_4)$$

and input resistance of the second stage,

$$R_{i_2} = \beta_2 (r'_{e_2} + R_6)$$

Similarly, the output resistance of the first stage,

$$R_{o_1} = R_3 \parallel R_{i_2}$$

and output resistance of the second stage,

$$R_{o_2} = R_5$$

∴ Voltage gain of the first stage,

$$A_{v_1} = \beta \times \frac{R_{o_1}}{R_{i_1}} = \frac{R_{o_1}}{r'_{e1} + R_4}$$

and voltage gain of the second stage,

$$A_{v_2} = \beta_2 \times \frac{R_{o_2}}{R_{i_3}} = \frac{R_{o_2}}{r'_{e2} + R_4}$$

Now the overall voltage gain is given by the relation,

$$A_v = A_{v_1} \cdot A_{v_2}$$

3.12.2 Frequency Response of Direct Coupled Amplifier

Figure 4.36 shows the frequency response (*i.e.*, a graph of dB voltage gain versus frequency) of a direct coupled amplifier. It is evident from this figure, the *gain is uniform up to a certain frequency denoted by f_2. Beyond this frequency, the gain rolls off slowly.* The gain rolls off at high frequencies due to the increased emitter diode capacitance and stray wiring capacitance.

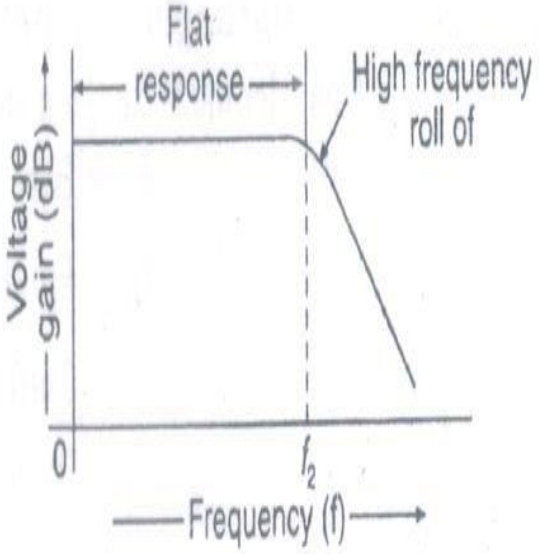


Fig 3.24 Frequency response of direct coupled amplifier.

4.12.3 Advantages and Disadvantages of Direct Coupled Amplifier Advantages

1. The circuit arrangement is very simple because it uses a minimum number of resistors.
2. The circuit cost is low because of the absence of expensive coupling devices.
3. It can amplify very low frequency signals down to zero frequency.

Disadvantages

1. It cannot amplify high frequency signals.
2. It has poor temperature stability. Because of this, its, Q-point shifts. In a multistage direct coupled amplifier, the Q-point shifts are amplified in succeeding stages. Thus a small d.c. shift, in the first stage can cause the final stage to be either saturated or cut- off. All integrated circuit amplifiers are direct coupled because of the difficulty of fabricating large integrated capacitors.

3.12.4 Applications of Direct Coupled Amplifiers

The direct coupled amplifiers are used in many electronic systems that handle signals, which change very slowly with time. Some of the important applications are as given below.

1. Analog computation.
2. Power supply regulators.
3. Bioelectric measurements.
4. Linear integrated circuits.

3.13 Darlington Emitter Follower Amplifier

The Darlington Amplifier consists of two cascaded emitter followers as shown in Figure 4.36. The configuration results in a set of improved amplifier characteristics.

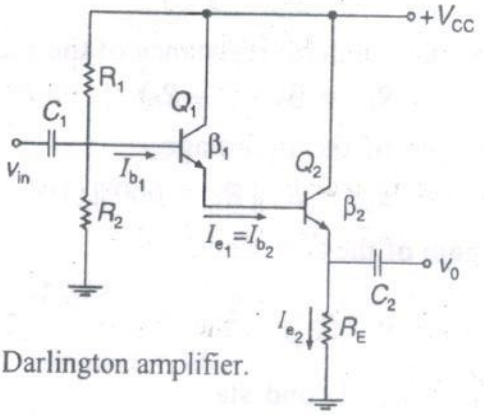


Fig 3.25 Darlington amplifier.

The Darlington amplifier has a high input resistance, low output resistance and high current gain. These characteristics make it very useful as a current amplifier. The voltage gain of a Darlington amplifier is less than unity.

3.13.1 Darlington Amplifier Characteristics

Consider the Darlington amplifier circuit shown in Figure 4.36.

Let I_{b_1} = Base current of Q_1 transistor,

I_{e_1} = Emitter current of Q_1 transistor,

β_1 = Current gain of Q_1 transistor,

I_{b_2} = Base current of Q_2 transistor. Its value is equal to the emitter current of Q_1 transistor,

I_{e_2} = Emitter current of Q_2 transistor, and

β_2 = Current gain of Q_2 transistor.

1. *Current gain*. We know that the emitter current of Q_2 transistor,

$$I_{e_1} = \beta_1 \cdot I_{b_1}$$

and emitter current of Q_2 transistor,

$$I_{e_2} = \beta_2 \cdot I_{b_2} = \beta_2 \cdot I_{e_1} \quad \ldots (\because I_{b_2} = I_{e_1})$$

$$= \beta_2 (\beta_1 \cdot I_{b_1}) \quad \ldots (\because I_{e_1} = \beta_1 \cdot I_{b_1})$$

$$= \beta_1 \cdot \beta_2 \cdot I_{b_1} = \beta^2 \cdot I_{e_1}$$

Now let both the transistors used in the amplifier be identical. Then current gain β_1 and β_2 will be equal. In that case, emitter current of Q_2 transistor

Now let both the transistors used in the amplifier be identical. Then current gain β_1 and β_2 will be equal. In that case, emitter current of Q_2 transistor,

$$I_{e_2} = \beta^2 \cdot I_{b_1} \quad \ldots (\because \beta_1 = \beta_2 = \beta^2)$$

$\therefore$ Overall current gain,

$$A_I = \frac{I_{e_2}}{I_{b_1}} = \beta^2$$

2. *Input resistance.* We know that input resistance of the second stage is given by the relation,

$$R_{i_2} = \beta_2 (r'_{e_2} + R_E)$$
$$= \beta_2 \cdot R_E \quad \ldots (\text{If } R_E \quad r_{e2})$$

It is the value of resistance seen by the emitter of Q_1 transistor and is given by the relation,

$$R'_{i_1} = \beta_1 (r'_{e_1} + R_{i_2})$$
$$= \beta_1 \cdot R_{i_2} \quad \ldots (\text{If } R_{i_2} >> r'_{e_1})$$
$$= \beta_1 \cdot \beta_2 \cdot R_E \quad \ldots (\because R_{i2} = \beta_2 \cdot R_E)$$

For identical transistor, we know that current gain β_1 and β_2 are also equal. Therefore input resistance,

$$R'_{i_1} = \beta^2 \cdot R_E$$

and input resistance of the amplifier stage,

$$R_{i_1} = (R_1 \parallel R_2) \parallel R'_{i_1} = (R_1 \parallel R_2) \parallel \beta^2 \cdot R_E$$

$$= R_1 \parallel R_2 \quad \ldots (\because (R_1 \parallel R_2) << \beta^2 \cdot R_E)$$

3. *Output resistance*. The output resistance of the first stage is given by the relation,

$$R_{o_1} = r'_{e_1} + \frac{R_1 \parallel R_2}{\beta_1}$$

and output resistance of the second stage,

$$R_{o_2} = r'_{e_2} + \frac{R_{o_1}}{\beta_2}$$

$$= r'_{e_2} + \frac{r'_{e_1} + \dfrac{R_1 \parallel R_2}{\beta_1}}{\beta_2}$$

$$= r'_{e_2} + \frac{r'_{e_1}}{\beta_2} + \frac{R_1 \parallel R_2}{\beta_1 \cdot \beta_2}$$

$$= r'_{e_2} \quad \ldots (\because \frac{r'_{e1}}{\beta_2} \text{ and } \frac{(R_1 \parallel R_2)}{\beta_1 \cdot \beta_2} \text{ are negligible})$$

4. *Voltage gain*. The voltage gain of Darlington amplifier is given by the relation,

$$A_v = \frac{v_o}{v_{in}} \quad \ldots (i)$$

The value of output voltage of a Darlington amplifier,

$$v_o = I_{e_2} \cdot R_E$$

and the input voltage,

$$v_{in} = I_{e_1} \cdot r'_{e_1} + I_{e_2}(r'_{e_2} + R_E) \quad \ldots (ii)$$

The above expression is obtained by applying Kirchoff's Voltage Law to the input circuit of the Darlington amplifier. Substituting the value of I_{e_1} (equal to I_{e2}/β_2) in equation (ii)

$$v_{in} = \frac{I_{e_2}}{\beta_2} r'_{e_1} + I_{e_2}(r'_{e_2} + R_E)$$

$\therefore$ Voltage gain,

$$A_v = \frac{I_{e_2} \cdot R_E}{\dfrac{I_{e_2}}{\beta_2} \cdot r'_{e_1} + I_{e_2}(r'_{e_2} + R_E)} = \frac{R_E}{\dfrac{r'_{e_1}}{\beta_2} + (r'_{e_2} + R_E)}$$

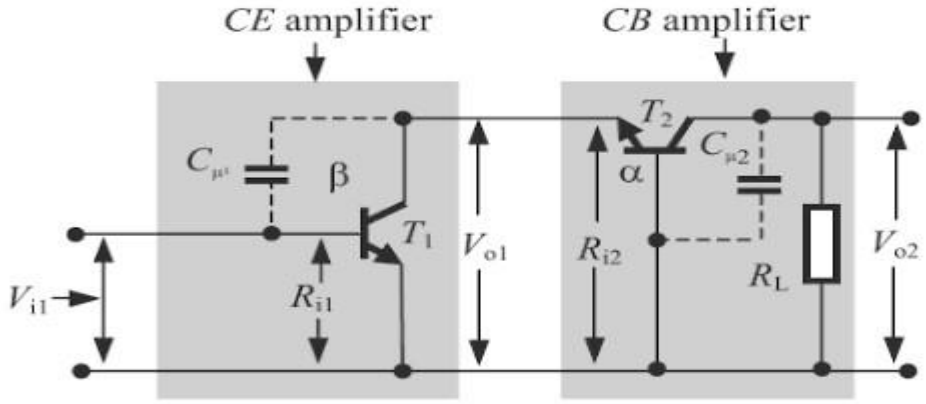
$$\approx 1 \quad \ldots (\because R_E >> r'_{e_2} \text{ or } r'_{e1}/\beta_2)$$

3.14 Cascode amplifier

An amplifier consisting of a common emitter input stage that drives a common base output stage.

Figure 4.37 show the cascode-amplifier configuration using BJT's. In this case, a common-emitter amplifier drives a common-base amplifier. It is a well-known fact that, at higher frequencies, the gain of the *RC*-coupled amplifier drops. This is because of the shunting effect of the Miller capacitance C_μ and the emitter-base capacitance C_π. With cascode connection, the effect of the Miller capacitance can be seen to get reduced; as a result, the high-frequency cut off gets extended by a factor of about 10.

Figure 4.37 shows the basic cascode amplifier circuit. As shown in the figure, and as stated above, a cascode amplifier consists of a *CE* amplifier driving a *CB* amplifier. To make a simplified analysis of the cascode amplifier, assume that the current gain (*CE*) of transistor T_1 is β and that (*CB*) of transistor T_2 is α. From basic principles, we find that for the *CE* stage.



Cascode amplifier using BJT's

Fig 3.26

$$A_{V1} = \beta \frac{R_{o1}}{R_{i1}} \qquad (1)$$

where A_{V1} = voltage gain, R_{i1} = input impedance and R_{o1} = output impedance of the *CE* stage. Similarly, we have

$$A_{V2} = \alpha \frac{R_{o2}}{R_{i2}} \qquad (2)$$

where A_{V2} = voltage gain, R_{i2} = input impedance and R_{o2} = output impedance of the CE stage. From Fig. 4.37 , we find that $R_{o2} = R_L$. Using Eqs. (1) and (2), we get the overall gain of the cascode amplifier as

$$A_V = A_{V1} \times A_{V2} = \beta_1 \frac{R_{o1}}{R_{i1}} \times \alpha_2 \frac{R_L}{R_{i2}} \tag{3}$$

But, we see from Fig. 4.37 that $R_{i2} = R_{o1}$. Also, we have $\alpha_2 = 1$. Then, we get

$$A_V = \beta_1 \times \frac{R_L}{R_{i1}} \tag{4}$$

From Eq. (4), we find that the gain of the cascode amplifier is equal to that of a single stage of the CE amplifier.

Even though the cascode amplifier has a gain equal to that of a CE amplifier, we find that its high-frequency region of operation extends beyond that of the CE amplifier. This is because, as stated before, the parasitic Miller capacitances ($C_{\mu 1}$ and $C_{\mu 2}$) of the two transistors are not directly connected, as can be seen from Fig. 4.37 . This prevents direct feedback connection between the output and the input of the cascode amplifier.

3.15 Comparison of Cascade and Cascode amplifier

Cascade amplifier	Cascode amplifier
Combination of two or more transistor's in any of the configuration.	combination of common collector and Common base configuration
output of the first amplifying device (transistor) is fed as input to the second amplifying device	An amplifier consisting of a common emitter input stage that drives a common base output stage.

3.16 Introduction to Large Signal Amplifiers

Consider a public address system (P.A.) or amplifying system as shown in the Fig. 5.1.

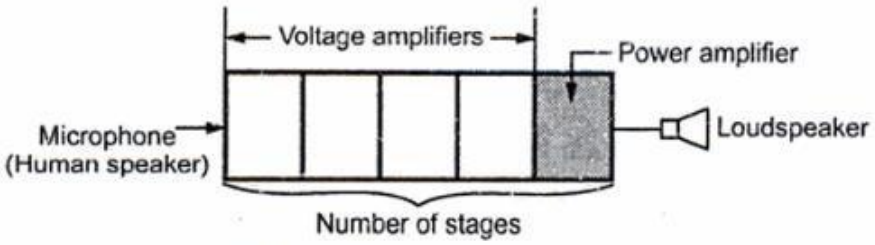


Fig 3.27 Amplifying or P.A. system

The system consists of many stages connected in cascade. Hence basically it is a multistage amplifier. The input is sound signal of a human speaker and the output is given to the loudspeaker which is an amplified input signal. The input and the intermediate stages are small signal amplifiers. The sufficient voltage gain is obtained by all the intermediate stages. Hence these stages are called **voltage amplifiers**.

But the last stage gives an output to the load like a loud speaker. Hence the last stage must be capable of delivering an appreciable amount of a.c. power to the load. So it must be capable of handling large voltage or current swings or in other words large signals. The main aim is to develop sufficient power hence the voltage gain is not important, in the last stage. Such a stage, which develops and feeds sufficient power to the load like loudspeaker, servomotor, handling the large signals is called **Large Signal Amplifier** or **Power Amplifier.**

Power amplifiers find their applications in the public address systems, radio receivers, driving servomotor in industrial control systems, tape players, T.V. receivers, cathode ray tubes etc.

3.17 Comparison of Voltage Amplifiers and Power amplifiers

sl.no	Characteristics	Voltage Amplifier	Power Amplifier
1	Current Gain	High, exceeding 100	Low 20-50
2	Collector Load	High about 10KΩ	Low 5-20Ω
3	Input Voltage	Low, a few mV	High, 2-4V
4	Collector Current	Low about 1mA	High exceeding 100mA
5	Power output	Low	High
6	Power dissipation capacity	Less than 0.5W	More than 0.5W
7	Output Impedence	High about 10KΩ	Low about 200Ω
8	Coupling	Usually RC coupling	Transformer or tuned circuit

3.18Features of Power Amplifiers

The various features of power amplifiers are,

1. A power amplifier is the last stage of multistage amplifier. The previous stages develop sufficient gain and the **input signal level or amplitude of a power amplifier is large** of the order of few volts.
2. The **output of power amplifier has large current and voltage swings.** As it handles large signals called power amplifiers.
3. **The h-parameter analysis** is applicable to the small signal amplifiers and hence **cannot be used for the analysis of power amplifiers**. The analysis of power amplifiers is carried out graphically by drawing a load line on the output characteristics of the transistors used in it.
4. The power amplifiers i.e large signal amplifiers are used to feed the loads like loudspeakers having low impedance. So for maximum power transfer the impedance matching is important. Hence **the power amplifiers must have low output impedance**. Hence common collecter or emitter follower circuit is very common in power amplifiers. The common emitter circuit with a step down transformer for impedance matching is also commonly used in power amplifiers.
5. The power amplifiers develop an a.c. power of the order of few watts. Similarly large power gets dissipated in the form of heat, at the junctions of the transistors used in the power amplifiers. **Hence the transistors used in the power amplifiers are of large size, having large power dissipation rating, called power transistors.** Such transistors have heat sinks. A heat sink is a metal cap having bigger surface area, press fit on the body of a transistor, to get more surface area, in order to dissipate the heat to the surroundings. In general, the power amplifiers have bulky components.
6. A faithful reproduction of the signal, after the conversion, is important. Due to nonlinear nature of the transistor characteristics, there exists a harmonic distortion in the signal. Ideally signal should not be distorted. **Hence the analysis of signal distortion in case of the power amplifiers is important.**
7. Many a times, the power amplifiers are used in public address systems and many audio circuits to supply large power to the loudspeakers. **Hence power amplifiers are also called audio amplifiers or audio frequency (A.F.) power amplifiers.**

3.19 Classification of Large Signal Amplifiers

For an amplifier, a quiescent operating point (Q point) is fixed by selecting the proper d.c. biasing to the transistors used. The quiescent operating point is shown on the load line, which is plotted on the output characteristics of the transistor. The position of the quiescent point on the load line decides the class of operation of the power amplifier. The various classes of the power amplifiers are :

i) Class A ii) Class B iii) Class C and iv) Class AB

These variations in I_C and V_{CE}, due to the change in I_B, can be shown graphically with the help of a load line as shown in the Fig. 5.2.

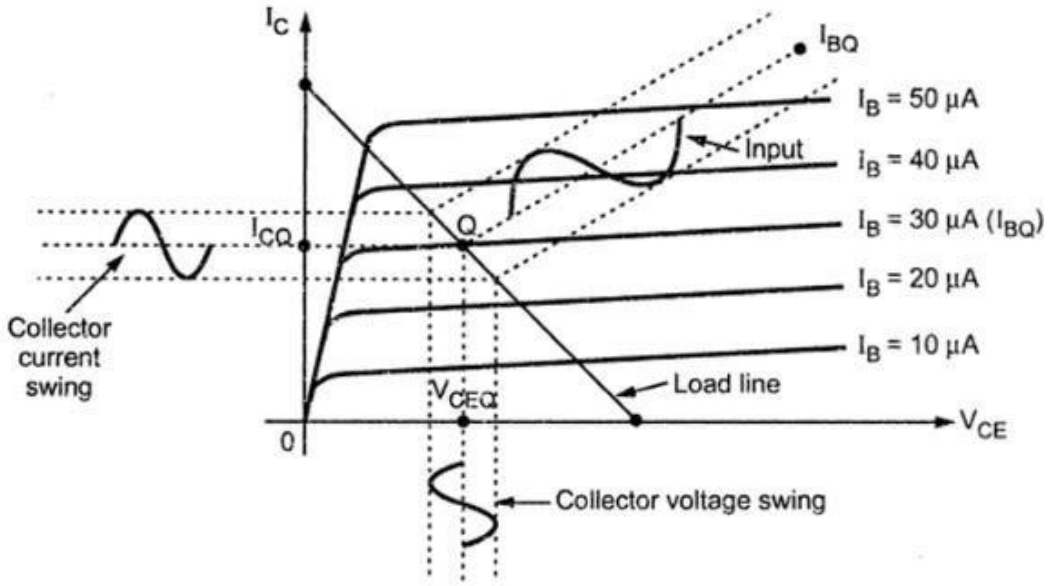


Fig 3.28 Graphical representation of I_B, I_C and V_{CE} swings

The collector current varies above and below its quiescent value, in phase with the base current. The collector-to-emitter voltage varies above and below its quiescent value, 180° out of phase with the base current, as shown in the Fig. 5.2.

3.20 Class A Amplifier

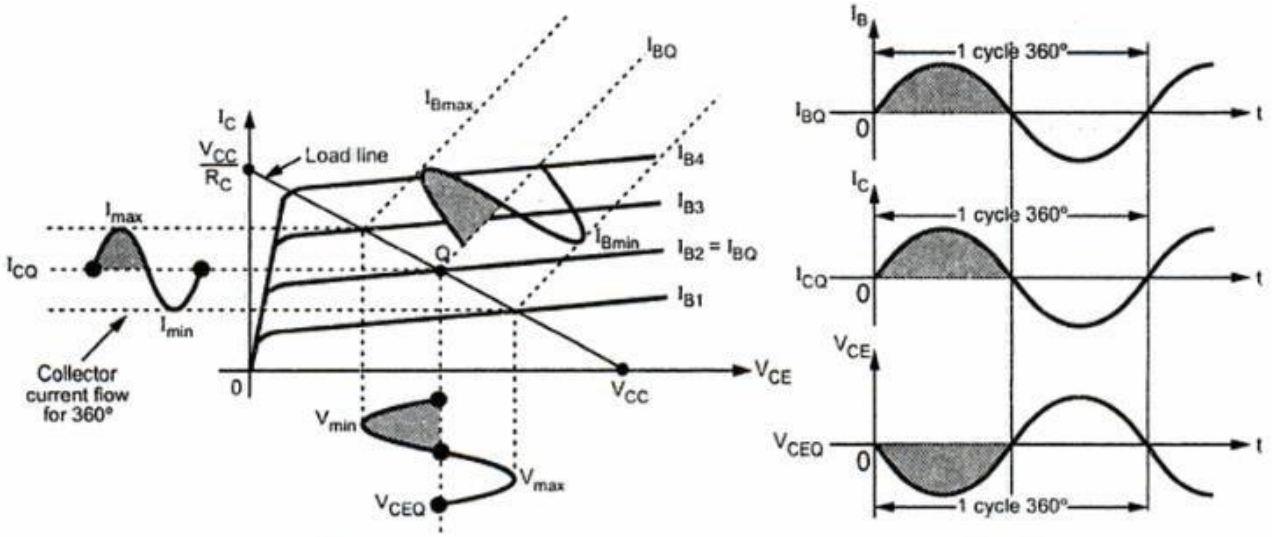
The power amplifier is said to be class A amplifier if the Q point and the input signal are selected such that the output signal is obtained for a full input cycle.

Key Point: *For this class, position of the Q point is approximately at the midpoint of the load line.*

For all values of input signal, the transistor remains in the active region and never enters into cut-off or saturation region. When an a.c. input signal is applied, the collector voltage varies sinusoidally hence the collector current also varies sinusoidally. The collector current flows for 360° (full cycle) of the input signal. In other words, the angle of the collector current flow is 360° i.e. one full cycle.

The current and voltage waveforms for a class A operation are shown with the help of output characteristics and the load line, in the Fig. 5.3.

As shown in the Fig. 5.3, for full input cycle, a full output cycle is obtained. Here signal is faithfully reproduced, at the output, without any distortion. This is an important feature of a class A operation. The efficiency of class A operation is very small.



Waveforms representing class A operation

Fig 3.29

3.21 Class B Amplifier

The power amplifier is said to be class B amplifier if the Q point and the input signal are selected, such that the output signal is obtained only for one half cycle for a full input cycle.

Key Point: *For this operation, the Q point is shifted on X-axis i.e. transistor is biased to cut-off.*

Due to the selection of Q point on the X-axis, the transistor remains, in the active region, only for positive half cycle of the input signal. Hence this half cycle is reproduced at the output. But in a negative half cycle of the input signal, the transistor enters into a cut-off region and no signal is produced at the output. The collector current flows only for 180° (half cycle) of the input signal. In other words, the angle of the collector current flow is 180° i.e. one half cycle.

The current and voltage waveforms for a class B operation are shown in the Fig. 5.4.

As only a half cycle is obtained at the output, for full input cycle, the output signal is distorted in this mode of operation. To eliminate this distortion, practically two transistors are used in the alternate half cycles of the input signal. Thus overall a full cycle of output signal is obtained across the load. Each transistor conducts only for a half cycle of the input signal.

The efficiency of class B operation is much higher than the class A operation.

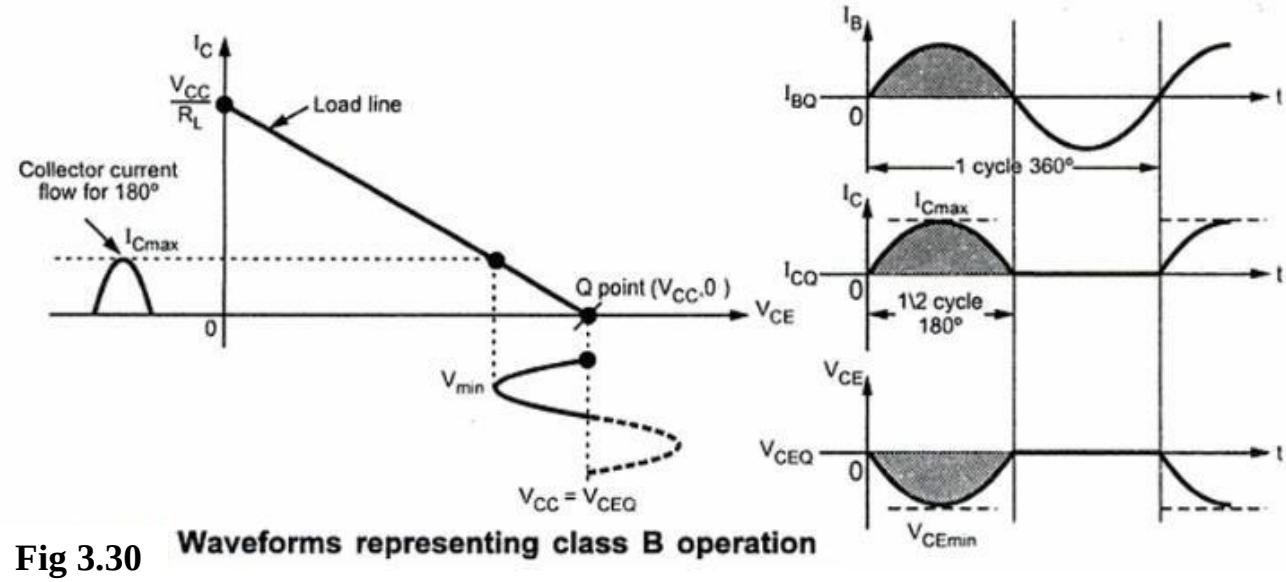


Fig 3.30 **Waveforms representing class B operation**

3.22 Class C Amplifier

The power amplifiers is said to be class C amplifier, if the Q point and the input signal are selected such that the output signal is obtained for less than a half cycle, for a full input cycle.

Key Point : *For this operation, the Q point is to be shifted below X-axis.*

Due to such a selection of the Q point, transistor remains active, for less than a half cycle. Hence only that much part is reproduced at the output. For remaining cycle of the input cycle, the transistor remains cut-off and no signal is produced at the output. The angle of the collector current flow is less than 180°.

The current and voltage waveforms for a class C amplifier operation are shown in the Fig. 5.5

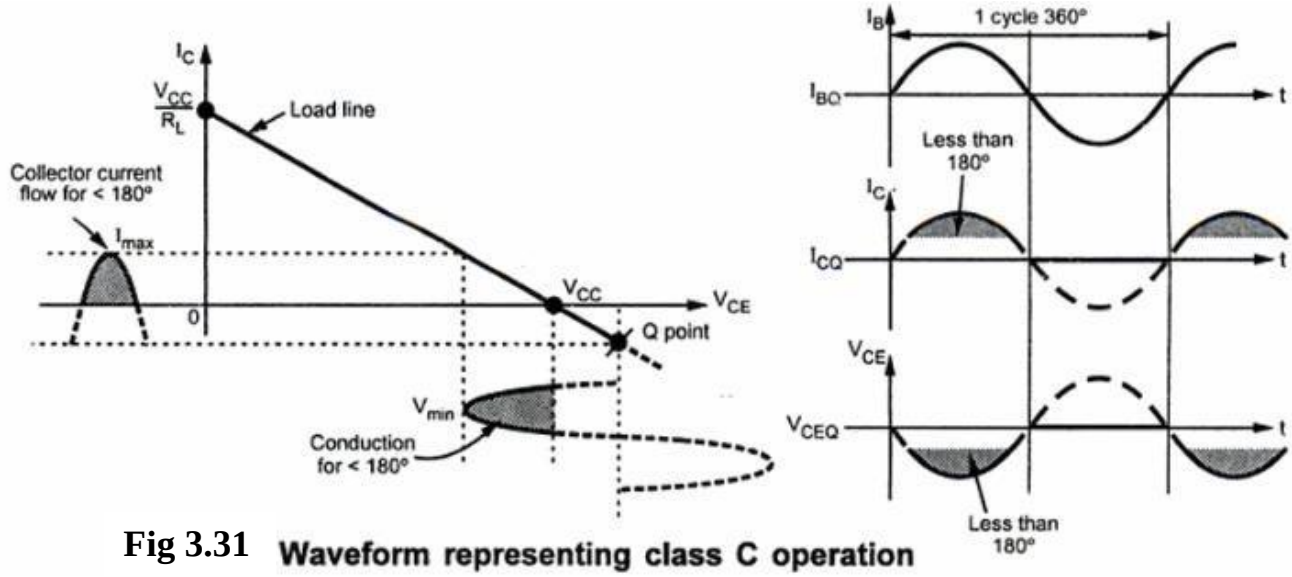


Fig 3.31 Waveform representing class C operation

Key Point : *In class C operation, the transistor is biased well beyond cut-off. As the collector current flows for less than 180°, the output is much more distorted and hence the class C mode is never used for A.F. power amplifiers.*

But the efficiency of this class of operation is much higher and can reach very close to 100 %.

Applications : The class C operation is not suitable for audio frequency power amplifiers. The class C amplifiers are used in tuned circuits used in communication areas and in radio frequency (RF) circuits with tuned RLC loads. As used in tuned circuits, class C amplifiers are called **tuned amplifiers**. These are also used in mixer or converter circuits used in radio receivers and wireless communication systems.

The Fig. 5.6 shows the calss C tuned amplifier.

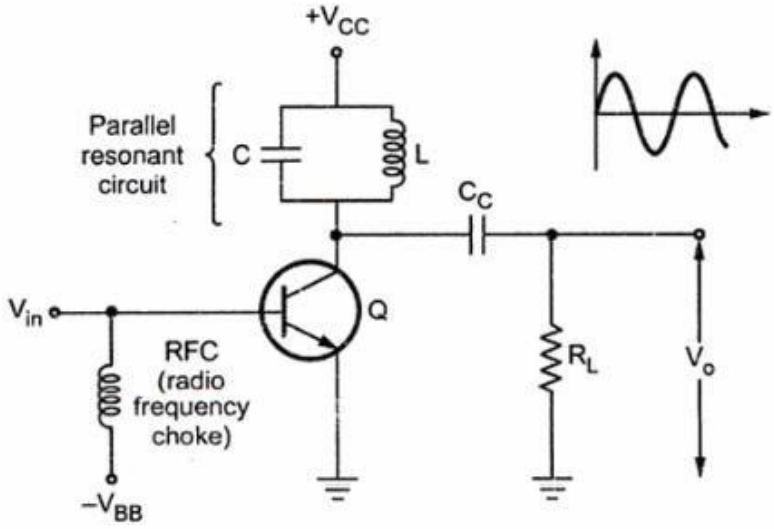


Fig 3.32 Class C tuned amplifier

The LC parallel circuit is a parallel resonant circuit. This circuit acts as a load impedance. Due to class C operation, the collector current consists of a series of pulses containing harmonics i.e. many other frequency components along with the fundamental frequency component of input. The parallel tuned circuit is designed to be tuned to the fundamental input frequency. Hence it eliminates the harmonics and produce a sine wave of fundamental component of input signal. As the transistor and coil losses are small, the most of the d.c. input power is converted to a.c. load power. Hence efficiency of class C is very high.

3.23 Class AB Amplifier

The power amplifier is said to be class AB amplifier, if the Q point and the input signal are selected such that the output signal is obtained for more than 180° but less than 360°, for a full input cycle.

Key Point : *The Q point position is above X-axis but below the midpoint of a load line.*

The current and voltage waveforms for a class AB operation, are shown in the Fig. 5.7.

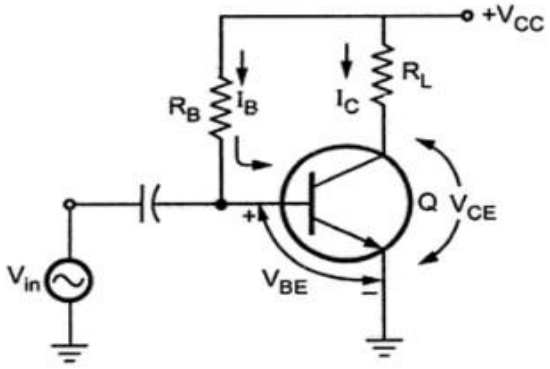
3.23.1 Comparison of amplifier classes

Class	A	B	C	AB
Operating cycle	360°	180°	Less than 180°	180° to 360°
Position of Q point	Centre of load line	On X-axis	Below X-axis	Above X-axis but below the centre of load line
Efficiency	Poor, 25 % to 50 %	Better, 78.5 %	High	Higher than A but less than B 50 % to 78.5 %
Distortion	Absent No distortion	Present More than class A	Highest	Present

3.24 Analysis of Class A Amplifiers

The class A amplifiers are further classified as **directly coupled** and **transformer coupled** amplifiers. In directly coupled type, the load is directly connected in the collector circuit. While in the transformer coupled type, the load is coupled to the collector using a transformer called an output transformer. Let us study in detail the various aspects of the two types of class A amplifiers.

3.24.1 Series Fed, Direct Coupled Class A Amplifier



Large signal class A amplifier

Fig 3.33

A simple fixed-bias circuit can be used as a large signal class A amplifier as shown in the Fig. 5.8.

The difference between small signal version of this circuit is that the signals handled by this large signal circuit are of the order of few volts. Similarly the transistor used, is a power transistor. The value of R_B is selected in such a way that the Q point lies at the centre of the d.c. load line.

The circuit represents the directly coupled class A amplifier as the load is directly connected in the collector circuit. Most of the times the load is a loudspeaker, the impedance of which varies from 3 to 4 ohms to 16 ohms. The beta of the transistor used is less than 100.

Key Point : *This is called **directly coupled**, as the load R_L is directly connected in the collector circuit of power transistor.*

The overall circuit handles large power, in the range of a few to tens of watts without providing much voltage gain.

The graphical representation of a class A amplifier is shown in the Fig. 5.9.

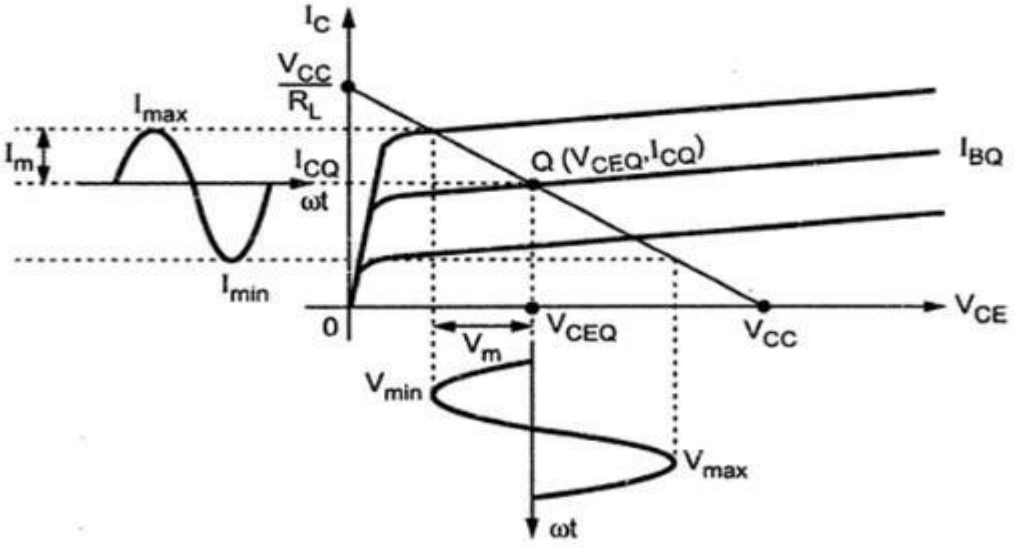


Fig 3.34 Graphical representation of class A amplifier

Applying Kirchhoff's voltage law to the circuit shown in the Fig. 5.8, we get

$$V_{CC} = I_C R_L + V_{CE}$$

$$\therefore \quad I_C R_L = -V_{CE} + V_{CC}$$

$$\therefore \quad I_C = \left[-\frac{1}{R_L}\right] V_{CE} + \frac{V_{CC}}{R_L} \qquad \ldots (1)$$

The equation is similar to equation (1) of section and thus the slope of the load line is $-\frac{1}{R_L}$ while the Y-intercept is $\frac{V_{CC}}{R_L}$.

The change is because the collector resistance R_C is named as load resistance R_L in this circuit. The Q point is adjusted approximately at the centre of the load line.

5.6.1 DC Operation

The collector supply voltage V_{CC} and resistance R_B decides the d.c. base-bias current I_{BQ}. The expression is obtained applying KVL to the B-E loop and with $V_{BE} = 0.7$ V.

$$\therefore \quad \boxed{I_{BQ} = \frac{V_{CC} - 0.7}{R_B}} \qquad \ldots (2)$$

The corresponding collector current is then,

$$\boxed{I_{CQ} = \beta I_{BQ}} \qquad \ldots (3)$$

From the equation (1), the corresponding collector to emitter voltage is,

$$\boxed{V_{CEQ} = V_{CC} - I_{CQ} R_L} \qquad \ldots (4)$$

Hence the Q point can be defined as Q (V_{CEQ}, I_{CQ}).

DC Power Input

The d.c. power input is provided by the supply. With no a.c input signal, the d.c. current drawn is the collector bias current I_{CQ} . Hence d.c. power input is,

$$\boxed{P_{DC} = V_{CC} I_{CQ}} \qquad \ldots (5)$$

It is important to note that even if a.c. input signal is applied, the average current drawn from the d.c. supply remains same. Hence equation (5) represents d.c. power input to the class A series fed amplifier.

AC Operation

When an input a.c. signal is applied, the base current varies sinusoidally.

Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the Fig. 5.9.

The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector to emitter voltage varies around its quiescent value. The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

AC Power Output

For an alternating output voltage and output current swings, shown in the Fig. 5.9, we can write,

V_{min} = Minimum instantaneous value of the collector (output) voltage

V_{max} = Maximum instantaneous value of the collector (output) voltage

and V_{pp} = Peak to peak value of a.c. output voltage across the load.

$$\therefore \quad V_{pp} = V_{max} - V_{min} \quad \ldots (6)$$

Now V_m = Amplitude (peak) of a.c. output voltage as shown in the Fig. 5.9.

$$\therefore \quad \boxed{V_m = \frac{V_{pp}}{2} = \frac{V_{max} - V_{min}}{2}} \quad \ldots (7)$$

Similarly we can write for the output current as,

I_{min} = Minimum instantaneous value of the collector (output) current

I_{max} = Maximum instantaneous value of the collector (output) current

and I_{pp} = Peak to peak value of a.c. output (load) current

$$\therefore \quad I_{pp} = I_{max} - I_{min} \quad \ldots (8)$$

Now I_m = Amplitude (peak) of a.c. output (load) current as shown in the Fig. 5.9

$$\therefore \quad \boxed{I_m = \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2}} \quad \ldots (9)$$

Hence the r.m.s. values of alternating output voltage and current can be obtained as,

$$V_{rms} = \frac{V_m}{\sqrt{2}} \quad \ldots (10)$$

$$I_{rms} = \frac{I_m}{\sqrt{2}} \quad \ldots (11)$$

Hence we can write,

$$V_{rms} = I_{rms} R_L \quad \ldots (12)$$

i.e.

$$V_m = I_m R_L \quad \ldots (13)$$

The a.c. power delivered by the amplifier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.

i) Using r.m.s values

$$\therefore \quad \boxed{P_{ac} = V_{rms}\ I_{rms}} \qquad \text{... (14)}$$

$$\text{or} \quad \boxed{P_{ac} = I_{rms}^2\ R_L} \qquad \text{... (15)}$$

$$\text{or} \quad \boxed{P_{ac} = \frac{V_{rms}^2}{R_L}} \qquad \text{... (16)}$$

ii) Using peak values

$$P_{ac} = V_{rms}\ I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

$$\therefore \quad \boxed{P_{ac} = \frac{V_m\ I_m}{2}} \qquad \text{... (17)}$$

$$\text{or} \quad \boxed{P_{ac} = \frac{I_m^2\ R_L}{2}} \qquad \text{... (18)}$$

$$\text{or} \quad \boxed{P_{ac} = \frac{V_m^2}{2\,R_L}} \qquad \text{... (19)}$$

iii) Using peak to peak values

$$P_{ac} = \frac{V_m\ I_m}{2} = \frac{\left(\frac{V_{PP}}{2}\right)\left(\frac{I_{PP}}{2}\right)}{2}$$

$$\boxed{P_{ac} = \frac{V_{pp}\ I_{pp}}{8}} \qquad \text{... (20)}$$

$$\text{or} \quad \boxed{P_{ac} = \frac{I_{pp}^2\ R_L}{8}} \qquad \text{... (21)}$$

$$\text{or} \quad \boxed{P_{ac} = \frac{V_{PP}^2}{8\,R_L}} \qquad \text{... (22)}$$

But as $V_{pp} = V_{max} - V_{min}$ and $I_{pp} = I_{max} - I_{min}$; from equation (20), the a.c. power can be expressed as below, for graphical calculations.

$$\boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}} \qquad \text{... (23)}$$

Efficiency

The efficiency of an amplifier represents the amount of a.c. power delivered or transferred to the load, from the d.c. source i.e. accepting the d.c. power input. The generalised expression for an efficiency of an amplifier is,

Maximum Efficiency

For maximum efficiency calculation, assume maximum swings of both the output voltage and the output current. The maximum swings are shown in the Fig. 5.10.

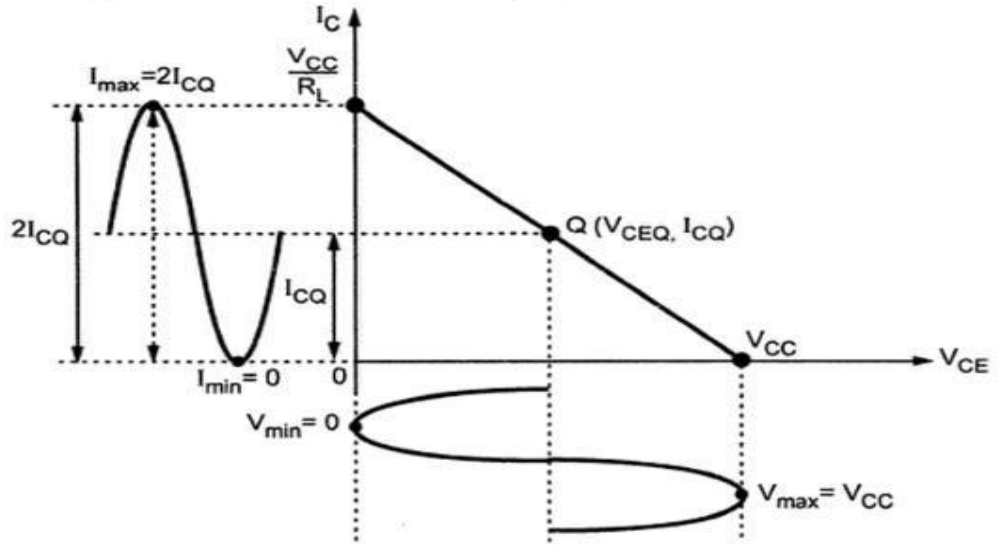


Fig 3.35 Maximum voltage and current swings

From the Fig. 5.10, we can see that the minimum voltage possible is zero and maximum voltage possible is V_{CC}, for a maximum swing. Similarly the minimum current is zero and the maximum current possible is 2 I_{CQ}, for a maximum swing.

$$\left.\begin{array}{l} V_{max} = V_{CC} \text{ and } V_{min} = 0 \\ I_{max} = 2\,I_{CQ} \text{ and } I_{min} = 0 \end{array}\right\} \text{ for maximum swing}$$

Using equation (25) we can write,

$$\%\,\eta_{max} = \frac{(V_{CC}-0)(2I_{CQ}-0)}{8\,V_{CC}\,I_{CQ}} \times 100 = \frac{2\,V_{CC}\,I_{CQ}}{8\,V_{CC}\,I_{CQ}} \times 100$$

$$= 25\ \%$$

Key Point : *Thus the maximum efficiency possible in case of directly coupled series fed class A amplifier is just 25 %.*

This maximum efficiency is an ideal value. For a practical circuit, it is much less than 25 %, of the order of 10 to 15 %.

Key Point : *Very low efficiency is the biggest disadvantage of class A amplifier.*

Power Dissipation

As stated earlier, power dissipation in large signal amplifier is also large. The amount of power that must be dissipated by the transistor is the difference between the d.c. power input P_{dc} and the a.c. power delivered to the load P_{ac}.

P_d = Power dissipation

i.e. $\boxed{P_d = P_{DC} - P_{ac}}$ ... (26)

The maximum power dissipation occurs when there is zero a.c. input signal. When a.c. input is zero, the a.c. power output is also zero. But transistor operates at quiescent condition, drawing d.c. input power from the supply equal to $V_{CC}\ I_{CQ}$. This entire power gets dissipated in the form of heat. Thus d.c. power input without a.c. input signal is the maximum power dissipation.

$$\boxed{(P_d)max = V_{CC}\ I_{CQ}} \quad \text{... (27)}$$

Advantages and Disadvantages of Class A amplifier

The **advantages** of directly coupled class A amplifier can be stated as,

1. The circuit is simple to design and to implement.
2. The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.
3. Less number of components required as load is directly coupled.

The disadvantages are,

1. The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
2. Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
3. The output impedance is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
4. The efficiency is very poor, due to large power dissipation.

3.25 Transformer Coupled Class A Amplifier

As stated earlier, for maximum power transfer to the load, the impedance matching is necessary. For loads like loudspeaker, having low impedance values, impedance matching is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directly coupled class A amplifier is very much high. This problem can be eliminated by using a transformer to deliver power to the load.

5.7.1 Properties of Transformer

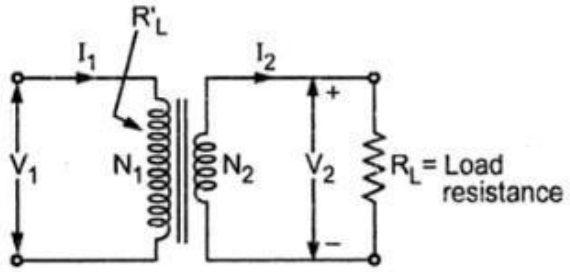


Fig 3.36 Transformer with load

Consider a transformer as shown in the Fig. 5.11 which is connected to a load of resistance R_L.

While analysing the transformer, it is assumed that the transformer is ideal and there are no losses in the transformer. Similarly the winding resistances are assumed to be zero.

Let N_1 = Number of turns on primary

N_2 = Number of turns on secondary

V_1 = Voltage applied to primary

V_2 = Voltage on secondary

I_2 = Primary current

i) Turns Ratio : The ratio of number of turns on secondary to the number of turns on primary is called turns ratio of the transformer denoted by n.

$$\therefore \quad \boxed{n = \text{Turns ratio} = \frac{N_2}{N_1}} \qquad \ldots (1)$$

Some times it is specified as $\frac{N_2}{N_1} : 1$ or $\frac{N_1}{N_2} : 1$.

ii) Voltage Transformation : The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be step up or step down transformer.

$$\therefore \quad \frac{V_2}{V_1} = \frac{N_2}{N_1} = n \qquad \ldots (2)$$

In the amplifier analysis, the load impedance is going to be small. And the transformer is to be used for impedance matching. Hence it has to be a step down transformer. Hence

number of turns on primary are more than the secondary and turns ratio is less than unity, for such a step down transformer.

iii) Current Transformation : The current in the secondary winding is inversely proportional to the number of turns of the windings.

$$\therefore \quad \frac{I_2}{I_1} = \frac{N_1}{N_2} = \frac{1}{n} \qquad \ldots (3)$$

iv) Impedance Transformation : As current and voltage get transformed from primary to secondary, an impedance 'seen' from either side (primary or secondary) also changes.

Now the impedance of the load on secondary is R_L as shown in the Fig. 5.11. The primary and secondary winding resistances are assumed to be zero. This load impedance R_L, gets reflected on the primary side and behaves as if connected in the primary side. Such impedance transferred from secondary to primary is denoted as R_L'.

Now using the equations (2) and (3) and the Fig. 5.11, we can write,

$$R_L = \frac{V_2}{I_2} \text{ and } R_L' = \frac{V_1}{I_1}$$

But $$V_1 = \frac{N_1}{N_2} V_2 \text{ and } I_1 = \frac{N_2}{N_1} I_2$$

$$\therefore \quad R_L' = \frac{\frac{N_1}{N_2} V_2}{\frac{N_2}{N_1} I_2} = \left(\frac{N_1}{N_2}\right)^2 \times \frac{V_2}{I_2} = \frac{R_L}{\left(\frac{N_2}{N_1}\right)^2} = \frac{R_L}{n^2}$$

$$\therefore \quad \boxed{R_L' = \frac{R_L}{n^2} = \left(\frac{N_1}{N_2}\right)^2 R_L} \qquad \ldots (4)$$

The R_L' is the **reflected impedance** and is related to the square of the turns ratio of the transformer. Remember that for a step down transformer, the secondary voltage is less than the primary. And high voltage side is always high impedance side. **Hence R_L' is always higher than R_L, for a step down transformer.**

3.25.1 Analysis of Transformer Coupled Class A Amplifier

The basic circuit of a transformer coupled amplifier is shown in the Fig. 5.12. The loudspeaker connected to the secondary acts as a load having impedance of R_L ohms.

The transformer used is a step down transformer with the turns ratio as

$$\boxed{n = N_2/N_1}$$

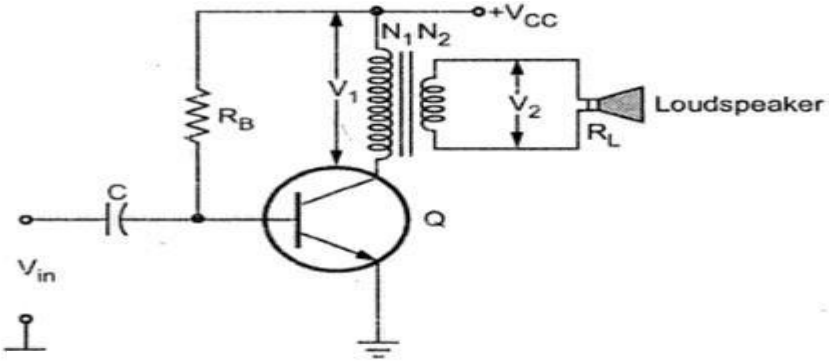


Fig 3.37 Transformer coupled class A amplifier

DC Operation

It is assumed that the winding resistances are zero ohms. Hence for d.c. purposes, the resistance is 0 Ω. There is no d.c. voltage drop across the primary winding of the transformer. The slope of the d.c. load line is reciprocal of the d.c. resistance in the collector circuit, which is zero in this case. Hence slope of the d.c. load line is ideally infinite. This tells that the d.c. load line in the ideal condition is a vertically straight line.

Applying Kirchhoff's voltage law to the collector circuit we get,

$$V_{CC} - V_{CE} = 0$$

i.e. $V_{CC} = V_{CE}$ ... Drop across winding is zero

This is the d.c. bias voltage V_{CEQ} for the transistor.

So $$\boxed{V_{CEQ} = V_{CC}} \quad \text{... (5)}$$

Hence the d.c. load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{CC}$.

The intersection of d.c. load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is I_{CQ}.

DC Power Input

The d.c. power input is provided by the supply voltage with no signal input, the d.c. current drawn is the collector bias current I_{CQ}.

Hence the d.c. power input is given by,

So $$\boxed{P_{DC} = V_{CC}\, I_{CQ}} \quad \text{... (6)}$$

The expression is same as derived earlier for series fed directly coupled class A amplifier.

AC Operation

For the a.c. analysis, it is necessary to draw an a.c. load line on the output characteristics.

For a.c. purposes, the load on the secondary is the load impedance R_L ohms. And the reflected load on the primary i.e. R_L' can be calculated using the equation (4). The load line drawn with a slope of $\left(\frac{-1}{R_L'}\right)$ and passing through the operating point i.e. quiescent point Q is called **a.c. load line**. The d.c. and a.c. load lines are shown in the Fig. 5.13.

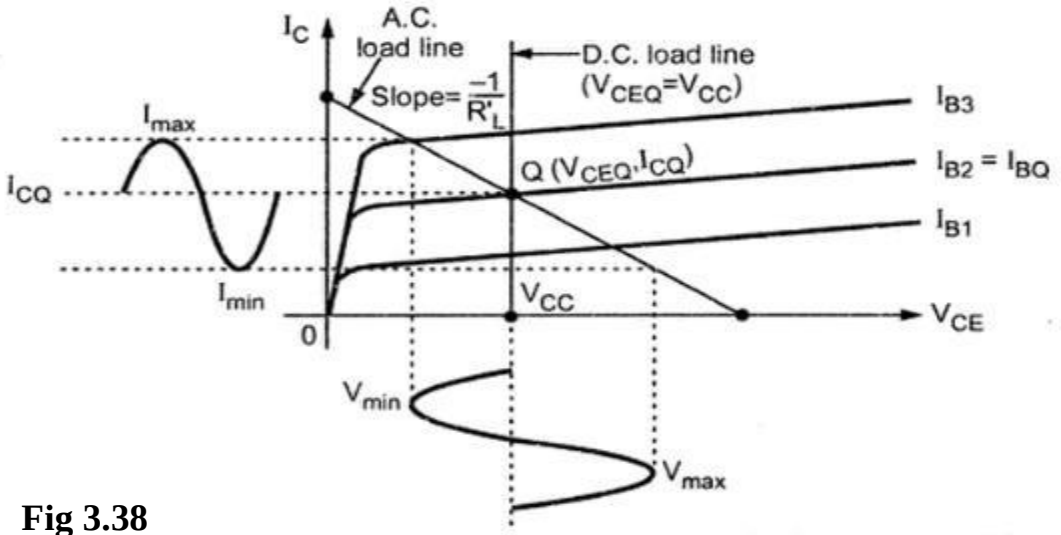


Fig 3.38

Load lines for transformer coupled class A amplifier

The output current i.e. collector current varies around its quiescent value I_{CQ}, when a.c. input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value V_{CEQ} which is V_{CC} in this case.

AC Output Power

The a.c. power developed is on the primary side of the transformer. While calculating this power, the primary values of voltage and current and reflected load R_L' must be considered. The a.c. power delivered to the load is on the secondary side of the transformer. While calculating load voltage, load current, load power the secondary voltage, current and the load R_L must be considered.

Let

V_{1m} = Magnitude or peak value of primary voltage

V_{1rms} = R.M.S value of primary voltage

I_{1m} = Peak value of primary current

I_{1rms} = R.M.S value of primary current.

Hence the a.c. power developed on the primary is given by,

$$P_{ac} = V_{1rms}\, I_{1rms} \quad \ldots (7)$$

$$P_{ac} = I_{1rms}^2\, R'_L \quad \ldots (8)$$

$$P_{ac} = \frac{V_{1rms}^2}{R'_L} \quad \ldots (9)$$

$$P_{ac} = \frac{V_{1m}}{\sqrt{2}} \cdot \frac{I_{1m}}{\sqrt{2}} = \frac{V_{1m}\, I_{1m}}{2} \quad \ldots (10)$$

$$P_{ac} = \frac{I_{1m}^2\, R'_L}{2} \quad \ldots (11)$$

$$P_{ac} = \frac{V_{1m}^2}{2\, R'_L} \quad \ldots (12)$$

Similarly the a.c. power delivered to the load on secondary, also can be calculated, using secondary quantities.

Let V_{2m} = Magnitude or peak value of secondary or load voltage

$V_{2\,rms}$ = R.M.S value of secondary or load voltage

I_{2m} = Magnitude or peak value of secondary or load current.

I_{2rms} = R.M.S. value of secondary or load current

$$\boxed{P_{ac} = V_{2rms}\ I_{2rms} = I_{2rms}^2\, R_L = \frac{V_{2rms}^2}{R_L}} \quad \ldots (13)$$

or

$$\boxed{P_{ac} = \frac{V_{2m}\ I_{2m}}{2} = \frac{I_{2m}^2\, R_L}{2} = \frac{V_{2m}^2}{2R_L}} \quad \ldots (14)$$

Power delivered on primary is same as power delivered to the load on secondary, assuming **ideal transformer**. Primary and Secondary values of voltages and currents are related to each other through the turns ratio of the transformer.

The generalised expression for a.c. power output represented by the equation (23) in section (6.7), can be used as it is for transformer coupled amplifier. The expression is mentioned again for the convenience of the reader.

$\therefore$

$$\boxed{P_{ac} = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}}$$

Efficiency

The general expression for the efficiency remains same as that given by equations (24) and (25)

$$\% \eta = \frac{P_{ac}}{P_{dc}} \times 100 = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8 V_{CC} I_{CQ}} \times 100$$

Maximum Efficiency

Assume maximum swings of both the output voltage and output current, to calculate maximum efficiency, as shown in the Fig. 5.14.

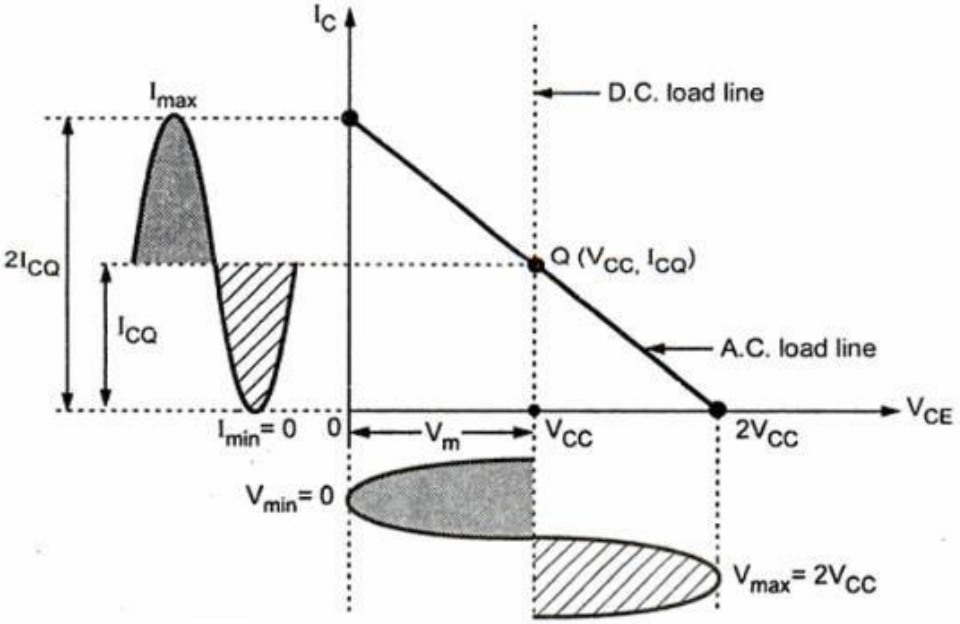


Fig 3.39 Maximum voltage and current swings

From the Fig. 5.14, assuming that the Q point is exactly at the centre of the load line, for maximum swing we can write,

$$\left.\begin{aligned} V_{min} &= 0 \text{ and } V_{max} = 2 V_{CC} \\ I_{min} &= 0 \text{ and } I_{max} = 2 I_{CQ} \end{aligned}\right\} \text{ for maximum swing}$$

Using equation (25) of section 6.7,

$$\% \eta_{max} = \frac{(2V_{CC} - 0)(2I_{CQ} - 0)}{8 V_{CC} I_{CQ}} \times 100$$

$$= \frac{4 V_{CC} I_{CQ}}{8 V_{CC} I_{CQ}} \times 100 = 50 \%$$

Key Point : *Hence maximum possible theoretical efficiency in case of transformer coupled class A amplifier is 50 %.*

Power Dissipation

The power dissipation by the transistor is the difference between the a.c. power output and the d.c. power input. The power dissipated by the transformer is very small due to negligible (d.c.) winding resistances and can be neglected.

$$\therefore \quad P_d = P_{DC} - P_{ac} \quad \ldots (16)$$

When the input signal is larger, more power is delivered to the load and less is the power dissipation. But when there is no input signal, the entire d.c. input power gets dissipated in the form of heat, which is the maximum power dissipation.

$$\therefore \quad \boxed{(P_d)_{max} = V_{CC}\, I_{CQ}} \quad \ldots (17)$$

Thus the class A amplifier dissipates less power when delivers maximum power to the load. While it dissipates maximum power while delivering zero power to the load i.e. when load is removed and there is no a.c. input signal. The maximum power dissipation decides the maximum power dissipation rating for the power transistor to be selected for an amplifier.

Advantages and Disadvantages of Transformer Coupled Class A Amplifier

The **advantages** of transformer coupled class **A amplifier** circuit are,

1. The efficiency of the operation is higher than directly coupled amplifier.
2. The d.c. bias current that flows through the load in case of directly coupled amplifier is stopped in case of transformer coupled.
3. The impedance matching required for maximum power transfer is possible.

The **disadvantages** are,

1. Due to the transformer, the circuit becomes bulkier, heavier and costlier compared to directly coupled circuit.
2. The circuit is complicated to design and implement compared to directly coupled circuit.
3. The frequency response of the circuit is poor.

3. The r.m.s value of the primary voltage is $(V_1)_{rms}$ as calculated above.

$$\therefore \quad (V_1)_{rms} = \mathbf{5.8787\ V}$$

3.27 Analysis of Class B Amplifiers

As stated earlier, for class B operation, the quiescent operating point is located on the X-axis itself. Due to this collector current flows only for a half cycle for a full cycle of the input signal. Hence the output signal is distorted. To get a full cycle across the load, a pair of transistors is used in class B operation. The two transistors conduct in alternate half cycles of the input signal and a full cycle across the load is obtained. The two transistors are identical in characteristics and called matched transistors.

Depending upon the types of the two transistors whether p-n-p or n-p-n, the two circuit configurations of class B amplifier are possible. These are,

1. When both the transistors are of same type i.e. either n-p-n or p-n-p then the circuit is called **push pull class B** A.F. power amplifier circuit.
2. When the two transistors form a complementary pair i.e. one n-p-n and other p-n-p then the circuit is called **complementary symmetry class B** A.F. power amplifier circuit. Let us analyse these two circuits of class **B** amplifiers in detail.

3.27.1 Push Pull Class B Amplifier

The push pull circuit requires two transformers, one as input transformer called **driver transformer** and the other to connect the load called **output transformer.** The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown in the Fig. 5.15.

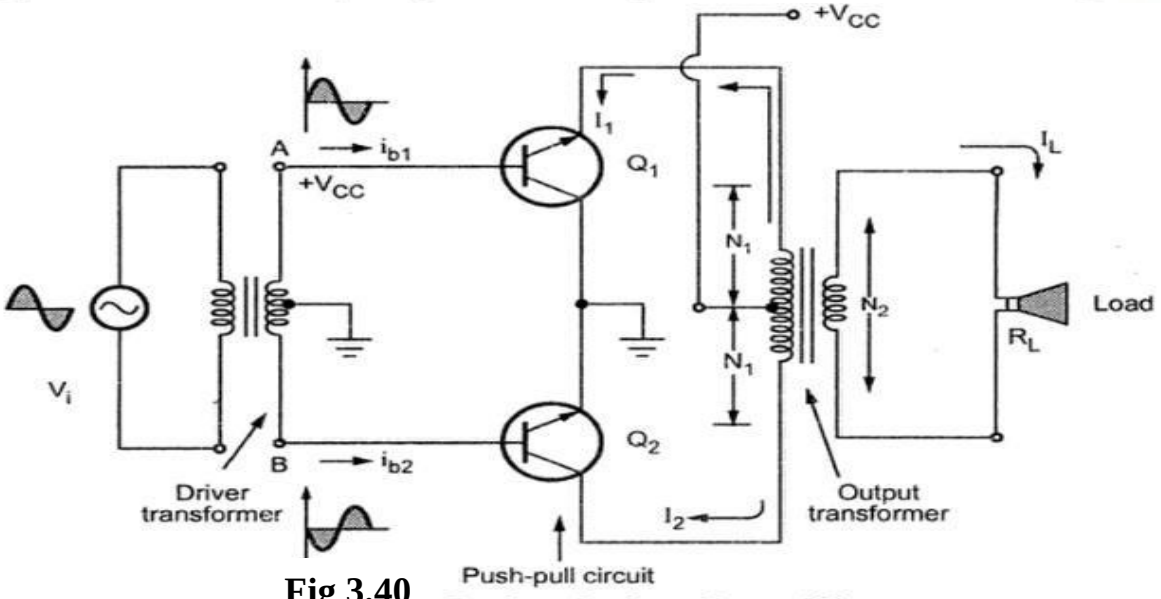


Fig 3.40 Push pull class B amplifier

In the circuit, both Q_1 and Q_2 transistors are of n-p-n type. The circuit can use both Q_1 and Q_2 of p-n-p type. In such a case, the only change is that the supply voltage must be $-V_{CC}$, the basic circuit remains the same. Generally the circuit using n-p-n transistors is used. Both the transistors are in common emitter configuration.

The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded. The centre tap on the primary of the output transformer is connected to the supply voltage + V_{CC}.

With respect to the center tap, for a positive half cycle of input signal, the point A shown on the secondary of the driver transformer will be positive. While the point B will be negative. Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q_1 and Q_2 will be 180° out of phase.

The transistor Q_1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q_2 conducts for the negative half cycle of the input producing negative half cycle across the load. Thus across the load, we get a full cycle for a full input cycle. The basic push pull operation is shown in the Fig. 5.16.

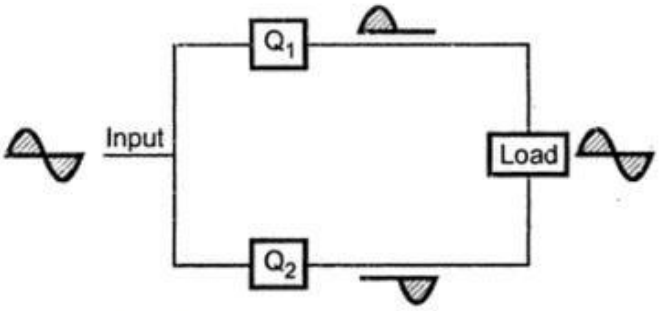


Fig 3.41 Basic push pull operation

When point A is positive, the transistor Q_1 gets driven into an active region while the transistor Q_2 is in cut-off region. While when point A is negative, the point B is positive, hence the transistor Q_2 gets driven into an active region while the transistor Q_1 is in cut-off region.

The waveforms of the input current, base currents, collector currents and the load current are shown in the Fig. 5.17.

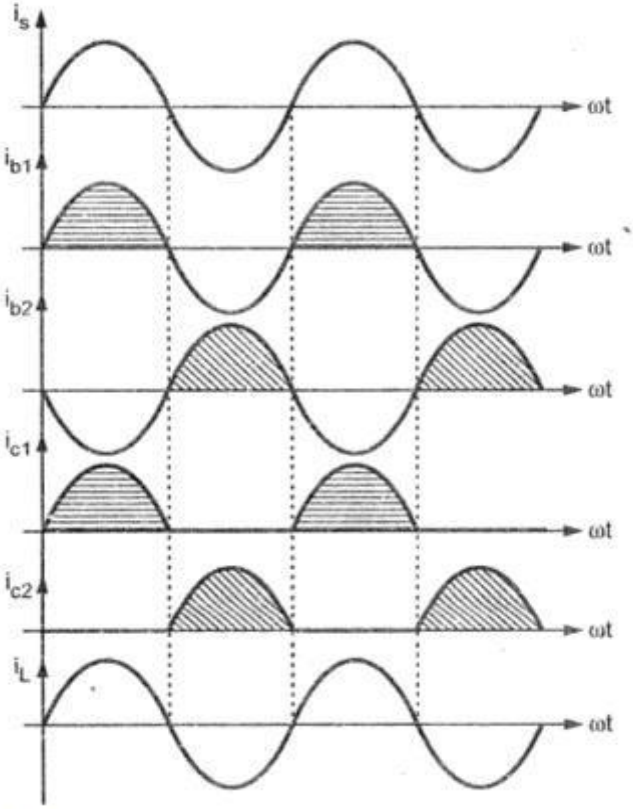


Fig 3.42 Waveforms for push pull class B amplifier

DC Operation

The d.c. biasing point i.e. Q point is adjusted on the X-axis such that $V_{CEQ} = V_{CC}$ and I_{CEQ} is zero. Hence the co-ordinates of the Q point are $(V_{CC}, 0)$. There is no d.c. base bias voltage.

DC Power Input

Each transistor output is in the form of half rectified waveform. Hence if I_m is the peak value of the output current of each transistor, the d.c. or average value is $\frac{I_m}{\pi}$, due to half rectified waveform. **The two currents, drawn by the two transistors, form the d.c. supply are in the same direction. Hence the total d.c. or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.**

$$\therefore \quad \boxed{I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}} \qquad \ldots (1)$$

The total d.c. power input is given by,

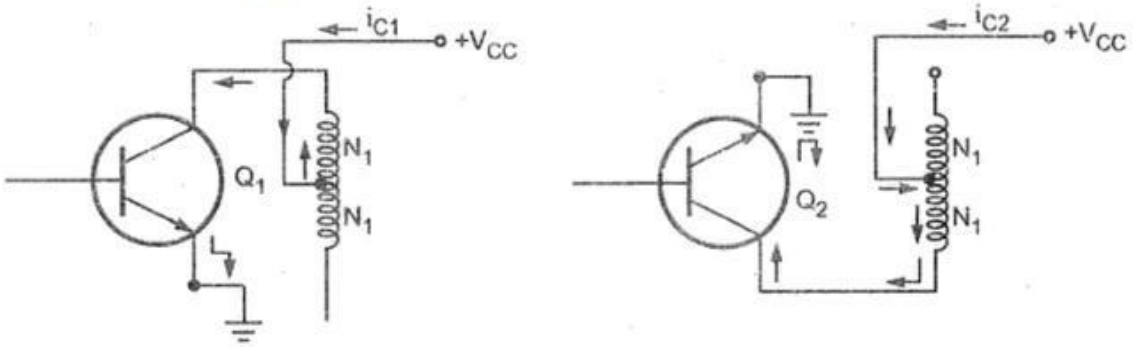
$$P_{DC} = V_{CC} \times I_{dc}$$

$$\therefore \quad \boxed{P_{DC} = \left(\frac{2I_m}{\pi}\right) V_{CC}} \qquad \ldots (2)$$

AC Operation

When the a.c. signal is applied to the driver transformer, for positive half cycle Q_1 conducts. The path of the current drawn by the Q_1 is shown in the Fig. 5.18 (a).

For the negative half cycle Q_2 conducts. The path of the current drawn by the Q_2 is shown in the Fig. 5.18 (b).



(a) Q_1 conduction **Fig 3.43** (b) Q_2 conduction

It can be seen that when Q_1 conducts, lower half of the primary of the output transformer does not carry any current. Hence only N_1 number of turns carry the current. While when Q_2 conducts, upper half of the primary does not carry any current. Hence again only N_1 number of turns carry the current. Hence the reflected load on the primary can be written as,

$$\therefore \quad \boxed{R'_L = \frac{R_L}{n^2}} \qquad \ldots (3)$$

where $n = \frac{N_2}{N_1}$

The slope of the a.c. load line (magnitude of slope) can be represented interms of V_m and I_m as,

$$\frac{1}{R'_L} = \frac{I_m}{V_m}$$

$$\therefore \quad \boxed{R'_L = \frac{V_m}{I_m}} \qquad \ldots (4)$$

where I_m = Peak value of the collector current

AC Power Output

As I_m and V_m are the peak values of the output current and the output voltage respectively, then

$$V_{rms} = \frac{V_m}{\sqrt{2}}$$

and $$I_{rms} = \frac{I_m}{\sqrt{2}}$$

Hence the a.c. power output is expressed as,

$$P_{ac} = V_{rms}\ I_{rms} = I_{rms}^2\ R_L' = \frac{V_{rms}^2}{R_L'} \quad \ldots (5)$$

While using peak values it can be expressed as,

$$\therefore \quad \boxed{P_{ac} = \frac{V_m I_m}{2} = \frac{I_m^2 R_L'}{2} = \frac{V_m^2}{2R_L'}} \quad \ldots (6)$$

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation.

$$\% \eta = \frac{P_{ac}}{P_{DC}} \times 100 = \frac{\left(\frac{V_m I_m}{2}\right)}{\frac{2}{\pi} V_{CC} I_m} \times 100$$

$$\therefore \quad \boxed{\% \eta = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100} \quad \ldots (7)$$

Maximum Efficiency

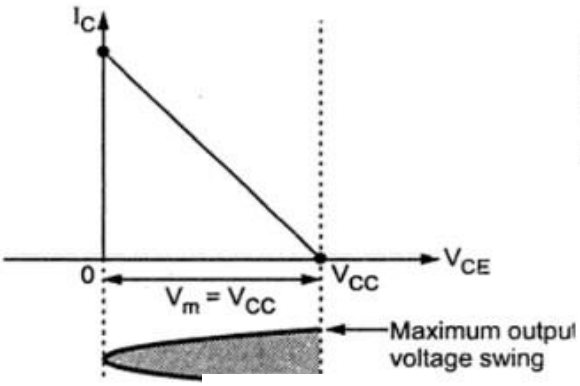


Fig 3.44

From the equation (7), it is clear that as the peak value of the collector voltage V_m increases, the efficiency increases. The maximum value of V_m possible is equal to V_{CC} as shown in the Fig. 5.19.

$$\boxed{V_m = V_{CC} \text{ for maximum } \eta}$$

$$\therefore \ \%\ \eta_{max} = \frac{\pi}{4} \times \frac{V_{CC}}{V_{CC}} \times 100$$

$$= 78.5\ \%$$

Key Point : *Thus the maximum possible theoretical efficiency in case of push pull class B amplifier is 78.5 % which is much higher than the transformer coupled class A amplifier.*

For practical circuits it is upto 65 to 70 %.

Power Dissipation

The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$\therefore \qquad P_d = P_{DC} - P_{ac} = \frac{2}{\pi} V_{CC}\, I_m - \frac{V_m\, I_m}{2}$$

$$\therefore \qquad P_d = \frac{2}{\pi} V_{CC} \frac{V_m}{R'_L} - \frac{V_m^2}{2R'_L} \qquad \ldots (8)$$

Advantages and Disadvantages of Push Pull Class B Amplifier

The advantages of push pull class B operation are :

1. The efficiency is much higher than the class A operation.
2. When there is no input signal, the power dissipation is zero.
3. The even harmonics get cancelled. This reduces the harmonic distortion.
4. As the d.c. current components flow in opposite direction through the primary winding, there is no possibility of d.c. saturation of the core.
5. Ripples present in supply voltage also get eliminated.
6. Due to the transformer, impedance matching is possible.

The disadvantages of the circuit are :

1. Two center tap transformers are necessary.
2. The transformers, make the circuit bulky and hence costlier.
3. Frequency response is poor.

3.28 Complementary Symmetry Class B Amplifier

As stated earlier, instead of using same type of transistors (n-p-n or p-n-p), one n-p-n and other p-n-p is used, the amplifier circuit is called as complementary symmetry class B amplifier. This circuit is transformer less circuit. But with common emitter configuration, it becomes difficult to match the output impedance for maximum power transfer without an output transformers. Hence the matched pair of complementary transistors are used in common collector (emitter follower) configuration, in this circuit. This is because common collector configuration has lowest output impedance and hence the impedance matching is possible. In addition, voltage feedback can be used to reduce the output impedance for matching.

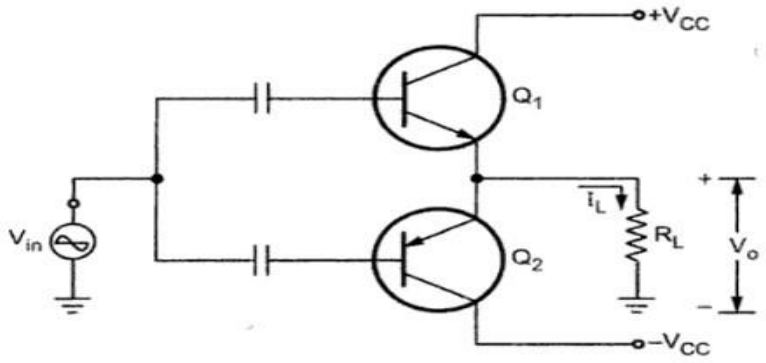


Fig 3.45 Complementary symmetry class B amplifier

The basic circuit of complementary symmetry class-B amplifier is shown in the Fig. 5.20.

The circuit is driven from a dual supply of $\pm V_{CC}$. The transistor Q_1 is n-p-n while Q_2 is of p-n-p type.

In the positive half cycle of the input signal, the transistor Q_1 gets driven into active region and starts conducting. The same signal gets applied to the base of the Q_2 but as it is of complementary type, remains in off condition, during positive half cycle. This results into positive half cycle across the load R_L. This is shown in the Fig. 5.21.

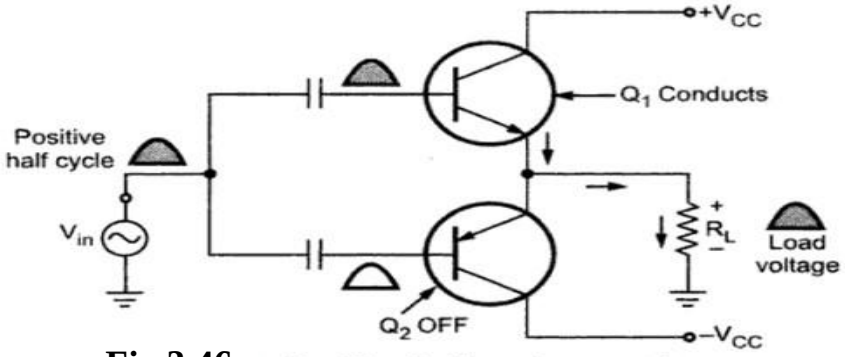
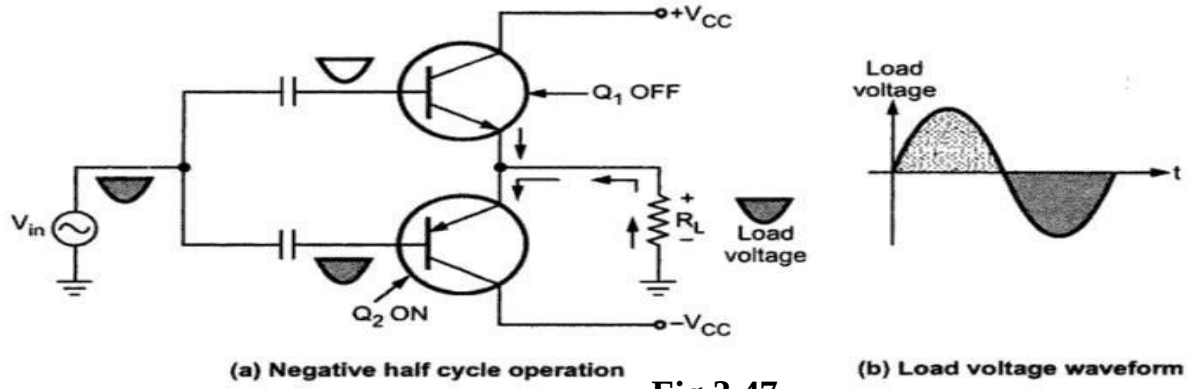


Fig 3.46 Positive half cycle operation

During the negative half cycle of the signal, the transistor Q_2 being p-n-p gets biased into conduction. While the transistor Q_1 gets driven into cut off region. Hence only Q_2 conducts during negative half cycle of the input, producing negative half cycle across the load R_L, as shown in the Fig. 5.22 (a).

Thus for a complete cycle of input, a compiete cycle of output signal is developed across the load as shown in the Fig. 5.22 (b)



(a) Negative half cycle operation (b) Load voltage waveform

Fig 3.47

3.11.1 Mathematical Analysis

All the results derived for push pull transformer coupled class B amplifier are applicable to the complementary class B amplifier. The **only change is that as the output transformer is not present, hence in the expressions, R_L value must be used as it is, instead of R'_L.**

3.11.2 Advantages and Disadvantages of Complementary Symmetry Class B Amplifier

The advantages are :

1. As the circuit is transformerless, its weight, size and cost are less.
2. Due to common collector configuration, impedance matching is possible.
3. The frequency response improves due to transformerless class B amplifier circuit.

The disadvantages are :

1. The circuit needs two separate voltage supplies.
2. The output is distorted to cross-over distortion.

3.12 Comparison of Push Pull and Complementary symmetry circuits

	Push Pull Class B	Complementary Symmetry Class B
1.	Both the transistors are similar either pnp or npn.	Transistors are complementary type i.e. one npn other pnp.
2.	The transformer is used to connect the load as well as input.	The circuit is transformerless.
3.	The impedance matching is possible due to the output transformer.	The impedance matching is possible due to common collector circuit.
4.	Frequency response is poor.	Frequency response is improved.
5.	Due to transformers, the circuit is bulky, costly and heavier.	As transformerless, the circuit is not bulky and costly.
6.	Dual power supply is not required.	Dual power supply is required.
7.	Efficiency is higher than class A.	The efficiency is higher than the push pull.

3.29 Class D Amplifier

The Fig. 5.23 shows the basic concept of class D amplifier. The amplifier consists of two complementary symmetry transistors driving a load R_L. This means one transistor is p-n-p and other is n-p-n.

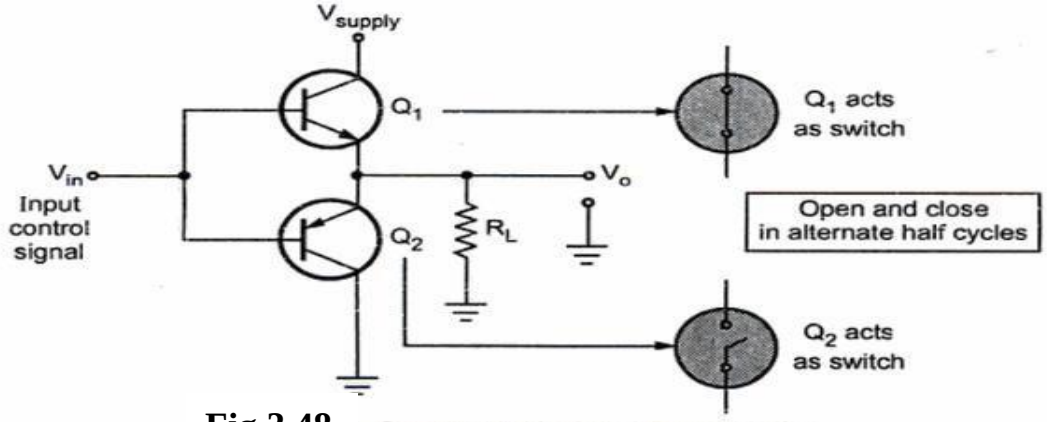


Fig 3.48 Concept of class D amplifier

The transistors are biased in such a way that they behave as ideal switches. When transistor is ON, it is biased to saturation so that voltage across it is zero while current is high. When transistor is OFF, it is biased to cut-off so that current through it is zero while voltage is high. Thus when input goes positive Q_1 conducts heavily acting as closed switch while Q_2 is OFF. While when input goes negative, Q_2 conducts heavily acting as closed switch while Q_1 is OFF. Thus the load voltage V_o across R_L has one of two possible values which are V_{supply} or 0 V. This is a type of digital output having two levels high and low.

The transistors dissipate almost zero power as in any of the states, either voltage is zero or current is zero for the transistors. Thus entire power input is available to the load. **Hence efficiency of class D amplifiers is almost 100 %.** The figure of merit which is the ratio of the maximum power dissipated in transistor to that delivered to the load, is zero. These facts make the class D amplifier as an ideal amplifier.

Practically class D amplifiers are designed to operate with digital or pulse type of signals. The basic block diagram of unit used along with class D amplifier in the application circuits is shown in the Fig. 5.24.

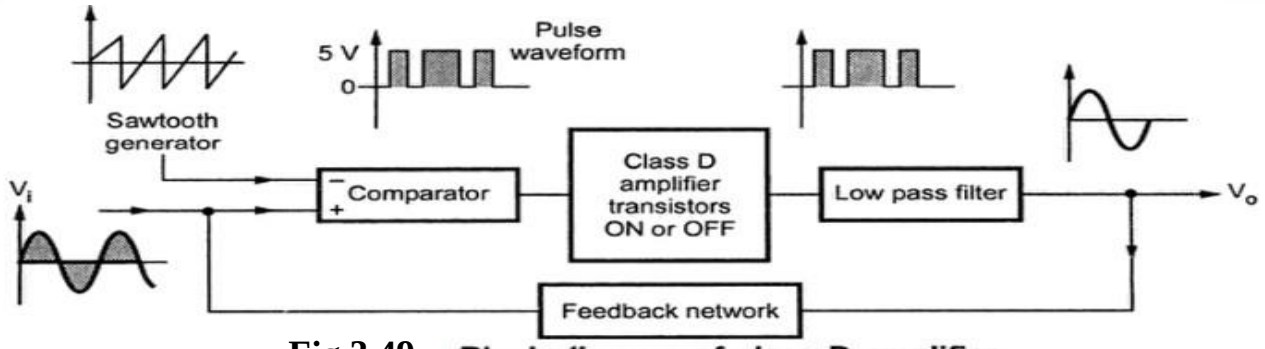


Fig 3.49 Block diagram of class D amplifier

The op-amp comparator is used for which one input is sawtooth type while other is sinusoidal. The comparator converts sinusoidal signal to digital pulse type signal with the help of sawtooth waveform. This is called **chopping** of sinusoidal signal to produce digital signal. This signal drives the class D smplifier. When pulse signal is high the transistors are ON and when it is low, the transistors are OFF. Thus most of the power supplied is delivered to the load by producing high power output signal. The digital signal is converted back to the original sinusoidal signal using low pass filter. Using feedback network, it is fed back to the comparator. Practically instead of power BJT, power MOSFET devices are used as driver devices for class D amplifier.

The class D amplifiers are mainly used in the pulse and digital circuits.

3.30 Distortion in Power Amplifiers

The input signal applied to the amplifiers is alternating in nature. The basic features of any alternating signal are amplitude, frequency and phase. The amplifier output should be reproduced faithfully i.e. there should not be the change or distortion in the amplitude, frequency and phase of the signal. Hence the possible distortions in any amplifier are amplitude distortion, phase distortions and frequency distortion. But the phase distortions are not detectable by human ears as human ears are insensitive to the phase changes. While **the change in gain of the amplifier with respect to the frequency is called frequency distortion.**

Key Point : *The frequency distortion is not significant in A.F. power amplifiers.*

In the earlier discussion, it is assumed that the transistor is perfectly linear device. That is the dynamic characteristics of a transistor is a straight line over the operating range [$i_c = Ki_b$]. But in practical circuits, the dynamic characteristics is not perfectly linear. Due to such nonlinearity in the dynamic characteristics, the waveform of the output voltage differs from that of the input signal. Such a distortion is called **nonlinear distortion** or **amplitude distortion** or **harmonic distortion.**

3.30.1 Harmonic Distortion

The harmonic distortion means the presence of the frequency components in the output wave form, which are not present in the input signal. The component with frequency same as the input signal is called fundamental frequency component. The additional frequency components present in the output signal are having frequency components which are integer multiples of fundamental frequency component. These components are called harmonic components or harmonics. For example if the **fundamental frequency** is f Hz, then the output signal contains fundamental frequency component at f Hz and additional frequency components at 2f Hz, 3f Hz, 4f Hz and so on. The 2f component is called **second harmonic**, the 3f component is called **third harmonic** and so on. The fundamental frequency component is not considered as a harmonic. Out of all the harmonic components, the second harmonic has the largest amplitude.

As the second harmonic amplitude is largest, the second harmonic distortion is more important in the analysis of A.F. power amplifiers. The Fig. 5.24 shows the various harmonic components.

It can be seen from the Fig. 5.24 that the distorted waveform can be obtained by adding the fundamental and the harmonic components. The percentage harmonic distortion due to each order (2^{nd}, 3^{rd} and so on) can be calculated by comparing the amplitude of each order of harmonic with the amplitude of the fundamental frequency component.

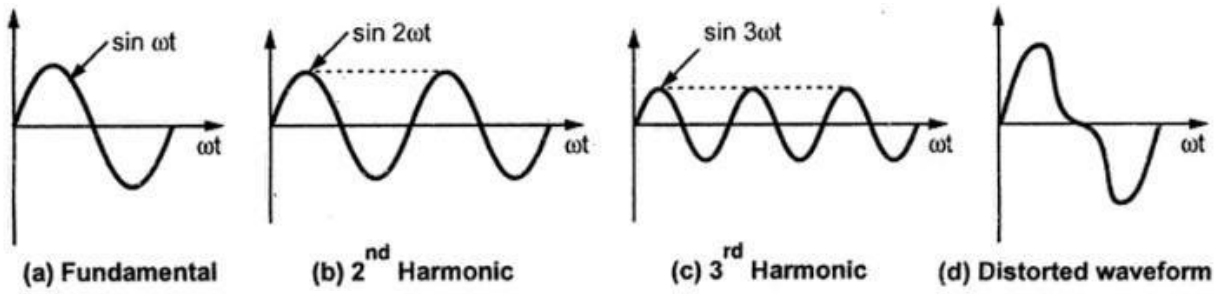


Fig 3.50 Distortion due to harmonic components

If the fundamental frequency component has an amplitude of B_1 and the n^{th} harmonic component has an amplitude of B_n then the percentage harmonic distortion due to n^{th} harmonic component is expressed as,

$$\% \; n^{th} \text{ harmonic distortion} = \% \; D_n = \frac{|B_n|}{|B_1|} \times 100 \qquad \ldots (1)$$

So $$\% \; D_2 = \frac{|B_2|}{|B_1|}, \; \% \; D_3 = \frac{|B_3|}{|B_1|}$$ and so on.

3.30.2 Total harmonic Distortion

When the output signal gets distorted due to various harmonic distortion components, the total harmonic distortion, which is the effective distortion due to all the individual components is given by

$$\% D = \sqrt{D_2^2 + D_3^2 + D_4^2 + \ldots} \times 100 \quad \ldots (2)$$

where D = Total harmonic distortion

As stated earlier, the most important component in the distortion is the second harmonic distortion. Let us discuss the graphical method of calculating second harmonic distortion.

3.30.3 Crossover Distortion

3.30.4 Elimination of Crossover Distortion

To eliminate the cross-over distortion some modifications are necessary, in the basic circuits of the class B amplifiers. The basic reason for the cross over distortion is the cut in voltage of the transistor junction. To overcome this cut-in voltage, a small forward biased is applied to the transistors. Let us see the practical circuits used to apply such forward biased, in the two types of class B amplifiers.

3.30.5 Intermediation Distortion

Another type of distortion present in the power amplifiers is intermodulation distortion. Due to the nonlinearity in the amplifier characteristics, sum and difference components of the input frequency appear at the output of the amplifier. These components distort the output of the power amplifier and such a distortion is called **intermodulation distortion.**

3.31 Thermal stability of power amplifier

The heat dissipation problem is very much analogous to a simple electric circuit and the Ohm's law. An electric current flows when there exists a potential difference while the heat flows when there exists a temperature difference ($T_2 - T_1$). Then similar to a electric resistance a thermal resistance can be obtained as,

$$\theta = \frac{T_2 - T_1}{P_d} \,^\circ C/W \text{ or } ^\circ C/mW \quad \ldots (3)$$

Where P_d is the heat dissipated or heat flow, due to the power dissipation.

From the above relation we can write,

$$T_2 - T_1 = \theta P_d \,^\circ C \quad \ldots (4)$$

and

$$P_d = \frac{T_2 - T_1}{\theta} \text{ W or mW} \quad \ldots (5)$$

Now to develop the thermal-electric analogy let us define some parameters as,

T_J = Junction Temperature

T_C = Case Temperature

T_A = Ambient Temperature

θ_{JA} = Total thermal resistance (junction to ambient)

θ_{JC} = Transistor thermal resistance (junction to case)

θ_{CS} = Insulator thermal resistance (case to heat sink)

θ_{SA} = Heat sink thermal resistance (heat sink to ambient)

The Fig. 5.26 shows a heat flow from a power transistor to ambient air via a heat sink.

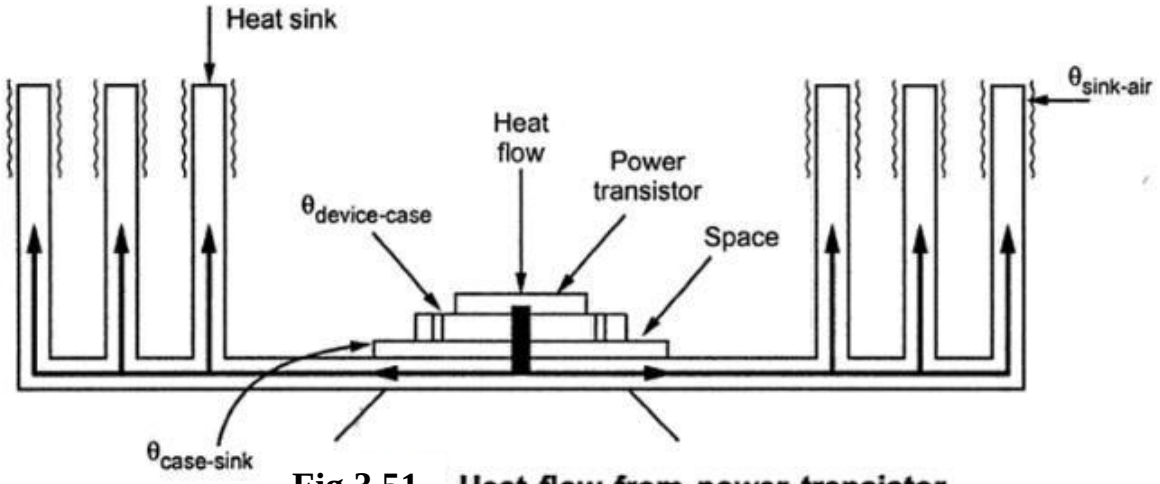


Fig 3.51 Heat flow from power transistor

From this heat flow diagram, an electrical analogous circuit can be obtained as,

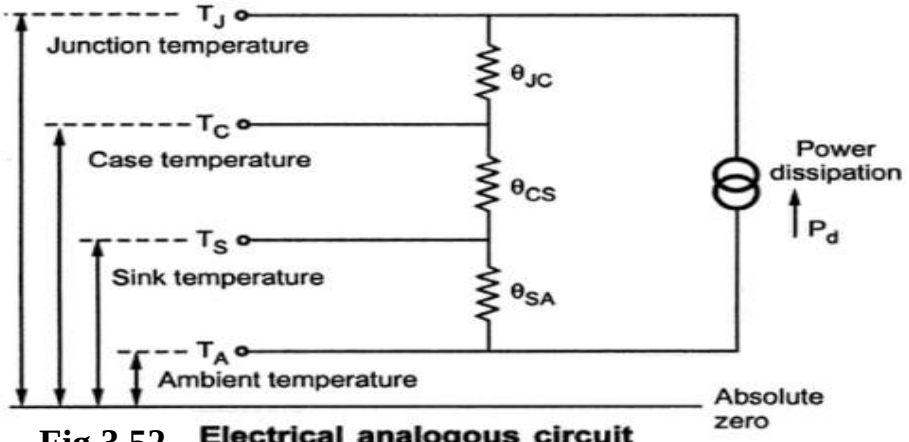


Fig 3.52 Electrical analogous circuit

The electrical analogous circuit is a simple series circuit.

Thus from the property of series circuit, the total thermal resistance can be obtained as,

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad °C/W \qquad \ldots (6)$$

But $\theta_{JA} = \dfrac{T_J - T_A}{P_d}$ ... from definition of θ in equation (3)

$$\therefore \quad T_J = P_d \theta_{JA} + T_A \qquad \ldots (7)$$

Thus the total power handling capacity P_d of the device can be obtained as,

$$P_d = \frac{T_J - T_A}{\theta_{JA}} = \frac{T_J - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}} \qquad \ldots (8)$$

Similarly the temperatures of case and sink can be obtained from,

$$\theta_{CS} = \frac{T_C - T_S}{P_d} \quad \ldots (9)$$

$$\theta_{SA} = \frac{T_S - T_A}{P_d} \quad \ldots (10)$$

or $$\theta_{CS} + \theta_{SA} = \frac{T_C - T_A}{P_d} \quad \ldots (11)$$

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4.1 INTRODUCTION

An ideal amplifier will provide a stable output which is in an amplified version of the input signal. But the gain and stability of practical amplifiers is not very good because of device parameter variation or due to changes in ambient temperature and nonlinearity of the device. This problem can be avoided by the technique of feedback wherein a portion of the output signal is feedback to the input and combined with the input signal to produce the desired output. The feedback can be either negative (degenerative) or positive (regenerative).In negative feedback a portion of the output signal is subtracted from the input signal and in positive feedback a portion of the output signal is added to the input signal to produce desired output. Negative feedback plays a very important role in almost all the amplifier stabilization of biasing circuits, it causes the location of the quiescent point to become stable. Thus it maintain a constant value of amplifier gain against temperature variation, supply voltage etc. The feedback may be classified into two types.

4.1.1Types of feedback

a.Positive feedback.

When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called positive feedback. This is illustrated in Fig. 1.1. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage Vf to be in phase with the input signalVin.The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers. One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

b.Negative feedback.

When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called negative feedback. This is illustrated in Fig. 1.2. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage Vf is 180° out of phase with the input signalVin.Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

c. Principles of Negative Voltage Feedback in Amplifiers

A feedback amplifier has two parts viz an amplifier and a feedback circuit. The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input. Fig. 1.3 *shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative. The output of the amplifier is 10 V. The fraction mv of this output i.e. 100 mV is fedback to the input where it is applied in series with the input signal of 101 mV. As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier. Referring to Fig. 1.3, we have, Gain of amplifier without feedback,The following points are worth noting:

1.When negative voltage feedback is applied, the gain of the amplifier is reduced. Thus, the gain of above amplifier without feedback is 10,000 whereas with negative feedback, it is only100.

2.When negative voltage feedback is employed, the voltage actually applied to the amplifier is extremely small. In this case, the signal voltage is 101 mV and the negative feedback is 100 mV so that voltage applied at the input of the amplifier is only 1mV.

3.In a negative voltage feedback circuit, the feedback fraction mv is always between 0 and 1.

4.The gain with feedback is sometimes called closed-loop gain while the gain without feedback is called open-loop gain. These terms come from the fact that amplifier and feedback circuits forma“loop”. When the loop is “opened” by disconnecting the feedback circuit from the input, the amplifier's gain is Av, the “open-loop” gain. When the loop is “closed” by connecting the feedback circuit, the gain decreases to Avf , the “closed-loop”gain.

d.Gain of Negative Voltage Feedback Amplifier

Consider the negative voltage feedback amplifier shown in Fig. 1.4. The gain of the amplifier without Feedback is Av. Negative feedback is then applied by feeding a fraction mv of the output voltage e0 back to amplifier input. Therefore, the actual input to the amplifier is the signal voltage eg minus feedback voltage m_V e0 i.e.,

Actual input to amplifier = $e_g - m_V e_0$

The output e0 must be equal to the input voltage $e_g - m_V e_0$ multiplied by gain Av of the amplifier i.e.,

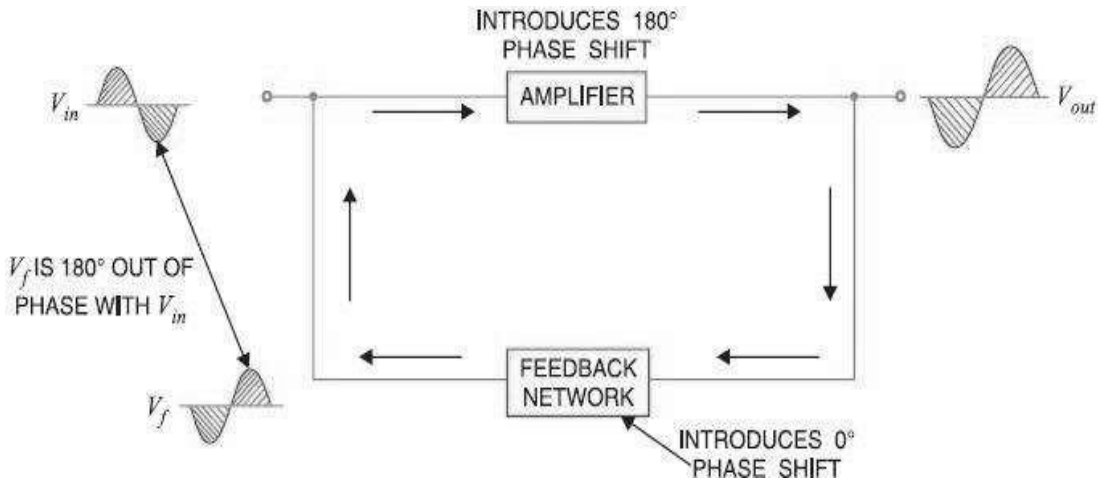


Fig 4.1 General feedback circuit

But e0/eg is the voltage gain of the amplifier with feedback. Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

It may be seen that the gain of the amplifier without feedback is Av. However, when negative voltage feedback is applied, the gain is reduced by a factor 1 + Av mv. It may be noted that negative voltage feedback does not affect the current gain of the circuit.

4.1.2 Advantages of Negative Voltage Feedback

The following are the advantages of negative voltage feedback in amplifiers:

(i) Gain stability. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product Av mv much greater than unity. Therefore, in the above relation, 1 can be

$$A_{vf} = \frac{A_v}{A_v m_v} = \frac{1}{m_v}$$

neglected as compared to Av mv and the expression become :

It may be seen that the gain now depends only upon feedback fraction mv i.e., on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

(ii) Reduces distortion. A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear distortion in large signal amplifiers. It can be proved mathematically that:

$$D_{vf} = \frac{D}{1 + A_v\, m_v}$$

where D = distortion in amplifier without feedback

D_{vf} = distortion in amplifier with negative feedback

It is clear that by applying negative voltage feedback to an amplifier, distortion is reduced by a factor 1 + Av mv.

(iii) Improves frequency response. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is *independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of theamplifier.

(iv) Increases circuit stability. The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilised or accurately fixed in value. This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

(v) Increases input impedance and decreases output impedance. The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

a) Input impedance. The increase in input impedance with negative voltage feedback can be explained. Suppose the input impedance of the amplifier is Zin without feedback and Z ′in with negative feedback. Let us further assume that input current is i1. Referring to Fig4.2, we

$$e_g - m_v e_0 = i_1 Z_{in}$$

Now

$$\begin{aligned} e_g &= (e_g - m_v e_0) + m_v e_0 \\ &= (e_g - m_v e_0) + A_v m_v (e_g - m_v e_0) \qquad [\because e_0 = A_v (e_g - m_v e_0)] \\ &= (e_g - m_v e_0)(1 + A_v m_v) \\ &= i_1 Z_{in} (1 + A_v m_v) \qquad [\because e_g - m_v e_0 = i_1 Z_{in}] \end{aligned}$$

or

$$\frac{e_g}{i_1} = Z_{in}(1 + A_v m_v)$$

have,

But eg/i1 = Z ′i n , the input impedance of the amplifier with negative voltage feedback.

$$Z'_{in} = Z_{in}(1 + A_v m_v)$$

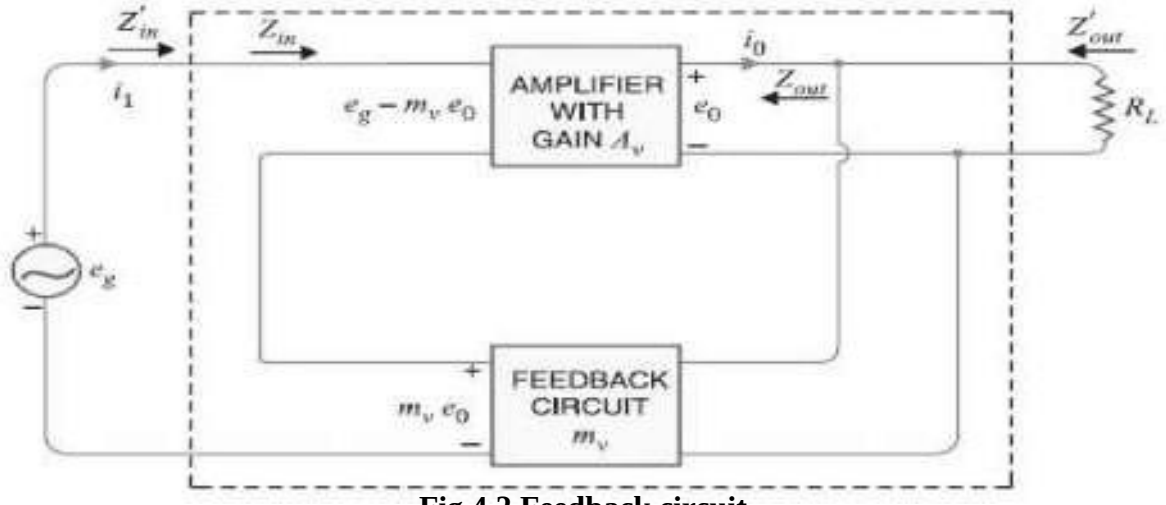


Fig 4.2 Feedback circuit

It is clear that by applying negative voltage feedback, the input impedance of the amplifier is increased by a factor 1 + Aν mv. As Aν mv is much greater than unity, therefore, input impedance is increased considerably. This is an advantage, since the amplifier will now present less of a load to its source circuit.

(b) Output impedance. Following similar line, we can show that output impedance with negative voltage feedback is givenby

$$\text{Voltage across } R_1 = \left(\frac{R_1}{R_1 + R_2}\right) e_0$$

$$\text{Feedback fraction, } m_v = \frac{\text{Voltage across } R_1}{e_0} = \frac{R_1}{R_1 + R_2}$$

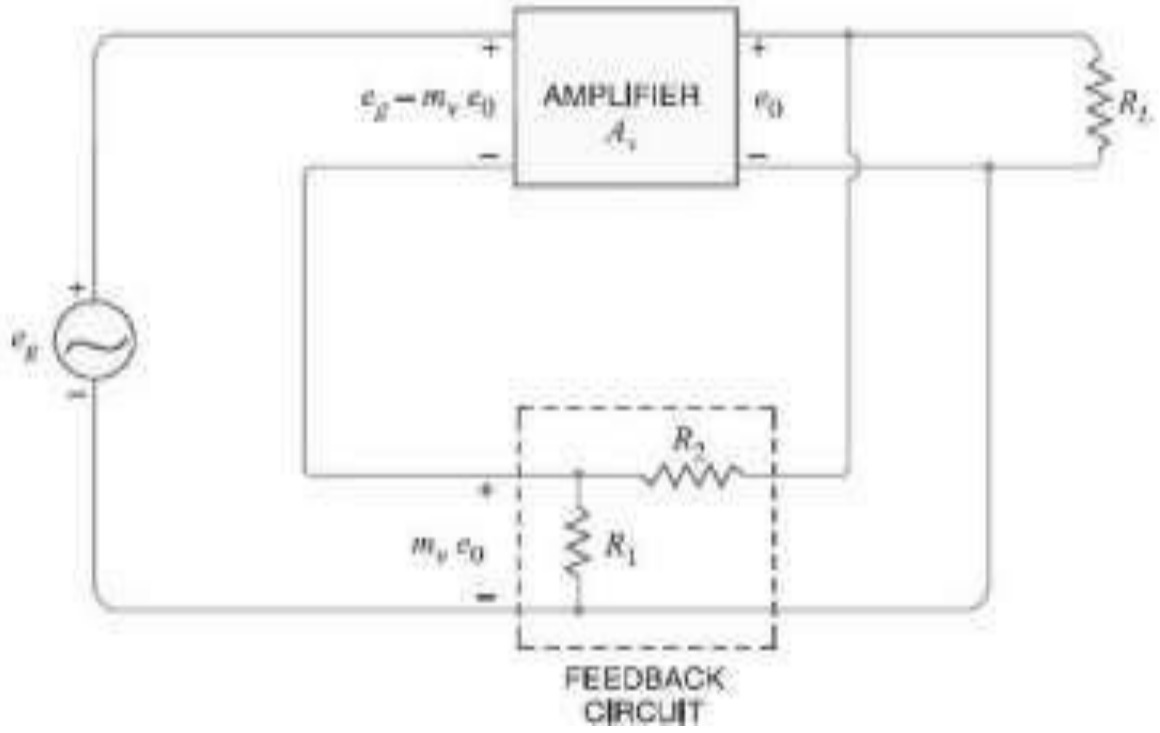


Fig 4.3 Negative Feedback circuit

$$Z'_{out} = \frac{Z_{out}}{1 + A_v m_v}$$

where Z'_{out} = output impedance with negative voltage feedback

Z_{out} = output impedance without feedback

It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor 1 + Avmv. This is an added benefit of using negative voltage feedback. With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

4.1.3 Disadvantages of negative feedback amplifier

- Reduced circuit overallgain
- Reduced stability at high frequency

4.2 Feedback Circuit

The function of the feedback circuit is to return a fraction of the output voltage to the input of the amplifier. Fig. 1.6 shows the feedback circuit of negative voltage feedback amplifier. It is essentially a potential divider consisting of resistances R1 and R2. The output voltage of the amplifier is fed to this potential divider which gives the feedback voltage to the input. Referring to Fig 4.4 it is clear that:

4.2.1 Basic Feedback Topologies

Depending on the input signal (voltage or current) to be amplified and form of the output (voltage or current), amplifiers can be classified into four categories. Depending on the amplifier category, one of four types of feedback structures should be used.

Voltage series feedback (*Af = Vo/Vs)* – Voltage amplifier Voltage shunt feedback (*Af = Vo/Is)* – Trans-resistance amplifierCurrent series feedback (*Af = Io /Vs)* - Trans-conductance amplifier Current shunt feedback (*Af = Io/Is)* - Current amplifier

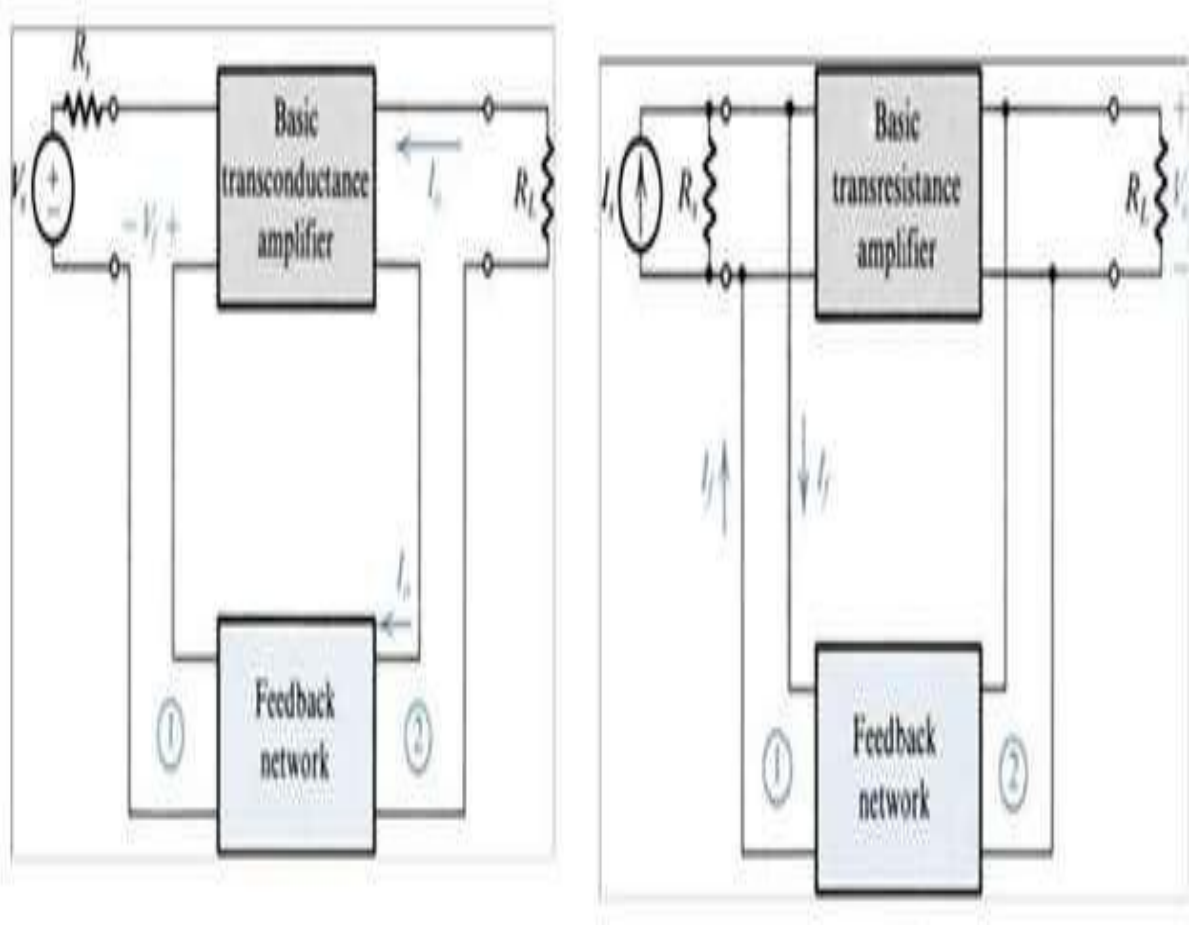
Here voltage refers to connecting the output voltage as input to the feedback network. Similarly current refers to connecting the output current as input to the feedback network. Series refers to connecting the feedback signal in series with the input voltage; Shunt refers to connecting the feedback signal in shunt (parallel) with an input current source.

Table Effects of Feedback[a]

Feedback Type	x_s	x_o	Gain Stabilized	Input Impedance	Output Impedance	Ideal Amplifier
Series voltage	v_s	v_o	$A_{vf} = \frac{A_v}{1 + A_v\beta}$	$R_i(1 + A_v\beta)$	$\frac{R_o}{1 + \beta A_{voc}}$	Voltage
Series current	v_s	i_o	$G_{mf} = \frac{G_m}{1 + G_m\beta}$	$R_i(1 + G_m\beta)$	$R_o(1 + \beta G_{msc})$	Transconductance
Parallel voltage	i_s	v_o	$R_{mf} = \frac{R_m}{1 + R_m\beta}$	$\frac{R_i}{1 + R_m\beta}$	$\frac{R_o}{1 + \beta R_{moc}}$	Transresistance
Parallel current	i_s	i_o	$A_{if} = \frac{A_i}{1 + A_i\beta}$	$\frac{R_i}{1 + A_i\beta}$	$R_o(1 + \beta A_{isc})$	Current

[a] Formulas given assume an ideal controlled source for the feedback network (as shown in Figure 9.14), zero source impedance for series feedback, and infinite source impedance for parallel feedback. Gains with subscripts sc and oc are for short-circuit and open-circuit loads, respectively. The gains A_v, G_m, R_m, and A_i are for the actual load.

(a) (b)



(c) (d)

Fig 4.4 Topologies of feedback circuit

4.22 Types of Negative Feedback Connection

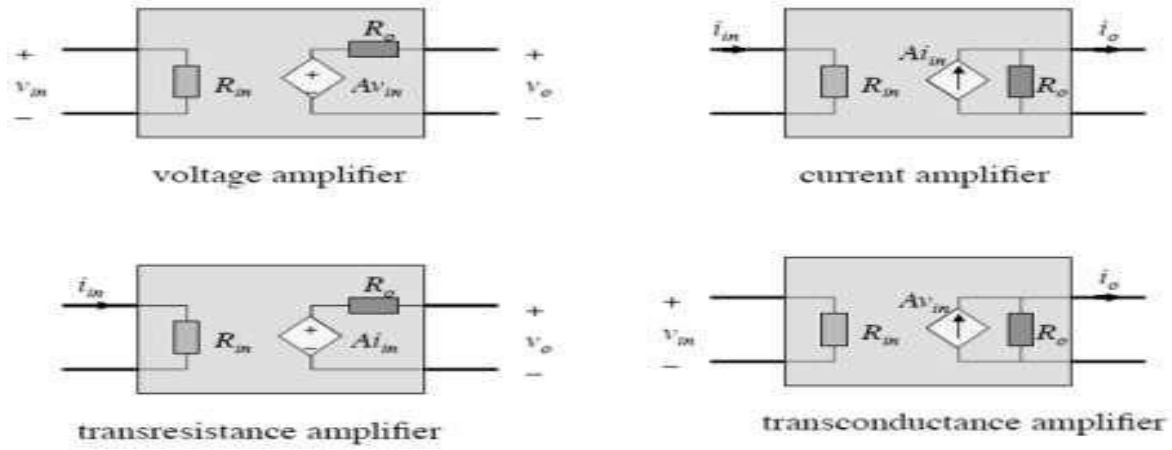
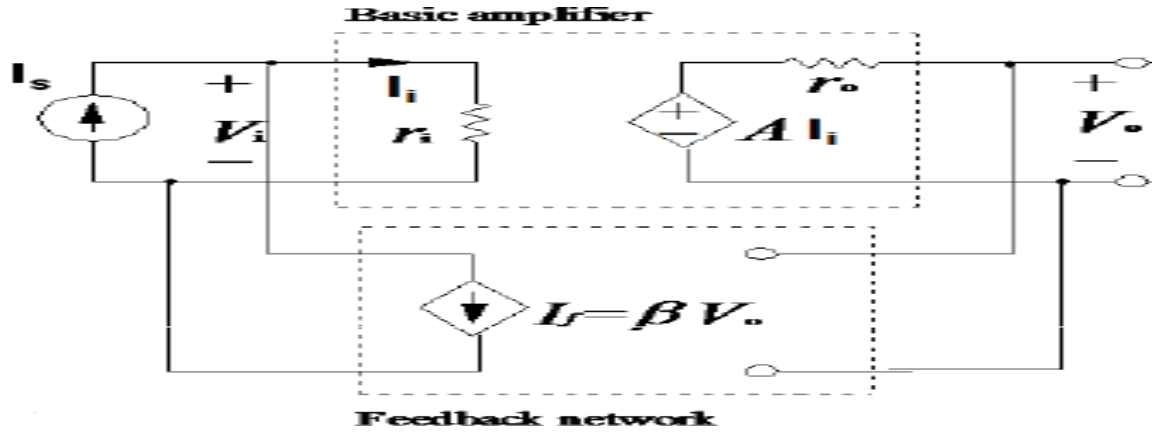


Fig 4.5 Models of Amplifier

4.3Feedback topologies

4.3.1 Voltage shunt feedback



Voltage gain

$$V_o = A \cdot I_i = A(I_S - I_f)$$
$$I_f = \beta \cdot V_o$$
$$A(I_S - \beta V_o) = V_o$$
$$AI_S = (1 + \beta A)V_o$$
$$A_f = \frac{V_o}{I_S} = \left(\frac{A}{1 + \beta A}\right)$$

Input impedance

$$Z_{\text{in}} = \frac{V_i}{I_S} = \frac{V_i}{I_i + I_f}$$
$$= \frac{I_i \cdot r_i}{I_i + \beta V_o)} = \frac{I_i \cdot r_i}{I_i + \beta A I_i}$$
$$Z_{\text{in}} = \frac{r_i}{(1 + \beta A)}$$

Output impedance

$$Z_{\text{out}}\,|_{V_S=0} = \frac{V_o}{I_o}$$

from input port,

$$I_i = -I_f = -\beta V_o$$

from output port,

$$I_o = \frac{V_o - AI_i}{r_o} = \frac{V_o + \beta A V_o}{r_o}$$

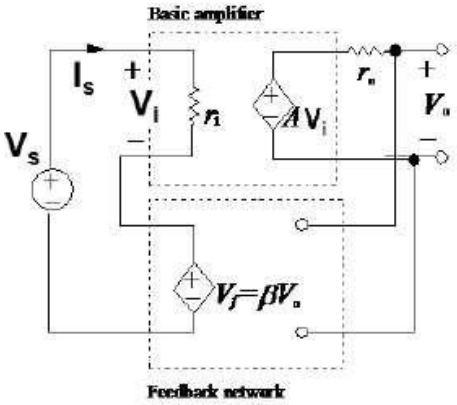
$$Z_{\text{out}} = \frac{V_o}{I_o} = \frac{r_o}{(1 + \beta A)}$$

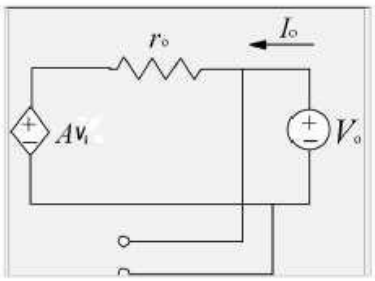
4.3.2 Voltage series feedback

$$V_o = A \cdot V_i = A(V_S - V_f)$$
$$V_f = \beta \cdot V_o$$
$$A(V_S - \beta V_o) = V_o$$
$$AV_S = (1+\beta A)V_o$$
$$A_f = \frac{V_o}{V_S} = (\frac{A}{1+\beta A})$$

$$Z_{\text{in}} = \frac{V_S}{I_S} = \frac{V_i + V_f}{I_S}$$
$$= \frac{V_i + \beta V_o}{I_S} = \frac{V_i + \beta A V_i}{I_S}$$
$$Z_{\text{in}} = \frac{V_i(1+\beta A)}{I_S} = r_i(1+\beta A)$$

$$Z_{\text{out}}|_{V_S=0} = \frac{V_o}{I_o}$$
$$I_o = \frac{V_o - A \cdot V_i}{r_o}$$
$$V_i + \beta \cdot V_o = V_S = 0$$
$$V_i = -\beta \cdot V_o$$
$$I_o = \frac{V_o + A \cdot \beta \cdot V_o}{r_o}$$
$$Z_{\text{out}} = \frac{V_o}{I_o} = \frac{r_o}{1+A \cdot \beta}$$

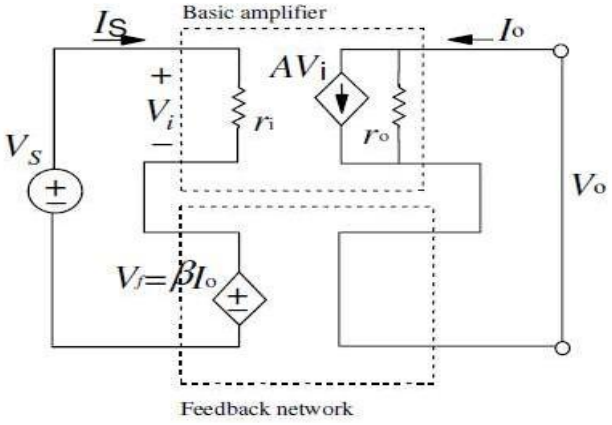




4.3.3 Current series feedback

Voltage Gain

$$I_o = A \cdot V_i = A(V_S - V_f)$$
$$V_f = \beta \cdot I_o$$
$$A(V_S - \beta I_o) = I_o$$
$$AV_S = (1+\beta A)I_o$$
$$A_f = \frac{I_o}{V_S} = (\frac{A}{1+\beta A})$$



Input Impedance

$$Z_{\text{in}} = \frac{V_S}{I_S} = \frac{V_i + V_f}{I_S}$$
$$= \frac{V_i + \beta V_o}{I_S} = \frac{V_i + \beta A V_i}{I_S}$$
$$Z_{\text{in}} = \frac{V_i(1+\beta A)}{I_S} = r_i(1+\beta A)$$

Output Impedance

$$V_i + V_f = V_S = 0$$

$$I_o = \frac{V_o + A \cdot \beta \cdot I_o}{r_o}$$

$$Z_{\text{out}}\,|_{V_S=0} = \frac{V_o}{I_o}; I_o = \frac{V_o - A \cdot V_i}{r_o}$$

$$\boxed{Z_{\text{out}} = \frac{V_o}{I_o} = \frac{r_o}{1 + A \cdot \beta}}$$

4.4 OSCILLATORS

4.4.1 Introduction

An oscillator is a circuit that produces a repetitive signal from a dc voltage. The feedback type oscillator which rely on a positive feedback of the output to maintain the oscillations. The relaxation oscillator makes use of an RC timing circuit to generate a non-sinusoidal signal such as square wave.

The requirements for oscillation are described by the Baukhausen criterion:

- The magnitude of the loop gain Aβ must be1
- The phase shift of the loop gain A β must be 0^o or 360^o or integer multiple of2pi

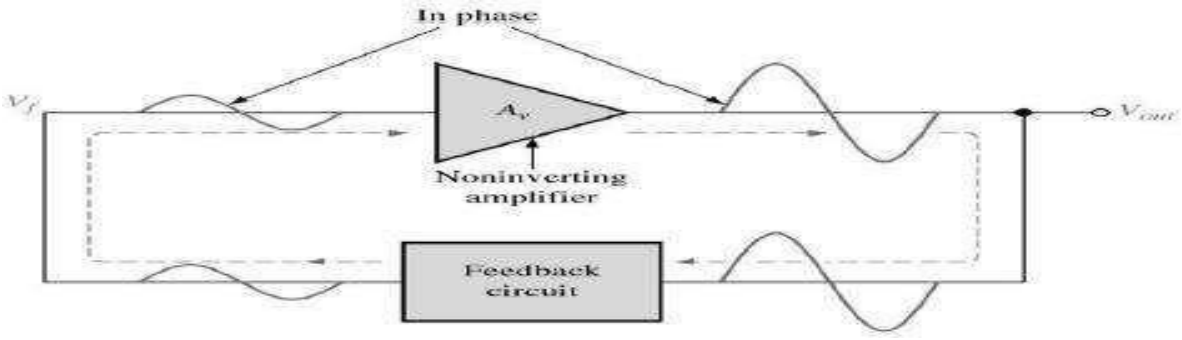


Fig 4.6 Oscillators

- In both the oscillators above, the loop gain is set by componentvalues
- In practice the gain of the active components is veryvariable
- If the gain of the circuit is too high it willsaturate
- If the gain of the circuit is too low the oscillation willdie

Real circuits need some means of stabilizing the magnitude of the oscillation to cope with variability in the gain of the circuit

4.4.2 Barkhausan criterion

The conditions for oscillator to produce oscillation are given by Barkhausan criterion. They are:

- The total phase shift produced by the circuit should be 360^o or0^o
- The Magnitude of loop gain must be greater than or equal to 1(ie)$|A\beta| \geq 1$

In practice loop gain is kept slightly greater than unity to ensure that oscillator work even if there is a slight change in the circuit parameters

4.4.3 Mechanism of start ofoscillation

The starting voltage is provided by noise, which is produced due to random motion of electrons in resistors used in the circuit. The noise voltage contains almost all the sinusoidal frequencies. This low amplitude noise voltage gets amplified and appears at the output terminals. The amplified noise drives the feedback network which is the phase shift network. Because of this the feedback voltage is maximum at a particular frequency, which in turn represents the frequency of oscillation.

4.4.4 LC Oscillator:

Oscillators are used in many electronic circuits and systems providing the central "clock" signal that controls that controls the sequential operation of the entire system. Oscillators convert a DC input (the supply voltage) into an AC output (the waveform), which can have a wide range of different wave shapes and frequencies that can be either complicated in nature or simple sine waves depending upon the application.

Oscillators are also used in many pieces of test equipment producing either sinusoidal sine wave, square, saw tooth or triangular shaped waveforms or just a train of pulse of a variable or constant width. LC Oscillators are commonly used in radio-frequency circuits because of their good phase noise characteristics and their ease ofimplementation.

An Oscillator is basically an Amplifier with "Positive Feedback", or regenerative feedback (in-phase) and one of the many problems in electronic circuit design is stooping amplifiers from oscillating while trying to get oscillators to oscillate. Oscillators work becausethey overcome the losses of their feedback resonator circuit either in the form of a capacitor or both in the same circuit by applying DC energy at the required frequency into this resonator circuit.In other words, an oscillator is an amplifier which uses positive feedback that generates an output frequency without the use of an inputsignal.

It is self-sustaining. Then an oscillator has a small signal feedback amplifier with an open-loop gain equal to or slightly greater than one for oscillations to start but to continue oscillations the average loop gain must return to unity. In addition to these reactive components, an amplifying device such as an Operational Amplifier or Bipolar Transistors required. Unlike an amplifier there is no external AC input required to cause the Oscillator to work as the DC supply energy is converted by the oscillator into AC energy at the required frequency.

4.5 Basic Oscillator Feedback Circuit

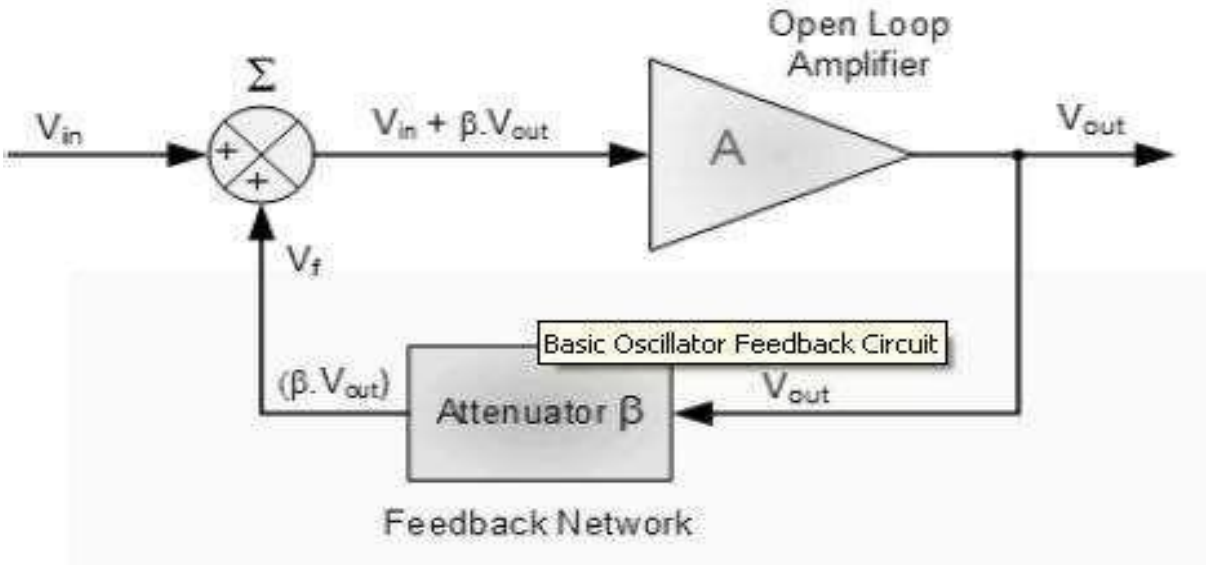


Fig 4.7 Basic Oscillator Feedback Circuit

Where: β is a feedback fraction.

$$\text{Gain, } Av = \frac{Vout}{Vin}$$

A = open loop voltage gain

$$Av \times Vin = Vout$$

$$Av(Vin - \beta Vout) = Vout$$

β is the feedback fraction

$$Av.Vin - Av.\beta.Vout = Vout$$

Aβ = the loop gain

$$Av.Vin = Vout(1 + A\beta)$$

1 + Aβ = the feedback factor

$$\therefore \frac{Vout}{Vin} = Gv = \frac{A}{1 + A\beta}$$

Gv = the closed loop gain

4.5.1 Basic Oscillator Feedback Circuit withFeedback

Oscillators are circuits that generate a continuous voltage output waveform at a required frequency with the values of the inductors, capacitors or resistors forming a frequency selective LC resonant tank circuit and feedback network. This feedback network is an attenuation network which has a gain of less than one ($\beta<1$) and starts oscillations when A $\beta>1$ which returns to unity (A $\beta=1$) once Oscillations commence. The LC oscillator's frequency is controlled using a tuned or resonant inductive/capacitive (LC) circuit with the resulting output frequency being known as the Oscillation Frequency.By making the oscillators feedback a reactive network the phase angle of the feedback will vary as a function of frequency and this is called Phase-shift.

There are basically types of Oscillators:

- Sinusoidal Oscillators - these are known as Harmonic Oscillators and are generally a: LC Tuned-feedback" or "RC tuned-feedback" type Oscillator that generates a purely sinusoidal waveform which is of constant amplitude andfrequency.

- Non-Sinusoidal Oscillators – these are known as Relaxation Oscillators and generate complex non-sinusoidal waveforms that changes very quickly from one condition of stability to another such as "Square-wave", "Triangular-wave" or "Saw toothed-wave" typewaveforms.

4.5.2 Resonance

When a constant voltage but of varying frequency is applied to a circuit consisting of an inductor, capacitor and resistor the reactance of both the Capacitor/Resistor and Inductor/Resistor circuits is to change both the amplitude and the phase of the output signal due to the reactance of the componentsused.At high frequencies the reactance of a capacitor is very low acting as a short circuit while the reactance of the inductor is high acting as an open circuit. At low frequencies the reverse is true, the reactance of the capacitor acts as an open circuit and the reactance of the inductor acts as a shortcircuit.Between these two extremes the combination of the inductor and capacitor produces a "Tuned" or "Resonant" circuit that has a Resonant Frequency, (fr) in which the capacitive and inductive reactance's are equal and cancel out each other, leaving only the resistance of the circuit to oppose the flow of current. This means that there is no phase shift as the current is in phase with the voltage. Consider the circuit below.

4.5.3 B**asic LC Oscillator TankCircuit**

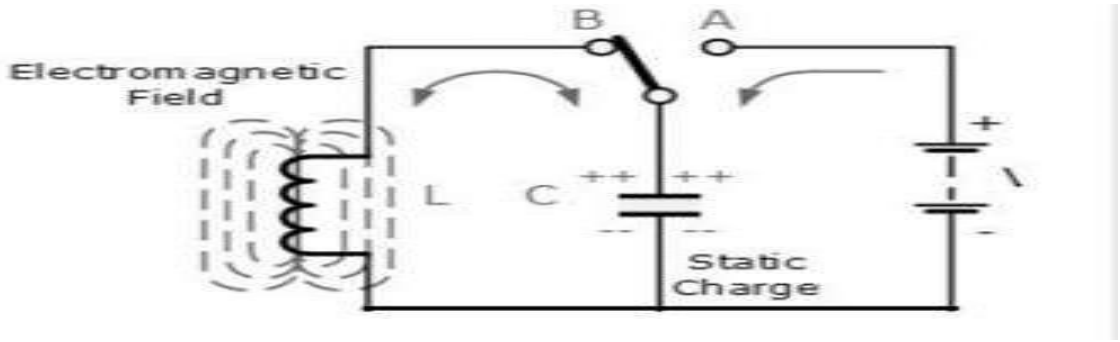


Fig 4.8 Basic LC Oscillator TankCircuit

The circuit consists of an inductive coil, L and a capacitor, C. The capacitor stores energy in the form of an electrostatic field and which produces a potential (static voltage) across its plates, while the inductive coil stores its energy in the form of an electromagnetic field.The capacitor is charged up to the DC supply voltage, V by putting the switch in positionA. When the capacitor is fully charged the switch changes to position B. The charged capacitor is now connected in parallel across the inductive coil so the capacitor begins to discharge itself through the coil.The voltage across C starts falling as the current through the coil begins to rise. This rising current sets up an electromagnetic field around the coil which resists this flow of current. When the capacitor, C is completely discharged the energy that was originally stored in thecapacitor, C as an electrostatic filed is now stored in the inductive coil, L as an electromagnetic field around the coils windings.As there is now no external voltage in the circuit to maintain the current within the coil, it starts to fall as the electromagnetic field begins to collapse. A back emf is induced in the coil (e=-Ldi/dt) keeping the current flowing in the original direction. This current now charges up the capacitor, c with the opposite polarity to its original charge.C continues to charge up until the current reduces to zero and the electromagnetic field of the coil has collapsed completely. The energy originally introduced into the circuit through the switch, has been returned to the capacitor which again has an electrostatic voltage potential across it, although it is now of the opposite polarity. The capacitor now starts to discharge again back through the coil and the whole process os repeated. The polarity of the voltage changes as the energy is passed back and forth between the capacitor and inductor producing an AC type sinusoidal voltage and current waveform.

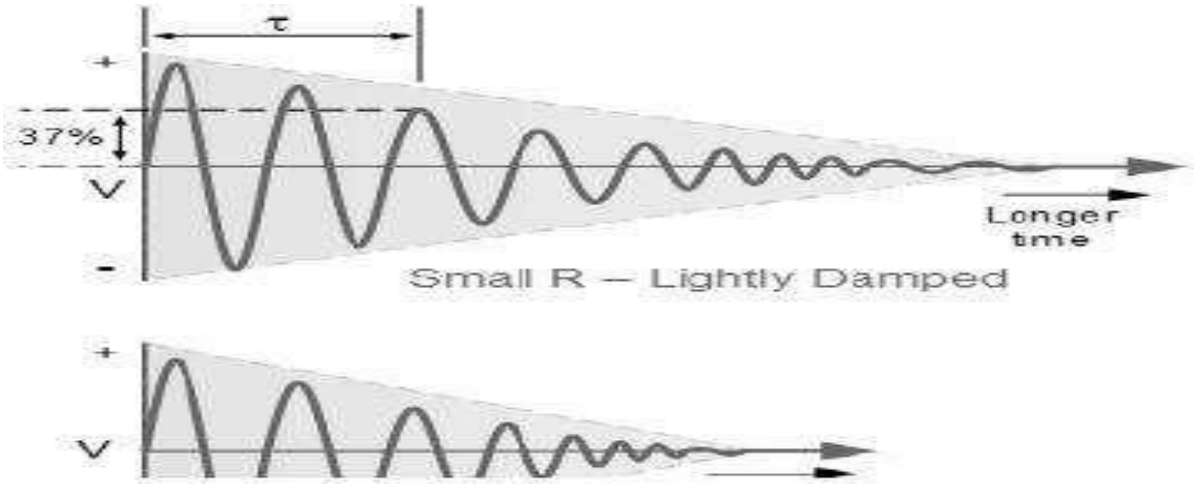


Fig 4.9 Basic LC Oscillator Tank Circuit Output

This then forms the basis of an LC oscillator's tank circuit and theoretically this cycling back and forth will continue indefinitely. However, every time energy is transferred from C to L or from L to C losses occur which decay the oscillations.This oscillatory action of passing energy back and forth between the capacitor, C to the inductor, L would continue indefinitely if it was not for energy losses within the circuit. Electrical energy is lost in the DC or real resistance of the inductors coil, in the dielectric of the capacitor, and in radiation from the circuit so the oscillation steadily decreases until they die away completely and the processstops.Then in a practical LC circuit the amplitude of the oscillatory voltage decreases at each half cycle of oscillation and will eventually die away to zero. The oscillations are then said to be "damped" with the amount of damping being determined by the quality or Q-factor of the circuit.

4.5.3.1 Damped Oscillations

The frequency of the oscillatory voltage depends upon the value of the inductance and capacitance in the LC tank circuit. We now know that for resonance to occur in the tank circuit, there must be a frequency point were the value of XC, the capacitive reactance is the same as the value of XL, the inductive reactance ($X_L = X_C$) and which will therefore cancel out each other out leaving only the DC resistance in the circuit to oppose the flow of current. If we now place the curve for inductive reactance on top of the curve for capacitive reactance so that both curves are on the same axes, the point of intersection will give us the resonance frequency point, (fr or ωr) as shown below.

4.5.4 Resonance Frequency

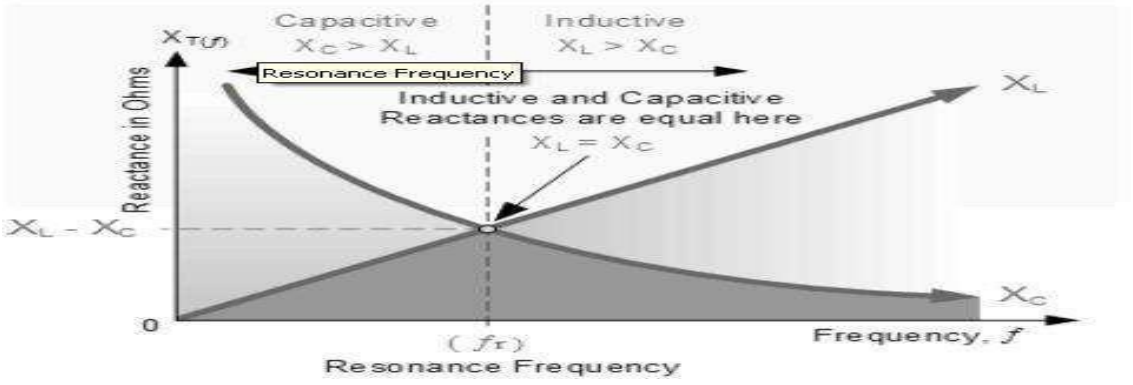


Fig 4.10 Resonance Frequency

Where: fr is in Hertz, L is in Henries and C is in Farads. Then the frequency at which this will happen is given as:

$$X_L = 2\pi f L \quad \text{and} \quad X_C = \frac{1}{2\pi f C}$$

$$\text{at resonance:} \quad X_L = X_C$$

$$\therefore \quad 2\pi f L = \frac{1}{2\pi f C}$$

$$2\pi f^2 L = \frac{1}{2\pi C}$$

$$\therefore \quad f^2 = \frac{1}{(2\pi)^2 LC}$$

$$f = \frac{\sqrt{1}}{\sqrt{(2\pi)^2 LC}}$$

Then by simplifying the above equation we get the final equation for ResonantResonantFrequency of a LCOscillator

$$f_I = \frac{1}{2\pi\sqrt{LC}}$$

Where:L is the Inductance in Henries C is the Capacitance in Farads

fr is the Output Frequency in Hertz

This equation shows that if either L or C are decreased, the frequency increases. This output frequency is commonly given the abbreviation of (fr) to identify it as the "resonant frequency". To keep the oscillations going in an LC tank circuit, we have to replace all the energy lost in each oscillation and also maintain the amplitude of these oscillations at a

constantlevel.The amount of energy replaced must therefore be equal to the energy lost during eachcycle. If the energy replaced is too large the amplitude would increase until clipping of the supply rails occurs. Alternatively, if the amount of energy replaced is too small the amplitude would eventually decrease to zero over time and the oscillations wouldstop.The simplest way of replacing this lost energy is to take part of the output from the LC tank circuit, amplify it and then feed it back into the LC circuit again. This process can be achieved using a voltage amplifier using an op-amp, FET or bipolar transistor as its active device.However, if the loop gain of the feedback amplifier is too small, the desired oscillation decays to zero and if it is too large, the waveform becomes distorted. To produce a constant oscillation, the level of the energy fed back to the LC network must be accurately controlled.Then there must be some form of automatic amplitude or gain control when the amplitude tries to vary from a reference voltage either up or down. To maintain a stable oscillation the overall gain of the circuit must be equal to one or unity. Any less and the oscillations will not start or die away to zero, any more the oscillations will occur but the amplitude will become clipped by the supply rails causing distortion. Consider the circuitbelow.

4.6 Basic Transistor LC OscillatorCircuit

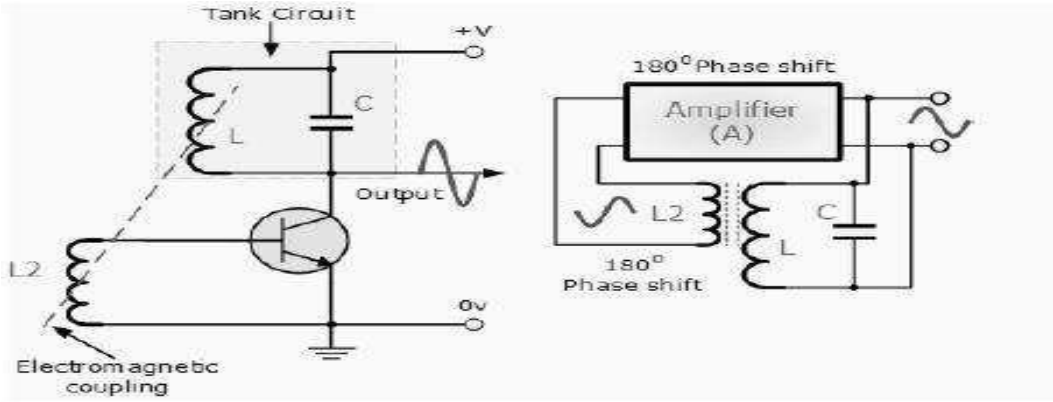


Fig 4.11 Basic Transistor LC OscillatorCircuit

A Bipolar Transistor is used as the LC oscillator's amplifier with the tuned LC tank circuit acts as the collector load. Another coil L2 is connected between the base and the emitter of the transistor whose electromagnetic field is "mutually" coupled with that of coil L. Mutual inductance exists between the two circuits.The changing current flowing in one coil circuit induces, by electromagnetic induction, a potential voltage in the other (transformer effect) so as the oscillations occur in the tuned circuit, electromagnetic energy is transferred from coil L to coil L2 and a voltage of the same frequency as that in the tuned circuit is applied between the base and emitter of the transistor.

In this way the necessary automatic feedback voltage is applied to the amplifying transistor. The amount of feedback can be increased or decreased by altering the coupling between the two coils L and L2. When the circuit is oscillating its impedance is resistive and the collector and base voltages are 180 out of phase. In order to maintain oscillations (called frequency stability) the voltage applied to the tuned circuit must be "in-phase" with the oscillations occurring in the tuned circuit.

Therefore, we must introduce an additional 180^o phase shift into the feedback path between the collector and the base. This is achieved by winding the coil of L2 in the correct direction relative to coil L giving us the correct amplitude and phase relationships for the Oscillators circuit or by connecting a phase shift network between the output and input of the amplifier.The LC Oscillator is therefore a "Sinusoidal Oscillator" or a "Harmonic Oscillator" as it is more commonly called. LC oscillators can generate high frequency sine waves for use in radio frequency (RF) type applications with the transistor amplifier being of a Bipolar Transistor or FET.Harmonic Oscillators come in many different forms because there are many different ways to construct an LC filter network and amplifier with the most common being the Hartley LC Oscillator**,** Colpitts LC Oscillator**,** Armstrong Oscillator and Clapp Oscillator to name afew.

4.6.1 Types of LC Oscillators

- Hartley oscillator.
- Colpitts oscillator.
- Clapp oscillator.
- Armstrong oscillator.

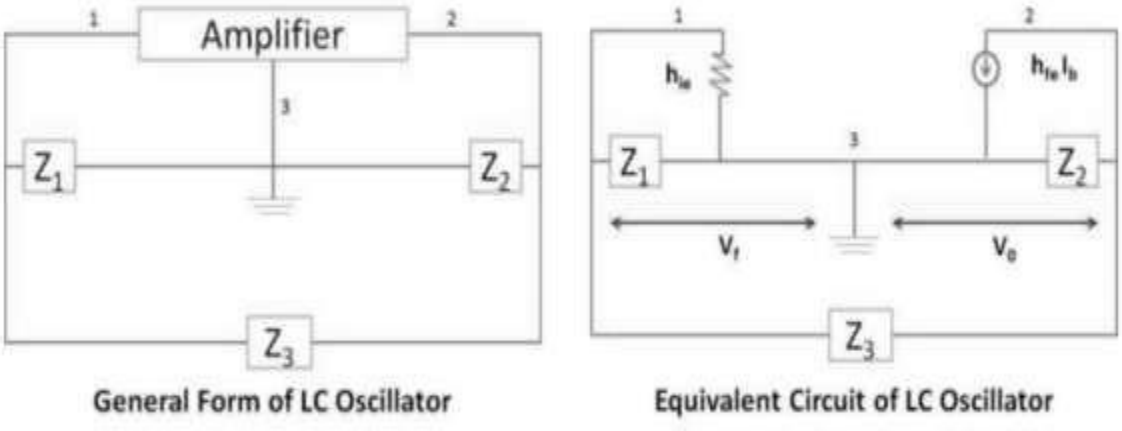


Fig 4.12 General Form of LC Oscillators

In the general form of LC oscillator any of the active devices such as Vacuum tube,

$$Z' = z_1 \parallel h_{ie} = \frac{z_1 h_{ie}}{z_1 + h_{ie}}$$

$$Z_L = z' + z_3 \parallel z_2$$

$$Z_L = \frac{z_1 z_3 h_{ie}}{z_3 z_1 + z_3 h_{ie}} \parallel z_2 \qquad Z_L = \frac{\frac{z1z2z3hie}{z3z1 + z3hie}}{\frac{z1z2z3 + z2z3hie + z1z3hie}{z3z1 + z3hie}}$$

$$Z_L = \frac{z_1 h_{ie}}{z_1 + h_{ie}} + z_3 \parallel z_2 \qquad \boxed{Z_L = \frac{z2\,[\,h_{ie}(z_1 + z_3) + z_1 z_3]}{h_{ie}(z_1 + z_2 + z_3) + z_1 z_3 + z_1 z_2}}$$

Transistor, FET, Op-Amp may be used in the amplifier section.

$$V_o = -I_1(Z^1 + Z_3) = -I_1 \frac{h_{ie} z_3 + h_{ie} z_1 + z_1 z_3}{h_{ie} + z_1}$$

$$V_f = -I_1 Z^1 = -I_1 \frac{z_1 h_{ie}}{z_1 + h_{ie}} \qquad V_f = \frac{Z' V_o}{z' + z3}$$

$$\beta = \frac{V_f}{V_o} = \frac{z_1 h_{ie}}{h_{ie}(z_1 + z3) + z1z3}$$

$$A_v = \frac{-h_{fe}}{h_{ie}} Z_L$$

$$A_v \beta = 1$$

$$\frac{-h_{fe}}{h_{ie}} \quad \frac{z2\,[\,h_{ie}(z_1 + z_3) + z_1 z_3]}{h_{ie}(z_1 + z_2 + z_3) + z_1 z_3 + z_1 z_2} \quad \frac{z_1 h_{ie}}{h_{ie}(z_1 + z3) + z1z3} = 1$$

General Equation of LC Oscillator:

$$\boxed{h_{ie}(z_1 + z_2 + z_3) + z_1 z_2 (1 + h_{fe}) z_1 z_3 = 0}$$

4.6.2 The Hartley Oscillator

The main disadvantages of the basic LC Oscillator circuit we looked at in the previous tutorial is that they have no means of controlling the amplitude of the oscillations and also, it is difficult to tune the oscillator to the required frequency.However, it is possible to feedback exactly the right amount of voltage for constant amplitude oscillations. If we feed back more than is necessary the amplitude of the oscillations can be controlled by biasing the amplifier in such a way that if the oscillations increase in amplitude, the bias is increased and the gain of the amplifier is reduced.

If the amplitude of the oscillations decreases the bias decreases and the gain of the amplifier increases, thus increasing the feedback. In this way the amplitude of the oscillations are kept constant using a process known as Automatic Base Bias**.**One big advantage of automatic base bias in a voltage controlled oscillator, is that theoscillator can be made more efficient by providing a Class-B bias or even a Class-C bias condition of the transistor. This has the advantage that the collector current only flows during part of the oscillation cycle so the quiescent collector current is verysmall.

Then this "self-tuning" base oscillator circuit forms one of the most common types of LC parallel resonant feedback oscillator configurations called the Hartley Oscillator circuit.

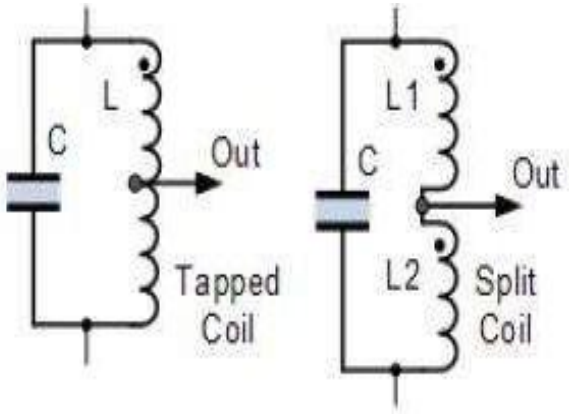


Fig 4.13 LC parallel resonant feedback oscillator

4.6.2.1 Hartley Oscillator Tuned Circuit

In the Hartley Oscillator the tuned LC circuit is connected between the collector and the base of the transistor amplifier. As far as the oscillatory voltage is concerned, the emitter is connected to a tapping point on the tuned circuit coil.The feedback of the tuned tank circuit is taken from the centre tap of the inductor coil or even two separate coils in series which are in parallel with a variable capacitor, C as shown.The Hartley circuit is often referred to as a split-inductance oscillator because coil L is centre-tapped. In effect, inductance L acts like two separate coils in very close proximity with the current flowing through coil section XY induces a signal into coil section YZbelow.

A Hartley Oscillator circuit can be made from any configuration that uses either a single tapped coil (similar to an autotransformer) or a pair of series connected coils in parallel with a single capacitor as shown below.

4.6.2.2 Basic Hartley Oscillator Circuit

When the circuit is oscillating, the voltage at point X (collector), relative to point Y (emitter), is 180^o out-of-phase with the voltage at point Z (base) relative to point Y. At the frequency of oscillation, the impedance of the Collector load is resistive and an increase in Base voltage causes a decrease in the Collector voltage. Then there is a 180 phase change in the voltage between the Base and Collector and this along with the original 180 phase shift in the feedback loop provides the correct phase relationship of positive feedback for oscillations to be maintained.

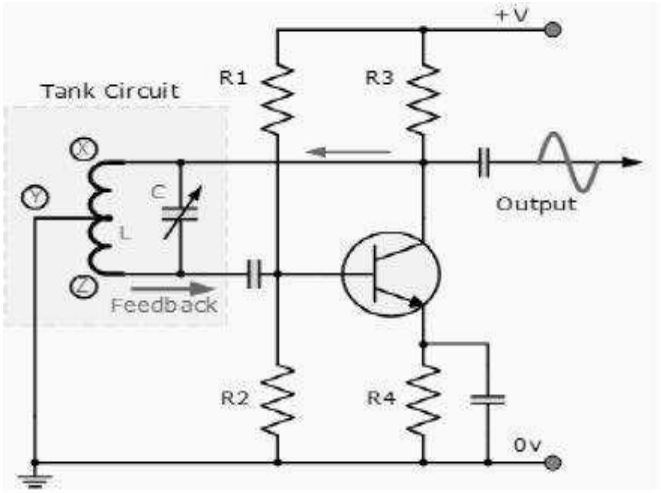


Fig 4.14 Hartley Oscillator

The amount of feedback depends upon the position of the "tapping point" of the inductor. If this is moved nearer to the collector the amount of feedback is increased, but the output taken between the Collector and earth is reduced and vice versa.Resistors, R1 and R2 provide the usual stabilizing DC bias for the transistor in the normal manner while the capacitors act as DC-blocking capacitors.In this Hartley Oscillator circuit, the DC Collector current flows through part of the coil and for this reason the circuit is said to be "Series-fed" with the frequency of oscillation of the Hartley Oscillator being given as.

$$f = \frac{1}{2\pi\sqrt{L_T C}}$$

where: $L_T = L_1 + L_2 + 2M$

The frequency of oscillations can be adjusted by varying the "tuning" capacitor, C or by

varying the position of the iron-dust core inside the coil (inductive tuning) giving an output overa wide range of frequencies making it very easy to tune. Also the Hartley Oscillator produces an output amplitude which is constant over the entire frequency range.As well as the Series-fed Hartley Oscillator above, it is also possible to connect the tuned Tank circuit across the amplifier as a shunt-fed oscillator as shownbelow.

4.7 Armstrong oscillator

The Armstrong oscillator (also known as Meissner oscillator) is named after the electrical engineer Edwin Armstrong, its inventor. It is sometimes called a tickler oscillator because the feedback needed to produce oscillations is provided using a tickler coil via magnetic coupling between coil L and coil T.Assuming the coupling is weak, but sufficient to sustain oscillation, the frequency is determined primarily by the tank circuit (**L** and **C** in the illustration) and is approximately given by. In a practical circuit, the actual oscillation frequency will be slightly different from the value provided by this formula because of stray capacitance and inductance, internal losses (resistance), and the loading of the tank circuit by the ticklercoil.This circuit is the basis of the regenerative receiver for amplitude modulated radio signals. In that application, an antenna is attached to an additional tickler coil, and the feedback is reduced, for example, by slightly increasing the distance between coils **T** and **L**, so the circuit is just short ofoscillation.The result is a narrow-band radio-frequency filter and amplifier. The non- linear characteristic of the transistor or tube provides the demodulated audio signal.

4.8 Colpitts Oscillator

The Colpitts Oscillator, named after its inventor Edwin Colpitts is another type of LC oscillator design. In many ways, the Colpitts oscillator is the exact opposite of the Hartley Oscillator we looked at in the previous tutorial. Just like the Hartley oscillator, the tuned tank circuit consists of an LC resonance sub-circuit connected between the collector and the base of a single stage transistor amplifier producing a sinusoidal output waveform.

The basic configuration of the Colpitts Oscillator resembles that of the Hartley Oscillator but the difference this time is that the centre tapping of the tank sub-circuit is now made at the junction of a "capacitive voltage divider" network instead of a tapped autotransformer type inductor as in the Hartleyoscillator.

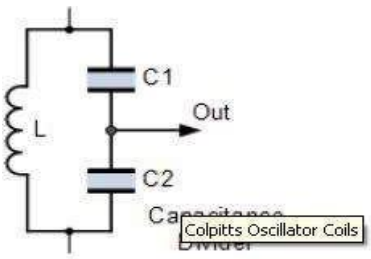


Fig 4.15 Armstrong oscillator

4.8.1 Colpitts Oscillator Circuit

The Colpitts oscillator uses a capacitor voltage divider as its feedback source. The two capacitors, C1 and C2 are placed across a common inductor, L as shown so that C1, C2 and L forms the tuned tank circuit the same as for the Hartley oscillator circuit.

The advantage of this type of tank circuit configuration is that with less self and mutual inductance in the tank circuit, frequency stability is improved along with a more simple design. As with the Hartley oscillator, the Colpitts oscillator uses a single stage bipolar transistor amplifier as the gain element which produces a sinusoidal output. Consider the circuit below.

4.8.2 Basic Colpitts Oscillator Circuit

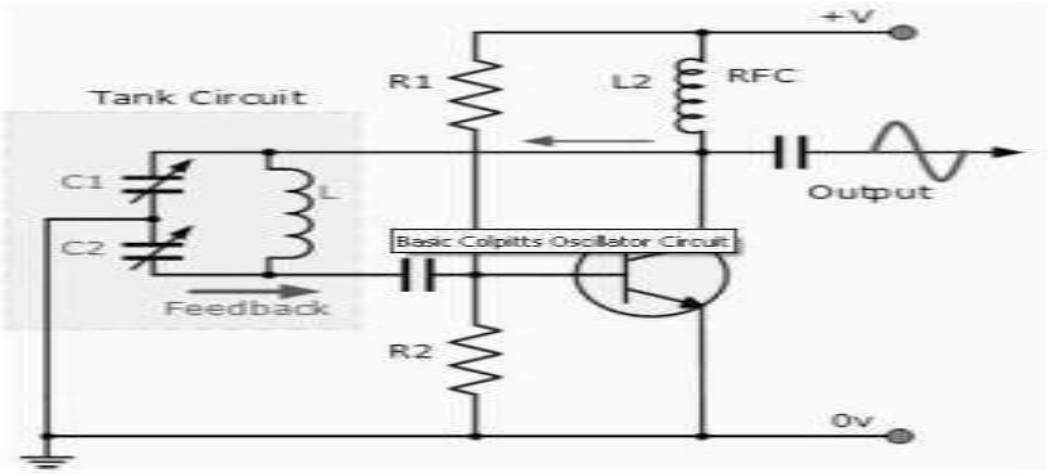


Fig 4.16 Basic Colpitts Oscillator Circuit

The transistor amplifiers emitter is connected to the junction of capacitors, C1 and C2 which are connected in series and act as a simple voltage divider. When the power supply is firstly applied, capacitors C1 and C2 charge up and then discharge through the coil L. The oscillations across the capacitors are applied to the base-emitter junction and appear in the amplified at the collector output. The amount of feedback depends on the values of C1 and C2 with the smaller the values of C the greater will be the feedback.The required

external phase shift is obtained in a similar manner to that in the Hartley oscillator circuit with the required positive feedback obtained for sustained un-damped oscillations. The amount of feedback is determined by the ratio of C1 and C2 which are generally "ganged" together to provide a constant amount of feedback so as one is adjusted the other automaticallyfollows.

The frequency of oscillations for a Colpitts oscillator is determined by the resonant frequency of the LC tank circuit and is given as:

$$f_r = \frac{1}{2\pi\sqrt{L\,C_T}}$$

where C_T is the capacitance of C1 and C2 connected in series and is given as:.

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2} \quad \text{or} \quad C_T = \frac{C_1 \times C_2}{C_1 + C_2}$$

The configuration of the transistor amplifier is of a Common Emitter Amplifier with the Output signal 180^o out of phase with regards to the input signal. The additional 180^o phase shift require for oscillation is achieved by the fact that the two capacitors are connected together in series but in parallel with the inductive coil resulting in overall phase shift of the circuit being zero or 360^o. Resistors, R1 and R2 provide the usual stabilizing DC bias for the transistor in the normal manner while the capacitor acts as a DC-blocking capacitors. The radio- frequency choke (RFC) is used to provide a high reactance (ideally open circuit) at the frequency of oscillation, (fr) and a low resistance at DC.

4.9 RC Phase-Shift Oscillator

In a RC Oscillator the input is shifted 180^o through the amplifier stage and180^o again through a second inverting stage giving us "$180^o + 180^o = 360^o$" of phase shift which is the same as 0^o thereby giving us the required positive feedback. In other words, the phase shift of the feedback loop should be "0".In a Resistance-Capacitance Oscillator or simply an RC Oscillator, we make use of the fact that a phase shift occurs between the input to a RC network and the output from the same network by using RC elements in the feedback branch, for example.

4.9.1 RC Phase-Shift Network

The circuit on the left shows a single resistor -capacitor network and whose output voltage "leads" the input voltage by some angle less than 90 ^{o}. An ideal RC circuit would produce a phase shift of exactly 90^o.The amount of actual phase shift in the circuit depends upon the

values of the resistor and the capacitor, and the chosen frequency of oscillations with the phase angle (Φ) being given as:

$$\phi = \tan^{-1} \frac{X_C}{R}$$

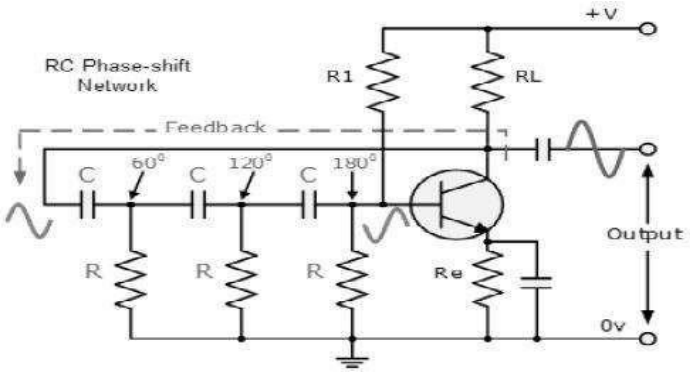


Fig 4.17 RC Phase-Shift Network

The RC Oscillator which is also called a Phase Shift Oscillator**,** produces a sine wave output signal using regenerative feedback from the resistor- capacitor combination. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tankcircuit).

This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360^o. By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done using a 3-ganged variable capacitor

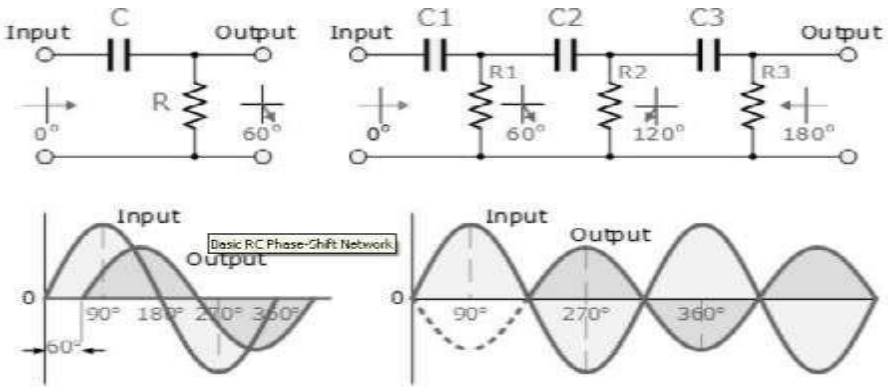


Fig 4.18 RC Phase-Shift Network

If all the resistors, R and the capacitors, C in the phase shift network are equal in value, then the frequency of oscillations produced by the RC oscillator is given as:

$$f = \frac{1}{2\pi CR\sqrt{6}}$$

4.9.2 WIEN BRIDGEOSCILLATOR

One of the simplest sine wave oscillators which uses a RC network in place of the conventional LC tuned tank circuit to produce a sinusoidal output waveform, is the Wien Bridge Oscillator.The Wien Bridge Oscillator is so called because the circuit is based on a frequency-selective form of the Whetstone bridge circuit. The Wien Bridge oscillator is a two-stage RC coupled amplifier circuit that has good stability at its resonant frequency, low distortion and is very easy to tune making it a popular circuit as an audio frequency oscillatorWein Bridge Oscillator is used in audio and sub-audio frequency ranges (20 – 20 kHz). This type of oscillator is simple in design, compact in size, and remarkably stable in its frequency output. Furthermore, its output is relatively free from distortion and its fre•quency can be varied easily. However, the maximum frequency output of a typical Wien bridge oscillator is only about 1 MHz. This is also, in fact, a phase-shift oscillator. It employs two transistors, each producing a phase shift of 180°, and thus producing a total phase-shift of 360° or 0°.

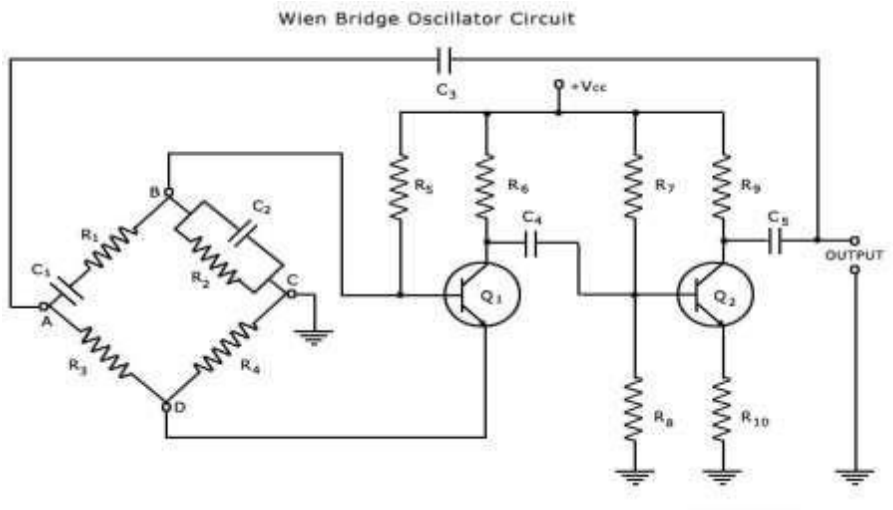


Fig 4.19 Wien Bridge oscillator

It is essentially a two-stage amplifier with an R-C bridge circuit. R-C bridge circuit (Wien bridge) is a lead-lag network. The phase'-shift across the network lags with increasing frequency and leads with decreasing frequency. By adding Wien-bridge feedback network,

the oscillator becomes sensitive to a signal of only one particular frequency. This particular frequency is that at which Wien bridge is balanced and for which the phase shift is 0°.If the Wien-bridge feedback network is not employed and output of transistor Q_2 is feedback to transistor Q_1 for providing regeneration required for producing oscillations, the transistor Q_1 will amplify signals over a wide range of frequencies and thus direct coupling would result in poor frequency stability. Thus by employing Wien-bridge feedback network frequency stability is increased.In the bridge circuit R_1 in series with C_1, R_3, R_4 and R_2 in parallel with C_2 form the four arms. This bridge circuit can be used as feedback network for an oscillator, provided that the phase shift through the amplifier is zero. This requisite condition is achieved by using a two stage amplifier, as illustrated in the figure. In this arrangement the output of the second stage is supplied back to the feedback network and the voltage across the parallel combination C_2 R_2 is fed to the input of the first stage. Transistor Q_1 serves as an oscillator and amplifier whereas the transistor Q_2 as an inverter to cause a phase shift of 180°. The circuit uses positive and negative feedbacks. The positive feedback is through R_1 C_1 R_2, C_2 to transistor Q_1 and negative feedback is through the voltage divider to the input of transistor Q_1. Resistors R_3 and R_4 are used to stabilize the amplitude of theoutput.

The two transistors Q_1 and Q_2 thus cause a total phase shift of 360° and ensure proper positive feedback. The negative feedback is provided in the circuit to ensure constant output over a range of frequencies.

This is achieved by taking resistor R_4 in the form of a temperature sensitivelamp,whoseresistanceincreaseswiththeincreaseincurrent.Incasetheamplitudeofthe output tends to increase, more current would provide more negative feedback. Thus the output would regain its original value. A reverse action would take place in case the output tends to fall. The amplifier voltage gain, A $R_3 + R_4 / R_4 = R_3 / R_4 + 1 = 3$

Since $R_3 = 2\ R_4$, The above corresponds with the feedback network attenuation of 1/3. Thus, in this case, voltage gain A, must be equal to or greater than 3, to sustain oscillations.

To have a voltage gain of 3 is not difficult. On the other hand, to have a gain as low as 3 may be difficult. For this reason also negative feedback is essential.

4.9.3 Wien Bridge Oscillator – Working

The circuit is set in oscillation by any random change in base current of transistor Q_1, that may be due to noise inherent in the transistor or variation in voltage of dc supply. This variation in base current is amplified in collector circuit of transistor Q_1 but with a phase-shift of 180°. the output of transistor Q_1 is fed to the base of second transistor Q_2 through

capacitor C4. Now a still further amplified and twice phase-reversed signal appears at the collector of the transistor Q2. Having been inverted twice, the output signal will be in phase with the signal input to the base of transistor Q1 A part of the output signal at transistor Q2 is fedback to the input points of the bridge circuit (point A-C). A part of this feedback signal is applied to emitter resistor R4 where it produces degenerative effect (or negative feedback). Similarly, a part of the feedback signal is applied across the base-bias resistor R2 where it produces regenerative effect (or positive feedback). At the rated frequency, effect of regeneration is made slightly more than that of degeneration so as to obtain sustained oscillations. The continuous frequency variation in this oscillator can be had by varying the two capacitors C1 and C2 simultaneously. These capacitors are variable air-gang capacitors. We can change the frequency range of the oscillator by switching into the circuit different values of resistors R1 and R2. The advantages and disadvantages of Wien bridge oscillators are givenbelow:

Advantages

- Provides a stable low distortion sinusoidal output over a wide range offrequency.
- The frequency range can be selected simply by using decade resistanceboxes.
- The frequency of oscillation can be easily varied by varying capacitances C1 and C2 simultaneously. The overall gain is high because of twotransistors.

Disadvantages

- The circuit needs two transistors and a large number of othercomponents.
- The maximum frequency output is limited because of amplitude and the phase-shift characteristics ofamplifier.

4.10 Quartz Crystal Oscillators

One of the most important features of any oscillator is its frequency stability, or in other words its ability to provide a constant frequency output under varying load conditions. Some of the factors that affect the frequency stability of an oscillator include: temperature, variations in the load and changes in the DC power supply.

Frequency stability of the output signal can be improved by the proper selection of the components used for the resonant feedback circuit including the amplifier but there is a limit to the stability that can be obtained from normal LC and RC tank circuits.To obtain a very high level of oscillator stability a Quartz Crystal is generally used as the frequency

determining device to produce another types of oscillator circuit known generally as a Quartz Crystal Oscillator, (XO).

4.11 Crystal Oscillator

When a voltage source is applied to a small thin piece of quartz crystal, it begins to change shape producing a characteristic known as the Piezo-electric effect.This piezo-electric effect is the property of a crystal by which an electrical charge produces a mechanical force by changing the shape of the crystal and vice versa, a mechanical force applied to the crystal produces an electrical charge.Then, piezo-electric devices can be classed as Transducers as they convert energy of one kind into energy of another (electrical to mechanical or mechanical to electrical).This piezo-electric effect produces mechanical vibrations or oscillations which are used to replace the LC tank circuit in the previous oscillators.

There are many different types of crystal substances which can be used as oscillators with the most important of these for electronic circuits being the quartz minerals because of their greater mechanical strength. The quartz crystal used in a Quartz Crystal Oscillator is a very small, thin piece or wafer of cut quartz with the two parallel surfaces metallised to make the required electrical connections. The physical size and thickness of a piece of quartz crystal is tightly controlled since it affects the final frequency of oscillations and is called the crystals "characteristic frequency". Then once cut and shaped, the crystal cannot be used at any other frequency. In other words, its size and shape determines itsfrequency.

The crystals characteristic or resonant frequency is inversely proportional to its physical thickness between the two metallised surfaces. A mechanically vibrating crystal can be represented by an equivalent electrical circuit consisting of low resistance, large inductance and small capacitance as shown below.

4.11.1 Quartz Crystal

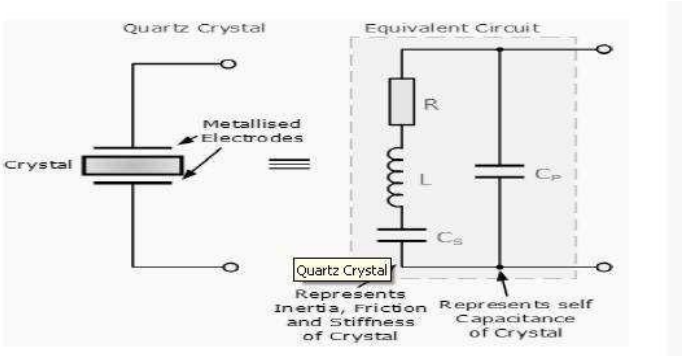


Fig 4.20 Quartz Crystal

The equivalent circuit for the quartz crystal shows an RLC series circuit, which represents the

mechanical vibrations of the crystal, in parallel with a capacitance, Cp which represents the electrical connections to the crystal. Quartz crystal oscillators operate at "parallel resonance", and the equivalent impedance of the crystal has a series resonance where Cs resonates with inductance, L and a parallel resonance where L resonates with the series combination of Cs and Cp as shown.

4.11.2 Crystal Reactance

The slope of the reactance against frequency above, shows that the series reactance at frequency fs is inversely proportional to Cs because below fs and above fp the crystal appears capacitive, i.e. dX/df, where X is the reactance.

The slope of the reactance against frequency above, shows that the series reactance at frequency fs is inversely proportional to Cs because below fs and above fp the crystal appears capacitive, i.e. dX/d f, where X is the reactance. Between frequencies fs and fp, the crystal app ears inductive as the two parallel capacitances cancel out. The point where the reactance values of the capacitances and inductance cancel each other out Xc = XL is the fundamental frequency of the crystal.

A quartz crystal has a resonant frequency similar to that of an electrically tuned tank circuit but with a much higher Q factor due to its low resistance, with typical frequencies ranging from 4 kHz to 10MHz. The cut of the crystal also determines how it will behave as some crystals will vibrate at more than one frequency. Also, if the crystal is not of a parallel or uniform thickness it has two or more resonant frequencies having both a fundamental frequency and harmonics such as second or third harmonics. However, usually the fundamental frequency is stronger or pronounced than the others and this is the one used. The equivalent circuit above has three reactive components and there are two resonant frequencies, the lowest is a series type frequency and the highest a parallel type resonantfrequency.We have seen in the previous tutorials, that an amplifier circuit will oscillate if it has a loop gain greater or equal to one and the feedback is positive. In a Quartz Crystal Oscillator circuit the oscillator will oscillate at the crystals fundamental parallel resonant frequency as the crystal always wants to oscillate when a voltage source is applied to it.

However, it is also possible to "tune" a crystal oscillator to any even harmonic of the fundamental frequency,(2nd, 4th, 8^{th} etc.) And these are known generally as Harmonic OscillatorsWhile Overtone Oscillators vibrate at odd multiples of the fundamental frequency, 3rd, 5th, 11th etc). Generally, crystal oscillators that operate at overtone frequencies do so

using their series resonant frequency output.

The output signal at the collector is then taken through an 180^o phase shifting network which includes the crystal operating in a series resonant mode. The output is also fed back to the input which is "in-phase" with the input providing the necessary positive feedback. Resistors, R1 and R2 bias the resistor in a Class A type operation while resistor

Re is chosen so that the loop gain is slightly greater than unity.

Capacitors, C1 and C2 are made as large as possible in order that the frequency of oscillations can approximate to the series resonant mode of the crystal and is not dependent upon the values of these capacitors.

The circuit diagram above of the Colpitts Crystal Oscillator circuit shows that capacitors, C1 and C2 shunt the output of the transistor which reduces the feedback signal.

Therefore, the gain of the transistor limits the maximum values of C1 and C2. The output amplitude should be kept low in order to avoid excessive power dissipation in the crystal otherwise could destroy itself by excessive vibration.

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UNIT -5
Electronic Circuits-SECA1305

5.1 Introduction to tuned circuits

When a radio or television set is turned on, many events take place within the "receiver" before we hear the sound or see the picture being sent by the transmitting station. Many different signals reach the antenna of a radio receiver at the same time. To select a station, the listener adjusts the tuning dial on the radio receiver until the desired station is heard. Within the radio or TV receiver, the actual "selecting" of the desired signal and the rejecting of the unwanted signals are accomplished by means of a tuned circuit.

A tuned circuit consists of a coil and a capacitor connected in series or parallel. Whenever the characteristics of inductance and capacitance are found in a tuned circuit, the phenomenon as Resonance takes place.

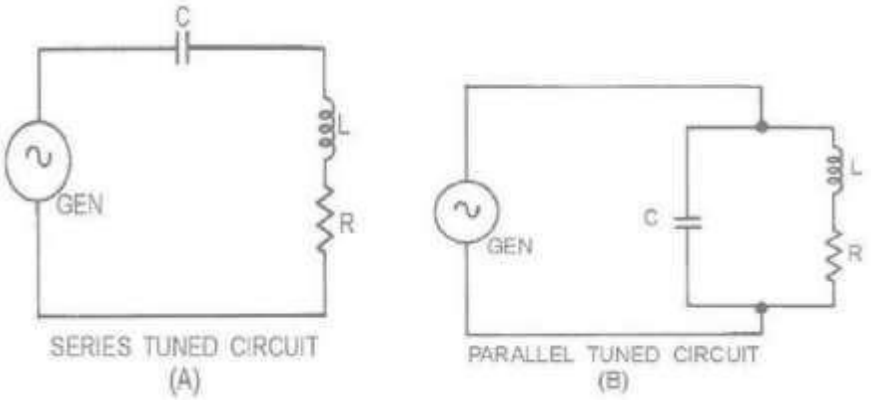


Fig 5.1 Resonance circuits

The frequency applied to an LCR circuit causes XL and XC to be equal, and the circuit is RESONANT. If XL and XC are equal ONLY at one frequency (the resonant frequency). This fact is the principle that enables tuned circuits in the radio receiver to select one particular frequency and reject all others.This is the reason why so much emphasis is placed on XL and XC. figure Shows that a basic tuned circuit consists of a coil and a capacitor, connected either in series, view (A), or in parallel, view (B).The resistance (R) in the circuit is usually limited to the inherent resistance of the components (particularly the resistance of the coil).

5.2 Tuned amplifier

Communication circuit widely uses tuned amplifier and they are used in MW & SW radio frequency 550 KHz – 16 MHz, 54 – 88 MHz, FM 88 – 108 MHz, cell phones 470 - 990 MHz

Band width is 3 dB frequency interval of pass band and –30 dB frequencyinterval

Tune amplifiers are also classified as A, B, C similar to power amplifiers based on conduction angle ofdevices.

A. Series resonant circuit

Series resonant features minimum impedance (RS) at resonant.

f r = ½ √LC; q = L/Rs at resonance L=1/c,BW=fr/Q

It behaves as purely resistance at resonance, capacitive below and inductiveabove resonance

B. Parallel resonant circuit

Parallel resonance features maximum impedance at resonance =L/RsC

At resonance Fr=1/2√1/(LC-Rs2/L2); if Rs=0,fr=1/2√(LC)

At resonance it exhibits pure resistance and below fr parallel circuit exhibits inductiveand above capacitiveimpedance

5.2.1 Need for tunedcircuits:

To understand tuned circuits, we first have to understand the phenomenon of self - induction. And to understand this, we need to know about induction. The first discovery about the interaction between electric current and magnetism was the realization that an electric current created a magnetic field around the conductor. It was then discovered that this effect could be enhanced greatly by winding the conductor into a coil. The effect proved to be two-way: If a conductor, maybe in the form of a coil was placed in a changing magnetic field, a current could be made to flow in it; this is called induction.

So imagine a coil, and imagine that we apply a voltage to it. As current starts to flow, a magnetic field is created. But this means that our coil is in a changing magnetic field, and this induces a current in the coil. The induced current runs contrary to the applied current, effectively diminishing it. We have discovered self-induction. What happens is that the self-induction delays the build-up of current in the coil, but eventually the current will reach its maximum and stabilize at a value only determined by the ohmic resistance in the coil and the voltage applied. We now have a steady current and a steady magnetic field. During the build-up of the field, energy wassupplied to the coil, where did that energy go? It went into the magnetic field, and as long as the magnetic field exists, it will be stored there.

Now imagine that we remove the current source. Without a steady current to uphold it, the magnetic field starts to disappear, but this means our coil is again in a variable field which induces a current into it. This time the current is in the direction of the applied current, delaying the decay of the current and the magnetic field till the stored energy is spent. This can give a funny effect: Since the coil must get rid of the stored energy, the voltage over it rises indefinitely until a current can run somewhere! This means you can get a surprising amount of sparks and arching when coils are involved. If the coil is large enough, you can actually get an electric shock from a low-voltage source like an ohmmeter.

5.2.2 Applications of tuned amplifier

A tuned amplifier is a type of electronic device designed to amplify specific ranges of electrical signals while ignoring or blocking others. It finds common use in devices that work with radio frequency signals such as radios, televisions, and other types of communication equipment; however, it also can be useful in many other applications. Tuned amplifiers can be found in aircraft autopilot systems, audio systems, scientific instruments, spacecraft, or anywhere else there is a need to select and amplify specific electronic signals while ignoringothers.

The most common tuned amplifiers an average person interacts with can be found in home or portable entertainment equipment, such as FM stereo receivers. An FM radio has a tuned amplifier that allows listening to only one radio station at a time. When the knob is turned to change the station, it adjusts a variable capacitor, inductor, or similar device inside the radio, which alters the inductive load of the tuned amplifier circuit. This retunes the amplifier to allow a different specific radio frequency to be amplified so a different radio station can beheard.

5.3 CLASSIFICATION:

- Single tunedamplifier
- Double tunedamplifier
- Stagger tunedamplifier

5.3.1 Single tuned amplifier

Single Tuned Amplifiers consist of only one Tank Circuit and the amplifying frequency range is determined by it. By giving signal to its input terminal of various Frequency Ranges. The Tank Circuit on its collector delivers High Impedance on resonant Frequency, Thus the amplified signal is Completely Available on the output Terminal. And for input signals other than Resonant Frequency, the tank circuit provides lower impedance, hence most of the signals get attenuated at collectorTerminal.

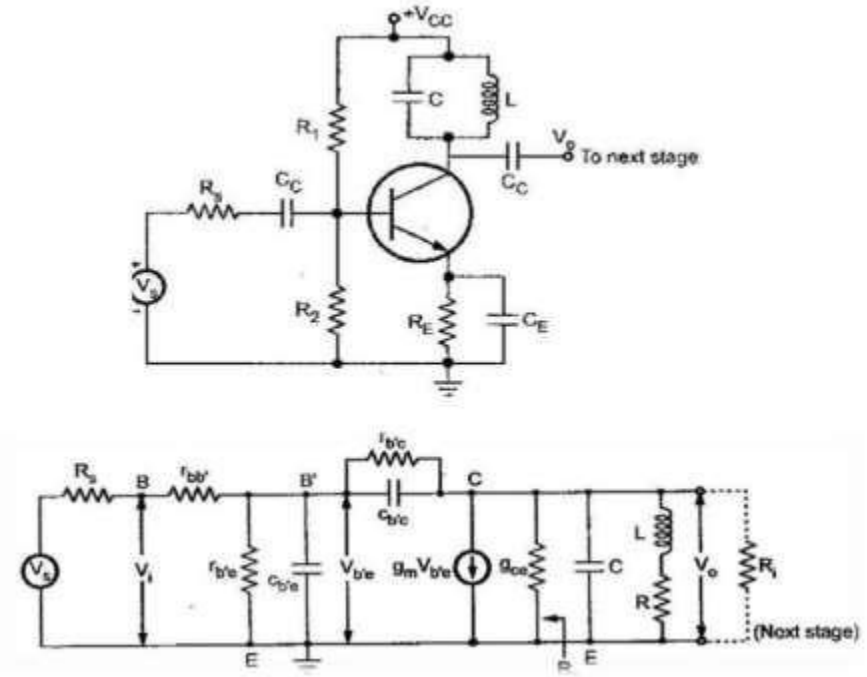


Fig 5.2 .Single Tuned Amplifiers

Ri- input resistance of the next stage

R**0**-output resistance of the generator gmVb`e Cc & CE are negligible small

The equivalent circuit is simplified by

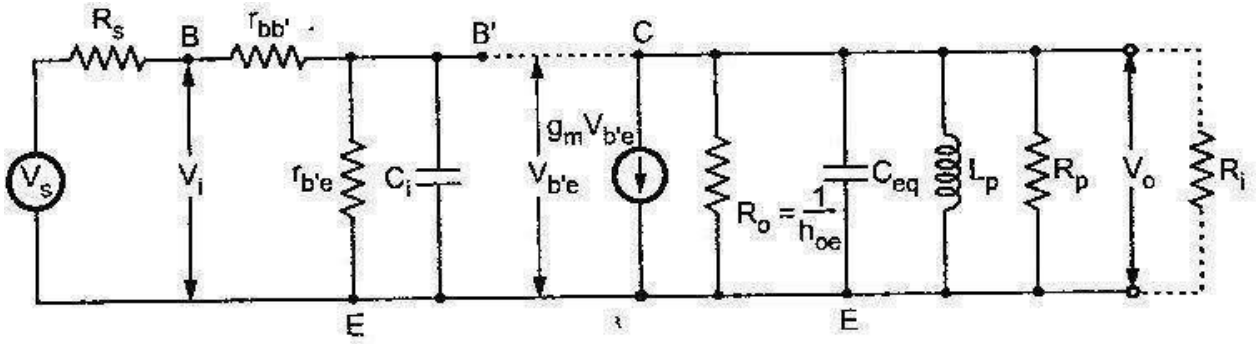


Fig 5.3 Simplified equivalent circuit

$$C_i = C_{b'e} + C_{b'c}(1 - A)$$

$$C_{eq} = C_{b'c}\left(\frac{A-1}{A}\right) + C$$

Where,

$$g_{ce} = \frac{1}{r_{ce}} = h_{oe} - g_m\, h_{re} \approx h_{oe} = \frac{1}{R_o}$$

A-Voltage gain of the amplifier C-tuned circuit capacitance

5.3.2 Double tuned amplifier

An amplifier that uses a pair of mutually inductively coupled coils where both primary and secondary are tuned, such a circuit is known as “double tuned amplifier”. Its response will provide substantial rejection of frequencies near the pass band as well as relative flat pass band response. The disadvantage of potential instability in single tuned amplifiers can be overcome in Double tunedamplifiers.

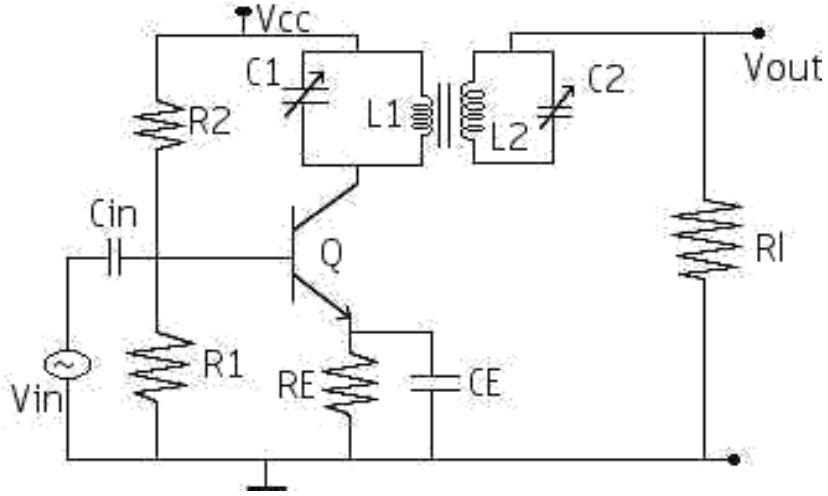


Fig 5.4 Double Tuned Amplifier

A double tuned amplifier consists of inductively coupled two tuned circuits. One L1, C1 and the other L2, C2 in the Collector terminals. A change in the coupling of the two tuned circuits results in change in the shape of the Frequency responsecurve.By proper adjustment of the coupling between the two coils of the two tuned circuits, the required results (High selectivity, high Voltage gain and required bandwidth) may be obtained.

Operation:

The high Frequency signal to be amplified is applied to the input terminal of the amplifier. The resonant Frequency of tuned circuit connected in the Collector circuit is made equal to signal Frequency by varying the value of C1. Now the tuned circuit L1, C1 offers very high Impedance to input signal Frequency and therefore, large output is developed across it. The output from the tuned circuit L1, C1 is transferred to the second tuned circuit L2, C2 through Mutual Induction. Hence the Frequency response in Double Tuned amplifier depends on the Magnetic Coupling of L1 and L2

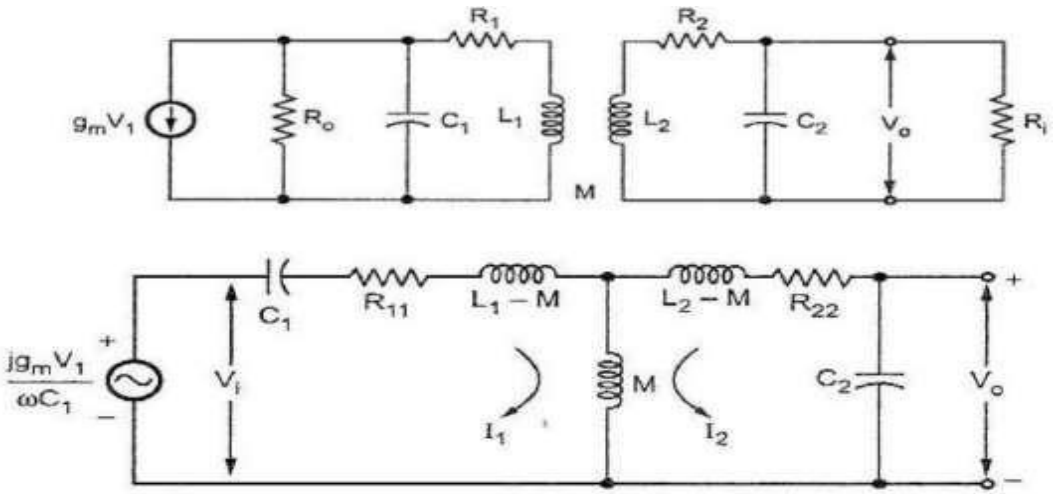


Fig 5.5 Equivalent circuit of double tuned amplifier:

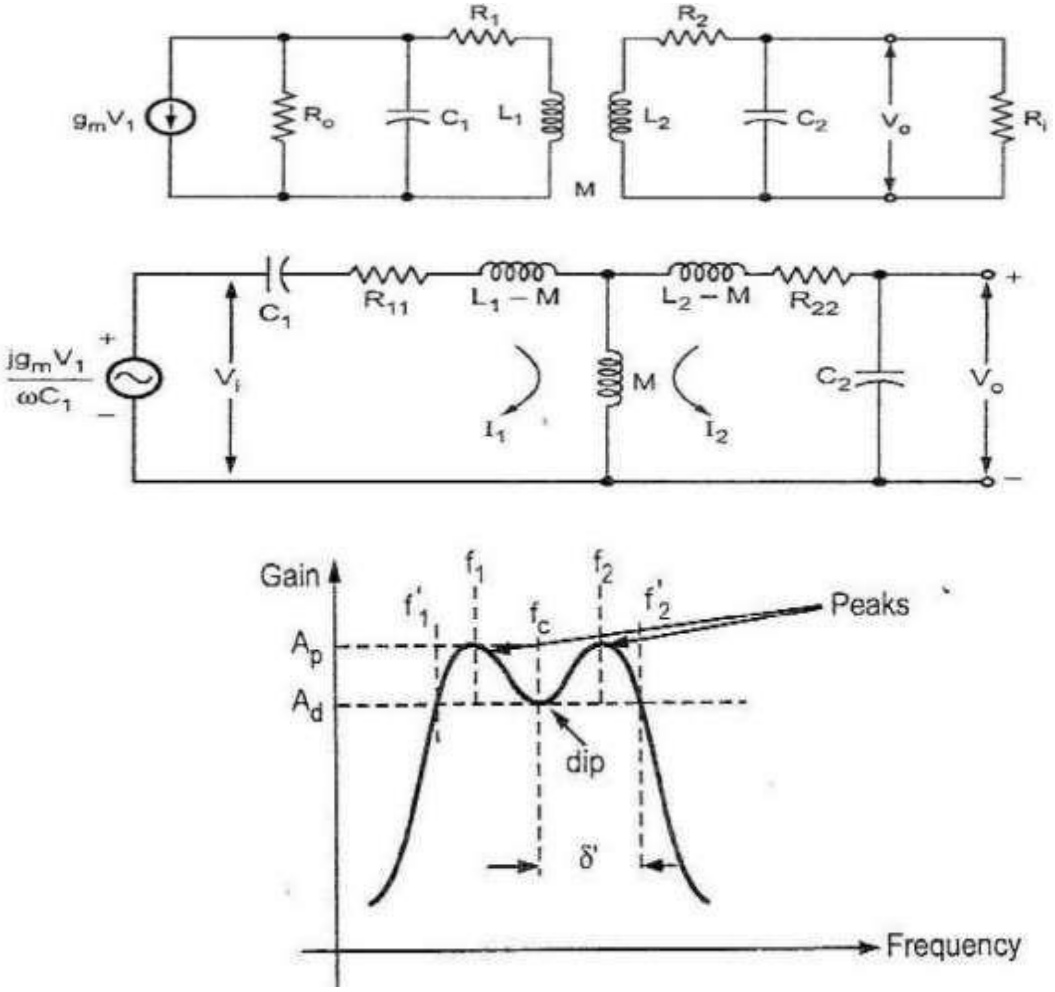


Fig 5.6 Graph of double tuned amplifier

Two gain peaks in frequencies f1 and f2

$$k^2Q^2 = 1, \text{ i.e. } k = \frac{1}{Q},\ f_1 = f_2 = f_r$$

This condition is known as critical coupling.

For the values of k<1/Q the peak gain is less than the maximum gain and the coupling is poor. For the values k>1/Q, the circuit is over coupled and the response shows double peak.

The gain magnitude at peak is given as,

$$|A_p| = \frac{g_m \omega_o \sqrt{L_1 L_2}\, kQ}{2}$$

And gain at the dip at $\delta = 0$ is given as,

$$|A_d| = |A_p| \frac{2kQ}{1+k^2Q^2}$$

Thisdoublepeak usefulwhen more bandwidth is required

The ratio of peak and dip gain is denoted as γ and it represents the magnitude of the ripple in the gain curve.

$$\gamma = \frac{|A_p|}{kQ} = \frac{1+k^2Q^2}{\gamma+\sqrt{\gamma^2-1}}$$

Using quadratic simplification and positive sign

Bandwidth:

$$BW = 2\delta' = \sqrt{2}\,(f_2 - f_1)$$

At 3dB Bandwidth

$$3 \text{ dB BW} = \frac{3.1\, f_r}{Q}$$

5.3.3 Stagger tuned amplifier

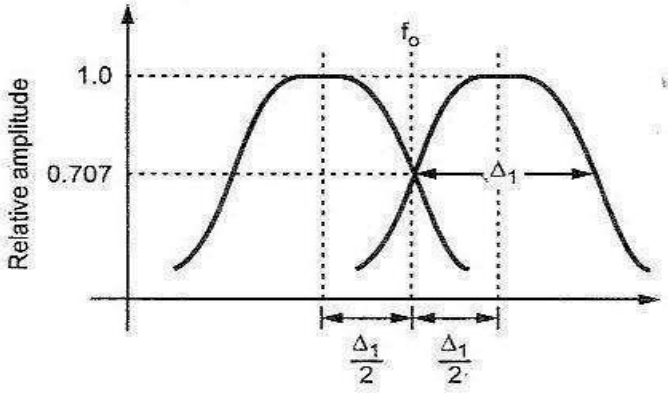
Double tuned amplifier gives greater 3 dB bandwidth having steeper sides and flat top.

But alignment of double tuned amplifier is difficult.

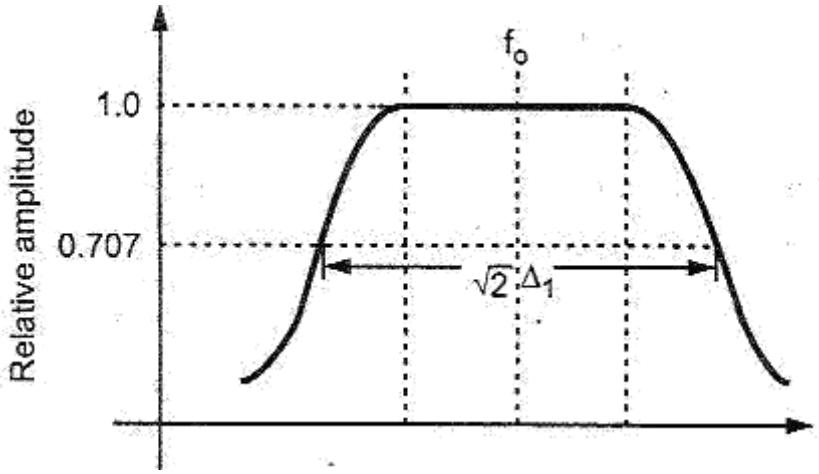
To overcome this problem two single tuned cascaded amplifiers having certain bandwidth are taken and their resonant frequencies are so adjusted that they are separated by an amount equal to the bandwidth of each stage. Since the resonant frequencies are displaced or staggered, they are known as staggered tuned amplifiers. If it is desired to build a wide band high gain amplifier, one procedure is to use either single tuned or double tuned circuits which have been heavily loaded so as to increase the bandwidth.

The gain per stage is correspondingly reduced, by virtue of the constant gain -bandwidth

product. The use of a cascaded chain of stages will provide for the desired gain. Generally, for a specified gain and bandwidth the double tuned cascaded amplifier is preferred, since fewer tubes are often possible, and also since the pass-band characteristics of the double tuned cascaded chain are more favourable, falling more sensitive to variations in tube capacitance and coil inductance than the single tuned circuits.



Response of individual stages



Over all response

Fig 5.6 Response of Stagger Tuned Amplifiers

Stagger Tuned Amplifiers are used to improve the overall frequency response of tuned Amplifiers. Stagger tuned Amplifiers are usually designed so that the overall response exhibits maximal flatness around the centre frequency. It needs a number of tuned circuits operating in union. The overall frequency response of a Stagger tuned amplifier is obtained by adding the individual response together.Since the resonant Frequencies of different tuned circuits are displaced or staggered, they are referred as Stagger Tuned Amplifier.

The main advantage of stagger tuned amplifier is increased bandwidth. Its Drawback is Reduced Selectivity and critical tuning of many tank circuits. They are used in RF amplifier

stage in Radio Receivers.

Analysis:

Gain of the single tuned amplifier:

$$\frac{A_v}{A_v \text{ (at resonance)}_1} = \frac{1}{1+j(X+1)}$$

$$\frac{A_v}{A_v \text{ (at resonance)}_2} = \frac{1}{1+j(X-1)}$$

where $X = 2\,Q_{eff}\,\delta$

Gain of the cascaded amplifier:

$$\frac{A_v}{A_v \text{ (at resonance)}_{cascaded}} = \frac{A_v}{A_v \text{ (at resonance)}_1} \times \frac{A_v}{A_v \text{ (at resonance)}_2}$$

$$\left|\frac{A_v}{A_v \text{ (at resonance)}}\right|_{cascaded} = \frac{1}{\sqrt{4+(2Q_{eff}\cdot\delta)^4}} = \frac{1}{\sqrt{4+16\,Q_{eff}^4\,\delta^4}}$$

$$= \frac{1}{2\sqrt{1+4\,Q_{eff}^4\,\delta^4}}$$

5.4 Class C Tuned Amplifier

Class C operation means that collector current flows for less than 180º. In a practical tuned class C amplifier, the collector current flows for much less than 180º; the current looks like narrow pulses as shown in Fig. As we shall see later, when narrow current pulses like these drive a high-Q resonant (i.e. LC) circuit, the voltage across the circuit is almost a perfect sine wave. One very important advantage of class C operation is its high efficiency. Thus 10 W supplied to a class A amplifier may produce only about 3.5 W of a.c. output (35 % efficiency). The same transistor biased to class C may be able to produce 7 W output (70 % efficiency). Class C power amplifiers normally use RF power transistors. The power ratings of such transistors range from 1 W to over 100 W.

Class C Operation

Fig. (i) shows the circuit of tuned class C amplifier. The circuit action is as under:

- When no a.c. input signal is applied, no collector current flows because the emitter diode(i.e. base-emitter junction) isunbiased.

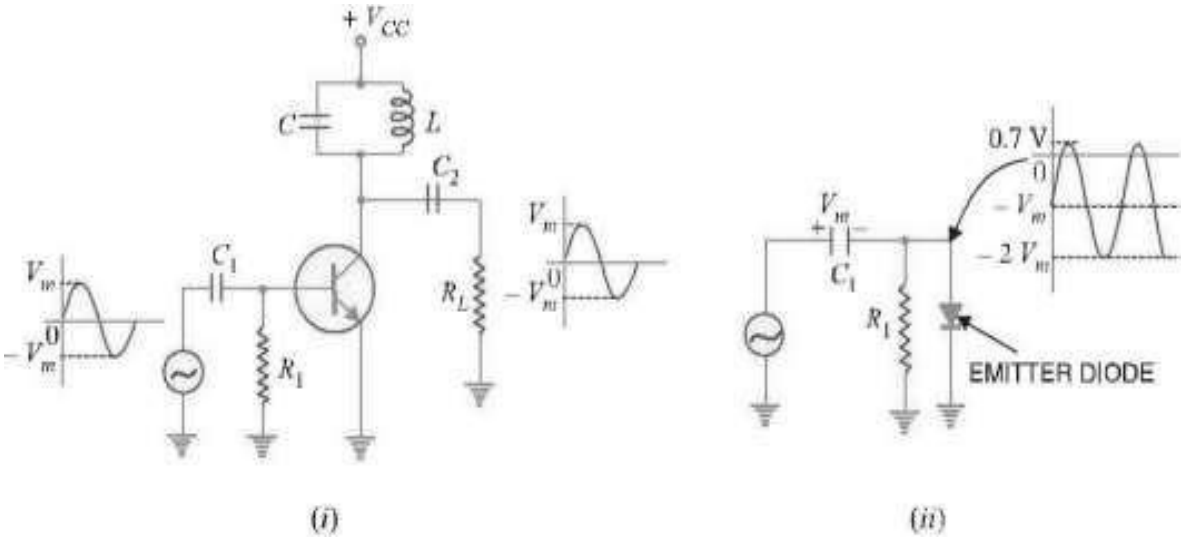
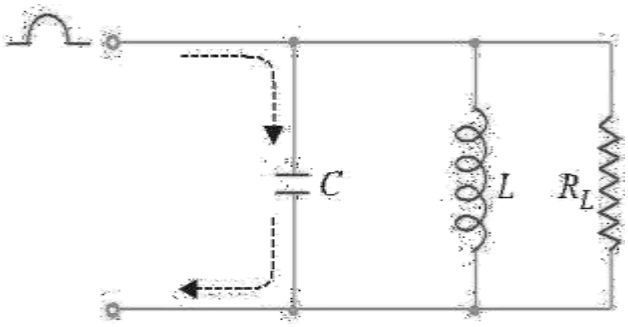


Fig 5.7 Circuit of tuned class C amplifier

- When an a.c. signal is applied, clamping action takes place as shown in Fig. (ii). The
- voltage across the emitter diode varies between + 0.7 V (during positive peaks of input signal) toabout

−2Vm (during negative peaks of input signal). This means that conduction of the transistor occurs only for a short period during positive peaks of the signal. This results in the pulsed output i.e. collector current waveform is a train of narrow pulses.

- When this pulsed output is fed to the LC circuit, **sine-wave output is obtained. This can be easily explained. Since the pulse is narrow, inductor looks like high impedance and the capacitor like a low impedance. Consequently, most of the current charges the capacitor



as shown inFig.

Fig 5.8 Equivalent Circuit of tuned class C amplifier

When the capacitor is fully charged, it will discharge through the coil and the load resistor,

setting up oscillations just as an oscillatory circuit does. Consequently, sine-wave output is obtained.(iv) If only a single current pulse drives the LC circuit, we will get damped sine-wave output. How-ever, if a train of narrow pulses drive the LC circuit, we shall get undamped sine-wave output.

5.5 Neutralization

A completely neutralized amplifier must fulfil two conditions. The first is that the inter electrode capacitance between the input and output circuits be cancelled. The second requirement is that the inductance of the screen grid and cathode assemblies and leads be completely cancelled. Cancellation of these common impedances between the input and output will theoretically prevent oscillation. This also applies in practice, but often not without some difficulty.

There are a variety of methods of accomplishing these ends that will fulfil the two conditions. At frequencies up to about 500 KHz it is not normally necessary to neutralize a grid- driven triode. A grounded-grid cathode-driven ceramic-metal triode can usually be operated up into the VHF range without neutralization. Tetrode and pentode amplifiers generally will operate into the HF range without neutralization. As the gain of the amplifier increases, the need to cancel feedback voltage becomes that much more necessary. For this reason, it is usually necessary to neutralize tetrodes and pentodes at the higher frequencies.

5.5.1 Neutralization Methods

In tuned RF amplifiers, transistor are used at the frequencies nearer to their unity gain bandwidths (i.e. fT), to amplify a narrow band of high frequencies centred on a radio frequency. At this frequency, the inter junction capacitance between base and collector, Cbc of the transistor becomes dominant, i.e., its reactance between low enough to be considered, which is otherwise infinitetobeneglectedasopencircuit.BeingCEconfigurationcapacitanceCbe,shownintheig.

3.35 come across input and output circuits of an amplifier. As reactance of Cbc at RF is low enough it provide the feedback path from collector to base. With this circuit condition, if some feedback signal manages to reach the input from output in a positive manner with proper phase shift, then there is possibility of circuit converted to a positive manner with proper phase shift, then there is possibility of circuit converted to an unstable one, generating its own oscillations and can stop working as anamplifier.This circuit will always oscillate if enough energy is fed back from the collector to the base in the correct phase to overcome circuit losses. Unfortunately, the conditions for best gain and selectivity are also those which promote oscillation. In order to prevent oscillations in tuned RF amplifiers it was necessary

to reduce the stage gain to a level that ensured circuit stability. This could be accomplished in several ways such as lowering the Q of tune circuits; stager tuning, losses coupling between the stages or inserting a 'loser' element into the circuit. While all these methods reduced gain, detuning and Q reduction had detrimental effects on selectivity. Instead of losing the circuit performance to achieve stability, the professor L.A. Hazeltine introduced a circuit in which the troublesome effect o the collector to base capacitance of the transistor was neutralized by introducing a signal which cancels the signal coupled through the collector to base capacitance. He proved that the neutralization can be achieved by deliberately feeding back a portion of the output signal to the input in such a way that it has the same amplitude as the unwanted feedback but the opposite phase. Later on many neutralizing circuits were introduced. Let us study some of thesecircuits.

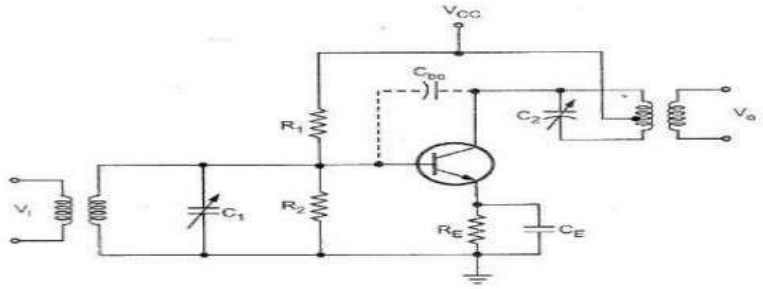


Fig 5.9 Circuit of tuned amplifier

5.5.2 Hazeltine Neutralization

The Fig. shows one variation of the Hazeline circuit. In this circuit a small value of variable capacitance CN is connected from the bottom of coil, point B, to the base. Therefore, the internal capacitance Cbc, shown dotted, feeds a signal from the top end of the coil, point A, to the transistor base and the CN feeds a signal o equal magnitude but opposite polarity room the bottom o coil, point B, to the base. The neutralizing capacitor, CN can be adjusted correctly to completely nullify the signal ed through theCbc.

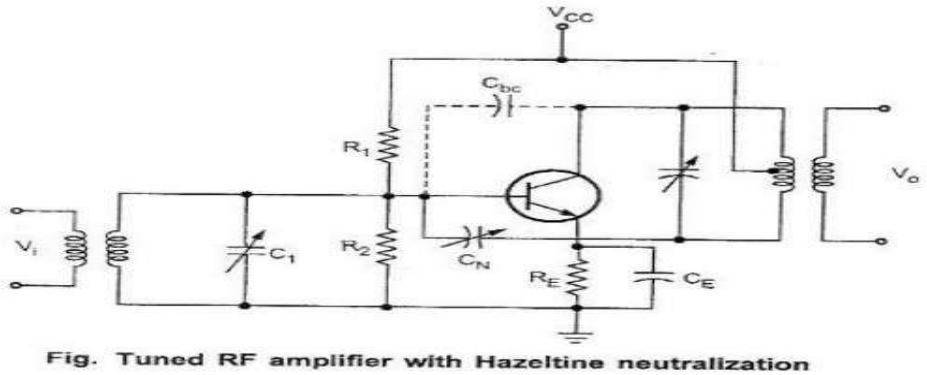


Fig. Tuned RF amplifier with Hazeltine neutralization

Fig 5.10 Circuit of Hazeltine Neutralization

5.5.3 Neutralization using coil

The Fig. shows the neutralization o RF amplifier using coil. In this circuit, L part of the tuned circuit at the base o next stage is oriented or minimum coupling to the other winding. It is wound on a separate from and is mounted at right angle to the coupled windings. If the windings are properly polarized, the voltage across L due to the circulating current in the base circuit will have the proper phase to cancel the signal coupled through the base to collector, Cbc capacitance.

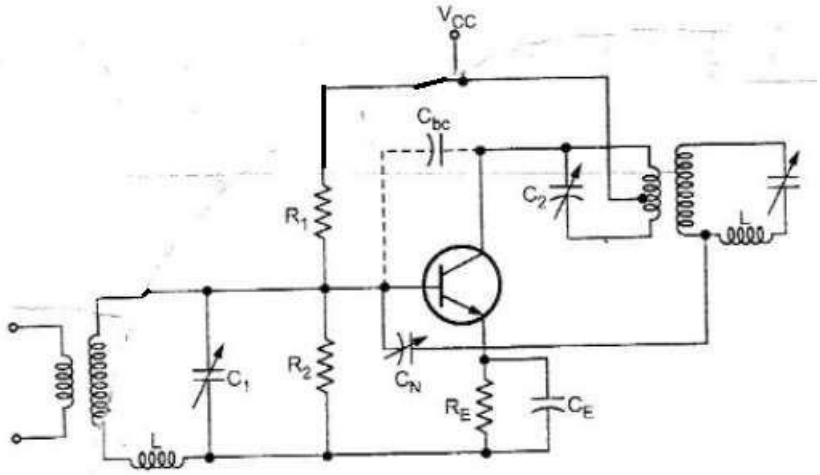


Fig. Tuned RF amplifier using coil

Fig 5.11Neutralization using coil

5.5.4 Unilateralisation

It is the phenomenon by which a signal can be transmitted from the input to the output alone and not vice versa. In a unilateralised amplifier both resistive and reactive effects are cancelled. Otherwise Use of an external feedback circuit in a high-frequency transistor amplifier to prevent undesired oscillation by cancelling both the resistive and reactive changes produced in the input circuit by internal voltage feedback; with neutralization, only the reactive changes are cancelled.

5.6 MULTIVIBRATORS

5.6.1 Introduction

The type of circuit most often used to generate square or rectangular waves is the multivibrator. A multivibrator, is basically two amplifier circuits arranged with regenerative feedback. One of the amplifiers is conducting while the other is cut off When an input signal to one amplifier is large enough, the transistor can be driven into cutoff, and its collector voltage will be almost V CC. However, when the transistor is driven into saturation, its collector voltage will be about 0 volts.

A circuit that is designed to go quickly from cutoff to saturation will produce a square or rectangular wave at its output. This principle is used in multivibrators. Multivibrators are classified according to the number of steady (stable) states of the circuit. A steady state exists when circuit operation is essentially constant; that is, one transistor remains in conduction and the other remains cut off until an external signal is applied.

The three types of multivibrators :

- ASTABLE
- MONOSTABLE
- BISTABLE.

The astable circuit has no stable state. With no external signal applied, the transistors alternately switch from cutoff to saturation at a frequency determined by the RC time constants of the coupling circuits.

The monostable circuit has one stable state; one transistor conducts while the other is cut off. A signal must be applied to change this condition. After a period of time, determined by the internal RC components, the circuit will return to its original condition where it remains until the next signalarrives.

The bistablemultivibrator has two stable states. It remains in one of the stable states until a trigger is applied. It then FLIPS to the other stable condition and remains there until another trigger is applied. The multivibrator then changes back (FLOPS) to its first stable state.

5.7 AstableMultivibrator

A multivibrator which generates square waves of its own (i.e. without any external trigger pulse) is known as astablemultivibrator. It is also called free ramming multivibrator. It has no stable state but only two quasi-stables (half-stable) makes oscillating continuously between these states. Thus it is just an oscillator since it requires no external pulse for its operation of course it does require D.C power.

In such circuit neither of the two transistors reaches a stable state. It switches back and forth

from one state to the other, remaining in each state for a time determined by circuit constants. In other words, at first one transistor conducts (i.e. ON state) and the other stays in the OFF state for some time. After this period of time, the second transistor is automatically turned ON and the first transistor turned OFF. Thus the multivibrator will generate a square wave of its own. The width of the square wave and it frequency will depend upon the circuit constants.

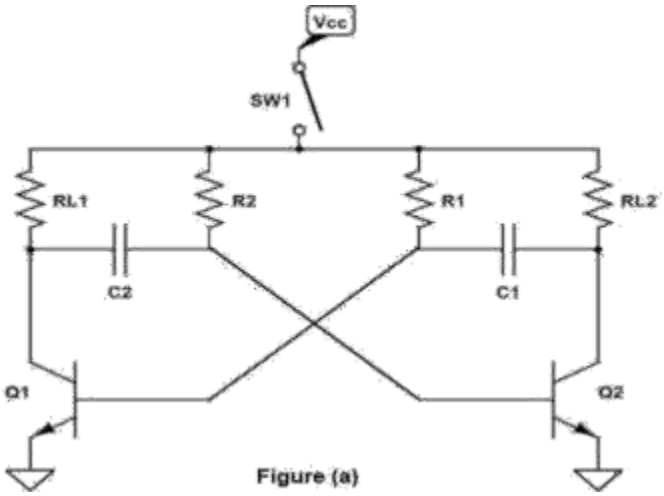


Fig 5.12collector coupled astable multivibrator

Here we like to describe.

- Collector - coupled Astabemultivibrator
- Emitter - coupled Astablemultivibrator

Figure (a) shows the circuit of a collector coupled astablemultivibrator using two identical NPN transistors Q1 and Q 2. It is possible to have R L1 = RL2 = RL = R1 = R2 = R and C 1 = C2 = C. In that case , the circuit is known as symmetrical astablemultivibrator. The transistor Q 1 is forward biased by the Vcc supply through resistor R2. Similarly the transistor Q2 is forward biased by the Vcc supply through resistor R1. The output of transistor Q1 is coupled to the input of transistor Q2 through the capacitor C2. Similarly the output of transistor Q2 is coupled to the input of transistor Q1 through the capacitor C1.

It consists of two common emitter amplifying stages. Each stage provides a feedback through a capacitor at the input of the other. Since the amplifying stage introduces a 180^o phase shift and another 180^o phase shift is introduced by a capacitor, therefore the feedback signal and the circuit works as an oscillator. In other words because of capacitive coupling none of the transistor can remain permanently out-off or saturated, instead of circuit has two quasi-stable states (ON and OFF) and it makes periodic transition between these two states.

The output of an Astablemultivibrator is available at the collector terminal of the either transistors as shown in figure (a). However, the two outputs are 180 ^{o} out of phase with each other. Therefore one of the outputs is said to be the complement of the other.Let us suppose that

When Q1is ON, Q2 is OFF and

When Q2 is ON, Q1 is OFF.

When the D.C power supply is switched ON by closing S, one of the transistors will start conducting before the other (or slightly faster than the other). It is so because characteristics of

no two similar transistors can be exactly alike suppose that Q1 starts conducting before Q2 does. The feedback system is such that Q1 will be very rapidly driven ton saturation and Q 2 to cut-off. The circuit operation may be explained as follows.

Since Q 1 is in saturation whole of VCC drops across R L1. Hence V C1 = 0 and point A is at zero or ground potential. Since Q2 is in cut -off i.e. it conducts no current, there is no drop across R

L2. Hence point B is at VCC. Since A is at 0V C2 starts to charge through R2 towards VCC.

When voltage across C2 rises sufficiently (i.e. more than 0.7V), it biases Q2 in the forward direction so that it starts conducting and is soon driven to saturation.

VCC decreases and becomes almost zero when Q 2 gets saturated. The potential of point B decreases from VCC to almost 0V. This potential decrease (negative swing) is applied to the base of

Q1 through C1. Consequently, Q1 is pulled out of saturation and is soon driven to cut-off.

Since, now point B is at 0V, C1 starts charging through R1 towards the target voltage VCC.

When voltage of C1 increases sufficiently. Q1 becomes forward-biased and starts conducting. In this way the whole cycle is repeated.

It is observed that the circuit alternates between a state in which Q1 is ON and Q2 is OFFand the state in which Q1 is OFF and Q2 is ON. This time in each state depends on RC values. Since each transistor is driven alternately into saturation and cut-off. The voltage waveform at either collector (points A and B in figure (b)) is essentially a square waveform with peak amplitude equal to VCC.

5.7.1 Calculation of switching times and frequency of oscillations:

The frequency of oscillations can be calculated by charging and discharging capacitances and its base resistance RB.The voltage across the capacitor can be written as

$$V_o = V_f - (V_f - V_i)e^{\frac{-t}{RC}} = V_B$$

Vi= intial voltage = VB =-VCC thus the transistors enters from ON to OFF state Vf = final voltage = VB = -VCC then the resistor enters from OFF to ON state T1 is ON & T2 is OFF the above equation can be writtenas

VB1=VC$\left[1-2e^{\frac{-t}{RB_2C_2}}\right]$

Substitute at t=T1, VB1=0 hence this equation becomes T1=.69RB2C2

The total time period T=.694(RB1C1+RB2C2) When RB!=RB2=R & C1=C2=C

T=1.39RC

Frequency of free running multivibrator is given by

$$F = \frac{1}{\text{total time period}(T)} = \frac{1}{1.39RC} = \frac{0.7}{RC}$$

the frequency stability of the circuit is not good as only the function of the product of RC but also depends on load resistances, supply voltages and circuit parameters. In order to stabilize the frequency, synchronizing signals are injected which terminate the unstable periods earlier than would occur naturally.

5.8 Bistablemultivibrator

The bistablemultivibrator has two absolutely stable states. It will remain in whichever state it happens to be until a trigger pulse causes it to switch to the other state. For instance, suppose at any particular instant, transistor Q 1 is conducting and transistor Q 2 is at cut-off. If left to itself, the bistablemultivibrator will stay in this position for ever. However, if an external pulse is applied to the circuit in such a way that Q 1 is cut-off and Q2 is turned on, the circuit will stay in the new position. Another trigger pulse is then required to switch the circuit back to its originalstate.In other words a multivibrator which has both the state stable is called a bistablemultivibrator. It is also called flip-flop, trigger circuit or binary. The output pulse is obtained when, and why a driving (triggering) pulse is applied to the input. A full cycle of

output is produced for every two triggering pulses of correct polarity and amplitude.

Figure (a) shows the circuit of a bistablemultivibrator using two NPN transistors. Here the output of a transistor Q2 is coupled put of a transistor Q1 through a resistor R2. Similarly, the output of a transistor Q1 is coupled to the base of transistor Q2 through a resistor R1. The capacitors C 2 and C1 are known as speed up capacitors. Their function is to increase the speed of the circuit in making abrupt transition from one stable state to another stable state. The base resistors (R3 and R4) of both the transistors are connected to a common source (-V BB). The output of a bistablemultivibrator is available at the collector terminal of the both the transistor Q1 and Q. However, the two outputs are the complements of each other.

Let us suppose, if Q1 is conducting, then the fact that point A is at nearly ON makes the base of Q2 negative (by the potential divider R2 - R4) and holds Q2 off. Similarly with Q2 OFF, the potential divider from VCC to -VBB (RL2, R1, R3) is designed to keep base of Q1 at about 0.7V ensuring that Q1 conducts. It is seen that Q1 holds Q2 OFF and Q2 hold Q1 ON. Suppose, now a positive pulse is applied momentarily to R. It will cause Q2 to conduct. As collector of Q2 falls to zero, it cuts Q1 OFF and consequently, the BMV switches over to its otherstate.

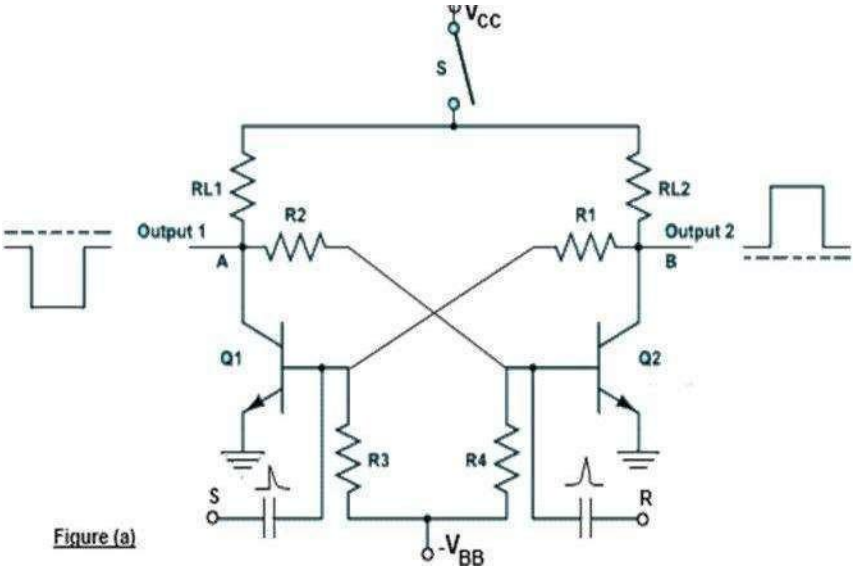


Fig 5.13 Circuit of a bistable multivibrator

Similarly, a positive trigger pulse applied to S will switch the BMV back to its original state.

Uses:

- In timing circuits as frequencydivider
- In countingcircuits
- In computer memory circuits

5.8.1 BistableMultivibrator Triggering

To change the stable state of the binary it is necessary to apply an appropriate pulse in the circuit, which will try to bring both the transistors to active region and the resulting regenerative feedback will result on the change of state.

Triggering may be of two following types:

(I) Asymmetricaltriggering

(II) Symmetricaltriggering

(I) Asymmetricaltriggering

In asymmetrical triggering, there are two trigger inputs for the transistors Q1 and Q2. Each trigger input is derived from a separate triggering source. To induce transition among the stable states, let us say that initially the trigger is applied to the bistable. For the next transition,now the identical trigger must appear at the transistor Q2. Thus it can be said that the asymmetrical triggering the trigger pulses derived from two separate source and connected to the two transistors Q1 and Q2 individually, sequentially change the state of the bistable.Figure (b) shows the circuit diagram of an asymmetrically triggered bistablemultivibrator.

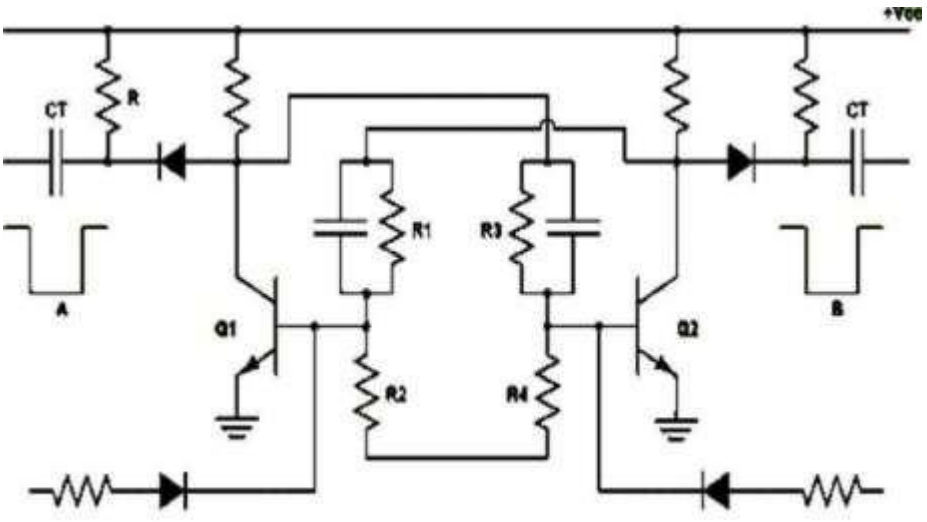


Figure: (b) Asymmetrical triggered bistable multivibrator

Fig 5.14 Circuit of aasymmetric bistable multivibrator

Initially Q1 is OFF and transistor Q2 is ON. The first pulse derived from the trigger source A, applied to the terminal turn it OFF by bringing it from saturation region to active transistor Q 1 is ON and transistor Q2 is OFF. Any further pulse next time then the trigger pulse is applied at the terminal B, the change of stable state will result with transistor Q2 On and transistor Q1 OFF.

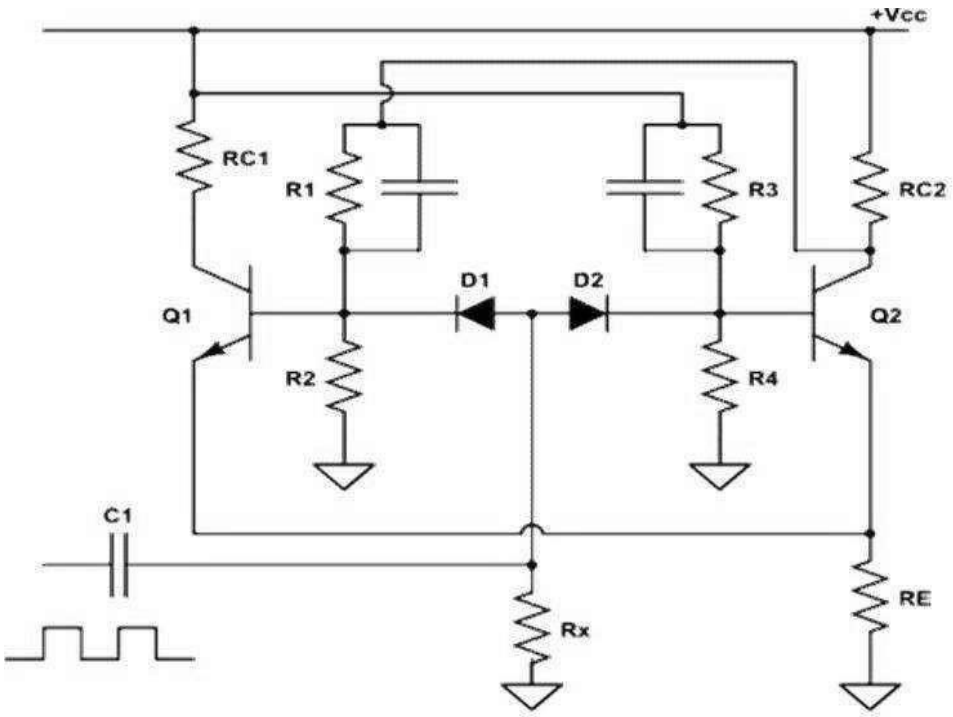


Figure (c): Symmetrical base triggering employing positive triggering pulses

Fig 5.15 Circuit of asymmetric triggered bistable multivibrator

Asymmetrical triggering finds its application in the generation of a gate waveform, the duration of which is controlled by any two independent events occurring at different time instants. Thus measurement of time interval is facilitated.

(II) Symmetrical triggering here are various symmetrical triggering methods called symmetrical collector triggering, symmetrical base triggering and symmetrical hybrid triggering. Here we would liked to explain only symmetrical base triggering (positive pulse) only as given under symmetrical BaseTriggering.

Figure (c) shows the circuit diagram of a binary with symmetrical base triggering applying a positive trigger pulses.Diodes D1 and D2 are steering diodes. Here the positive pulses, try to turn ON and OFF transistor. Thus when transistor Q1 is OFF and transistor Q2 is ON, the respective base voltages and VB1N, OFF and V B2N, ON. It will be seen that VB1N, OFF > VB1N, ON. Thus diode D2 is more reverse-biased compared to diode D1.When the positive differentiated pulse of amplitude greater than (VB1N, OFF + Vɣ) appears, the diode D1 gets forward biased, and transistor Q1 enters the active region and with subsequent regenerative feedback Q1 gets ON, and transistor Q2 becomes OFF. On the arrivalof the next trigger pulse now the diode D 2 will be forward biased and ultimately with regenerative feedback it will be in the ON state.

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