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SCHOOL OF ELECTRICAL AND ELECTRONICS

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

UNIT – I – ELECTRONIC CIRCUITS I – SECA1302

UNIT 1 BIASING OF BJT AND FET BJT 9 Hrs

– Need for biasing – Various biasing methods of BJT- Bias Circuit Design- DC Load Line - DC analysis of Transistor circuits-AC Load Line- AC analysis of Transistor Circuits- Quiescent Point – Thermal stability - Stability factors - Biasing of JFET - Various biasing methods of JFET - JFET Bias Circuit Design - MOSFET Biasing-Two port network.

BIASING OF BJT AND FET

Introduction

Bipolar Junction Transistor (BJT) consist of

- **3 terminals – E,B,C**
- **2 Junctions – JE (BE) and JC (CB)**
- **3 region(Stages) of operation**

Refer figure 1, 2 and 3

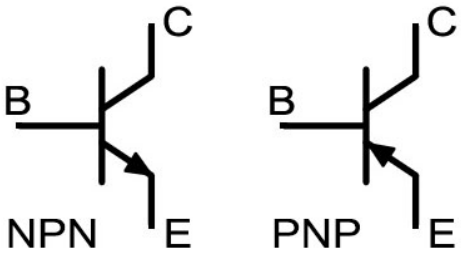


Figure 1. BJT (3 terminals)

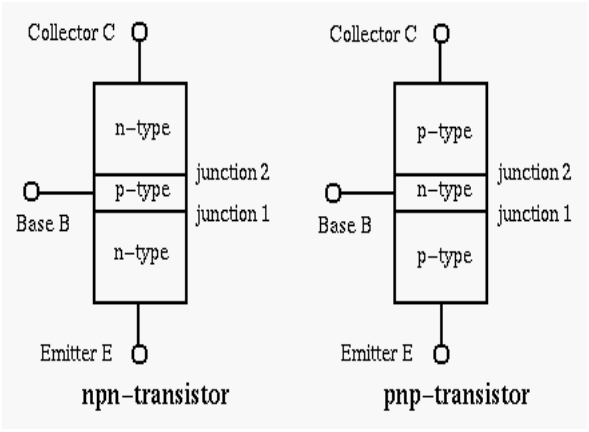


Figure 2. BJT (2 junctions)

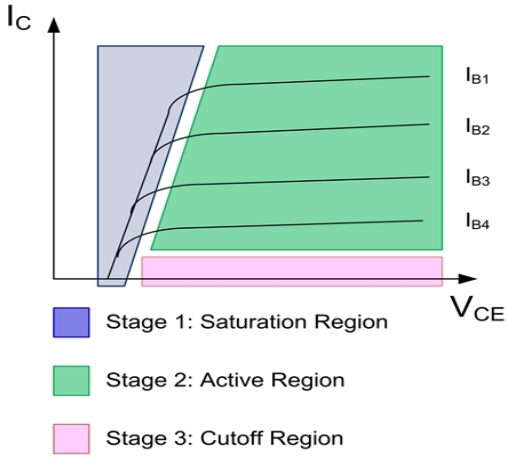
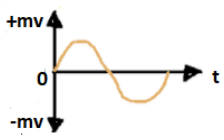
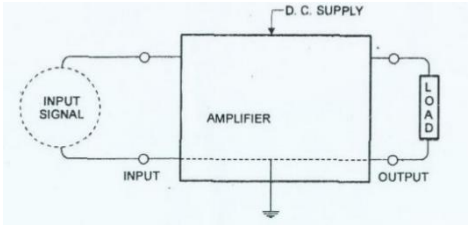


Figure 3. BJT (3region of operations)

The main application of transistor is amplification as shown in figure 4. The signal from the transducers like microphone, thermocouple etc, are very weak. The process of raising the level of signal strength (Amplitude increases) is called Amplification as shown in the below figure. There is No change in the wave shape and frequency.

Input signal





Amplified output signal

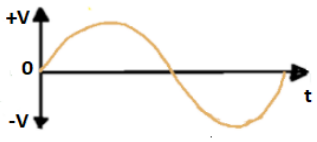


Figure 4. Amplifier

Essential components of Oscillator are: Amplifier and a positive feedback loop (figure 5)

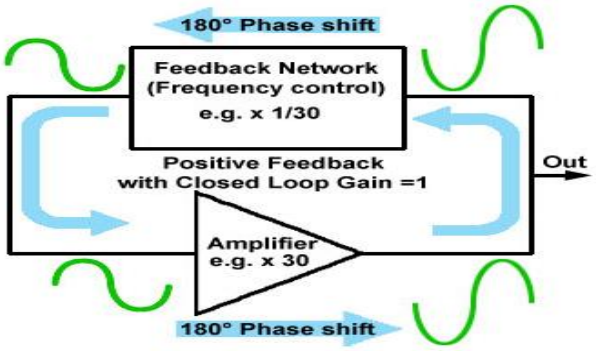


Figure 5. Oscillator

Different configuration of transistor (Refer table 1)

- ***Common Emitter (CE)***
- ***Common Base (CB)***
- ***Common Collector (CC)***

Table 1: Different configuration of transistor

SUMMARY: COMMON EMITTER	COMMON COLLECTOR	COMMON BASE
INPUT: VBE & IE	INPUT: VBC & IB	INPUT: VEB & IE
OUTPUT: VCE & IC	OUTPUT: VEC & IE	OUTPUT: VCB & IC

Comparison

Type	CE	CB	CC
input	Base	Emitter	Base
output	Collector	Collector	Emitter
common	Emitter	Base	Collector
V gain	large	large	none
I gain	large	none	large
application	first stage amplifier	high frequency amplifier	buffer

Figure 6. Configuration of transistor

CE configuration is commonly used because (Refer figure 6 and table 2)

1. ***It offers high voltage, current and power gain***
2. ***Its input and output impedance are best suited for many applications.***

Table 2. Region of operation of BJT(CE) and its Applications

Emitter Base Junction	Collector Base Junction	Region of Operation	Application
Reverese Biased	Reverese Biased	Cut-off	Open Switch
Forward Biased	Reverese Biased	Active	Amplifiers and Oscillators
Forward Biased	Forward Biased	Saturation Region	Closed Switch
Reverese Biased	Forward Biased	Inverse Mode	Digital Circuits

What is Biasing?

Biasing is defined as applying external DC voltage to a device to operate it in the desired region of operation. Types of Biasing,

- **Forward Bias**
- **Reverse Bias**

A transistor is based in order to make the emitter base junction forward biased and collector base junction reverse biased, so that it maintains in active region, to work as an amplifier shown in figure 7. The process of forcing the transistor into the active region is called biasing.

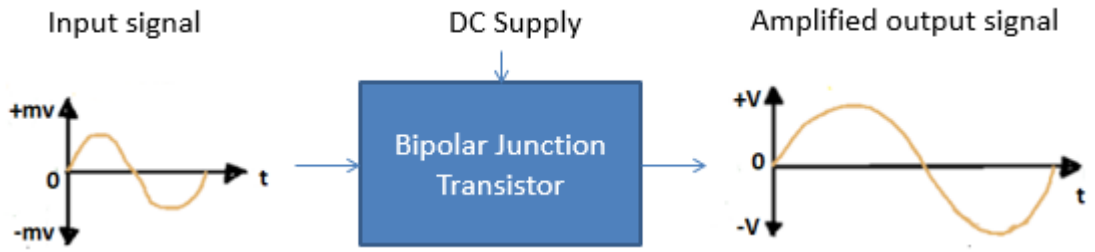


Figure 7. Transistor Biasing

The basic function of transistor is amplification. The process of raising the strength of weak signal without any change in its general shape or frequency is referred as faithful amplification.

- **For faithful amplification it is essential that:**

-Emitter-Base junction is forward biased

-Collector Base junction is reversed biased

-Proper zero signal collector current

Biasing Definition:

The proper flow of zero signal output current and the maintenance of proper output voltage during the passage of signal is called transistor biasing.

<u>Need for DC biasing</u>

- **To amplify a signal, two conditions have to be met.**

1. **The input voltage should exceed cut-in voltage for the transistor to be ON.**
2. **The BJT should be in the active region, to be operated as an amplifier for the entire AC signal.**

For, normal operation of the transistor amplifier circuit, the transistor must be biased so that it operates in the active region (linear) of the characteristics.

The DC sources supplies the power to the transistor circuit, to get the output signal power greater than the input signal power.

Q-Point (Static Operation Point)

When a transistor does not have an ac input, it will have specific dc values of I_C and V_{CE}. These values correspond to a specific point on the dc load line. This point is called the *Q-point*. The letter *Q* corresponds to the word (Latent) quiescent, meaning at rest. A quiescent amplifier is one that has no ac signal applied and therefore has constant dc values of I_C and V_{CE}. It is also called as quiescent point or simply Q-point as shown in figure 8.

- **When a line is drawn joining the saturation and cut off points, such a line can be called as Load line.**
- **This line, when drawn over the output characteristic curve, makes contact at a point called as Operating point.**
- **There can be many such intersecting points, but the Q-point is selected in such a way that irrespective of AC signal swing, the transistor remains in the active region.**

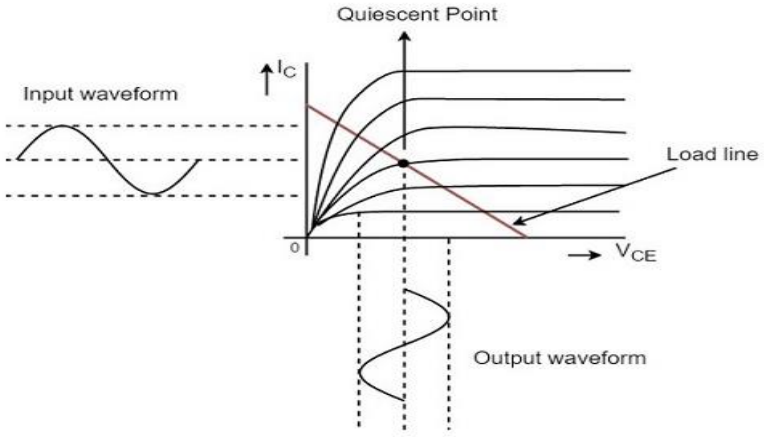


Figure 8. Q- point

- **Q-point is the operating point of the transistor (ICQ, VCEQ) at which it is biased. i.e. it operates in active region of input output characteristics.**

<u>Importance of Q-point in transistor</u>

1. **Input signal will be of the order millivolts or less.**
2. **If we directly input these signals to the amplifier they will not get amplified.**
3. **Only in active region of operation transistor acts as amplifier.**
4. **So we can establish appropriate DC voltages and currents through BJT by external sources so that BJT operates in active region and superimpose the AC signals to be amplified.**

The input signal applied is completely amplified and reproduced without any losses. This can be understood as Faithful Amplification. The operating point is so chosen such that it lies in the active region and it helps in the reproduction of complete signal without any loss. When the *Q*-point is centered, I_C and V_{CE} can both make the maximum possible transitions above and below their initial dc values. With respect to

Figure.9. When the *Q*-point is above the center on the load line, the input signal may cause the transistor to saturate. When this happens, a part of the output signal will be *clipped* off.

Figure.10. When the *Q*-point is below midpoint on the load line, the input signal may cause the transistor to cutoff. This can also cause a portion of the output signal to be clipped.

Figure.11. BJT should not be operated in the break over region. It causes damage to the BJT.

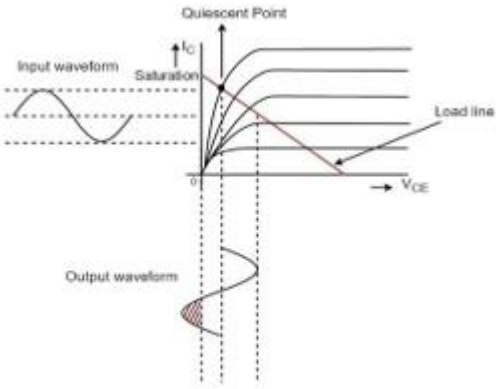


Figure 9. Near Saturation

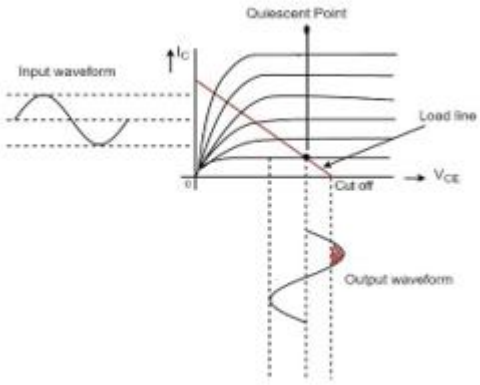


Figure 10. Near cutoff

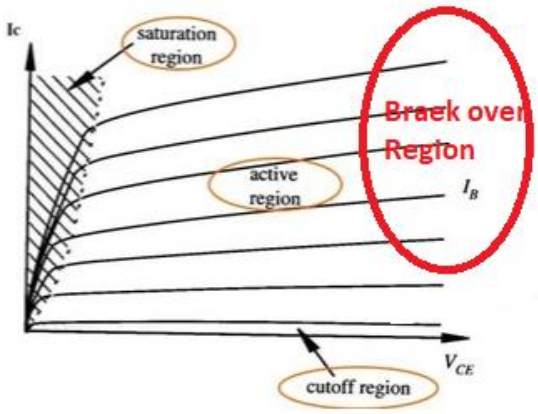


Figure 11. Breakover region

Factors that affect the operating point

- **The main factor that affect the operating point is the temperature. The operating point shifts due to change in temperature.**
- **As temperature increases, the values of ICE, β, VBE gets affected.**
- **ICBO gets doubled (for every 10º rise)**
- **VBE decreases by 2.5mv (for every 1º rise)**
- **So the main problem which affects the operating point is temperature. Hence operating point should be made independent of the temperature so as to achieve stability. To achieve this, biasing circuits are introduced.**

AC and DC Analysis of BJT

In a transistor amplifier, both dc and ac conditions prevail. The dc sources set up dc currents and voltages whereas the ac source (*i.e.* signal) produces fluctuations in the transistor currents and voltages. Therefore, a simple way to analyze the action of a transistor is to split the analysis into two parts *viz.* a dc analysis and an a.c. analysis. In the dc analysis, we consider all the dc sources at the same time and work out the dc currents and voltages in

the circuit. On the other hand, for ac analysis, we consider all the ac sources at the same time and work out the ac currents and voltages. By adding the dc and ac currents and voltages, we get the total currents and voltages in the circuit.

Load Line analysis

The output characteristics are determined experimentally and indicate the relation between VCE and IC. However, the same information can be obtained in a much simpler way by representing the mathematical relation between IC and VCE graphically. As discussed before, the relationship between VCE and IC is linear so that it can be represented by a straight line on the output characteristics. This is known as a load line. The points lying on the load line give the possible values of VCE and IC in the output circuit. As in a transistor circuit both dc and ac conditions exist, therefore, there are two types of load lines, namely: dc load line and ac load line. The former determines the locus of IC and VCE in the zero signal conditions and the latter shows these values when the signal is applied.

There are different methods in AC and DC analysis as shown in figure 12.

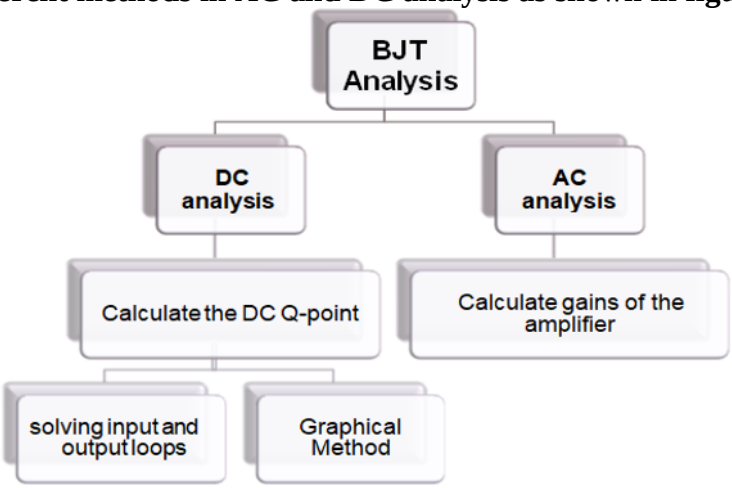


Figure 12. Methods of BJT analysis

DC analysis:

- **Find dc equivalent circuit by replacing all capacitors by open circuits and inductors by short circuits.**
- **Find Q-point from dc equivalent circuit by using appropriate large-signal transistor model.**

AC analysis:

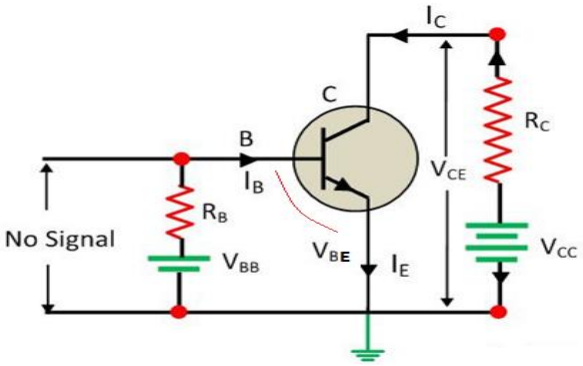
- **Find ac equivalent circuit by replacing all capacitors by short circuits, inductors by open circuits, dc voltage sources by ground connections and dc current sources by open circuits.**
- **Replace transistor by its small-signal model – Use small-signal ac equivalent to analyze ac characteristics of amplifier.**

DC Load Line (Static Load Line) (refer fig 13 and 14)

- **To draw DC load line of a transistor and we need to find the saturation current and cutoff voltage.**
- **The saturation current is the maximum possible current through the transistor and occurs at the point where the voltage across the collector is minimum.**
- **The cutoff voltage is the maximum possible voltage across the collector and occurs at zero collector current.**

Procedure

Step 1: Input DC operating point-Saturation & Cutoff point



Step 2

$+V_{BB} - I_B R_B - V_{BE} = 0$

P1= (0,---) and P2= (---,0)

$V_{BE=0}$; $I_B = V_{BB}/R_B$

$I_B = 0$; $V_{BE} = V_{BB}$

P1= (0, V_{BB}/R_B) and P2= (V_{BB},0)

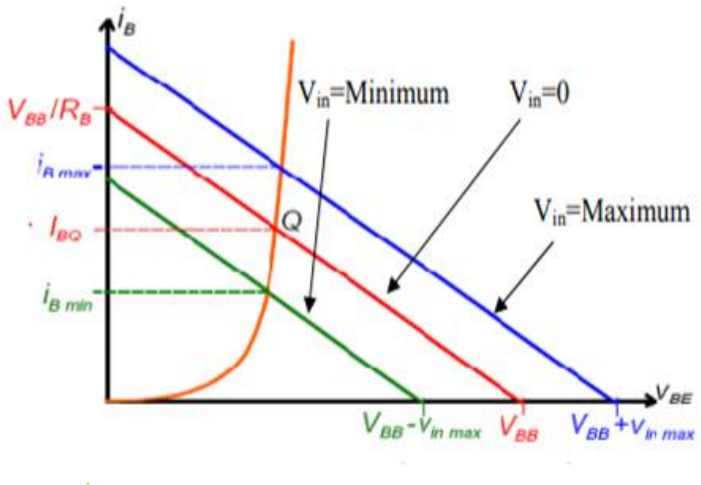


Figure 13.DC load line

Step 3: Output DC operating point

$+V_{cc} - I_c R_c - V_{CE} = 0$

Saturation Point P1= (0,---) and Cutoff point P2= (---,0)

$V_{CE=0}$; $I_c = V_{cc}/R_c$

$I_c = 0$; $V_{CE} = V_{cc}$

P1= (0, V_{cc} /R_c) and P2= (V_{cc},0)

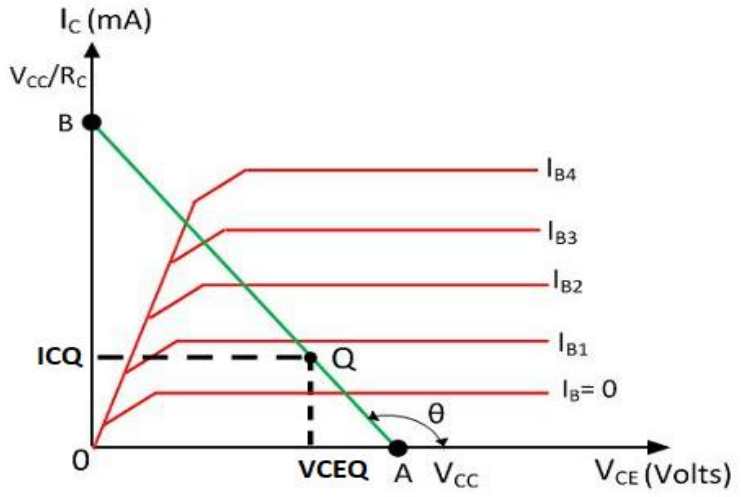
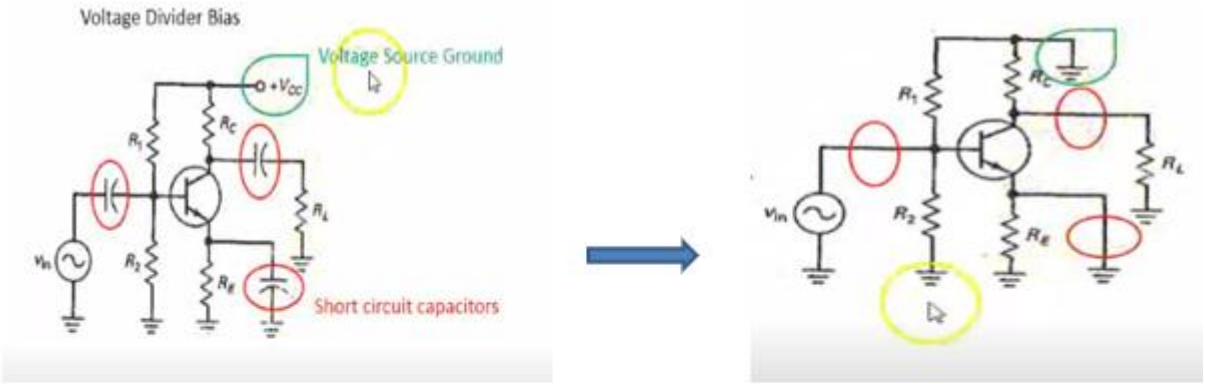


Figure 14. Operating point

AC Load Line (Dynamic Load Line)

Whereas the AC load line gives the peak-to-peak voltage (V_{pp}), or the maximum possible output swing for a given amplifier. This maximum V_{pp} is referred to as the compliance of the amplifier. The AC load line is a straight line with a slope equal to the AC impedance , it will vary with frequency, the slope of the AC load line depends on the frequency of the applied signal. The ratio of AC voltage to current in the device is defined by this line. The AC -Q point should be constant for both negative and positive half cycles of input signal.



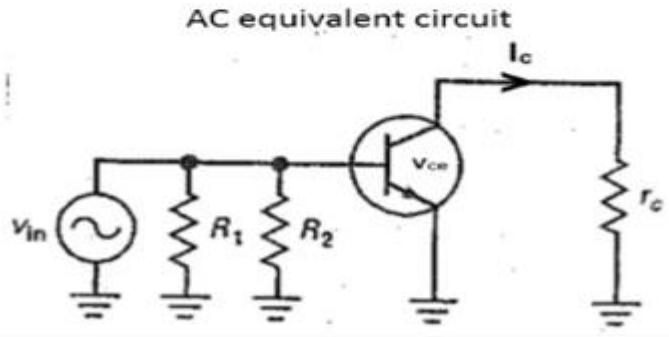
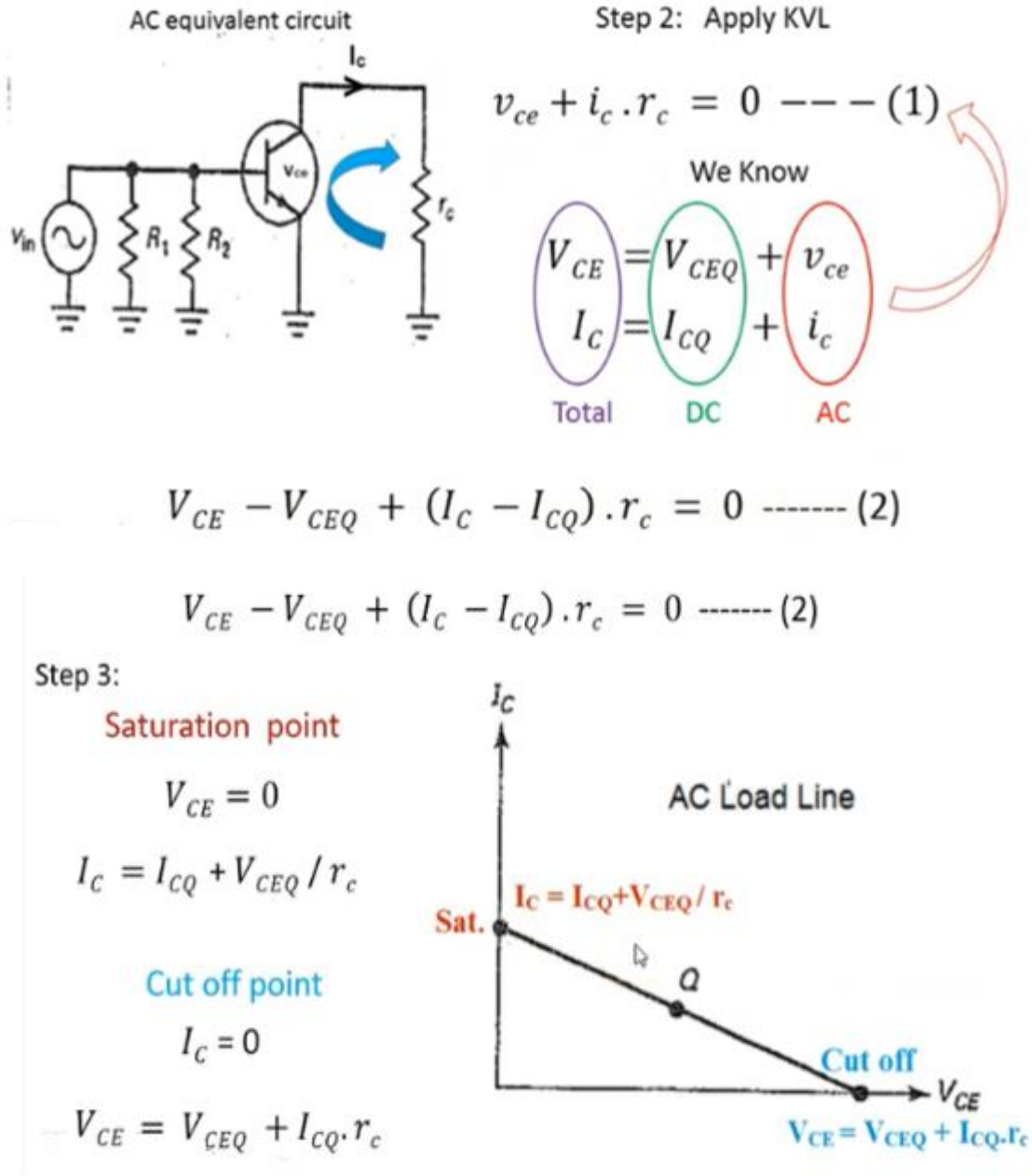


Figure 15.AC load line analysis



When AC and DC Load lines are represented in a graph, it can be understood that they are not identical. Both of these lines intersect at the Q-point or quiescent point. The endpoints of AC load line are saturation and cut off points.

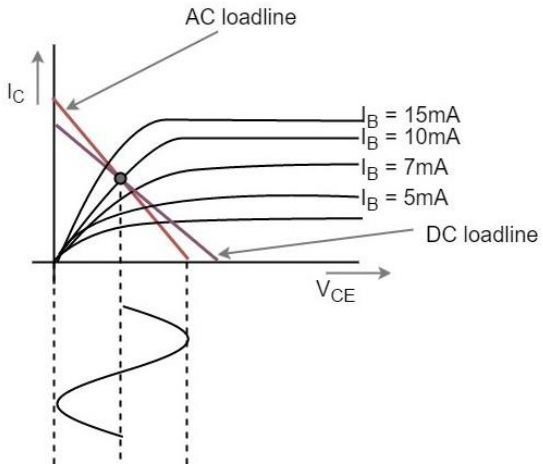


Figure 16. AC load line

Stabilization

The process of making the operating point independent of temperature changes or variations in transistor parameters is known as Stabilization.

- **Once the stabilization is achieved, the values of IC and VCE become independent of temperature variations or replacement of transistor. A good biasing circuit helps in the stabilization of operating point.**

<u>Need for Stabilization</u>

- **Stabilization of the operating point has to be achieved due to the following reasons.**
- **Temperature dependence of I_C**
- **Individual variations**
- **Thermal runaway**

Thermal runaway

The expression for collector current Ic is

$$I_C = \beta I_B + I_{CEO}$$

$$= \beta I_B + (\beta + 1) I_{CBO}$$

The flow of collector current and also the collector leakage current causes heat dissipation, If the operating point is not stabilized, there occurs a cumulative effect which increases this heat

dissipation. The self-destruction of such an unstabilized transistor is known as Thermal Runaway.

Stability factor

Stability factor used to understand the variation of collector current with the temperature dependent parameters such as saturation current I_{CO}, Base emitter voltage V_{BE} and β.

- ***Stable system – low stability factor***
- ***High stability factor- high sensitive to variations.***

$$S = \frac{dI_C}{dI_{CO}}$$

The stability factor is a measure of *bias stability* of a transistor circuit. It will be interesting to know that a *higher value of stability factor indicates poor stability, whereas a lower value indicates good stability.*

However, there are two other factors, which affect the stability of the d.c. biasing circuit, namely *variation in the base current* (I_B) *and the current gain* (β) with *temperature*. The stabilities, due to these two quantities, are measured by the stability factors S' and S'' respectively.

The stability factor S' may be defined as *the rate of change of collector current* (I_C) *with respect to the base current* (I_B) *keeping the common-emitter current gain* (β) *and reverse saturation current* (I_{CO}) *as constant.* Mathematically, the stability factor,

$$S' = \frac{dI_C}{dI_B}$$

The stability factor may also be expressed alternatively by using the relationship between base current (I_B), collector current (I_C) and reverse saturation current (I_{CO}). We know that the value of collector current in a transistor is given by the relation,

$$I_C = \beta \cdot I_B + (1 + \beta)\, I_{CO}$$

Differentiating the above expression with respect to I_C,

$$1 = \frac{d(\beta \cdot I_B)}{dI_C} + \frac{d(1+\beta)\, I_{CO}}{dI_C}$$

$$= \beta \times \frac{dI_B}{dI_C} + (1+\beta)\frac{dI_{CO}}{dI_C} \quad \text{... (Assuming } \beta \text{ as constant)}$$

$$= \beta \times \frac{dI_B}{dI_C} + (1+\beta)\frac{1}{S} \quad \left(\because\ S = \frac{dI_C}{dI_{CO}} \right)$$

$$\therefore \quad S = \frac{1+\beta}{1 - \beta\left(\frac{dI_B}{dI_C}\right)} \quad \text{... (i)}$$

The above expression is a general expression, which is very useful for determining the stability factor (S) of any biasing circuit. It can be done first by finding the relationship between the base current and collector current and then using the above equation to determine the value of stability factor.

Therefore it is more convenient to define the stability factor S' as the rate of change of collector current with respect to the base-to-emitter voltage *i.e.*,

$$S' = \frac{dI_C}{dV_{BE}}$$

Similarly, the stability factor, S'' may be defined as *the rate of change of collector current (I_C) with respect to current gain (β) keeping the base current (I_B) and reverse saturation current (I_{CO}) as constant*. Mathematically, the stability factor,

$$S'' = \frac{dI_C}{d\beta}$$

Stability factor is variation of collector current with respect to I_{CO} , V_{BE} *and* β *become S, S' , S'' respectively. It is defined as the degree of change in operating point due to variation in temperature.*

i) $$S = \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\,\beta \text{ constant}} \quad \text{or} \quad S = \left.\frac{\Delta I_C}{\Delta I_{CO}}\right|_{V_{BE},\beta \text{ constant}}$$

ii) $$S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}} \quad \text{or} \quad S' = \left.\frac{\Delta I_C}{\Delta V_{BE}}\right|_{I_{CO},\,\beta \text{ constant}}$$

iii) $$S'' = \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}} \quad \text{or} \quad S'' = \left.\frac{\Delta I_C}{\Delta \beta}\right|_{I_{CO},\,V_{BE} \text{ constant}}$$

Methods of Transistor Biasing

Transistor biasing is the controlled amount of voltage and current that must be given to a transistor for it to produce the desired amplification or switching effect. Practical circuits used to fix the Q point. Following are the commonly used methods for biasing the transistors.

- **Fixed-bias circuit (OR) Base Bias Circuit**
- **Collector to Base bias circuit & Modified Collector to Base bias circuit**
- **Voltage-divider bias (OR) Self Bias Circuit**
- **Emitter stabilized bias circuit**

Fixed Bias Circuit

The transistors base current, I_B remains constant for given values of Vcc, and therefore the transistors operating point must also remain fixed. These two resistors biasing network is used to establish the initial operating region of the transistor using a fixed current bias. This type of transistor biasing arrangement is also beta dependent biasing as the steady-state condition of operation is a function of the transistor's beta β value. As Temperature increases, collector current increases and base current decreases. When I_C increases - cannot achieve the good stabilization. Therefore, this type is called fixed bias type of circuit as shown in figure 17.

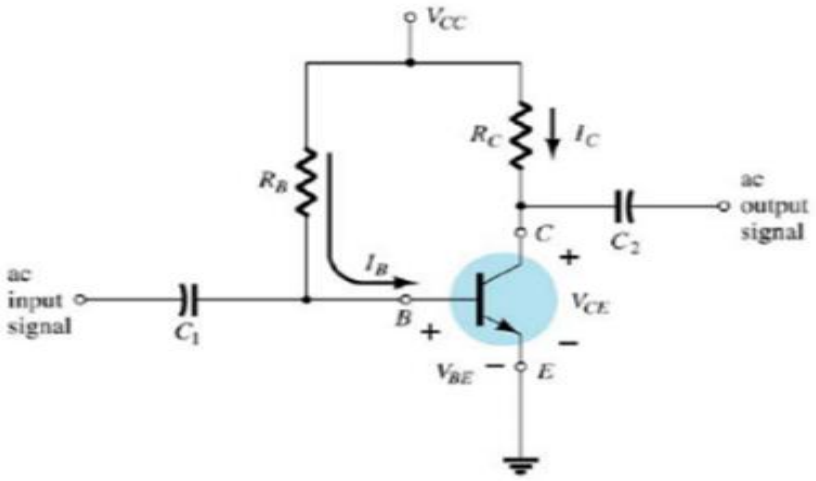
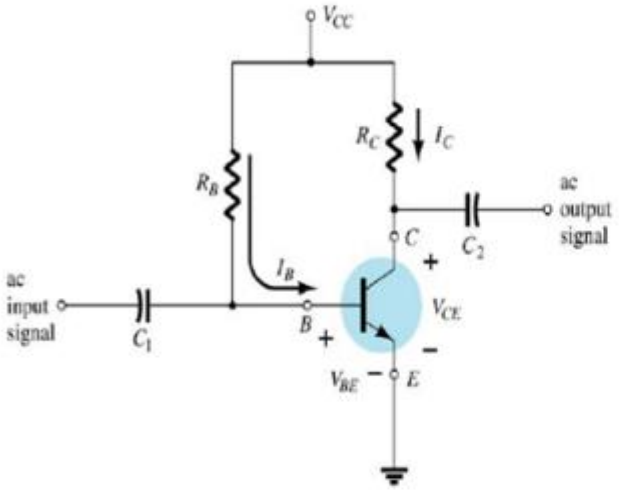


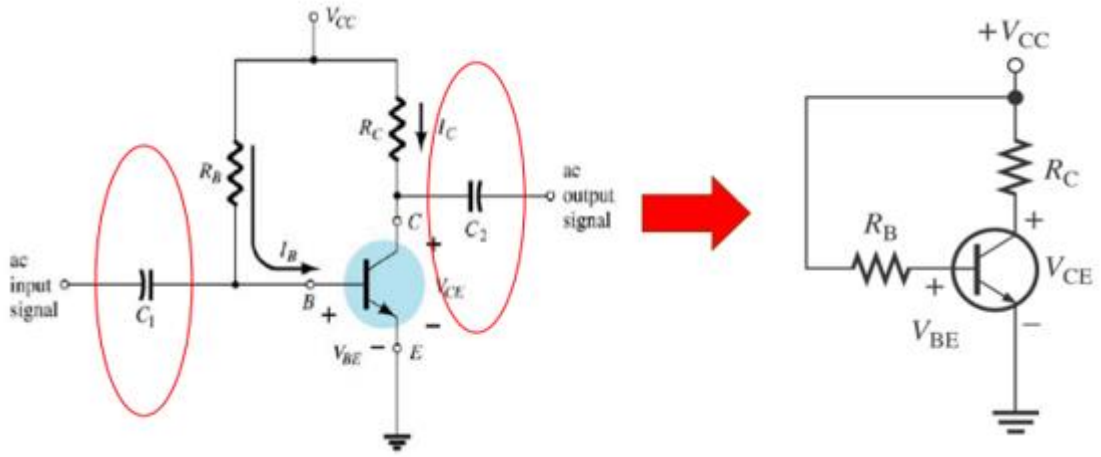
Figure 17. Fixed bias circuit



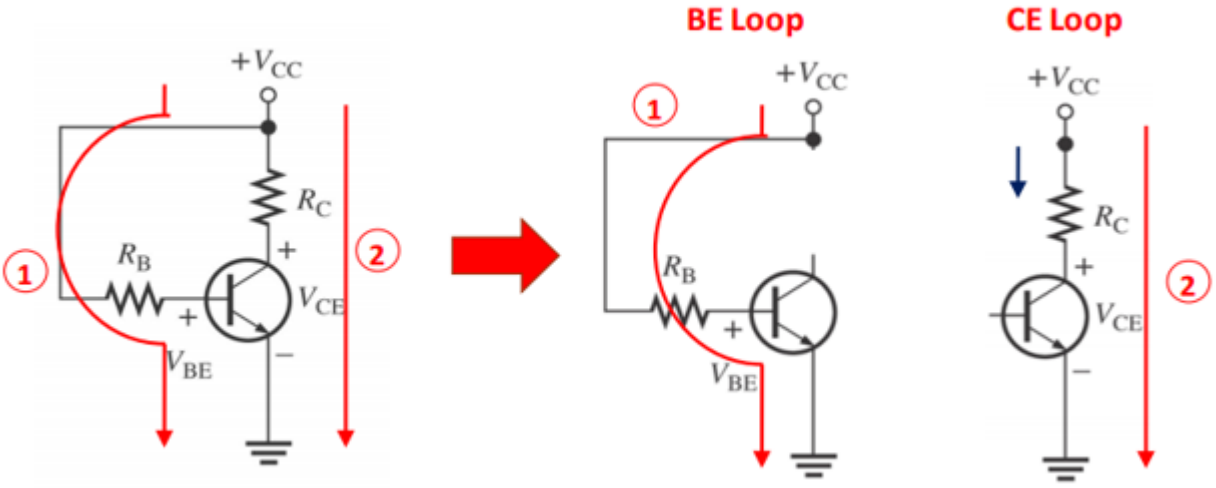
- This is common emitter (CE) configuration
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop (input loop)
  - CE loop(output loop)

Figure 18. Fixed bias circuit Analysis

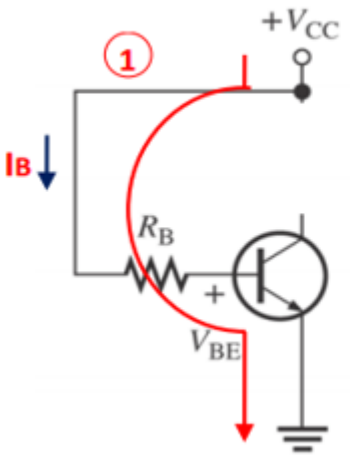
1st step: Locate capacitors and replace them with an open circuit



2nd step: Locate 2 main loops.



BE Loop Analysis

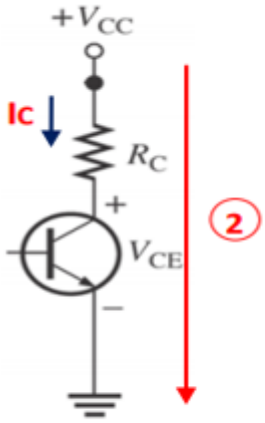


- From KVL;

$$-V_{CC} + I_B R_B + V_{BE} = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad (A)$$

CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} = 0$$

$$\therefore V_{CE} = V_{CC} - I_C R_C$$

- As we known;

$$I_C = \beta I_B \quad (B)$$

- Substituting (A) with (B)

$$I_C = \beta_{DC}\left(\frac{V_{CC} - V_{BE}}{R_B}\right)$$

Note that R_C does not affect the value of Ic

Stability factor S- Fixed Bias

$$S = \left.\frac{\partial Ic}{\partial Ico}\right|_{Vbe,\ \beta\ constant}$$

$$= \frac{(I + \beta)}{1 - \beta\frac{\partial Ib}{\partial Ic}}$$

For the fixed Bias Circuit Ib = Vcc / Rb

$$\therefore \frac{\partial Ib}{\partial Ic} = 0$$

$$\therefore \quad S = \frac{(I + \beta)}{1 - \beta(0)} \qquad \therefore \quad S = 1 + \beta$$

Stability factor S'- Fixed Bias

$$Ic = \beta Ib + Iceo$$

$$= \beta Ib + (\beta + 1) Icbo$$

$$= \beta \frac{Vcc - Vbe}{Rb} + (\beta + 1) Icbo$$

$$= \frac{\beta Vcc}{Rb} - \frac{\beta Vbe}{Rb} + (\beta + 1) Icbo$$

$$S' = \left.\frac{\partial Ic}{\partial Vbe}\right|_{Ico,\ \beta \text{ constant}}$$

$$\therefore \frac{\partial Ib}{\partial Vbe} = 0 - \frac{\beta}{Rb} + 0$$

$$\therefore \quad \boxed{S' = -\beta / Rb}$$

Stability factor S''- Fixed Bias

$$Ic = \beta Ib + Iceo$$

$$= \beta Ib + (\beta+1) Icbo$$

$$= \beta \frac{Vcc - Vbe}{Rb} + (\beta + 1) Icbo$$

$$= \frac{\beta Vcc}{Rb} - \frac{\beta Vbe}{Rb} + (\beta + 1) Icbo$$

$$S'' = \left.\frac{\partial Ic}{\partial \beta}\right|_{Ico,\ Vbe \text{ constant}}$$

$$\therefore \frac{\partial Ic}{\partial \beta} = \frac{Vcc}{Rb} - \frac{Vbe}{Rb} + Icbo$$

$$= Ib + Icbo$$

$$= Ib \text{ (approx)}$$

$$= Ic / \beta$$

$$\therefore \quad \boxed{S'' = Ic / \beta}$$

Merits:

- **It is simple to shift the operating point anywhere in the active region by merely changing the base resistor (RB).**
- **A very small number of components are required.**

Demerits:

- **The collector current IC does not remain constant with variation in temperature or power supply voltage. Therefore, the operating point is unstable.**
- **When the transistor is replaced with another one, considerable change in the value of β can be expected. Due to this change the operating point will shift.**

- **For small-signal transistors (e.g., not power transistors) with relatively high values of β (i.e., between 100 and 200), this configuration will be prone to thermal runaway (Uncontrolled feedback).**
- **To ensure absolute stability of the amplifier, a stability factor of less than 25 is preferred, and so small-signal transistors have large stability factors.**

Collector to base bias circuit (OR) Collector – Feedback Bias (OR)DC Bias with Voltage Feedback

- **To improve the stability of the bias circuit is to add feedback path from collector to base.**
- **Q point is slightly depends on transistor gain beta**
- **It is called DC bias with voltage feedback.**
- **It is an improvement over the fixed bias**
- **Biasing resistor is connected between collector and base of the transistor to provide a feedback path.**
- **Thus I_B flows through R_B and (I_c + I_B)flows through R_c**

<u>Circuit Analysis</u>

As temperature increases, I_c Increases, results drop across the collector resistance VR_C increases, so V_{CE} decreases and drop across R_B decreases.

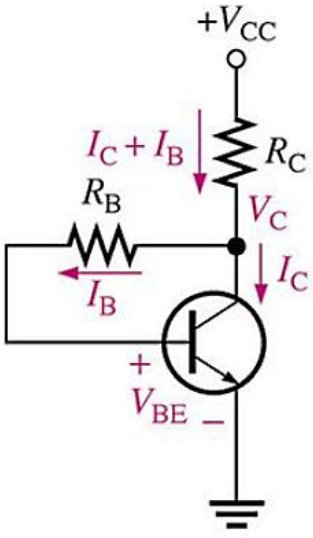


Figure 19. Collector to base bias circuit Analysis

Apply KVL in base circuit,

- $I_B = (V_C - V_{BE})/R_B$
- $I_C = (V_{CC} - V_{BE})/(R_C + R_B/\beta_{DC})$

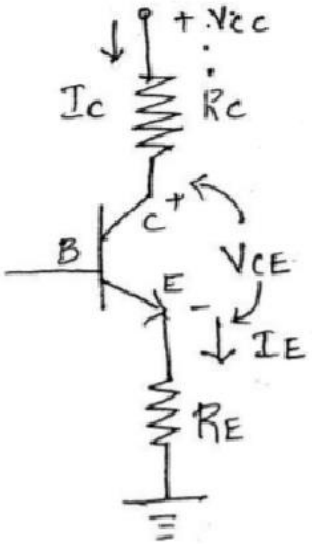


Figure 20. Collector to base bias circuit

Apply KVL at the output side

$V_{cc} - I_cR_c - V_{CE} - I_ER_E = 0$

$V_{CE} = V_{cc} - I_cR_c - I_ER_E$ (Approximately [$I_E \approx I_c$]

$V_{CE} = V_{cc} - I_c (R_c + R_E)$

$I_c = (V_{cc} - V_{CE}) / (R_c + R_E)$

R_B appears directly across input (base) and output (collector).Output is feedback to the input and increase in collector current decreases the base current. Negative feedback exists in the circuit ,so this circuit is called Voltage feedback bias circuit. Collector to bias circuit is having lesser stability factor than for fixed bias circuit.

<u>Stability factors – Collector to base bias</u>

$$Vcc = (Ib + Ic)Rc + IbRb + Vbe \qquad S = \left.\frac{\partial Ic}{\partial Ico}\right|_{Vbe,\ \beta \text{ constant}}$$

$$= IcRc + Ib(Rc + Rb) + Vbe$$

$$0 = \partial IcRc + \partial Ib(Rc + Rb) + 0 \qquad \text{after differentiation}$$

$$\text{or } - \partial IcRc = \partial Ib(Rc + Rb)$$

$$\therefore \quad \frac{\partial Ib}{\partial Ic} = \frac{-Rc}{Rc + Rb}$$

$$S = \frac{(I + \beta)}{1 - \beta \dfrac{\partial Ib}{\partial Ic}} = \frac{(I + \beta)}{1 + \beta \dfrac{Rc}{Rc + Rb}}$$

Stability factor S'

$$Ib = \frac{Vcc - IcRc - Vbe}{Rc + Rb} \qquad S' = \left.\frac{\partial Ic}{\partial Vbe}\right|_{Ico,\ \beta \text{ constant}}$$

$$\frac{Ic}{\beta} = \frac{Vcc - IcRc - Vbe}{Rc + Rb} \qquad Ic = \frac{\beta(Vcc - Vbe)}{Rb + (\beta + 1)\,Rc}$$

$$\frac{Ic}{\beta} + \frac{IcRc}{Rc + Rb} = \frac{Vcc - Vbe}{Rc + Rb} \qquad S' = \frac{\partial Ic}{\partial Vbe}$$

$$Ic\left[\frac{Rc + Rb + \beta Rc}{\beta(Rc + Rb)}\right] = \frac{Vcc - Vbe}{Rc + Rb} \qquad = \frac{-\beta}{Rb + (\beta + 1)\,Rc}$$

Stability factor S''

$$S'' = \left.\frac{\partial Ic}{\partial \beta}\right|_{Ico,\ Vbe \text{ constant}}$$

$$Vcc = (Ib + Ic)Rc + IbRb + Vbe$$

$$Vcc - Vbe = (Ib + Ic)Rc + IbRb$$

$$= Ib\,[(1 + \beta)Rc + Rb]$$

$$\therefore \quad Ib = \frac{Vcc - Vbe}{(1 + \beta)\,Rc + Rb}$$

$$\therefore \quad Ic = \frac{\beta(Vcc - Vbe)}{(1 + \beta)\,Rc + Rb}$$

$$\therefore \quad \frac{\partial Ic}{\partial \beta} = \frac{[(1 + \beta)Rc + Rb](Vcc - Vbe) - \beta(Vcc - Vbe)\,Rc}{[(1 + \beta)\,Rc + Rb]^2}$$

$$= \frac{(Vcc - Vbe)[(1 + \beta)Rc + Rb] - \beta Rc}{[(1 + \beta)\,Rc + Rb]^2}$$

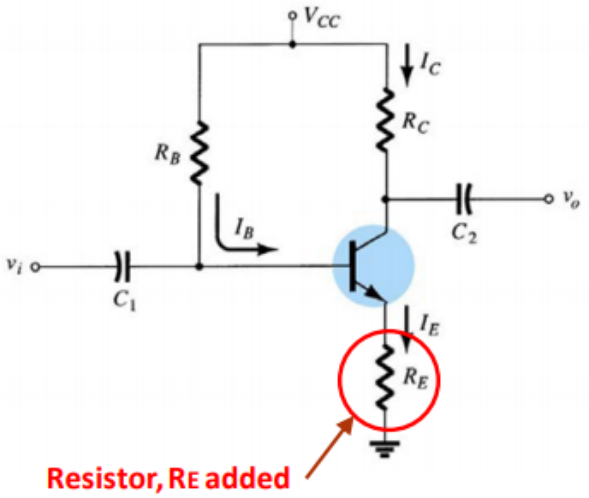
$$= \frac{(Vcc - Vbe)(Rc + Rb)}{[(1 + \beta)\,Rc + Rb]^2}$$

$$= \frac{Vcc - Vbe}{(1 + \beta)\,Rc + Rb} \times \frac{Rc + Rb}{(1 + \beta)\,Rc + Rb}$$

$$= \frac{Ib(Rc + Rb)}{(1 + \beta)\,Rc + Rb}$$

$$\therefore \quad S'' = \frac{Ic(Rc + Rb)}{\beta[(1 + \beta)\,Rc + Rb]}$$

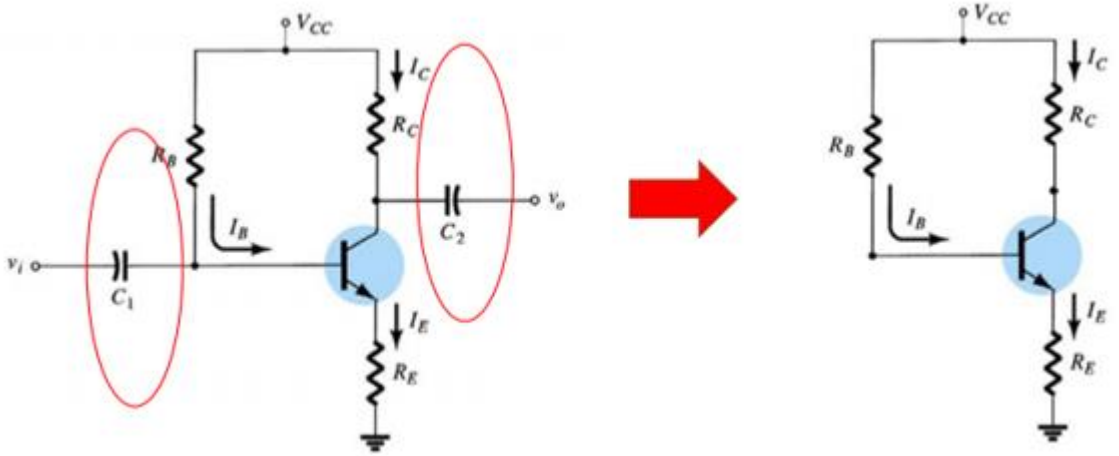
Fixed bias with emitter resistor



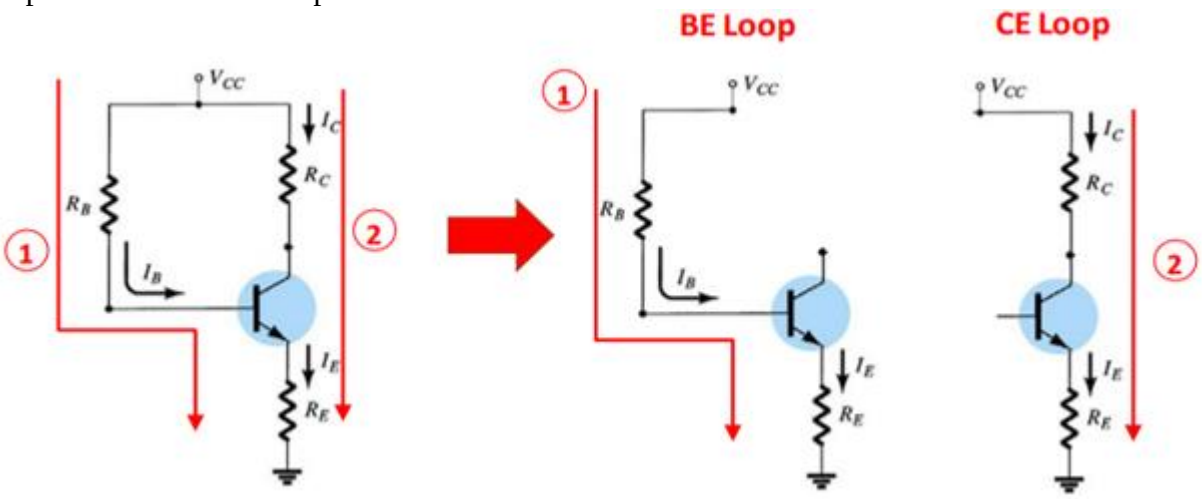
- An emitter resistor, R_E is added to improve stability
- 1st step: Locate capacitors and replace them with an open circuit
- 2nd step: Locate 2 main loops which;
  - BE loop
  - CE loop

Figure 21. Fixed bias with emitter resistor

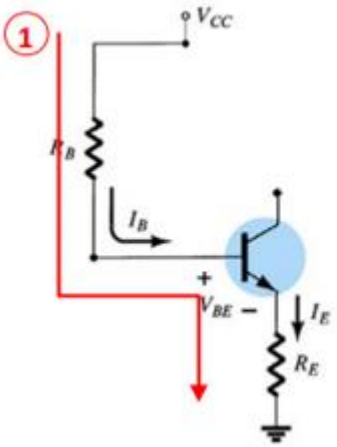
Step 1: Locate capacitors and replace them with an open circuit



Step 2: Locate 2 main loops



BE loop Analysis



- From kvl;

$$-V_{CC} + I_B R_B + V_{BE} + I_E R_E = 0$$

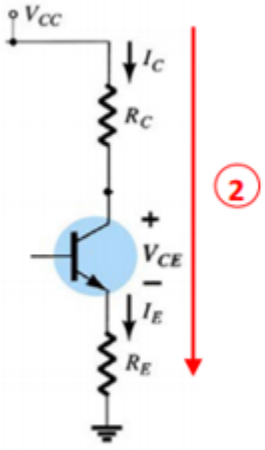
Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

$$-V_{CC} + I_B R_B + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

CE loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

- Assume;

$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$I_C = V_{CC} - V_{CE} / (R_C + R_E)$$

Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside condition, such as temperature, and transistor beta, changes.

Without Re

$$I_c = \left(\frac{V_{CC} - V_{BE}}{R_B} \right) \beta$$

With Re

$$I_c = \left(\frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \right) \beta$$

If the Ic is independent of beta and VBE, the Q point is not affected appreciably by variation in these parameters.

Fixed bias with emitter resistor

Advantage of using R_E:

i)Temperature increases and Ic increases

[I_c= ßI$_B$+(1+ ß)I_{cbo}]

ii) $I_E R_E$ increase and I_B decreases & I_c decrease

I_C = ß(V_{cc}-V_{BE})/[R_B+(ß+1) R_E]

ß+1≈ ß, therefore I_C = ß(V_{cc}-V_{BE})/[R_B+ßR_E]

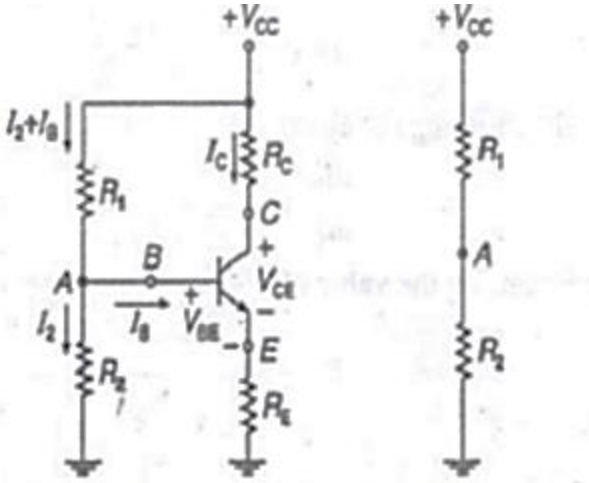
ßR_E › › R_B, therefore I_C = ß(V_{cc}-V_{BE})/[ßR_E]

I_C = (V_{cc}-V_{BE}) / R_E independent of ß

Voltage divider bias circuit

The name voltage divider is derived from the fact that resistors R_1 an R_2 form a potential divider across the V_{CC} supply. The voltage drop across resistor R_2 forward biases the base-emitter junction of a transistor. The emitter resistor (R_E) providers the d.c. stability.

Now let us analyse the base-emitter loop of the voltage divider bias circuit. A basic assumption is that the resistance looking into the base is much larger than that of the resistor R_2. If this is so, then the current through resistor R_1 flows almost completely into resistor R_2 and the two resistors may be considered effectively *in series* as shown in Fig. (*b*). The voltage at the junction of the resistor (*i.e.*, point *A*), which is also the voltage at the base of the transistor, is then determined simple by the voltage divider network of R_1 and R_2 and the supply voltage. If the current through resistors R_1 and R_2 is of the order of milliamperes and that through the base is of the order of the microamperes, then the base current component can be neglected.



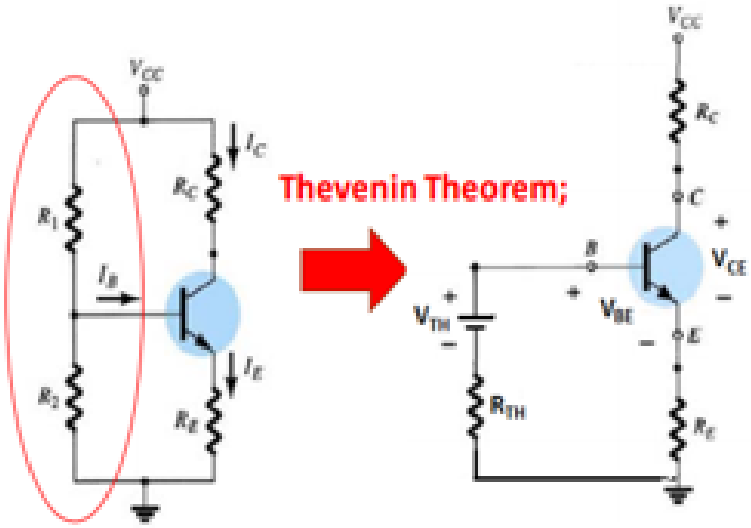
(*a*) Voltage divide bias circuit. (*b*) Voltage divider.

- **Voltage-divider bias is the most widely used type of bias circuit. Only one power supply is needed and voltage-divider bias is more stable (independent) than other bias types.**
- **R1 and R2 are used to provide potential divider**
- **If the Ic current increases due to change in temperature or change in β, The I_E also increases and voltage drop across R_E increases, reducing V_{BE}, thereby I_B and I_c also reduces- Hence negative feedback exists in emitter base circuit.**
- **A voltage divider in which the base current is small compared to the current in R2 is said to be a stiff voltage divider because the base voltage is relatively independent of the different transistor and temperature effects.**
- **Provides good Q-point stability with a single polarity supply voltage**
- **This is the biasing circuit wherein, ICQ and VCEQ are almost independent of beta.**
- **The level of IBQ will change with beta so as to maintain the values of ICQ and VCEQ almost same, thus maintaining the stability of Q point.**
- **Two methods of analyzing a voltage divider bias circuit are:**
- **Approximate method: direct method, saves time and energy.**
- **Exact method: can be applied to any voltage divider circuit (we use this method)**

Step 1: Locate capacitors and replace them with an open circuit

- **Step 2: Simplified circuit using Thevenin Theorem**
- **Step 3: Locate 2 main loops:**
  - **BE loop**
  - **CE loop**

2nd step: : Simplified circuit using **Thevenin Theorem**



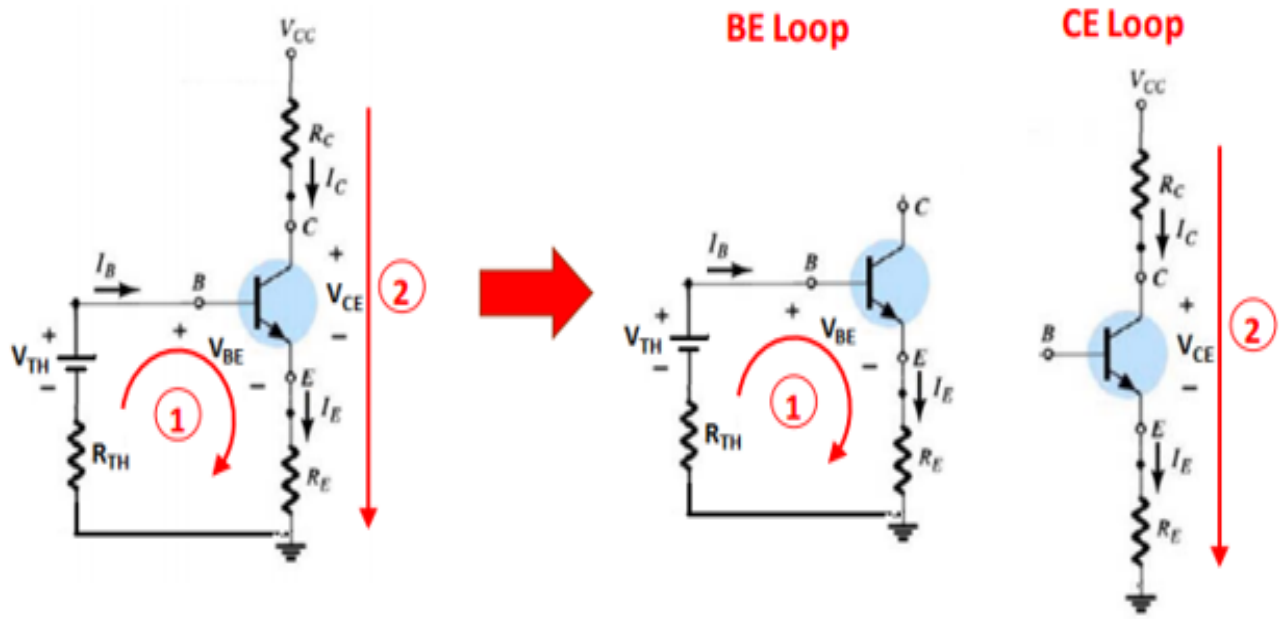
From Thevenin Theorem;

$$R_{TH} = R_1 // R_2 = \frac{R_1 \times R_2}{R_1 + R_2}$$

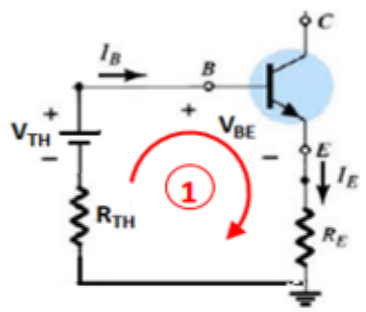
$$V_{TH} = \frac{R_2}{R_1 + R_2} V_{CC}$$

Simplified Circuit

Locate 2 main loops.



BE Loop Analysis



- From KVL;

$$-V_{TH} + I_B R_{TH} + V_{BE} + I_E R_E = 0$$

Recall; $I_E = (\beta + 1) I_B$

Substitute for I_E

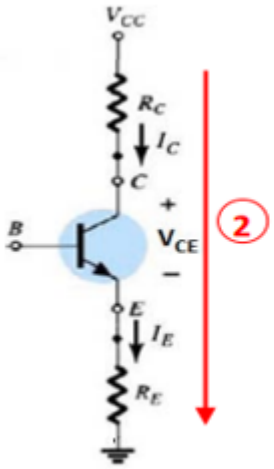
$$-V_{TH} + I_B R_{TH} + V_{BE} + (\beta + 1) I_B R_E = 0$$

$$\therefore I_B = \frac{V_{TH} - V_{BE}}{R_{RTH} + (\beta + 1) R_E}$$

Where $R_{TH} = R_B$

$I_B = (V_{TH} - V_{BE}) / R_B + (\beta + 1) R_E$

CE Loop Analysis



- From KVL;

$$-V_{CC} + I_C R_C + V_{CE} + I_E R_E = 0$$

- Assume;

$$I_E \approx I_C$$

- Therefore;

$$\therefore V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$I_c = (V_{CC} - V_{CE}) / (R_C + R_E)$

Stability factor of voltage Divider Bias

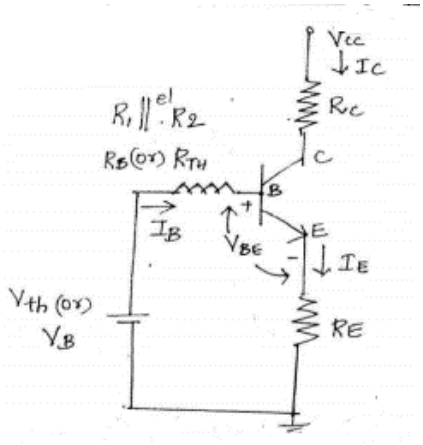


Figure 22. Stability factor

Stability factor (S):

$Vb = IbRb + Vbe + IeRe$

$= IbRb + Vbe + (Ib + Ic)Re$

where Rb = Rb1 ll Rb2

$$S = \left.\frac{\partial Ic}{\partial Ico}\right|_{Vbe,\ \beta \text{ constant}}$$

Differentiating,

$0 = \partial IbRb + 0 + \partial IbRe + \partial IcRe$

i.e. $\partial Ib(Rb + Re) = -\partial IcRe$

$$\therefore \frac{\partial Ib}{\partial Ic} = \frac{-Re}{Rb + Re} \qquad S = \frac{(I + \beta)}{1 - \beta \dfrac{\partial Ib}{\partial Ic}} = \frac{(I + \beta)}{1 + \beta \dfrac{Re}{Re + Rb}}$$

- In the above equation, if Rb << Re, then S becomes 1

$$Rb = Rb1 \text{ ll } Rb2$$

- Hence either Rb1 or Rb2 must be << Re
- Since Vb << Vcc, Rb2 is kept small wrt Rb1

Stability factor S':

$$Vb = IbRb + Vbe + IeRe$$

$$= IbRb + Vbe + (Ib + Ic)Re$$

$$= Ib(Rb + Re) + Vbe + IcRe$$

$$= Ic / \beta\,(Rb + Re) + Vbe + IcRe$$

$$S' = \left.\frac{\partial Ic}{\partial Vbe}\right|_{Ico,\ \beta \text{ constant}}$$

Or, $\beta Vb = Ic(Rb + Re) + \beta\, Vbe + \beta\, IcRe$

$$= Ic[Rb + (\beta + 1)Re] + \beta\, Vbe$$

$0 = \partial Ic[Rb + (\beta + 1)Re] + \beta \partial Vbe$ Differentiating,

Or, $\beta \partial Vbe = -\partial Ic\,[Rb + (\beta + 1)Re]$

$$S' = \frac{\partial Ic}{\partial Vbe} = \frac{-\beta}{Rb + (\beta + 1)\,Re}$$

Stability factor S'':

$$Vb = IbRb + Vbe + IeRe$$

$$= Ib(Rb + Re) + Vbe + IcRe$$

$$= Ic / \beta\,(Rb + Re) + Vbe + IcRe$$

$$S'' = \left.\frac{\partial Ic}{\partial \beta}\right|_{Ico,\ Vbe \text{ constant}}$$

Or, $\beta Vb = Ic(Rb + Re) + \beta\, Vbe + \beta\, IcRe$

Or, $\beta(Vb - Vbe) = Ic(Rb + Re) + \beta\, IcRe$

Differentiating,

$$\partial\beta(Vb - Vbe) = \partial Ic(Rb + Re) + \partial\beta IcRe + \partial Ic\, \beta Re$$

$$\partial\beta(Vb - Vbe - IcRe) = \partial Ic[Rb + Re + \beta Re]$$

$$\therefore S'' = \frac{\partial Ic}{\partial \beta} = \frac{Vb - Vbe - IcRe}{Rb + Re(1 + \beta)}$$

$$S'' = \frac{\partial Ic}{\partial \beta} = \frac{Vb - Vbe - IcRe}{Rb + Re(1+\beta)}$$

$$= \frac{Vb - Vbe - IeRe}{Rb + Re(1+\beta)}$$ As Ie = Ic

$$= \frac{Ib\,Rb}{Rb + Re(1+\beta)}$$

$$= \frac{Ib}{1 + (Re/Rb)(1+\beta)}$$

Hence Rb / Re must be small to make S'' smaller

Merits:

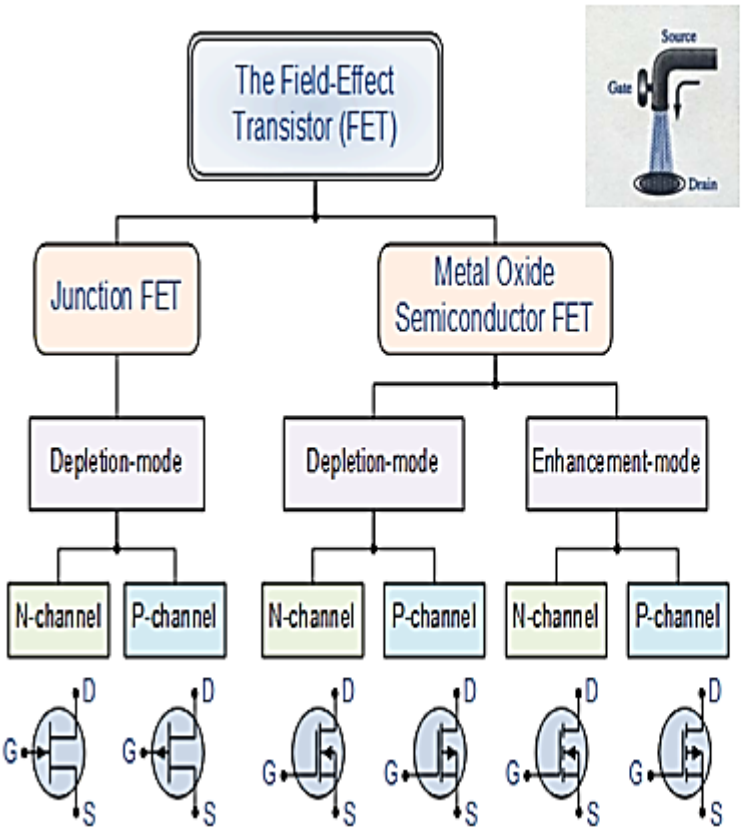
• Operating point is almost independent of β variation.

• Operating point stabilized against shift in temperature.

Demerits:

• As β-value is fixed for a given transistor, this relation can be satisfied either by keeping RE fairly large, or making R1||R2 very low

Introduction- FET



- **FET** is a **"Unipolar"** device

that depends only on the conduction of electrons (N-channel) or holes (P-channel).

- **FET – a three-terminal voltage-**

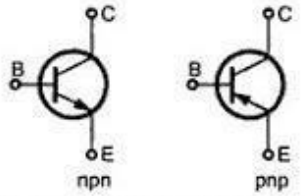
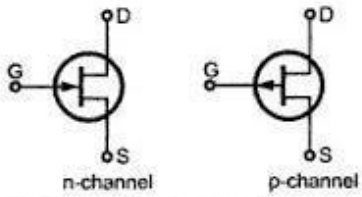
controlled device **used in amplification and switching** Application.

- FET is a **voltage-controlled device.**
- FET **high input resistance.** It

very sensitive to input voltage signals, **and easily damaged** by static electricity.

Figure 23. Types of FET

Table 3. Comparison of BJT and FET

Sr. No.	Parameter	BJT	JFET
1	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3	Types	npn and pnp	n-channel and p-channel.
4	Symbols		
5	Configurations	CE, CB, CC	CS, CG, CD
6	Input resistance	Less compare to JFET.	High compare to BJT.
7	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	Thermal stability	Less	More
10	Thermal runaway	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temeperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	Relation between input and output	Linear	Non-linear
12	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	Gain bandwidth product	High	Low

FET BIASING

- **The Parameters of FET is temperature dependent .**
- **When temperature increases drain resistance also increases, thus reducing the drain current.**
- **Unlike BJTs, thermal runaway does not occur with FETs .**

Different biasing circuits of FET are

1) **Fixed bias circuits**
2) **Self bias circuits**
3) **Voltage bias circuits**

General Equations:

For all FETs:

$$I_G \approx 0A \qquad I_D = I_S$$

For JFETs and Depletion-Type MOSFETs:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

For Enhancement-Type MOSFETs:

$$I_D = k(V_{GS} - V_T)^2$$

1) Fixed-Bias Configuration

- **The configuration includes the ac levels Vi and Vo and the coupling capacitors.**
- **The resistor is present to ensure that Vi appears at the input to the FET amplifier for the AC analysis.**

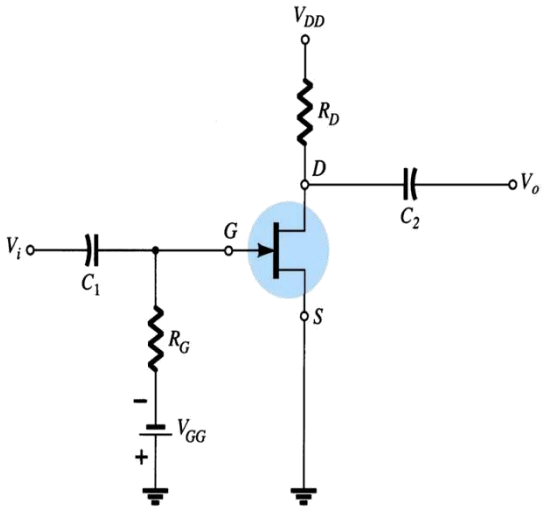


Figure 24. Fixed bias circuit

For the DC analysis,

- **Capacitors are open circuits**

$$I_G \cong 0A \qquad V_{RG} = I_G R_G = (0A)R_G = 0V$$

- **and**
- **The zero-volt drop across R_G permits replacing R_G by a short-circuit**

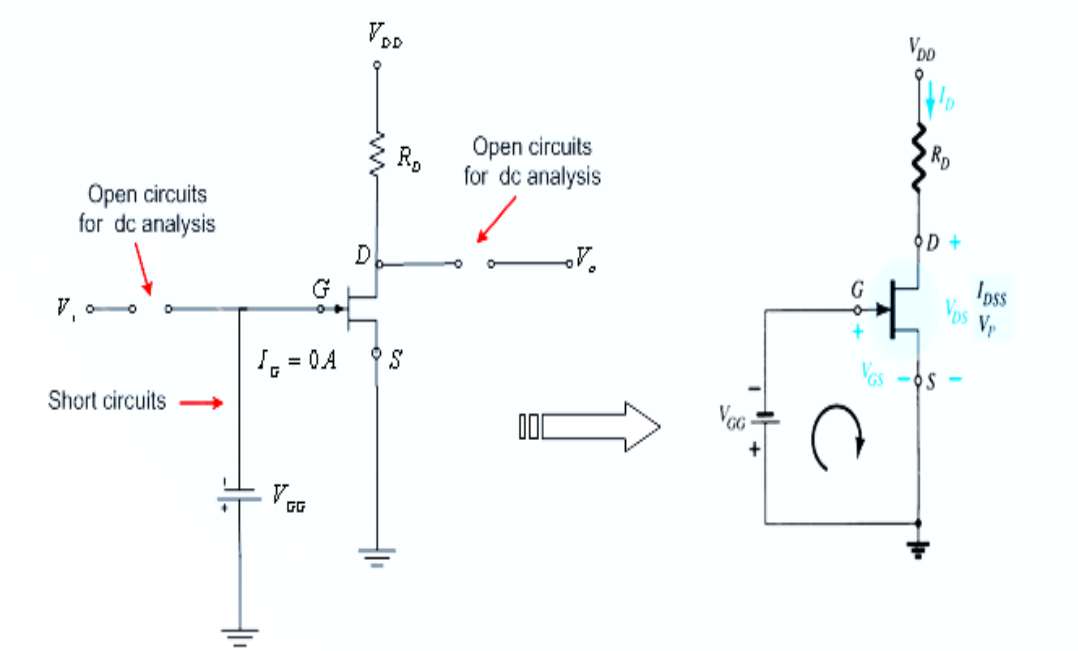


Figure 25. fixed bias analysis

Investigating the input loop

I_G=0A, therefore

$V_{RG}=I_GR_G=0V$

Applying KVL for the input loop,

$-V_{GG}-V_{GS}=0$

$V_{GG}= -V_{GS}$

- **It is called *fixed-bias configuration* due to V_{GG} is a fixed power supply so V_{GS} is fixed**
- **The resulting current,**

$$I_D = I_{DSS}(1-\frac{V_{GS}}{V_P})^2$$

Output loop KVL:

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_S = 0V$$

$$V_{DS} = V_D - V_S$$

$$V_D = V_{DS} + V_S$$

$V_S = 0$ $\quad V_D = V_{DS}$

$$V_{GS} = V_G - V_S$$

$$V_G = V_{GS} + V_S$$

$$V_S = 0$$

$$V_G = V_{GS}$$

- **Investigating the graphical approach.** **Graphical approach will be used to examine the dc analysis for FET because it is most popularly used rather than mathematical approach**
- **Using below tables, we can draw the graph**

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
0.5	$I_{DSS}/4$
V_P	0mA

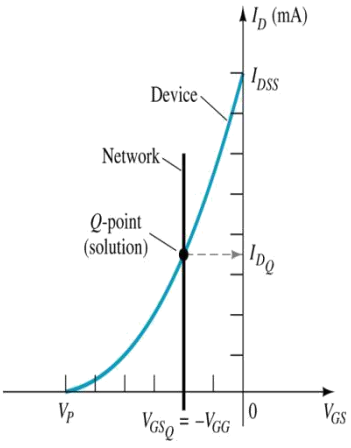


Figure 26. Q point

- **The fixed level of V_{GS} has been superimposed as a vertical line at**
- **The point where the two curves intersect is the common solution to the configuration – commonly referrers to as the quiescent or operating point.**
- **The quiescent level of I_D determine by drawing a horizontal line from the Q-point to the vertical I_D axis.**

2) Self bias

- **<u>Self-bias</u> is the most common type of biasing method for JFETs.**
- **JFET must be operated such that the gate-source junction is always reverse biased.**
- **The self-bias configuration eliminates the need for two dc supplies. The controlling V_{GS} is now determined by the voltage across the resistor R_S**
- **To keep the GS-junction reverse biased:**

  (a) V_{GS} will be -ve for *n*-channel (b) V_{GS} will be +ve for *p*-channel.

- **It can be achieved using self-bias arrangement as shown.**

- **The gate resistor, RG : not affect the bias**

because it has essentially no volt drop across it.

- **Therefore, the gate remains 0V.**
- **RG only to force the gate to be 0V and isolate an**

ac signal from ground in amplifier applications.

- **Self-biased JFETs:**

$I_D = I_S$ **for all JFET circuits**

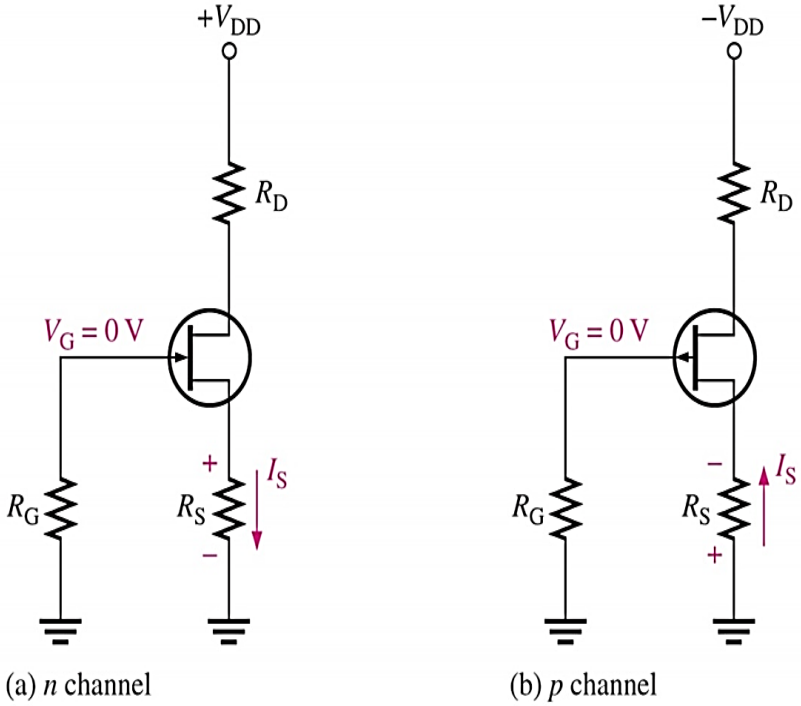


Figure 27. Self bias FET

KVL for Input Loop:

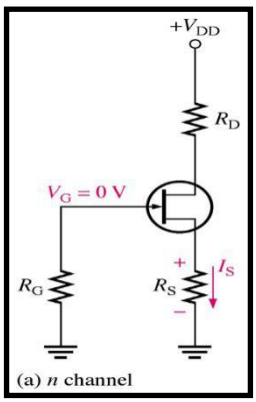
<u>For *n*-channel JFET</u>

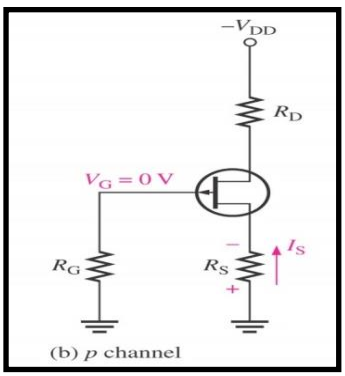
I_S **through** R_S **produces a voltage drop, making the Source -ve with respect to ground.**

Since, $I_S = I_D$ **and** $V_G = 0$, $V_S = I_D R_S$.

So: $V_{GS} = V_G - V_S = 0 - I_D R_S$

- ✓ ***(n channel)*** $V_{GS} = -I_D R_S$





<u>For *p*-channel JFET</u>

I_S through R_S produces a –ve voltage at Source,

making the Gate +ve with respect to ground.

Since, $I_S = I_D$, and $V_G = 0$, $-V_S = -I_D R_S$

$$V_{GS} = V_G - (-V_S) = 0 - (-I_D R_S)$$

- ✓ ***(p channel)*** $V_{GS} = I_D R_S$

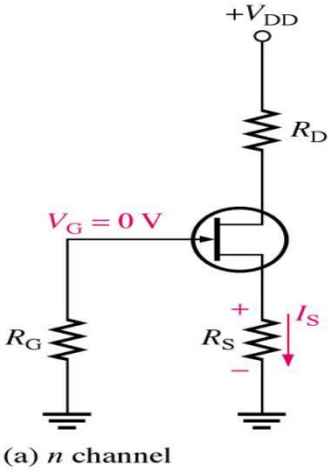
KVL for Output Loop:

$$+V_{DD} - I_D R_D - V_{DS} - V_S = 0$$

$$\therefore V_S = I_D R_S$$

$$+V_{DD} - I_D R_D - I_D R_S = V_{DS}$$

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$



(a) *n* channel

Graphical approach

- **Draw the device transfer charac**teristic
- Draw the network load line
  - Use $V_{GS} = -I_D R_S$ to draw straight line.
  - First point, $I_D = 0, \quad V_{GS} = 0$
  - Second point, any point from $I_D = 0$ to $I_D = I_{DSS}$.

Choose

$$I_D = \frac{I_{DSS}}{2} \text{ then}$$

$$V_{GS} = -\frac{I_{DSS} R_S}{2}$$

The quiescent point obtained at the intersection of the straight line plot and the device characteristic curve.

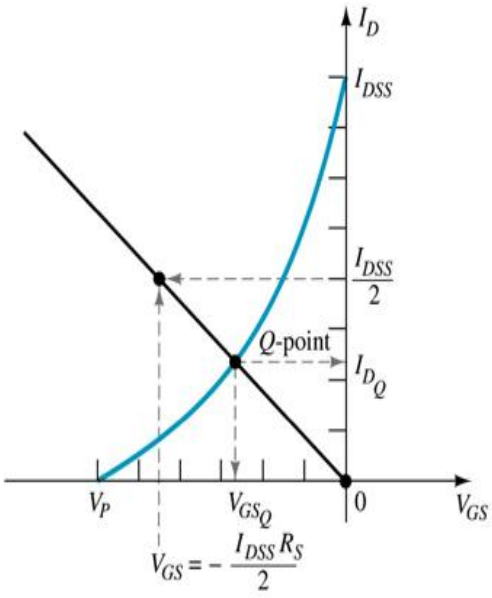


Figure 28. Q point

3) Voltage-Divider bias

- **The arrangement is the same as BJT but the DC analysis is different**
- **In BJT, IB provide link to input and output circuit, in FET VGS does the same**
- **The voltage at source, V_S of the JFET must be more +ve than the voltage at gate, V_G in order to keep the GS-junction reverse bias.**
- **Since I_D=I_S.**

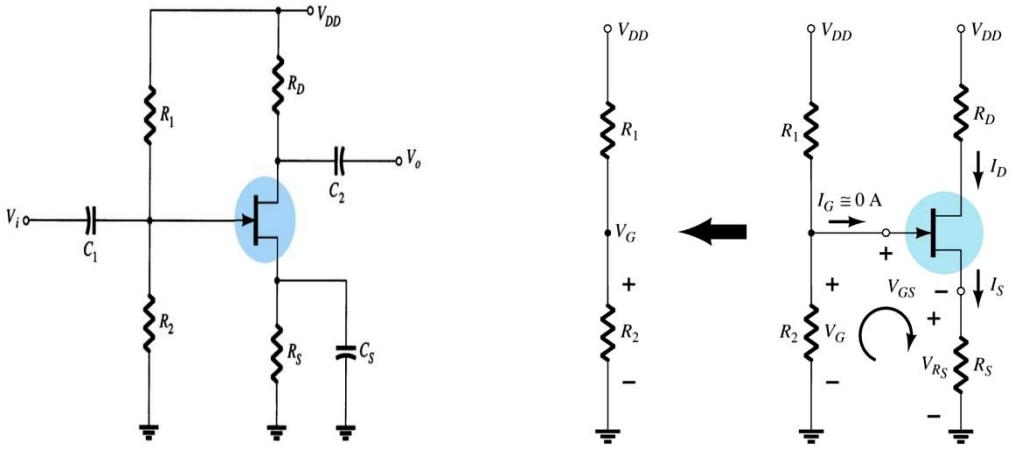


Figure 29. N channel JFET

- **The source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network.**
- **I_G = 0A ,Kirchoff's current law requires that I_{R1}= I_{R2} and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G.**

- **V_G can be found using the voltage divider rule :**

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Using Kirchoff's Law on the input loop: Rearranging and using ID =IS:

$$V_G - V_{GS} - V_{RS} = 0$$

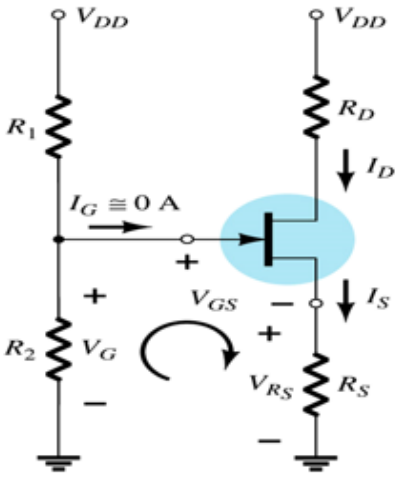
$$V_{GS} = V_G - I_D R_S$$

Using Kirchoff's Law on the Output loop:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$



1. **Plot the line: By plotting two points:**

$V_{GS} = V_G$, $I_D = 0$ and $V_{GS} = 0$, $I_D = V_G/R_S$

2. Plot the transfer curve by plotting I_{DSS}, V_P and calculated values of I_D.

3. Where the line intersects the transfer curve is the Q point for the circuit.

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be found.

$$I_{R1} = I_{R2} = \frac{V_{DD}}{R_1 + R_2}$$

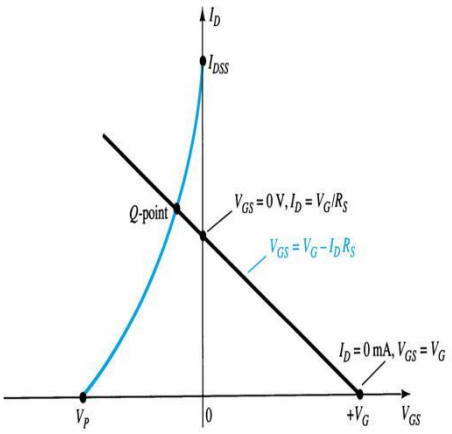


Figure 30. Q point Analysis

Advantage

provide the most stable Q-point value of I_D.

Disadvantage

circuit complexity makes it undesirable for most applications.

MOSFET BIASING

Design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor.

• An appropriate dc operating point or bias point is characterized by a stable and predictable dc drain current I_D and by a dc drain-to-source voltage V_{DS} that ensures operation in the saturation region for all expected input-signal levels.

- **The similarities in appearance between the transfer curves of JFETs and depletion-type N-MOSFETs permit a similar analysis of each in the dc domain.**
- **For JFETs and Depletion-Type MOSFETs:** $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- **For Enhancement-Type MOSFETs: The drain current is zero for levels of gate-to-source voltage, VGS less than the threshold level VGS(Th). For levels of VGS greater than VGS(Th), the drain current is defined by**

$$I_D = k(V_{GS} - V_T)^2$$

D-Type MOSFET Biasing Circuits

Zero-bias

•Self-Bias

•Voltage-Divider Bias

E-Type MOSFET Biasing Circuits

•Voltage-Divider Bias

- **Feedback Bias**

D-MOSFET biasing techniques

ZERO BIAS —is a popular biasing technique that can be used only with depletion-type MOSFETs.

• This form of bias is called zero bias because the potential difference between the gate-source region is zero.

Since there is no current in the gate circuit, no voltage is developed across RG, and V_{GS}=O Therefore I_D=IDSS, and

VDs=VDD-$l_D R_D$.

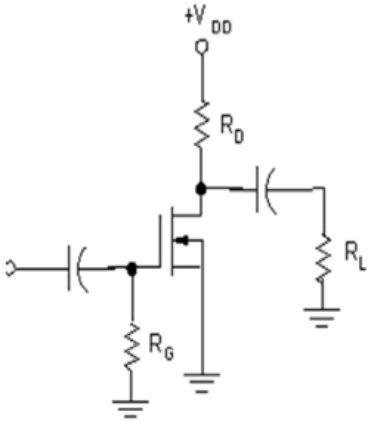


Figure 31. Zero bias

D-MOSFET SELF BIAS

Self-bias is the most common type of biasing method for JFETs. Notice there is no voltage applied to the gate. The voltage to ground from here will always be VG = OV.

- **However, the voltage from gate to source (VGS) will be negative for n channel and positive for p channel keeping the junction reverse biased.**
- **This voltage can be determined by the formulas below. $I_D = I_s$**
- **(n channel) $V_{GS} = V_G — V_s = -I_D R_s$**
- **(p channel) $V_{GS} = I_D R_s$**

$$V_{GS} + I_{DS} R_S = 0$$

$$\therefore I_{DS} = -\frac{V_{GS}}{R_S}$$

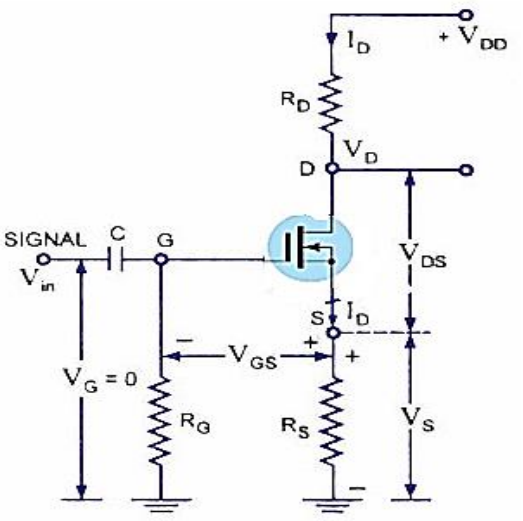
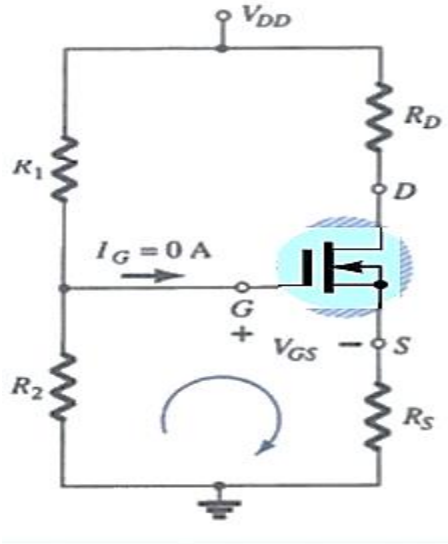


Figure 32. Self bias

D-MOSFET voltage divider bias

- **Depletion-type MOSFET bias circuits are similar to JFETs.**



- $I_D=I_{DSS}(1-V_{GS}/V_P)^2$
- Voltage-divider configuration results in:
- $V_{GS}=V_G-I_DR_S$
- Where $V_G=R_2xV_{DD}/(R_1+R_2)$

Figure 33. Voltage divider bias

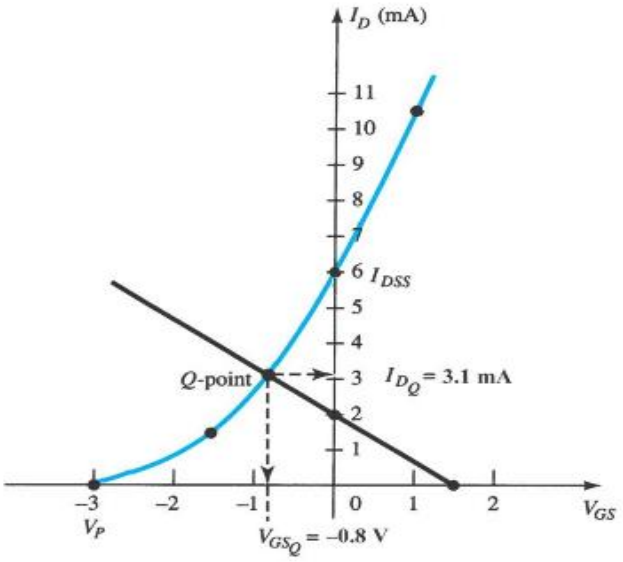


Figure 34. Q point analysis

E-MOSFET FEEDBACK BIASING

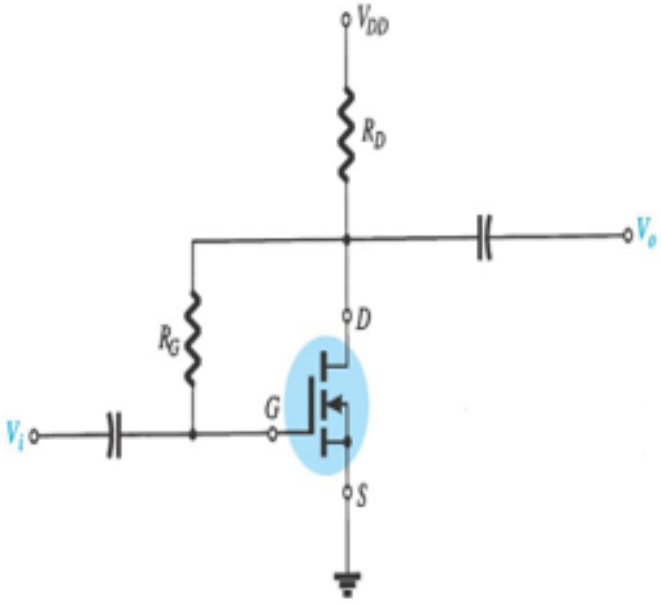


Figure 35. Feedback biasing

The resistor R_G brings a suitably large voltage to the gate to drive the MOSFETs "ON". Since I_G = 0 mA and V_{RG}=0V, we can draw the dc equivalent network.

- I_G=0 V
- V_D=V_G
- V_{DS}=V_{GS}
- V_{DS}=V_{DD}-$I_D R_D$
- V_{GS}=V_{DD}-$I_D R_D$
- When I_D=0 A:
  V_{GS}=V_{DD}
- When V_{GS}=0 V:
  I_D=V_{DD}/R_D

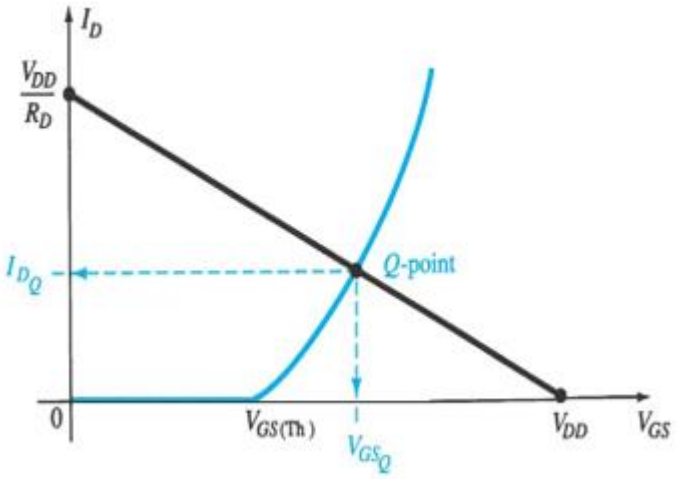


Figure 36. Q point analysis

E- MOSFETS VOLTAGE-DIVIDER BIASING

A second popular biasing arrangement for the enhancement-type MOSFETs. The fact that IG = 0 mA results in the following equation for VGG as derived from the

Again plot the line and the transfer curve to find the Q-point.
Using the following equations:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

Input loop : $V_{GS} = V_G - I_D R_S$

Output loop : $V_{DS} = V_{DD} - I_D (R_S + R_D)$

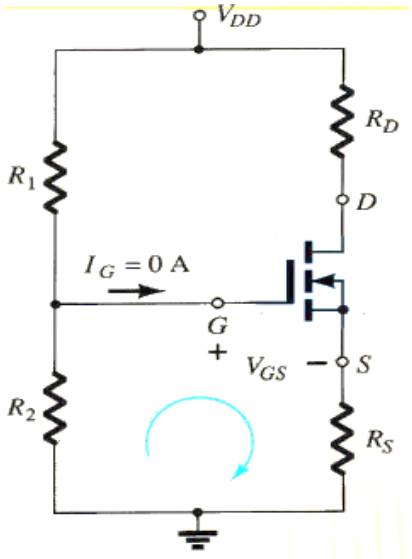


Figure 37. Voltage Divider biasing

- Voltage-divider configuration results in:
- $V_{GS}=V_G-I_DR_S$
- Where $V_G=R_2xV_{DD}/(R_1+R_2$
- $V_{DS}=V_{DD}-I_D(R_S+R_D)$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

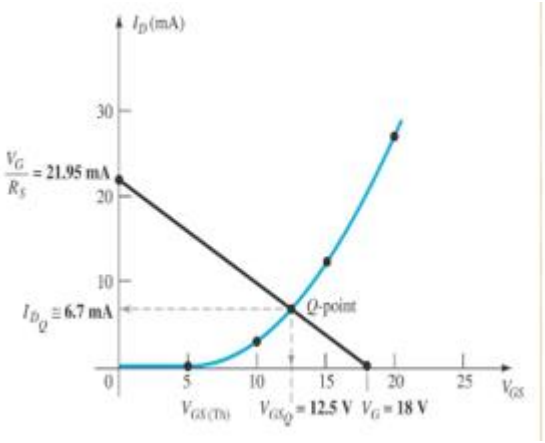


Figure 38. Q point analysis

1. Plot the line using $V_{GS} = V_G = (R_2V_{DD})/(R_1 + R_2)$, $I_D = 0$ and $I_D = V_G/R_S$ and $V_{GS} = 0$
2. Find k
3. Plot the transfer curve using V_{GSTh}, $I_D = 0$ and $V_{GS(on)}$, I_D(on); all given in the specification sheet.
4. Where the line and the transfer curve intersect is the Q-Point.
5. Using the value of I_D at the Q-point, solve for the other variables in the bias circuit.

TWO-PORT NETWORKS

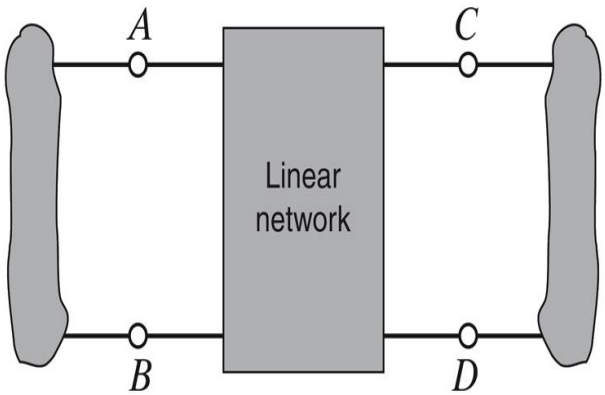


Figure 39. Two port Network

A two-port model is a description of a network that relates voltages and currents at two pairs of terminals. The network contains NO independent sources. Study the basic types of two-port models

- **Admittance parameters**
- **Impedance parameters**
- **Hybrid parameters**
- **Transmission parameters**

TEXT / REFERENCE BOOKS

1. Millman J and Halkias C., "Integrated Electronics", TMH, 2nd Edition, 2017.

2. S. Salivahanan, N. Suresh Kumar and A. Vallavaraj, "Electronic Devices and Circuits", TMH, 2nd Edition, 2017.

3. Donald. A. Neamen, "Electronic Circuits Analysis and Design", McGraw Hill Education (India) Private Ltd., 3rd Edition, 2010.

4. Robert L. Boylestad and Louis Nasheresky, "Electronic Devices and Circuit Theory", Pearson Education, 11th Edition, 2013.

5. Floyd, "Electronic Devices", Pearson Education, 9th Edition, 2012.

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SCHOOL OF ELECTRICAL AND ELECTRONICS

DEPARTMENT OF ELECTRONICS AND COMMMUNICATION ENGINEERING

UNIT - II
ELECTRONIC CIRCUITS-I – SECA1302

Unit 2 EQUIVALENT MODEL OF BJT AMPLIFIERS 9 Hrs

Hybrid model- Analysis of CE, CC and CB amplifiers using Hybrid equivalent circuits to obtain gain, input impedance and output impedance- Approximate Model- Analysis of CE, CC and CB amplifiers using Approximate model equivalent circuits to obtain gain, input impedance and output impedance -Small Signal Amplifiers – Analysis of CE, CC and CB amplifiers using small signal equivalent circuits to obtain gain, input impedance and output impedance.

Hybrid model

Every linear circuit having input and output can be analyzed as two port networks. In these networks there are four parameters called hybrid or h-parameters. Since these parameters have mixed dimension, so they are called hybrid parameters. This equivalent circuit, called Hybrid equivalent circuit or simply h-model, can replace a Thevenin or a Norton equivalent circuit, which both are shown to be two special cases of an h-model. The h-model contains both voltage and current sources and is shown to be very flexible and dynamic.

Benefits of h-parameters.

- **h-parameters are Real Numbers up to radio frequency.**
- **They are easy to measure.**
- **They can be determined from transistor static characteristic curves.**
- **They are convenient to use in circuit analysis and design.**
- **Easily convertible from one configuration to other.**
- **Readily supplied by manufacturers.**

Hybrid parameters or h-parameters are used to determine amplifier characteristic parameters such as voltage gain, input and output resistance etc., h-parameters are easy to measure and the procedure followed to obtain is quite simple and easy to understand

They are real numbers at audio frequencies. They can be easily obtained from the static characteristics of transistor itself. Hybrid model is an equivalent model used in small signal analysis ie. low frequency applications. h stands for hybrid consisting mixed parameters.

Two Port Network:

A pair of terminals through which a current may enter or leave a network is known as port. Every linear circuit is having input and output and can be analyzed as two-port networks. In these networks, there are four parameters called hybrid or h-parameters. Out of these four parameters one is measured in ohms, another is measured in mhos and other two are measured dimensionless. Since these parameters are of mixed dimension, these are called as hybrid parameters

For example, transistors are often regarded as two-ports, characterized by their h-parameters which are listed by the manufacturer. The equivalent circuit of a transistor can be drawn using simple approximation by retaining its essential features. These equivalent circuits will aid in analyzing transistor circuits easily and rapidly. A transistor can be treated as a two-port network. The terminal behavior of any two-port network can be specified by the terminal voltages V1 & V2 at parts 1 & 2 respectively and current i1 and i2, entering parts 1 & 2, respectively, as shown in figure.

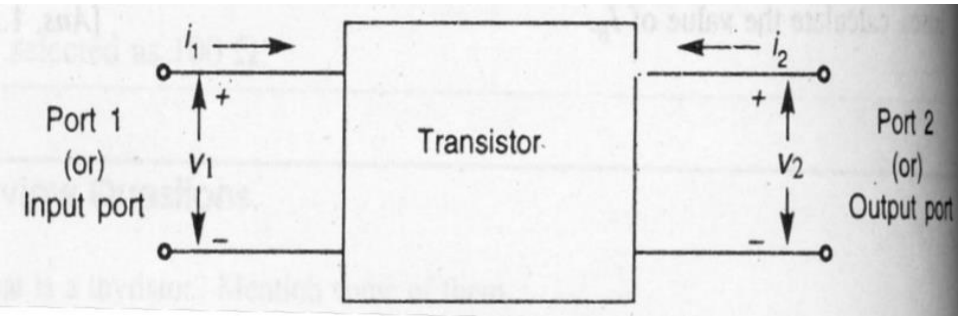

Fig 2.1 Two Port Network

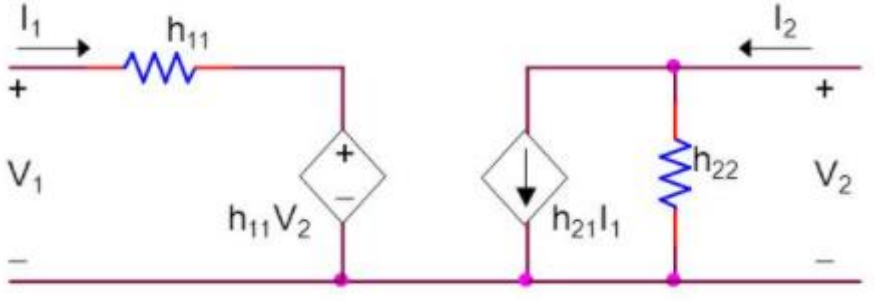

Fig 2.2 Hybrid Model of a Two Port Network

If the input current i1 and output Voltage V2 are takes as independent variables, the input voltage V1 and output current i2 can be written as

$$V_1=h_{11}I_1+h_{12}V_2$$

$$I_2=h_{21}I_1+h_{22}V_2$$

The four h parameters are h11, h12, h21 and h22 are defined as follows.
h11 = [V1 / i1] with V2 = 0 = Input Impedance with output part short circuited
h22 = [i2 / V2] with i1 = 0 = Output admittance with input part open circuited.
h12 = [V1 / V2] with i1 = 0 = reverse voltage transfer ratio with input part open circuited.
h21 = [i2 / i1] with V2 = 0 = Forward current gain with output part short circuited.

The dimensions of h – parameters are as follows: h11 - Ω, h22 – mhos h12, h21 – dimension less. as the dimensions are not alike, (i.e) they are hybrid in nature, and these parameters are called as hybrid parameters.

Table 2.1 h parameter Nomenclature of a transistor

S.No.	*h* parameter	Notation in CB	Notation in CE	Notation in CC
1.	h_{11}	h_{ib}	h_{ie}	h_{ic}
2.	h_{12}	h_{rb}	h_{re}	h_{rc}
3.	h_{21}	h_{fb}	h_{fe}	h_{fc}
4.	h_{22}	h_{ob}	h_{oe}	h_{oc}

Hybrid Analysis of CE

In common emitter transistor configuration, the input signal is applied between the base and emitter terminals of the transistor and output appears between the collector and emitter terminals. The input voltage (Vbe) and the output current (ic) are given by the following equations:

$$Vbe = hie.Ib + hre.Vce$$

$$Ie = hfe.Ib + hoe.Vce$$

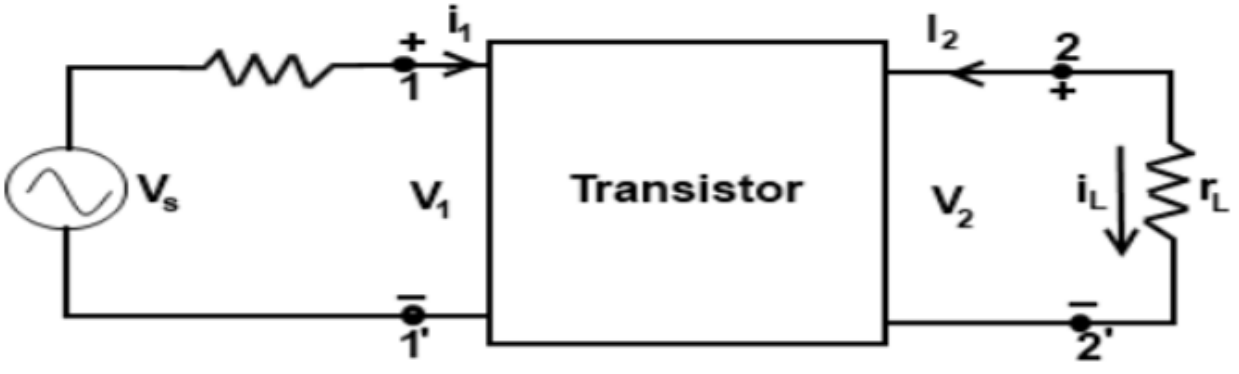

Fig 2.3 General Amplifier Circuit

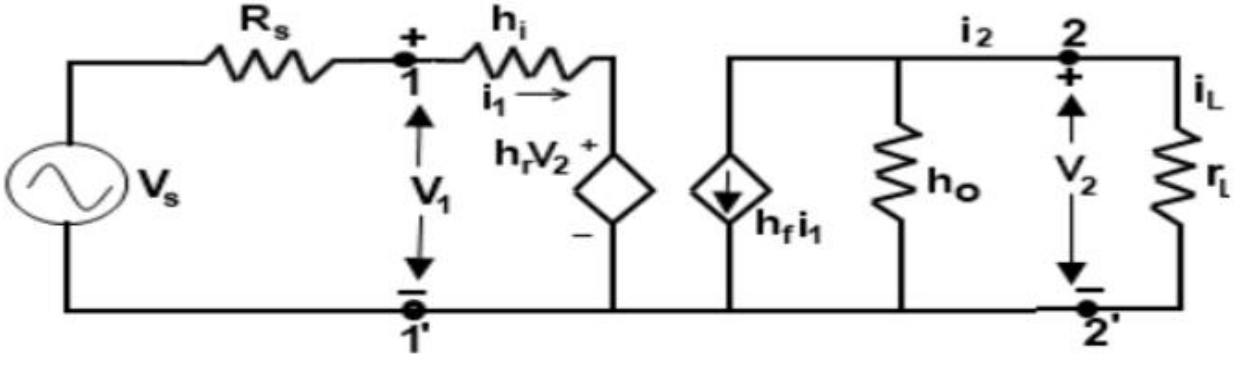

Fig 2.4 Hybrid Model of Amplifier

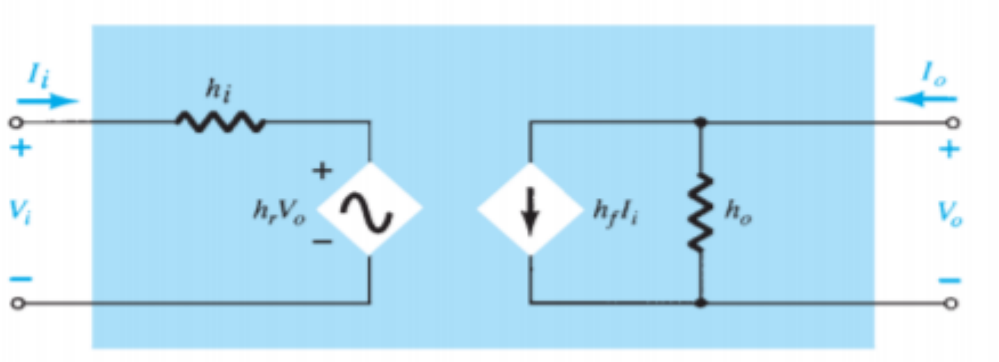

Fig 2.5 Hybrid Model of a Two Port Network

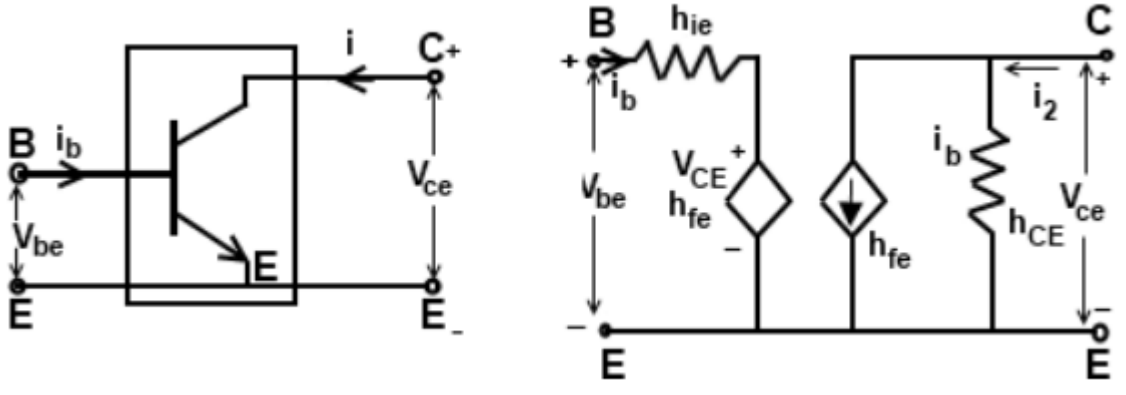

Fig 2.6 Hybrid Model of a Common Emitter BJT

Transistor Circuit Performance in h Parameters

Input Impedance:

The general expression for Input Impedance is

$$Z_{in} = h_{11} - \frac{h_{12}\, h_{21}}{h_{22} + \frac{1}{r_L}}$$

Using standard h parameter, its value for CE will be

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

Current Gain: The general expression for current gain is

$$A_i = \frac{h_{21}}{1 + h_{22}\, r_L}$$

Using standard h parameter, its value for CE will be

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

Voltage Gain: The general expression for voltage gain is

$$A_v = \frac{-h_{21}}{Z_{in}\left(h_{22} + \frac{1}{r_L}\right)}$$

Using standard h parameter, its value for CE will be

$$A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

Output Impedance:

The general expression for Output Impedance is

$$Z_{out} = \frac{1}{h_{22} - \frac{h_{21}\,h_{12}}{h_{11}}}$$

Using standard h parameter, its value for CE will be

$$Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\,h_{re}}{h_{ie}}}$$

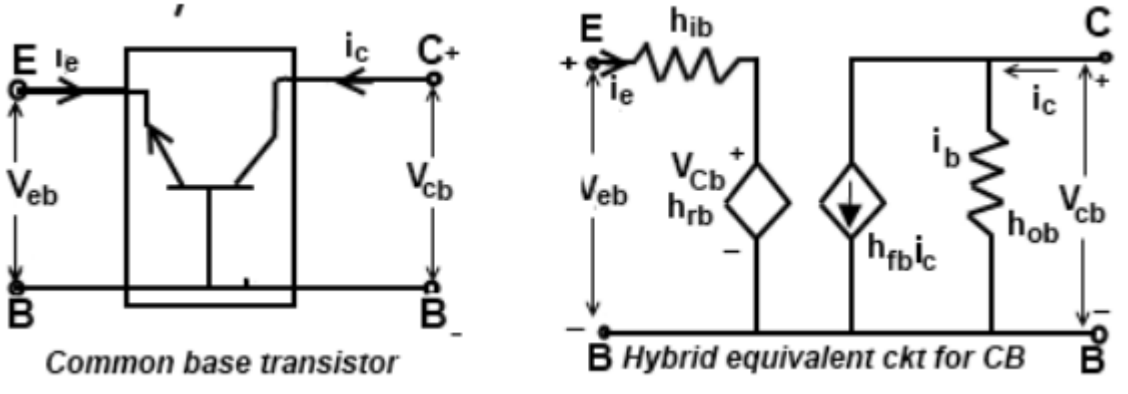

Fig 2.7 Hybrid Model of a Common Base BJT

The Common Collector Amplifier is another type of bipolar junction transistor, (BJT) configuration where the input signal is applied to the base terminal and the output signal taken from the emitter terminal. Thus, the collector terminal is common to both the input and output circuits. This type of configuration is called Common Collector, (CC) because the collector terminal is effectively "grounded" or "earthed" through the power supply. In many ways the common collector configuration (CC) is the reverse of the common emitter (CE) configuration as the connected load resistor is changed from the collector terminal for RC to the emitter terminal for RE.

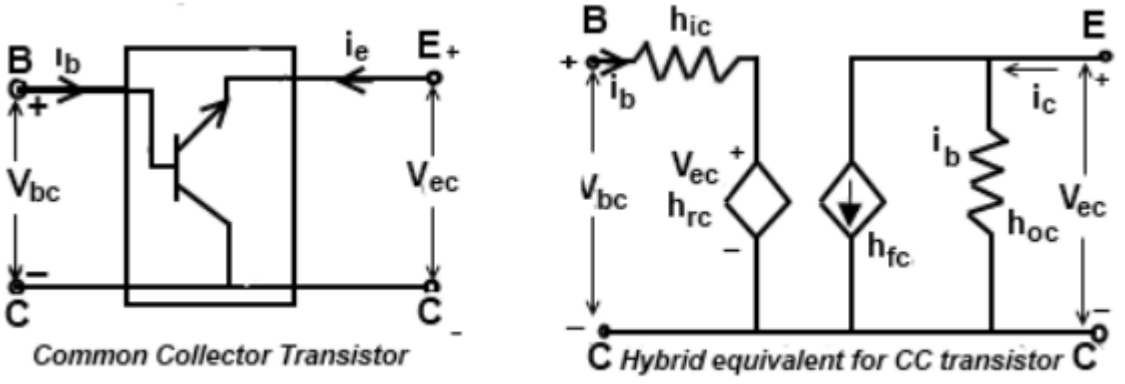

Fig 2.8 Hybrid Model of a Common Collector BJT

Table 2.2 h parameters for transistor configuration

Common Base	Common Emitter	Common Collector	Definitions
$h_{ib} = \frac{v_{eb}}{i_e}$	$h_{ie} = \frac{v_{be}}{i_b}$	$h_{ic} = \frac{v_{bc}}{i_b}$	**Input Impedance with Output Short Circuit**
$h_{rb} = \frac{v_{eb}}{v_{cb}}$	$h_{re} = \frac{v_{be}}{v_{ce}}$	$h_{rc} = \frac{v_{bc}}{v_{ec}}$	**Reverse Voltage Ratio Input Open Circuit**
$h_{fb} = \frac{i_c}{i_e}$	$h_{fe} = \frac{i_c}{i_b}$	$h_{fc} = \frac{i_e}{i_b}$	**Forward Current Gain Output Short Circuit**
$h_{ob} = \frac{i_c}{v_{cb}}$	$h_{oe} = \frac{i_c}{v_{ce}}$	$h_{oc} = \frac{i_e}{v_{ec}}$	**Output Admittance Input Open Circuit**

Approximate Model of Transistors

(*i*) Input impedance

$$\text{Input impedance, } Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

In actual practice, the second term in this expression is very small as compared to the first term.

$$\therefore \quad Z_{in} = h_{ie} \quad \text{... approximate formula}$$

(*ii*) Current gain

$$\text{Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

In actual practice, $h_{oe}\, r_L$ is very small as compared to 1.

$$\therefore \quad A_i = h_{fe} \quad \text{... approximate formula}$$

(*iii*) Voltage gain

$$\text{Voltage gain, } A_v = \frac{-\, h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

$$= \frac{-\, h_{fe}\, r_L}{Z_{in}\,(h_{oe}\, r_L + 1)}$$

Now approximate formula for Z_{in} is h_{ie}. Also $h_{oe}\, r_L$ is very small as compared to 1.

$$\therefore \quad A_v = -\frac{h_{fe}\, r_L}{h_{ie}} \quad \text{... approximate formula}$$

(*iv*) Output impedance

$$\text{Output impedance of transistor, } Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\, h_{re}}{h_{ie}}}$$

The second term in the denominator is very small as compared to h_{oe}.

$$\therefore \quad Z_{out} = \frac{1}{h_{oe}} \quad \text{... approximate formula}$$

The output impedance of transistor amplifier

$$= Z_{out} \| r_L \quad \text{where } {}^{*}r_L = R_C \| R_L$$

If the amplifier is unloaded (*i.e.* $R_L = \infty$), $r_L = R_C$.

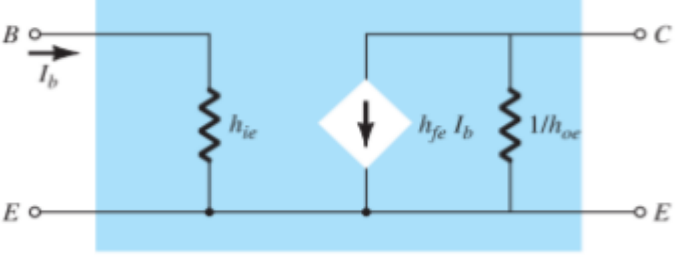

Fig 2.9 Approximate Model of Common Emitter

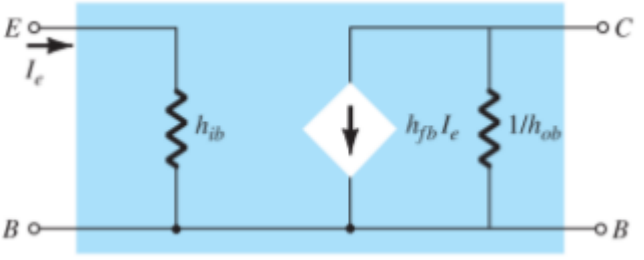

Fig 2.10 Approximate Model of Common Base

Input Impedance

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

By neglecting the reverse voltage gain we have

$$Z_{in} = h_{ie}$$

Current Gain

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

$$A_i = h_{fe}$$

Single Stage Common Emitter Amplifiers:

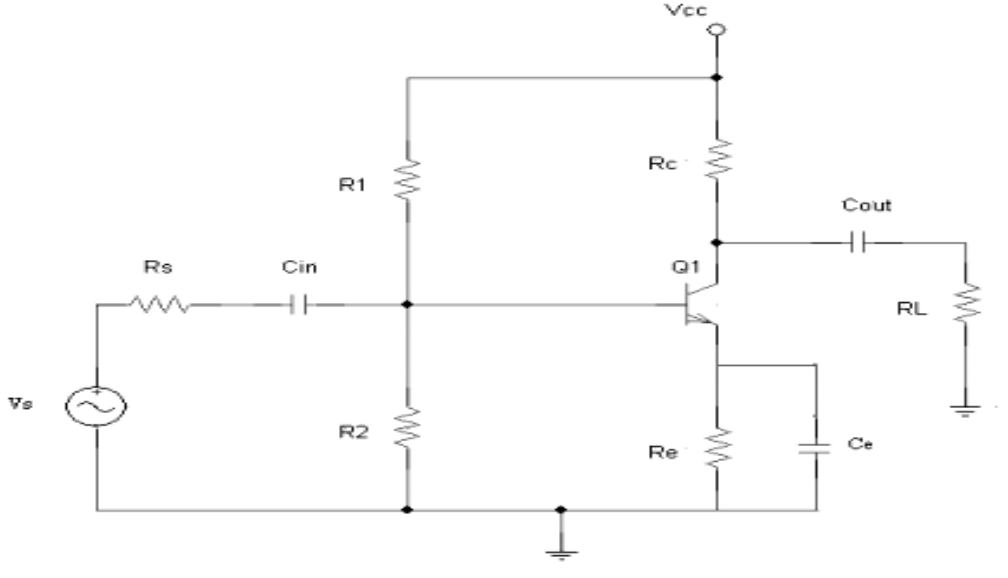

Fig 2.11 Single Stage CE

For the purpose of analysis, we replace the transistor by its h-parameter model. This results in the equivalent circuit, we assume sinusoidal input. Hence in the equivalent circuit, we have used rms value of voltages and currents namely I_b, V_b, I_c and V_c.

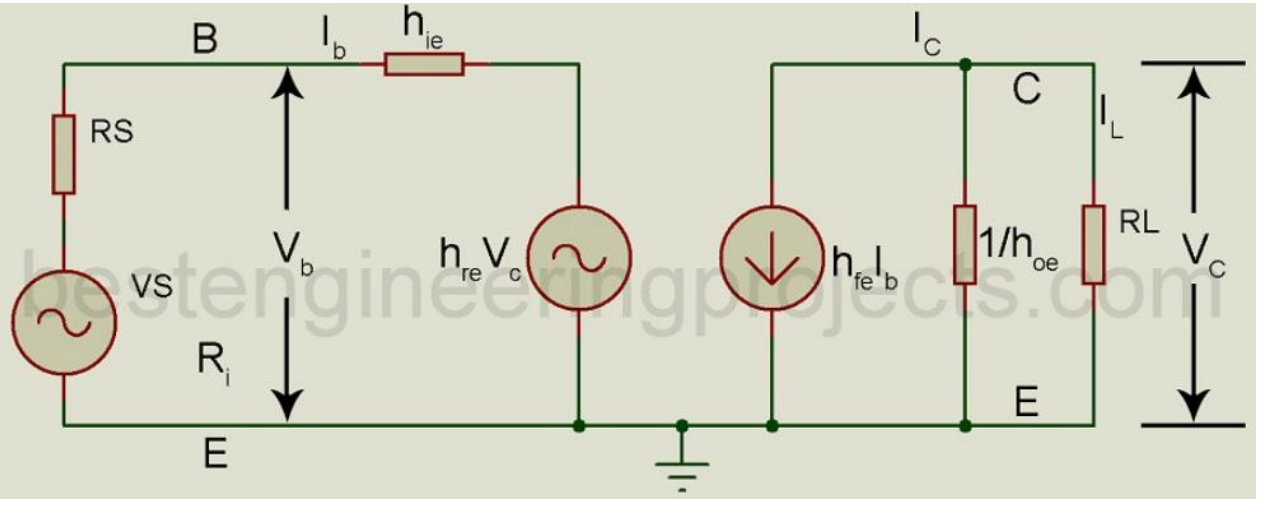

Fig 2.12 Equivalent Model

Current Gain or Current Amplification:

Current gain is defined as the ratio of the load current I_1 to the input current I_b. Thus,

Current Gain $A_I = \frac{I_L}{I_b} = -\frac{I_c}{I_b}$

Also $V_c = I_L \times R_L = -I_c \times R_L$

Combining Equations, we get,

$$I_c = h_{fe}I_b - h_{oe} \times I_c \times R_L or (1 + h_{oe} \times R_L)I_c = h_{fe} \times I_b$$

Hence current gain $A_I = -\frac{I_c}{I_b} = -\frac{h_{fe}}{1 + h_{oe} \times R_L}$

Input Impedance R_i:

This is the impedance between the input terminals B and E looking into the amplifier as

$$R_i = \frac{V_b}{I_b}$$

WKT $V_b = h_{ie} \times I_b + h_{re} \times V_c$

But $V_c = -I_c \times R_L = A_I I_b R_L$

Substituting the value of V_c

$V_b = h_i e \times + h_{re} A_I I_b R_L$

Hence input impedance $R_i = \frac{V_b}{I_b} = h_{ie} + h_{re} A_I R_L$

$= h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + Y_L}$

Where $Y_L = \frac{1}{R_L}$

Voltage Gain or Voltage Amplification:

It is the ratio of the output voltage V_c to the input voltage V_b. Thus,

Voltage Gain $A_v = \frac{V_c}{V_b} = -\frac{I_c R_L}{I_b R_i} = \frac{A_I R_L}{R_i}$

Output impedance $R_0 = \frac{1}{Y_0}$

Output Admittance Y_0:

It is the ratio of the output current I_c to the output voltage V_c with $V_s = 0$. Hence

$Y_0 = \frac{I_c}{V_c}$ **with $V_S = 0$**

On substituting the value of I_c

$Y_0 = h_{fe} \times \frac{I_b}{V_c} + h_{oe}$

But with $V_s = 0$, $(R_s + h_{ie}) I_b + h_{re} V_c = 0$

Or $\frac{I_b}{V_c} = -\frac{h_{re}}{h_{ie} + R_s}$

Combining Equations, we get, $Y_0 = h_{oe} - \frac{h_{fe} \times hre}{h_{ie} + R_s}$

The expression of AI, Ri, AV, Ro are therefore, the same as for CE amplifier except that h-parameter for CB configuration are used. Thus, we get:

Current gain $A_I = -\frac{I_c}{I_e} = -\frac{h_{fb}}{1 + h_{ob} \times R_L}$

Input resistance $R_i = \frac{V_e}{I_e} = h_{ib} - \frac{h_{fb} \times h_{rb}}{h_{ob} + Y_L}$

Where $Y_L = \frac{1}{R_L}$

Voltage Gain $A_V = \frac{V_c}{V_e} = \frac{A_I \times R_L}{R_i}$

Output admittance $Y_0 = \frac{I_c}{V_c} = h_{ob} - \frac{h_{fb} \times h_{rb}}{h_{ib} + R_s}$

Overall voltage gain $A_{VS} = \frac{V_c}{V_s} = A_V \times \frac{R_i}{R_i + R_s}$

Overall current gain $A_{IS} = \frac{I_L}{I_s} = A_I \frac{R_s}{R_i + R_s}$

Power Gain $A_P = \frac{P_L}{P_i} = A_V \times A_I = A_{I2} \times \frac{R_L}{R_i}$

Small Signal Analysis of Common Emitter

- **While Analyzing Small Signal amplifiers we need to draw an equivalent circuit of BJT and that circuit is called Small signal model of BJT**
- **In Small Signal Analysis we can do AC and DC analysis separately**
- **Small-signal analysis assumes that the transistor is correctly biased and concentrates on the linear behavior for small signals**
- **In Active Region the transistor will be showing linear behavior**
- **Small-signal modeling is a common analysis technique in electronics engineering which is used to approximate the behavior of electronic circuits containing nonlinear devices with linear equations**

Small-signal analysis assumes that the transistor is correctly biased and concentrates on the linear behavior for small signals, ignoring the messy non-linear. The DC sources are zeroed, the signal sources are activated, and linear circuit analysis is used to solve for the small-signal voltages and currents. Small ac signal refers to the input signal (V_{be}) whose magnitude is much small than thermal voltage (VT) i.e. V_{be} << V T 3 the transistor operates in the linear region for the whole cycle of input (called as a linear amplifier) the transistor is never driven into saturation or cut-off region on the other hand, if the input signal is too large. The fluctuations along the load line will drive the transistor into either saturation or cut off. This clips the peaks of the input and the amplifier is no longer linear. The hybrid model is suitable for small signals at mid band and describes the action of the transistor. Two equations can be derived from the diagram, one for input voltage V_{be} and one for the output i_c:

$$v_{be} = h_{ie}\, i_b + h_{re}\, v_{ce}$$
$$i_c = h_{fe}\, i_b + h_{oe}\, v_{ce}$$

If i_b is held constant (ib=0) then h_{re} and h_{oe} can be solved:

$$h_{re} = v_{be} / v_{ce} \mid i_b = 0$$
$$h_{oe} = i_c / v_{ce} \mid i_b = 0$$

Also, if v_{ce} is held constant (v_{ce}=0) then h_{ie} and h_{fe} can be solved:

$$h_{ie} = v_{be} / i_b \mid v_{ce} = 0$$
$$h_{fe} = i_c / i_b \mid v_{ce} = 0$$

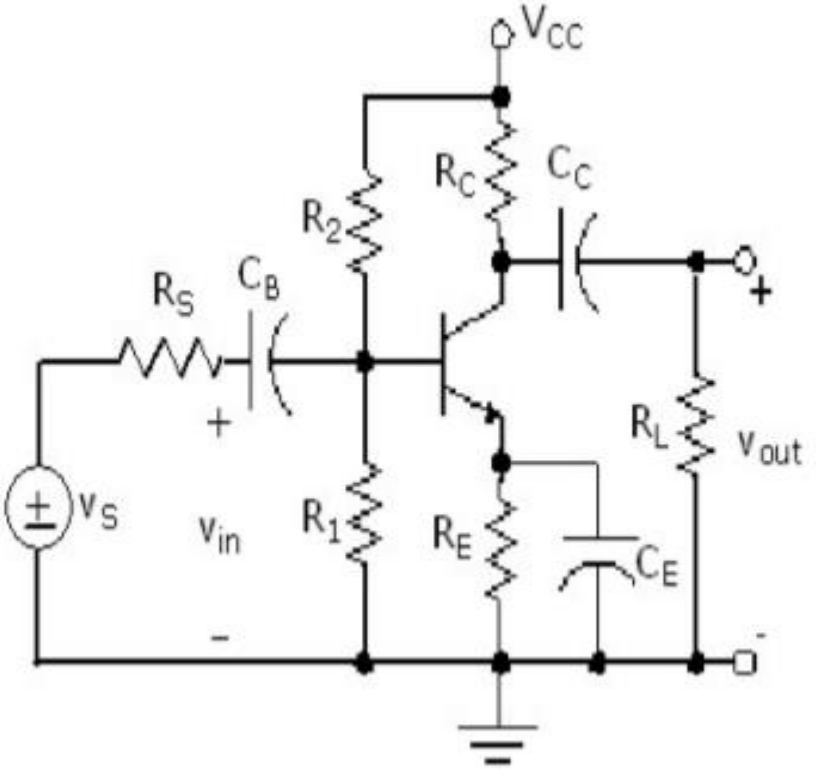

Fig 2.13 Common Emitter

The circuit diagram of a common-emitter (CE) amplifier is shown in Fig 2.13. The capacitor CB is used to couple the input signal to the input port of the amplifier, and CC is used to couple the amplifier output to the load resistor RL. We are interested in the bias currents and voltages, mid-band gain, and input and output resistances of the amplifier.

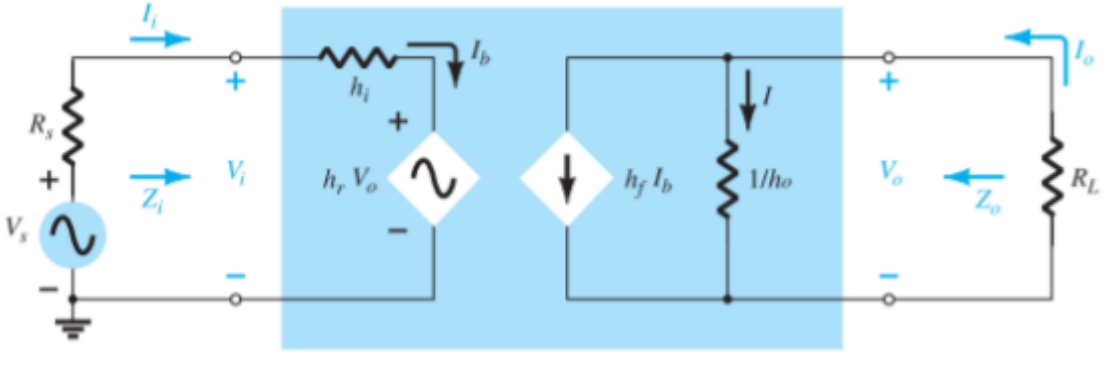

Fig 2.14 Equivalent Model

Current Gain, $A_i = I_o/I_i$

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

so that

$$\boxed{A_i = \frac{I_o}{I_i} = \frac{h_f}{1 + h_o R_L}}$$

Input Impedance, $Z_i = V_i/I_i$

$$V_i = h_i I_i + h_r V_o$$
$$V_o = -I_o R_L$$
$$V_i = h_i I_i - h_r R_L I_o$$
$$A_i = \frac{I_o}{I_i}$$
$$I_o = A_i I_i$$

$$V_i = h_i I_i - h_r R_L A_i I_i$$

$$Z_i = \frac{V_i}{I_i} = h_i - h_r R_L A_i \qquad A_i = \frac{h_f}{1 + h_o R_L}$$

$$\boxed{Z_i = \frac{V_i}{I_i} = h_i - \frac{h_f h_r R_L}{1 + h_o R_L}}$$

Voltage Gain, $A_v = V_o/V_i$

$$V_i = I_i h_i + h_r V_o$$

$$I_i = (1 + h_o R_L) I_o / h_f$$

and $I_o = -V_o / R_L$

$$V_i = \frac{-(1 + h_o R_L) h_i}{h_f R_L} V_o + h_r V_o$$

$$A_v = \frac{V_o}{V_i} = \frac{-h_f R_L}{h_i + (h_i h_o - h_f h_r) R_L}$$

Output Impedance, $Z_o = V_o/I_o$

$$V_s = 0$$

$$I_i = -\frac{h_r V_o}{R_s + h_i}$$

$$I_o = h_f I_i + h_o V_o$$

$$= -\frac{h_f h_r V_o}{R_s + h_i} + h_o V_o$$

$$Z_o = \frac{V_o}{I_o} = \frac{1}{h_o - [h_f h_r / (h_i + R_s)]}$$

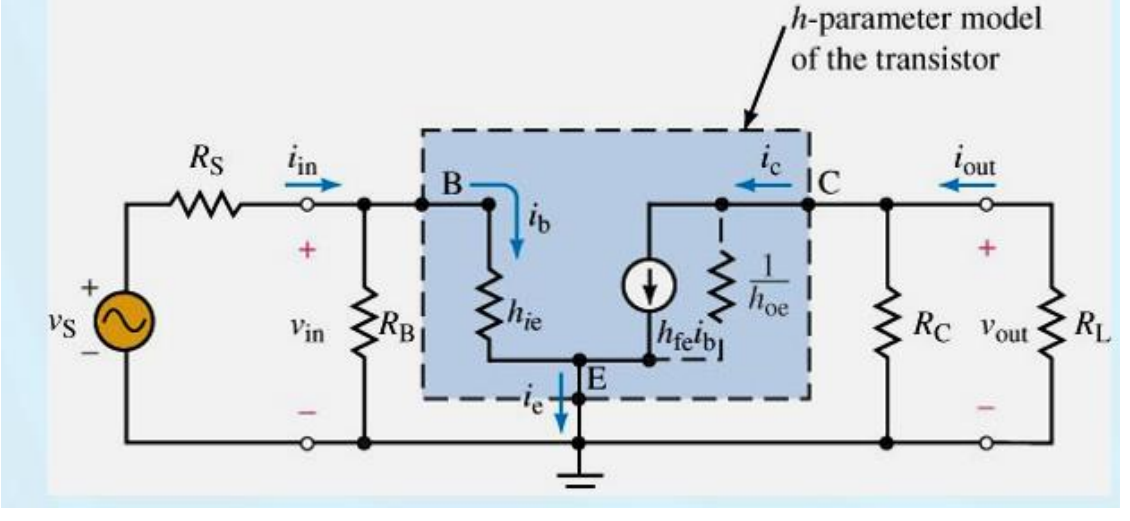

Fig 2.15 Small Signal Common Emitter

$$A_v = -\frac{h_{fe}\left(R_C \| R_L\right)}{h_{ie}}$$

$$A_i = \frac{h_{fe} R_B R_C}{\left(R_C + R_L\right)\left(R_B + h_{ie}\right)}$$

Zi=Rb||hie

Zo=Rc||RL

Small Signal Common Base:

The CB ac equivalent circuit is drawn, as always, by replacing the supply voltage and capacitors with short circuits. This gives the circuit in Fig. 6-36(a), which shows that the transistor base terminal (grounded via capacitor C1) is common to both input and output. Hence the name common base. The CB h-parameter circuit is now drawn by substituting the transistor h-parameter model into the ac equivalent circuit, giving the circuit in Fig. 6-36(b). Once again, the current directions and voltage polarities indicated in the h-parameter circuit are those produced by a positive-going signal voltage. Note that the feedback voltage generator (hrb vo) is not included in the CB h-parameter circuit. This is because the feedback voltage effect is so small that it can be neglected when deriving practical approximate equations for the circuit performance. This corresponds with the CE h-parameter circuit, but not with the CC h-parameter circuit, where the feedback voltage is very important.

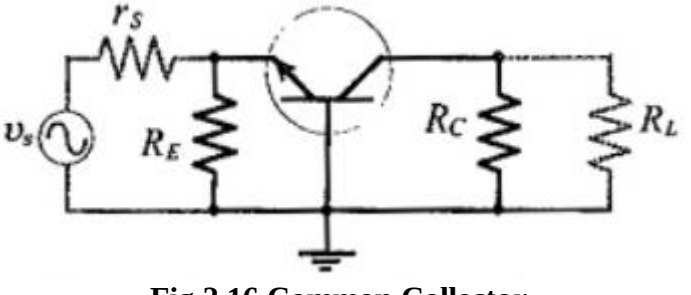

Fig 2.16 Common Collector

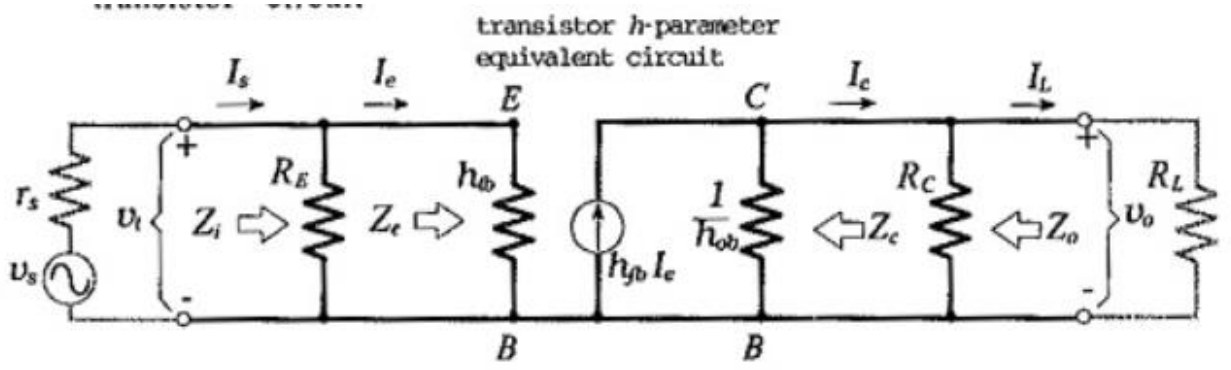

Fig 2.17 Common Collector Equivalent Circuit

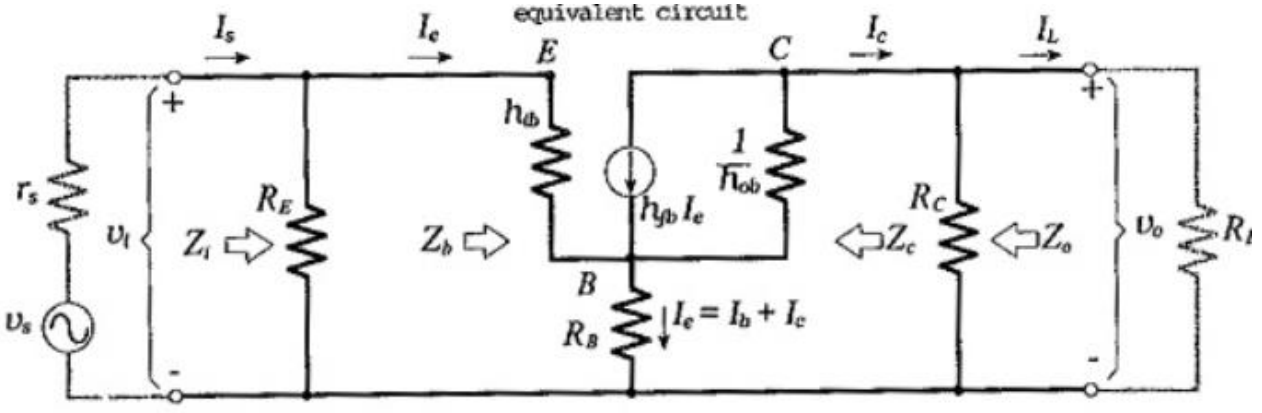

Fig 2.18 Simplified Equivalent Model

$$Z_e = h_{ib}$$

$$Z_i = Z_e \| R_E$$

$$Z_c = \frac{1}{h_{ob}}$$

$$Z_o \approx R_c$$

$$A_v = \frac{h_{fb}(R_C \| R_L)}{h_{ib}}$$

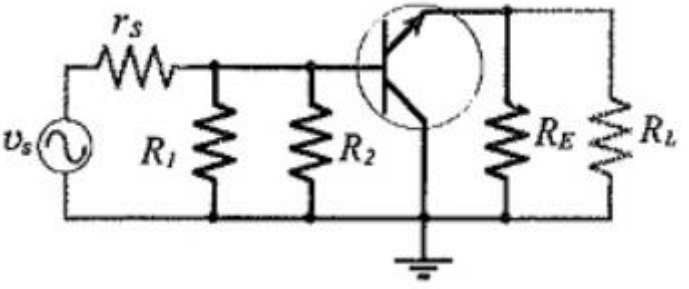

Fig 2.19 Common Collector Circuit

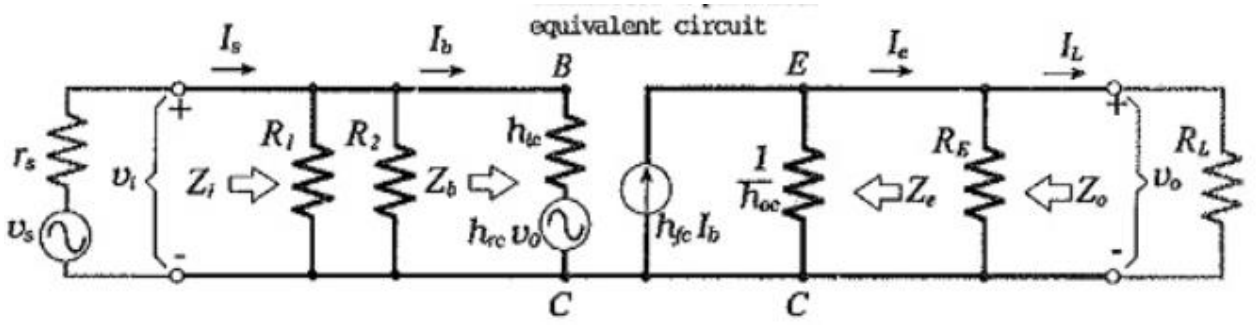

Fig 2.20 Equivalent Circuit

$$Z_b = h_{ic} + h_{fc}(R_E \| R_L)$$

$$Z_i \approx R_B \| Z_b = R_1 \| R_2 \| Z_b$$

$$Z_e = \frac{h_{ic} + (R_1 \| R_2 \| r_s)}{h_{fc}}$$

$$Z_o = Z_e \| R_E$$

$$A_v = \frac{(R_E \| R_L)}{h_{ib} + (R_E \| R_L)} \approx 1$$

Table 2.3 BJT Characteristics

Characteristic	Common base (CB)	Common emitter, (CE)	Common collector, (CC)
Input Dynamic Resistance	Very Low (less than 100 ohm)	Low (less than 1K)	Very High(750K)
Output Dynamic Resistance	Very High	High	Low
Current Gain	Less than 1	High	Very High
Voltage gain	Greater than CC but less than CE	Highest	Lowest (less than 1)
Power gain	Medium	Highest	Medium
Leakage current	Very small	Very large	Very large
Relationship between I/p and o/p	In phase	Out of phase(180º)	In phase

Application	**For High freq. applications**	**For Audio freq. Applications**	**For impedance Matching Applications**

References:

1. **Millman J and Halkias C., "Integrated Electronics", TMH, 2nd Edition, 2017.**
2. **S. Salivahanan, N. Suresh Kumar and A. Vallavaraj, "Electronic Devices and Circuits", TMH, 2nd Edition, 2017.**
3. **Donald. A. Neamen, "Electronic Circuits Analysis and Design", McGraw Hill Education (India) Private Ltd., 3rd Edition, 2010.**
4. **Robert L. Boylestad and Louis Nasheresky," Electronic Devices and Circuit Theory", Pearson Education, 11th Edition, 2013.**
5. **Floyd, "Electronic Devices", Pearson Education, 9th Edition, 2012.**

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UNIT-III

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UNIT 3 EQUIVALENT MODEL OF FET AND MOSFET AMPLIFIERS 9 Hrs

Small Signal equivalent circuit of FET and MOSFET - Analysis of CS, CD and CG JFET amplifiers using small signal equivalent circuits- Analysis of CS, CD and CG MOSFET amplifiers using small signal equivalent circuits

Small Signal FET Models

The small-signal FET *model (valid both for JFET and MOSFET) is used to relate small changes in FET current and voltages about the quiescent operating point. The model is different at low and high-frequencies. Therefore we shall study the small-signal models separately as the low-frequency FET model and high-frequency model. In both these models, the FET will be considered in common source configuration.

Small Signal Low-Frequency FET Model

FET SMALL SIGNAL ANALYSIS

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a current-controlled device and the FET is a voltage-controlled device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor (beta), the FET has a transconductance factor, gm.

FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

While the common-source configuration is the most popular, providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 A and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuit

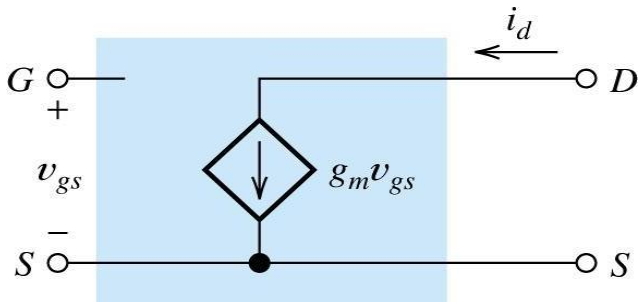


Fig. 3.1 Small signal model of FET

COMMON SOURCE AMPLIFIER

A common-source JFET amplifier is one in which the ac input signal is applied to the gate and the ac output signal is taken from the drain. The source terminal is common to both the input and output signal. A common-source amplifier either has no source resistor or has a bypassed source resistor, so the source is connected to ac ground. A self-biased common-source n-channel JFET amplifier with an ac source capacitive coupled to the gate is shown in Figure below. The resistor, RG, serves two purposes: It keeps the gate at approximately 0 V dc (because IGSS is extremely small), and its large value (usually several megohms) prevents loading of the ac signal source. A bias voltage is produced by the drop across RS. The bypass capacitor, C2, keeps the source of the JFET at ac ground.

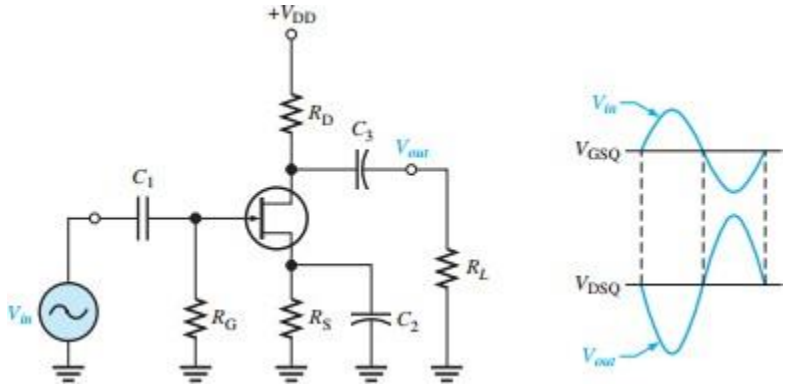


Fig.3.2 Self biased Common source Amplifier

The input signal voltage causes the gate-to-source voltage to swing above and below its Q-point value (VGSQ), causing a corresponding swing in drain current. As the drain current increases, the voltage drop across RD also increases, causing the drain voltage to decrease. The drain current swings above and below its Q-point value in phase with the

gate-to-source voltage. The drain-to-source voltage swings above and below its Q-point value (VDSQ) and is 180° out of phase with the gate-to-source voltage, as illustrated in Figure above. A Graphical Picture The operation just described for an n-channel JFET is illustrated graphically on both the transfer characteristic curve and the drain characteristic curve in Figure below. Part (a) shows how a sinusoidal variation, Vgs, produces a corresponding sinusoidal variation in Id. As Vgs swings from its Q-point value to a more negative value, Id decreases from its Q- point value. As Vgs swings to a less negative value, Id increases. The signal at the gate drives the drain current above and below the Q-point on the load line, as indicated by the arrows. Lines projected from the peaks of the gate voltage across to the ID axis and down to the VDS axis indicate the peak-to-peak variations of the drain current and drain-to-source voltage, as shown. Because the transfer characteristic curve is nonlinear, the output will have some distortion. This can be minimized if the signal swings over a limited portion of the load line.

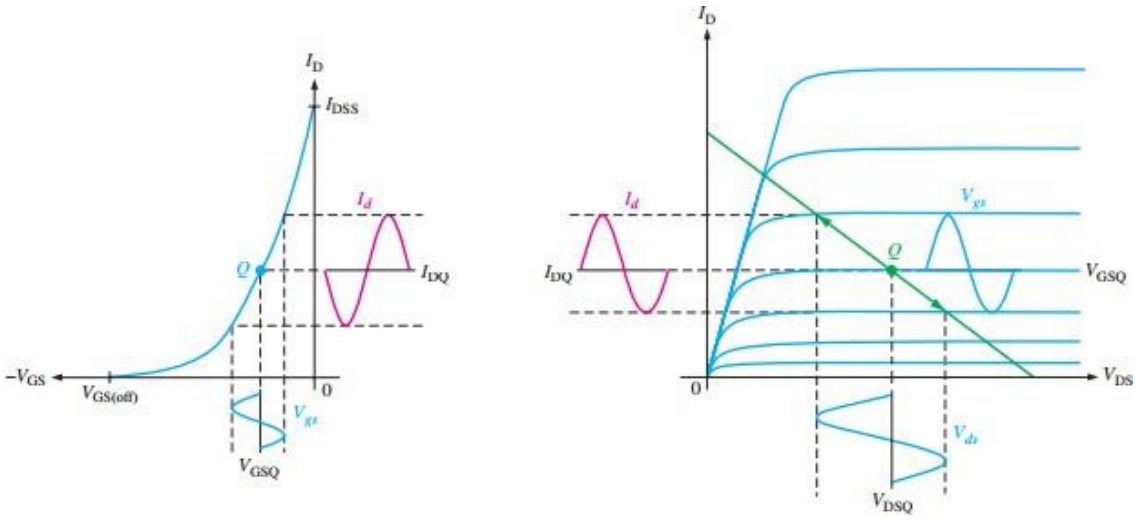


Fig 3.3 Transfer Characteristic curve and Drain curve for Common source JFET Amplifier

AC Equivalent Circuit to analyze the signal operation of the amplifier in Figure below ,an ac equivalent circuit is as follows. Replace the capacitors by effective shorts, based on the simplifying assumption that at the signal frequency. Replace the dc source by a ground, based on the assumption that the voltage source has a zero internal resistance. The VDD terminal is at a zero-volt ac potential and therefore acts as an ac ground.

The ac equivalent circuit is shown in Figure below. Notice that the VDD end of Rd and the source terminal are both effectively at ac ground. Recall that in ac analysis, the ac ground and the actual circuit ground are treated as the same point.

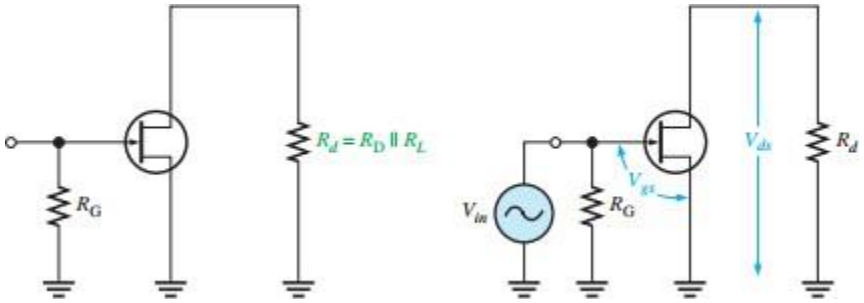


Fig 3.4 AC equivalent circuit for Common source amplifier

An ac voltage source is shown connected to the input in Figure above. Since the input resistance to a JFET is extremely high, practically all of the input voltage from the signal source appears at the gate with very little voltage dropped across the internal source resistance. Vgs = Vin

Vgs = Vin

Voltage Gain: The expression for JFET voltage gain that was given in Equation below applies to the common-source amplifier.

$$A_v = g_m R_d$$

Phase Inversion The output voltage (at the drain) is out of phase with the input voltage (at the gate). The phase inversion can be designated by a negative voltage gain, Recall that the common-emitter BJT amplifier also exhibited a phase inversion.

Input Resistance is derived as follows, because the input to a common-source amplifier is at the gate, the input resistance is extremely high. Ideally, it approaches infinity and can be neglected. As you know, the high input resistance is produced by the reverse-biased PN junction in a JFET and by the insulated gate structure in a MOSFET. The actual input resistance seen by the signal source is, the gate-to-ground resistor, RG, in parallel with the FET's input resistance, VGS IGSS. The reverse leakage current, IGSS, is typically given on the datasheet for a specific value of VGS so that the input resistance of the device can be calculated.

$$R_{in} = R_G \| \left(\frac{V_{GS}}{I_{GSS}}\right)$$

Common drain JFET amplifier

A common-drain JFET amplifier is one in which the input signal is applied to the gate and the output is taken from the source, making the drain common to both. Because it is common, there is no need for a drain resistor. A common-drain JFET amplifier is shown in Figure below. A common-drain amplifier is also called a source-follower. Self-biasing is used in this particular circuit. The input signal is applied to the gate through a coupling capacitor, C1, and the output signal is coupled to the load resistor through C2.

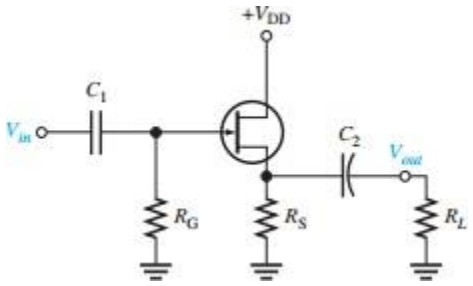


Fig. 3.5 Self biased Common Drain Amplifier

Voltage Gain as in all amplifiers, the voltage gain is Av Vout / Vin. For the source-follower, Vout is IdRs and Vin is Vgs IdRs as shown in above Figure. Therefore, the gate-to-source voltage gain is IdRs (Vgs IdRs). Substituting Id gmVgs into the expression gives the following result:

$$A_V = \frac{g_m v_{gs} R_s}{v_{gs} + g_m v_{gs} R_s}$$

The vgs term cancel so,

$$A_V = \frac{g_m R_s}{1 + g_m R_s}$$

Notice here that the gain is always slightly less than 1. If then a good approximation is since the output voltage is at the source, it is in phase with the gate (input) voltage.

Input Resistance because the input signal is applied to the gate, the input resistance seen by the input signal source is extremely high, just as in the common-source amplifier configuration. The gate resistor, RG, in parallel with the input resistance looking in at the gate is the total input resistance.

$$R_{in} = R_G \,||R_{IN(gate)}$$

where

$$R_{IN(gate)} = V_{GS} \,||I_{GSS}$$

Common Gate Amplifier

The common-gate FET amplifier configuration is comparable to the common-base BJT amplifier. Like the CB, the common-gate (CG) amplifier has a low input resistance. This is different from the CS and CD configurations, which have very high input resistances

Common-Gate Amplifier Operation A self-biased common-gate amplifier is shown in figure. The gate is connected directly to ground. The input signal is applied at the source terminal through C1. The output is coupled through C2 from the drain terminal.

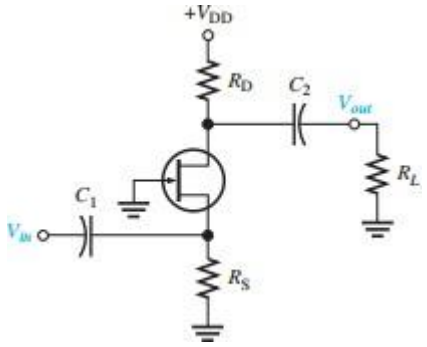


Fig 3.6 Common Gate Amplifier

Voltage Gain: The voltage gain from source to drain is developed as follows:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{V_d}{V_{gs}} = \frac{I_d\, R_d}{V_{gs}} = \frac{g_m\, V_{gs}\, R_d}{V_{gs}}$$

$$A_v = g_m R_d$$

Where Rd = RD || RL. Notice that the gain expression is the same as for the common-source JFET amplifier.

Input Resistance: As you have seen, both the common-source and common-drain configurations have extremely high input resistances because the gate is the input terminal. In contrast, the common-gate configuration where the source is the input terminal has a low input resistance. This is shown as follows. First, the input current is equal to the drain current

$$I_{in} = I_s = I_d = g_m\, V_{gs}$$

Second, the input voltage equals Vgs.

$$V_{in} = V_{gs}$$

Therefore, the input resistance at the source terminal is

$$R_{in} = \frac{V_{in}}{I_{in}} = \frac{V_{gs}}{g_m V_{gs}}$$

$$R_{in} = \frac{1}{g_m}$$

Small signal analysis of MOSFET:

Common Source configuration of E- MOSFET with potential divider biasing:

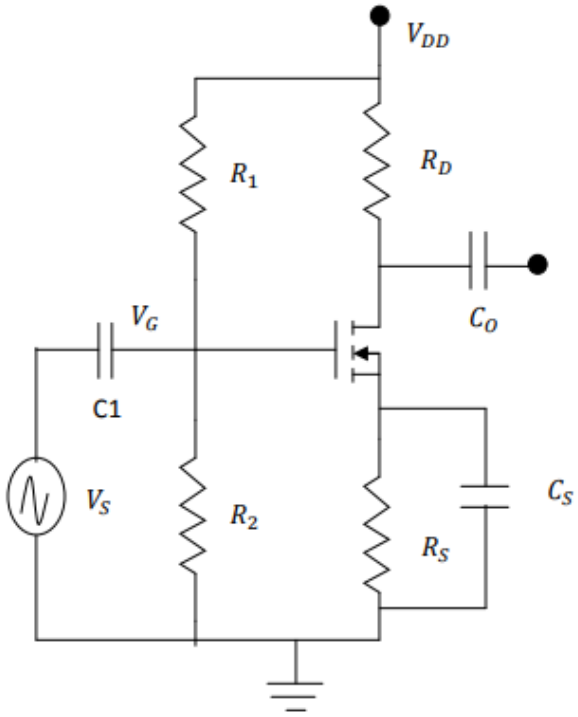
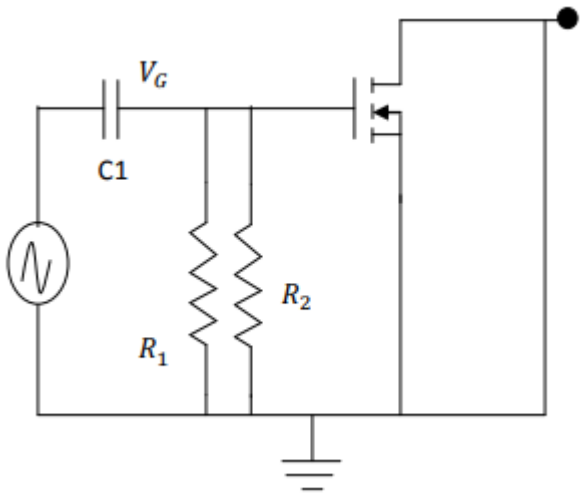


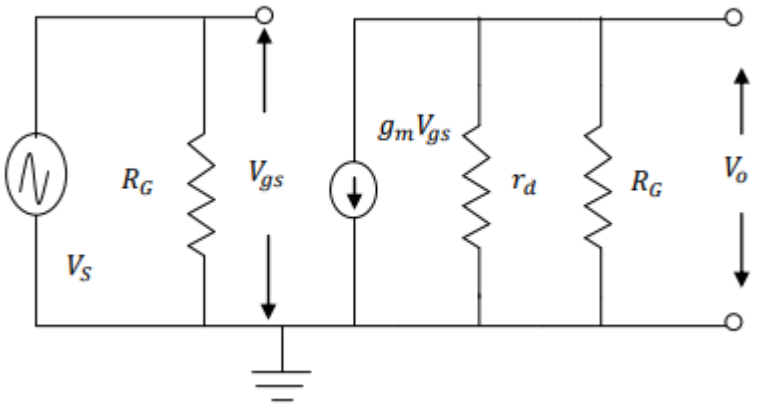
Fig 3.7 Circuit Diagram of common source amplifier



3.8 AC equivalent circuit

In common source configuration of E-MOSFET, the inputs is fed to the gate and output is taken at the drain. The resistor R_1 and R_2 acts as biasing resistors. For AC analysis the source is connected to ground and hence source terminal is connected to both input and output.

The circuit diagram of voltage-divider bias for E-MOSFET is shown in the above Figure 3.7. The AC equivalent model of the voltage–divider bias circuit of E-MOSFET can be obtained by shorting the capacitors and grounding the biasing sources as shown in the above figure. Replacing the devices by its small signal model, we get the figure shown below.



3.9 Small signal equivalent circuit for common source amplifier

Input impedance:

Input impedance is the resistance looking back from the input terminal. From the small signal signal model of voltage divider configuration of E-MOSFET shown in the above figure 3.9, the input impedance can be calculated as

$$Z_i = R_1 \,||R_2$$

Output impedance:

Output impedance is the resistance looking back from the output terminal. From the small signal; model of MOSFET, The output impedance is calculated as follows,

$$Z_o = R_D \,||\, r_d$$

When Vi = 0, gate-source voltage = 0, Therefore, is an open circuit. Hence the output impedance is equal to drain resistance.

Therefore, the output impedance is given by,

$$Z_o = R_D$$

Voltage gain:

Voltage gain is the ratio of output voltage to input voltage.

$$A_V = \frac{V_o}{V_i}$$

$$V_o = I_O(R_D \,||\, r_d) = I_D(R_D \,||\, r_d)$$

Where, $I_D = g_m V_{gs}$

Therefore,

$$A_V = \frac{V_o}{V_i} = -g_m R_D$$

Common Drain Amplifier:

The circuit diagram and the small signal diagram are as follows:

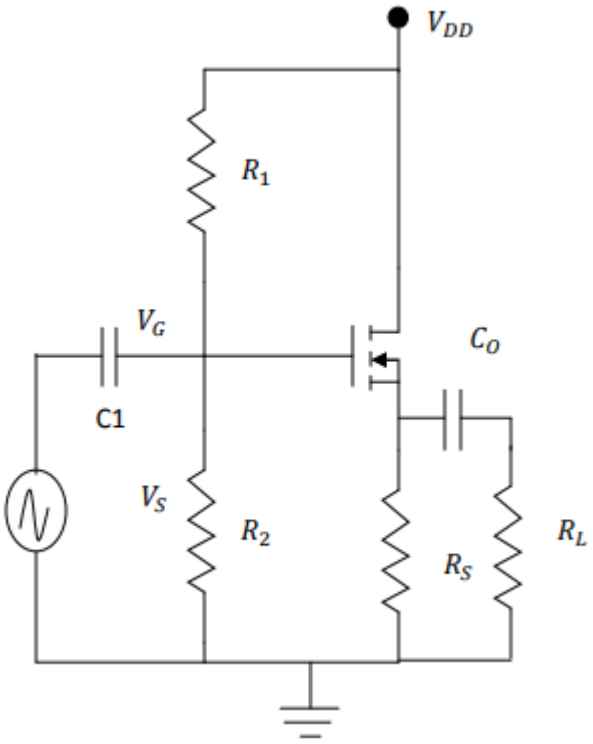


Fig.3.10 Circuit Diagram of Common Drain Amplifier

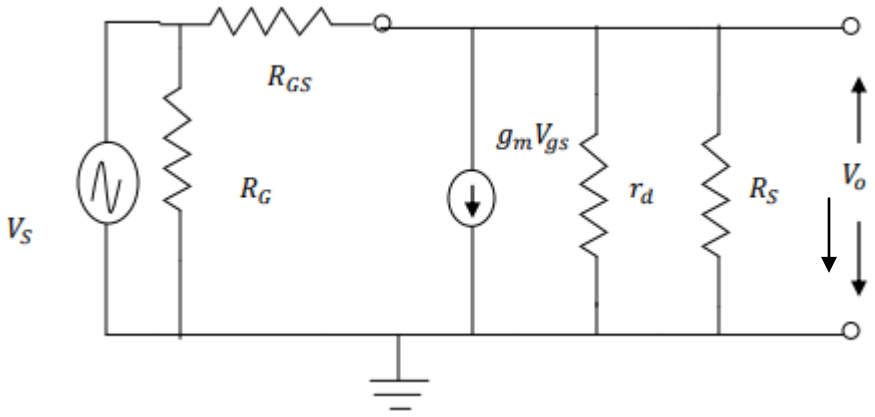


Fig 3.11 Small signal model of common drain amplifier

Input Impedance is given by,

$$Z_g = R_{GS}[1 + g_m(R_S || R_L)];$$

Therefore,

$$Z_i = R_G || Z_g$$

The output impedance is

$$Z_O = R_S || (1/g_m)$$

Voltage Gain is,

$$A_v = 1$$

Common Gate Amplifier:

The circuit diagram and the small signal model are given below:

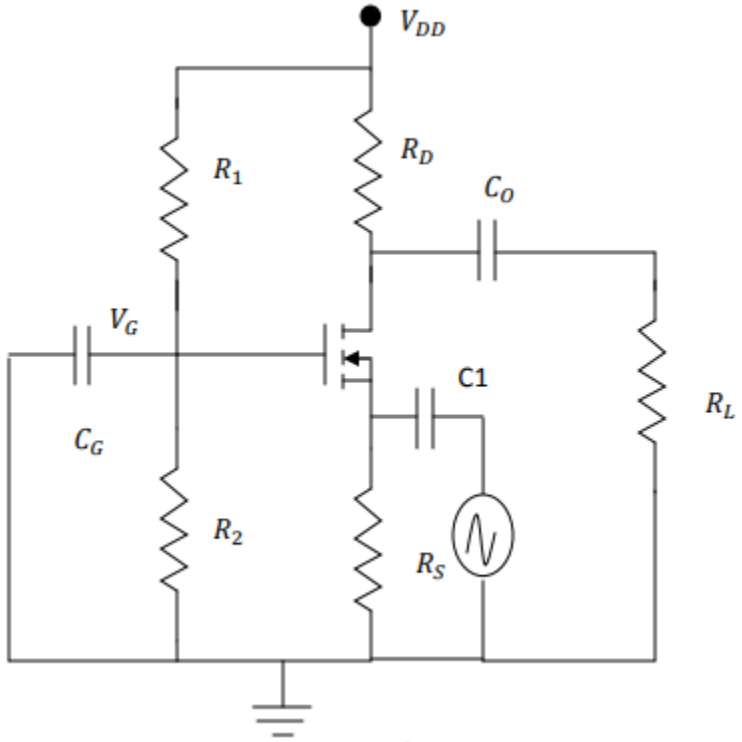


Fig.3.12 Circuit Diagram of mall signal model of common gate amplifier

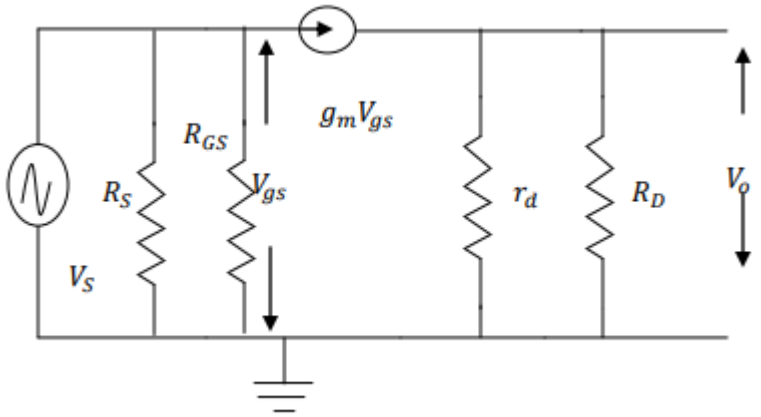


Fig. 3.13 Small signal model of common gate amplifier

Input Impedance,

$$Z_i = R_S || 1/g_m$$

Output Impedance,

$$Z_O = R_D || r_d$$

Voltage Gain,

$$A_V = \frac{V_o}{V_i} = g_m(R_D || r_d || R_L)$$

JFET and MOSFET small signal model Amplifiers || Review

It provides an excellent voltage gain with high input impedance. Due to these characteristics, it is often preferred over BJT.

Three basic FET configurations

Common source, common drain and common gate

1. MOSFET low frequency a.c Equivalent circuit

Figure shows the small signal low frequency a.c Equivalent circuit for n-channel JFET.

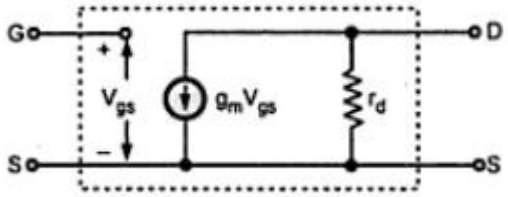


Fig. 3.13 Small signal model of JFET

Common Source Amplifier with Fixed Bias

Figure shows Common Source Amplifier with Fixed Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis.

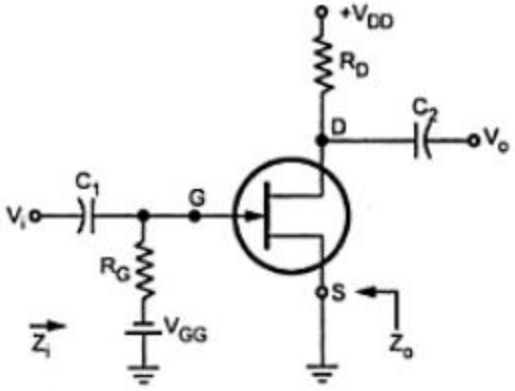


Fig. 3.14 Common Source Circuit of JFET

The following figure shows the low frequency equivalent model for Common Source Amplifier With Fixed Bias. It is drawn by replacing

All capacitors and d.c supply voltages with short circuit

JFET with its low frequency a.c Equivalent circuit

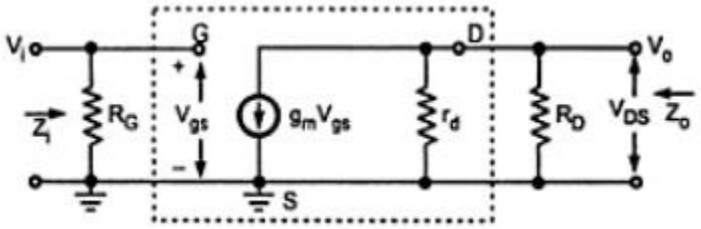


Fig. 3.15 Small Signal Model of CS MOSFET Amplifier

Input Impedance Zi

Zi = RG

Output Impedance Zo

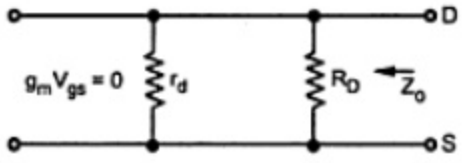


Fig. 3.16 Equivalent circuit Model of MOSFET for output

It is the impedance measured looking from the output side with input voltage Vi equal to Zero.

As Vi=0,Vgs =0 and hence gmVgs =0 . And it allows current source to be replaced by an open circuit.

$$Z_o = R_D \,||\, r_d$$

If the resistance rd is sufficiently large compared to RD, then

$$Z_o \approx R_D \qquad \because r_d >> R_D$$

Voltage Gain A_v :

The voltage gain $A_v = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$

Looking at Fig. we can write

$$V_o = -g_m V_{gs} \; (r_d \,||\, R_D)$$

As we know $V_i = V_{gs}$ we can write

$$V_o = -g_m V_i \; (r_d \,||\, R_D)$$

$$\therefore \quad A_v = \frac{V_o}{V_i} = -g_m \; (r_d \,||\, R_D)$$

and if $r_d >> R_D$,

$$A_v \approx -g_m R_D$$

Table summarizes performance of common source amplifier with fixed bias.

Parameter	Exact	With $r_d >> R_D$
Z_i	R_G	R_G
Z_o	$R_D \| r_d$	R_D
A_v	$-g_m (R_D \| r_d)$	$-g_m R_D$

2. Common source amplifier with self bias(Bypassed Rs)

Figure shows Common Source Amplifier With self Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

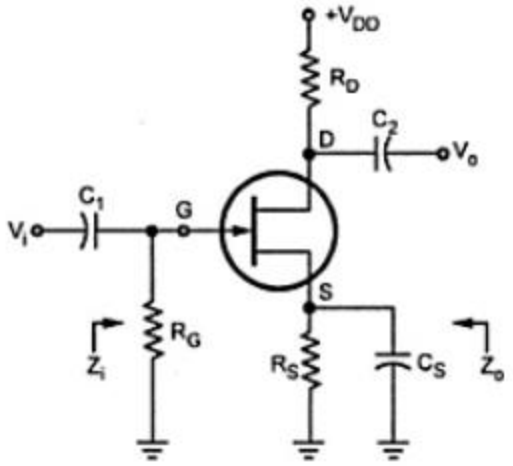


Fig. 3.17 Common Source amplifier model of MOSFET

The following figure 3.18 shows the low frequency equivalent model for Common Source Amplifier with self Bias.

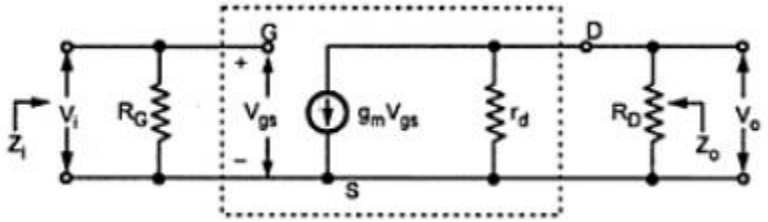


Fig.3.18.Small signal model for Common Source MOSFET

i) Input impedance Z_i :	$Z_i = R_G$
ii) Output impedance Z_o :	$Z_o = r_d \,\|\|\, R_D$
if $r_d >> R_D$	$Z_o \approx R_D$
iii) Voltage gain A_v :	$A_v = -g_m (r_d \,\|\|\, R_D)$
If $r_d >> R_D$	$A_v = -g_m R_D$

The negative sign in the voltage gain indicates there is a 180o phase shift between input and output voltages.

Common source amplifier with self bias (unbypassed Rs)

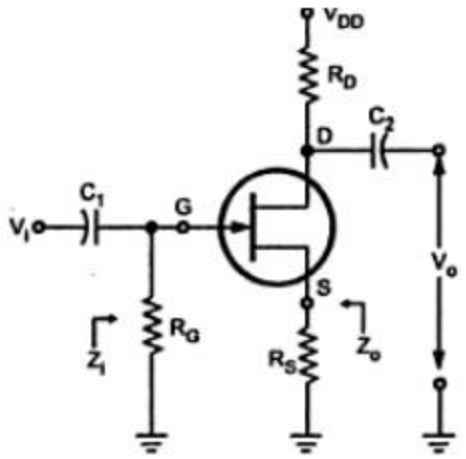


Fig.3.19. Common Source MOSFET amplifier

Now Rs will be the part of low frequency equivalent model as shown in figure. 3.19.

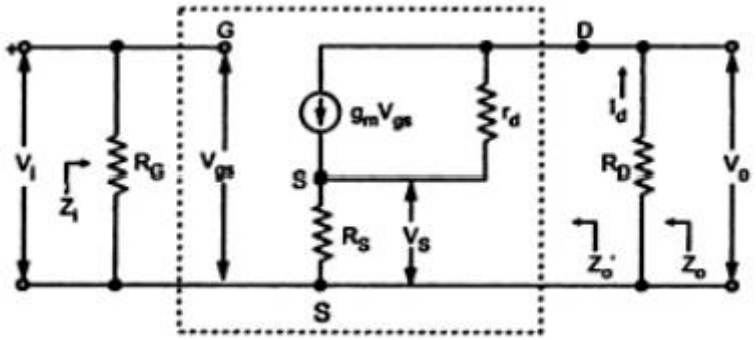


Fig.3.20. Small signal model for Common Source MOSFET amplifier

Input Impedance Zi

Zi = RG

Output Impedance Zo

It is given by

$$Z_o = Z_o' \| R_D$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

$$Z_o = [\, r_d + R_s\,(\mu + 1)\,] \| R_D$$

$$Z_o = [\, r_d + R_s\,(g_m\, r_d + 1)\,] \| R_D$$

Voltage gain (Av)
It is given by

$$A_v = \frac{V_o}{V_i}$$

We know that,

$$V_o = -I_d R_D$$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m r_d R_D}{r_d + R_s + R_D + g_m R_s r_d}$$

Dividing numerator and denominator by r_d we get,

$$\therefore \quad A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}}$$

If $r_d >> R_s + R_D$

$$A_v = \frac{V_o}{V_i} = \frac{-g_m R_D}{1 + g_m R_s}$$

Parameter	Bypassed R_S		Unbypassed R_S	
	Exact	$r_d >> R_D$	Exact	$r_d >> R_D$
Z_i	R_G	R_G	R_G	R_G
Z_o	$R_D \parallel r_d$	R_D	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$	$[r_d + R_S(g_m r_d + 1)] \parallel R_D$ or $[r_d + R_S(\mu + 1)] \parallel R_D$
A_v	$-g_m(R_D \parallel r_d)$	$-g_m R_D$	$\frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}}$	$\frac{-g_m R_D}{1 + g_m R_S}$

Common source amplifier with Voltage divider bias (Bypassed Rs)

Figure shows Common Source Amplifier With voltage divider Bias. The coupling capacitor C1 and C2 which are used to isolate the d.c biasing from the applied ac signal act as short circuits for ac analysis. Bypass capacitor Cs also acts as a short circuits for low frequency analysis.

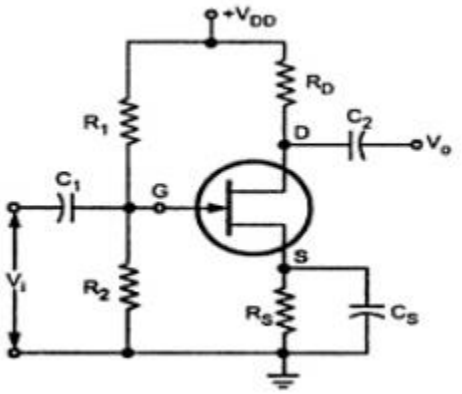


Fig.3.21. Common Source MOSFET amplifier with Voltage divider bias

The following Figure 3.21 shows the low frequency equivalent model for Common Source Amplifier with voltage divider Bias

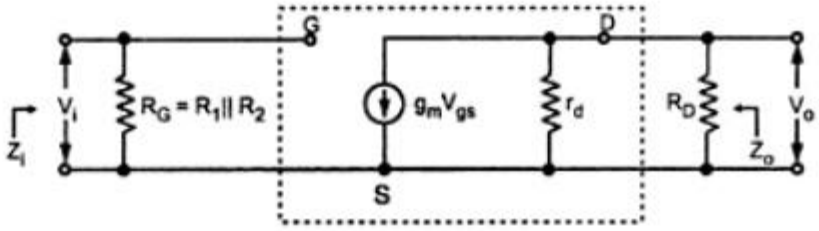


Fig3.10 **small model of Common source amplifier with Voltage divider bias(Bypassed Rs)**

The parameters are given by

$$R_G = R_1 \| R_2$$

$$Z_i = R_G$$

$$= R_1 \| R_2$$

$$Z_o = r_d \| R_D$$

if $r_d >> R_D$

$$Z_o \approx R_D$$

$$A_v = -g_m (r_d \| R_D)$$

If $r_d >> R_D$

$$A_v = -g_m R_D$$

The negative sign in the voltage gain indicates there is a 180o phase shift between input and output voltages.

ü Common Drain Amplifier

In this circuit, input is applied between gate and source and output is taken between source and drain.

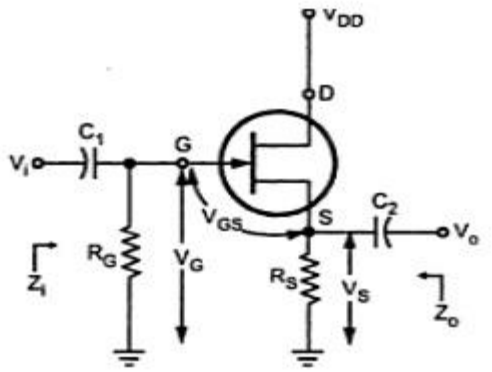


Fig3.12 **Circuit of Common Drain amplifier**

In this circuit, the source voltage is

Vs = VG+VGS

When a signal is applied to the MOSFET gate via C1 ,VG varies with the signal. As VGS is fairly constant and Vs = VG+VGS, Vs varies with Vi.

The following figure shows the low frequency equivalent model for common drain circuit.

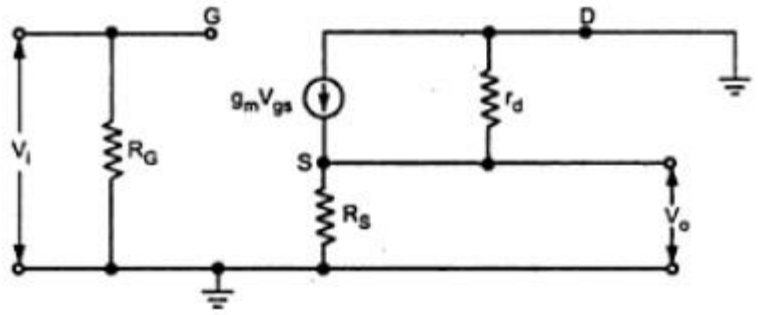


Fig3.13 **small model of Common Drain amplifier**

Input Impedance Zi

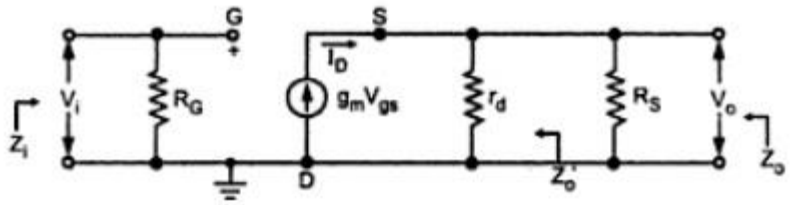


Fig3.13 Simplified small model of Common Drain amplifier

Zi = RG

Output Impedance Zo

It is given by

$$Z_o = Z_o' \| R_s$$

where $$Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i = 0}$$

Applying KVL to the outer loop we can have,

$$V_i + V_{gs} - V_o = 0$$

As $$V_i = 0,$$

$$V_{gs} = V_o$$

Looking at Fig. we can write that,

$$g_m V_{gs} = I_d$$

But Vgs = Vo, so

$$g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{1}{g_m}$$

$$\therefore \quad Z_o = \frac{1}{g_m} \| R_s$$

Voltage gain (Av)

It is given by

$$A_v = \frac{V_o}{V_i}$$

Looking at Fig. we can write that,

$$V_o = -I_d (r_d \,||\, R_s)$$

and $$I_d = g_m V_{gs}$$

$$\therefore \quad V_o = -g_m V_{gs} (r_d \,||\, R_s)$$

But

$$V_i = -V_{gs} + V_o$$

$$= -V_{gs} + [-g_m V_{gs} (r_d \,||\, R_s)]$$

Substitute the value Vo and Vi. Then

$$A_v = \frac{-g_m V_{gs} (r_d \,||\, R_s)}{-V_{gs} (1 + g_m (r_d \,||\, R_s))}$$

$$= \frac{g_m (r_d \,||\, R_s)}{1 + g_m (r_d \,||\, R_s)}$$

if $r_d >> R_s$

$$A_v = \frac{g_m R_s}{1 + g_m R_s}$$

if $g_m R_s >> 1$

$A_v \approx 1$, but it is always less than one.

Common drain circuit does not provide voltage gain.& there is no phase shift between input and output voltages.

Table summarizes the performance of common drain amplifier

	Exact	$r_d >> R_D$
Z_i	R_G	R_G
Z_o	$\frac{1}{g_m} \parallel R_s$	$\frac{1}{g_m} \parallel R_s$
A_v	$\frac{g_m (r_d \parallel R_s)}{1 + g_m (r_d \parallel R_s)}$	$\frac{g_m R_s}{1 + g_m R_s}$

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SCHOOL OF ELECTRICAL AND ELECTRONICS ENGINEERING

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

UNIT – IV

ELECTRONIC CIRCUITS 1- SECA1302

I. Introduction

UNIT 4 MULTISTAGE AMPLIFIERS AND FREQUENCY RESPONSE OF BJT AND FET AMPLIFIERS **9 Hrs**

Multistage Amplifiers- Methods of Coupling- RC Coupled- Transformer Coupled – Direct Coupled Amplifiers- Amplifier frequency response – Miller effect

Frequency response of transistor amplifiers with circuit capacitors – BJT frequency response – Low and High frequency analysis of CE,CB, CC - Frequency response of FET - Low and High frequency analysis of CS,CG, CD JFET & MOSFET.

4.1 Multistage Amplifiers

- **The performance obtainable from a single stage amplifier is often insufficient for many applications.**
- **Several stages may be combined forming a multistage amplifier. These stages are connected in cascade,**

i.e. output of the first stage is connected to form input of second stage, whose output becomes input of third stage, and so on.

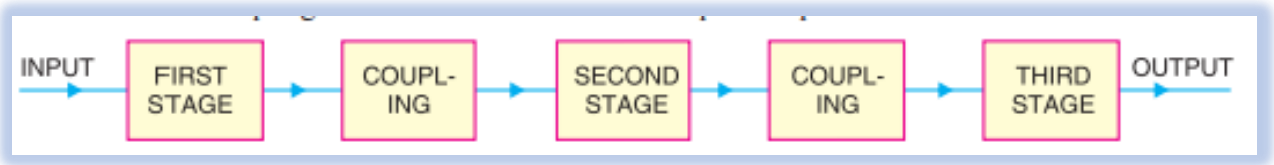


Figure 4.1 Block Diagram of Multistage Amplifier

- **Single amplifier is inadequate for practical purposes.**
- **Additional amplification over two or three stages is necessary. To achieve this, the output of each amplifier stage is coupled in some way to the input of the next stage. The resulting system is referred to as multistage amplifier.**

(OR)

A transistor circuit containing more than one stage of amplification is known as multistage transistor amplifier.Ex: Transistor radio receiver- Number of amplification stages may be six or more.

Cascading

- **In Multi-stage amplifiers, the output of first stage is coupled to the input of next stage using a coupling device. These coupling devices can usually be a capacitor or a transformer. This process of joining two amplifier stages using a coupling device can be called as Cascading.**
- **The following figure shows a two-stage amplifier connected in cascade.**

The overall gain is the product of voltage gain of individual stages.

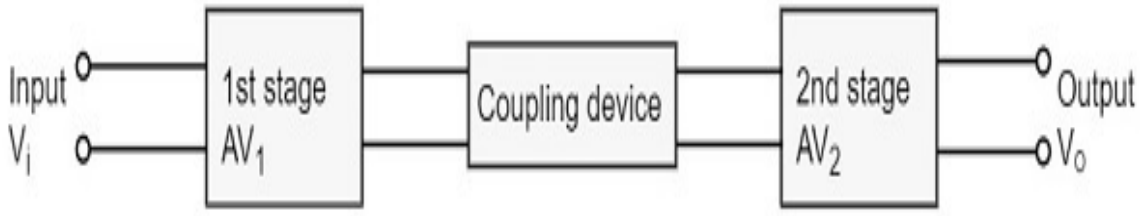


Figure 4.2 Two-stage amplifiers

Where A_V = Overall gain

A_{V1} = Voltage gain of 1st stage

A_{V2} = Voltage gain of 2nd stage Av

Av = Av1* Av2

Av = (V2/V1) * (Vo/V2) = Vo/V1

Multistage amplifiers:

- **Overall gain of an ac signal will get increased.**
- **Calculated by simply multiplying each gain together.**

The overall gain of a multistage amplifier is the product of the gains of the individual stages,

Gain (A) = A1* A2*A3*A4*... *An

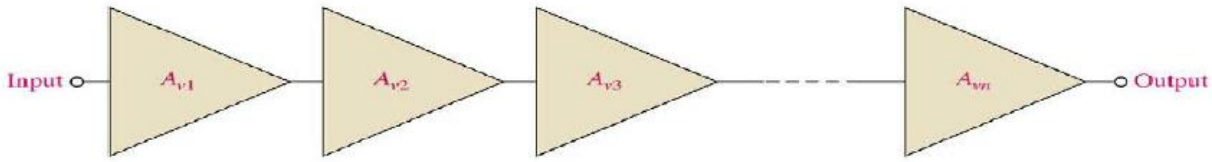


Figure 4.3 Multistage Amplifier

Need for multistage amplifiers:

- **To transfer the AC from the output of one stage to the input of next stage.**
- **To block the DC to pass from the output of one stage to the input of next stage, which means to isolate the DC conditions**
- **To amplify extremely weak signals to sufficient level, so that it can travel to a large distance.**

- **The distortion can be reduced by changing the signal within stages.**

To understand the working of multistage amplifiers, the following terms need to be known

1. **Gain**
2. **Decibel gain**
3. **Frequency response**
4. **Bandwidth**

Gain

The ratio of the output electrical quantity to the input of the amplifier is called its gain. It can be current gain or voltage gain or power gain.

The gain of a multistage amplifier is equal to the product of gains of individual stages.

E.g. G1, G2 and G3 are the individual voltage gains of a three- stage amplifier, then total voltage gain G is given by

$$G = G1 \times G2 \times G3$$

Decibel gain

While analyzing circuits in the *frequency domain*, it is more convenient to compare the amplitude ratio of the output to input values on a logarithmic scale rather than on a linear scale. So if we use the logarithmic ratio of two quantities, P_1 and P_2 we end up with a new quantity or level which can be presented using *Decibels*.

Unlike voltage or current which is measured in volts and amperes respectively, the decibel, or simple dB for short, is just a ratio of two values, well actually the ratio of one value against another known or fixed value, so therefore the decibel is a dimensionless quantity, but does have the "Bel" as its units after the telephone inventor, Alexander Graham Bell.

The ratio of any two values, where one is fixed or known and of the same qunatity or units, whether power, voltage or current, can be represented using decibels (dB) where "deci" means one tenth (1/10th) of a Bel. Clearly then there are 10 decibels (10dB) per Bel or 1 Bel = 10 decibels.

The decibel is commonly used to show the ratio of power change (increasing or decreasing) and is defined as the value which is ten times the Base-10 logarithm of two power levels. For example, 1 watt to 10 watts is the same power ratio as 10 watts to 100 watts, that is 10:1, so while there is a large difference in the number of watts, 9 compared to 90, the decibel ratio would be exactly the same. Hopefully then we can see that the decibel (dB) is a ratio used for comparing and calculating levels of power change and not the power itself.

Power gain $= 10\log_{10}[P_{out}/P_{in}]dB$

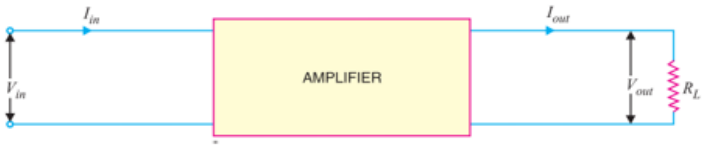


Figure 4.4 Amplifier Stage

$P_{in} = V_{in}^2 / R = R * I_{in}^2$

$P_{out} = V_{out}^2 / R = R * I_{out}^2$

Voltage gain in db = $10\log_{10}[(V_{out}^2 / R)/ (V_{in}^2 / R)] = 20\log_{10}[V_{out} / V_{in}]$

Current gain in db = $10\log_{10}[(R * I_{out}^2)/ (R * I_{in}^2)] = 20\log_{10}[I_{out} / I_{in}]$

Decibel gain

Advantages:

The following are the advantages of expressing the gain in db :

(a) The unit db is a logarithmic unit. Our ear response is also logarithmic i.e. loudness of sound heard by ear is not according to the intensity of sound but according to the log of intensity of sound.

Thus if the intensity of sound given by speaker (i.e. power) is increased 100 times, our ears hear a doubling effect ($\log_{10}$ 100 = 2).Hence, this unit tallies with the natural response of our ears.

(b) When the gains are expressed in db, the overall gain of a multistage amplifier is the sum of gains of individual stages in db.

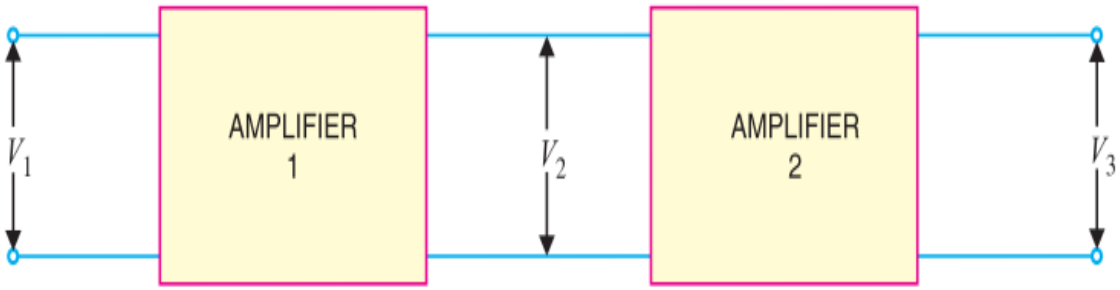


Figure 4.5 Two stage Amplifier

Gain as number =(V2/V1) * (V3/V2)

Gain in db = $20\log_{10}$(V2/V1) * (V3/V2)

Gain in db = $20\log_{10}$(V2/V1) + $20\log_{10}$(V3/V2)

G_1(db) + G_2(db)

Frequency response

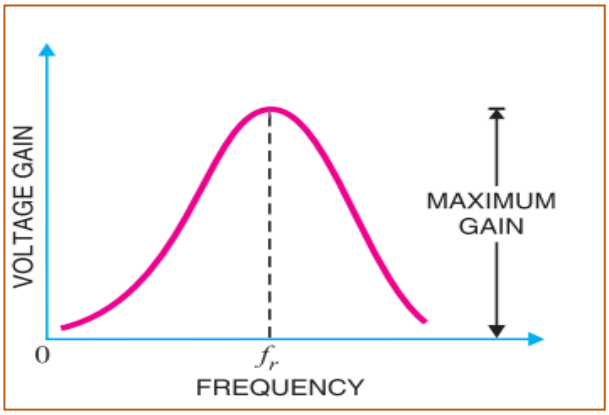


Figure 4.6 Frequency Response curve

The curve between voltage gain and signal frequency of an amplifier is known as frequency response.

- **The voltage gain of an amplifier varies with signal frequency.**
- **It is because reactance of the capacitors in the circuit changes with signal frequency and hence affects the output voltage and voltage gain.**
- **The gain of the amplifier increases as the frequency increases from zero till it becomes maximum at f_r , called Resonant frequency.**
- **If the frequency of signal increases beyond f_r , the gain decreases.**

Bandwidth

The range of frequency over which the voltage gain is equal to or greater than 70.7%(3db) of the maximum gain is known as bandwidth.

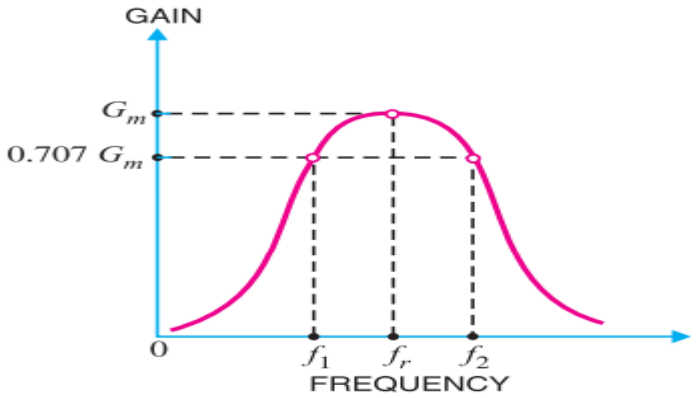


Figure 4.7 Bandwidth $f_2 - f_1$

1. Draw the 3db line from the maximum value and find f_1 and f_2 from the graph.

2. The (f 1) is called lower cut-off frequency & (f 2) is known as upper cut-off frequency

3. Therefore, $f_2 - f_1$ is the bandwidth. (i.e. Upper cutoff frequency – Lower cutoff frequency)

5. For distortion less amplification, it is important that signal frequency range must be within the bandwidth of the amplifier.

Bandwidth of an amplifier is the range of frequency at the limits of which its voltage gain falls by 3 db from the maximum gain.

The frequency f 1 or f 2 is also called 3-db frequency or half-power frequency.

Half Power Bandwidth

The half-power point or half-power bandwidth is the point at which the output power has dropped to half of its peak value; that is, at a level of approximately -3 dB

Half-power gain in dB = $10\log_{10}[(P_{out\ max}/2)/P_{outmax}]$

= $10\log_{10}[1/2]$ = -3 dB

Types of multistage amplifier

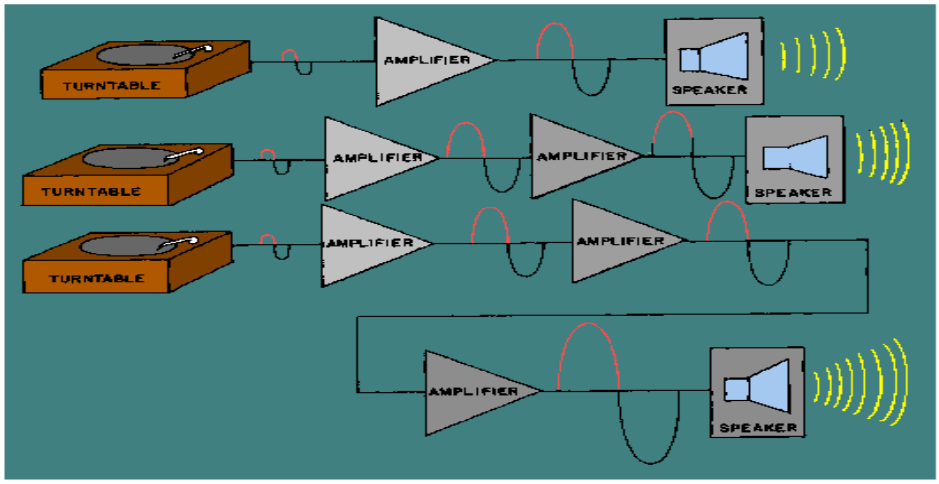


Figure 4.8 Multistage Amplifiers

The output of first stage is coupled to the input of next stage using a coupling device. The process of transferring energy between circuits is known as COUPLING.

There are various ways of coupling signals into and out of amplifier circuits.

Common methods of amplifier coupling

- **RC Coupled Amplifier**
- **Transformer Coupled Transistor Amplifier**
- **Direct Coupled Amplifier**

(i) In RC coupling, a capacitor is used as the coupling device. The capacitor connects the output of one stage to the input of the next stage in order to pass the a.c. signal on while blocking the d.c. bias voltages.

(ii) In transformer coupling, transformer is used as the coupling device. The transformer coupling provides the same two functions (viz. to pass the signal on and blocking d.c.) but permits in addition impedance matching.

(iii) In direct coupling or d.c. coupling, the individual amplifier stage bias conditions are so designed that the two stages may be directly connected without the necessity for d.c. isolation

4.2 RC Coupled Amplifier

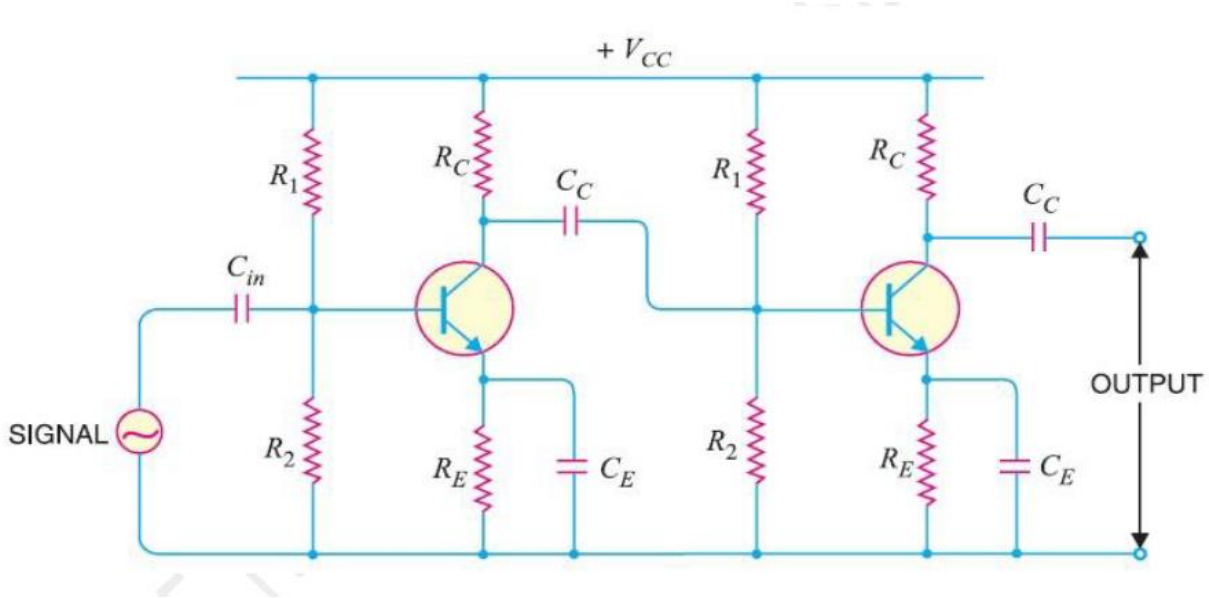


Figure 4.9 RC coupled Amplifier

- **As the coupling from one stage to next is achieved by a coupling capacitor (C_C) followed by a connection to a shunt resistor, therefore, such amplifiers are called Resistance - Capacitance coupled amplifiers.**
- **R_1, R_2 and R_E – used for biasing and stabilisation of network.**
- **C_E- emitter bypass capacitor offers low reactance path to the signal. Without it, the voltage gain of each stage would be lost.**
- **C_C transmits a.c. signal but blocks d.c. This prevents d.c. interference between various stages and the shifting of operating point**

Operation:

- **It may be mentioned here that total gain is less than the product of the gains of individual stages. It is because when a second stage is made to follow the first stage, the effective load resistance of first stage is reduced due to the shunting effect of the input resistance of second stage. This reduces the gain of the stage which is loaded by the next stage.**
- **For instance, in a 3-stage amplifier, the gain of first and second stages will be reduced due to loading effect of next stage. The overall gain shall be equal to the product of the gains of three stages.**

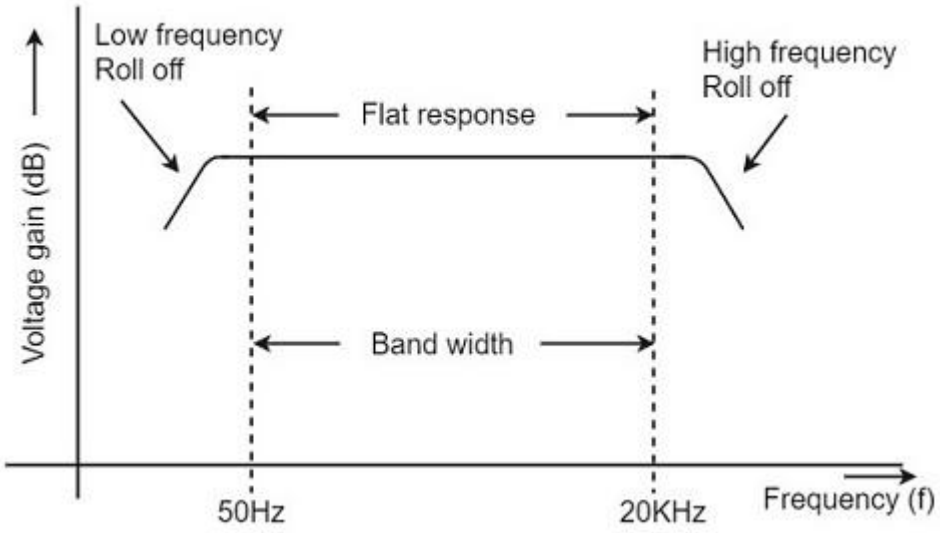


Figure 4.10 Frequency Response

The frequency response of a typical RC coupled amplifier :

(i) At low frequencies (< 50 Hz): two factors cause a falling of voltage gain

- ✓ **Reactance of coupling capacitor CC is quite high - very small part of signal will pass from one stage to the next stage.**
- ✓ **CE cannot shunt the emitter resistance RE effectively because of its large reactance at low frequencies.**

ii) At mid-frequencies (50 Hz to 20 kHz): the voltage gain of the amplifier is constant.

- ✓ **Thus, as the frequency increases in this range, reactance of CC decreases which tends to increase the gain.**
- ✓ **However, at the same time, lower reactance means higher loading of first stage and hence lower gain.**
- ✓ **These two factors almost cancel each other, resulting in a uniform gain at mid-frequency.**

(iii) At high frequencies (> 20 kHz): two reasons causes the voltage gain drops off

- ✓ **Reactance of CC is very small and it behaves as a short circuit- increases the loading effect of next stage and serves to reduce the voltage gain.**
- ✓ **Capacitive reactance of base-emitter junction is low which increases the base current. This reduces the current amplification factor β.**

Advantages :

(i) It has excellent frequency response.

(ii) **The gain is constant over the audio frequency range which is the region of most importance for speech, music etc.**

(iii) **It has lower cost since it employs resistors and capacitors which are cheap.**

(iv) **The circuit is very compact as the modern resistors and capacitors are small and extremely light.**

Disadvantages :

(i) **The RC coupled amplifiers have low voltage and power gain.**

(ii) **They have the tendency to become noisy with age, particularly in moist climates.**

(iii) **Impedance matching is poor.**

Applications:

- **The RC coupled amplifiers have excellent audio fidelity over a wide range of frequency.**
- **Therefore, they are widely used as voltage amplifiers e.g. in the initial stages of public address system.**

Note:

- **If other type of coupling (e.g. transformer coupling) is employed in the initial stages, this results in frequency distortion which may be amplified in next stages.**
- **However, because of poor impedance matching, RC coupling is rarely used in the final stages.**

❖ **RC coupling- used in initial stages**

❖ **Transformer coupling- used in final stages**

4.3 Transformer-Coupled Amplifier

In RC coupled amplifier, the effective load of each stage is decreased due to the low resistance and the voltage and power gain also gets decreased.

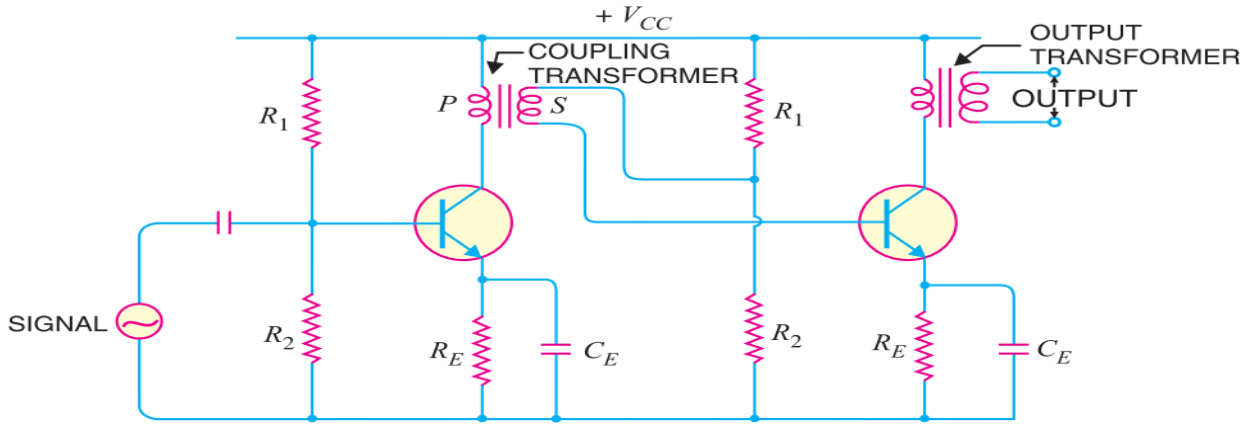


Fig 4.11 Transformer coupled Amplifier

- **R1 & R2 resistors provide the biasing and stabilization for the circuit.**
- **Cin isolates DC and allows only AC components from the input signal to the circuit.**
- **The emitter capacitor provides a low reactance path to the signal and offers stability to the circuit.**
- **The first stage of output is connected as an input to the second stage through secondary windings of the primary transformer.**
- **It is mostly used for power amplification.**
- **When an a.c. signal is applied to the base of first transistor, it appears in the amplified form across primary P of the coupling transformer.**
- **The voltage developed across primary is transferred to the input of the next stage by the transformer secondary S. The second stage renders amplification in an exactly similar manner.**
- **Impedance matching - By this property, low resistance of one stage can be reflected as high load resistance to the previous stage. Therefore the voltage at primary windings can be forwarded according to the ratio of secondary windings of the transformer.**

Frequency response

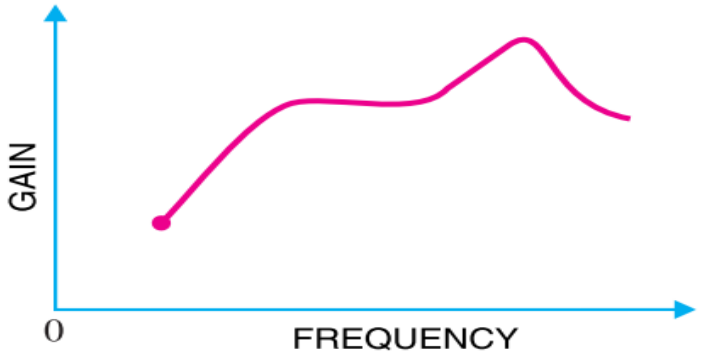


Figure 4.12 Frequency Response

- **It is clear that frequency response is rather poor i.e. gain is constant only over a small range of frequency.**
- **At low frequencies, the reactance of primary begins to fall, resulting in decreased gain.**
- **At high frequencies, the capacitance between turns of windings acts as a bypass condenser to reduce the output voltage and hence gain.**

- **Hence, transformer-coupled amplifier introduces frequency distortion. It is possible to achieve a fairly constant gain over the audio frequency range.**
- **Transformer coupled that achieves a frequency response may cost 10 to 20 times expensive than the RC coupled amplifier.**

Advantages

- **No signal power is lost in the collector or base resistors.**
- **An excellent impedance matching can be achieved in a transformer coupled amplifier**
- **Due to excellent impedance matching, transformer coupling provides higher gain.**
- **As a result, a single stage of properly designed transformer coupling can provide the gain of two stages of RC coupling.**

Disadvantages

- **It has a poor frequency response i.e. the gain varies considerably with frequency.**
- **The coupling transformers are bulky and fairly expensive at audio frequencies.**
- **Frequency distortion is higher i.e. low frequency signals are less amplified as compared to the high frequency signals.**
- **Transformer coupling tends to introduce *hum in the output.**
- **(There are hundreds of turns of primary and secondary. These turns will multiply an induced e.m.f. from nearby power wiring. As the transformer is connected in the base circuit, therefore, the induced hum voltage will appear in amplified form in the output.)**

Applications

- **Transformer coupling is mostly employed for impedance matching.**
- **In general, the last stage of a multistage amplifier is the power stage. Here, a concentrated effort is made to transfer maximum power to the output device e.g. a loudspeaker.**
- **For maximum power transfer, the impedance of power source should be equal to that of load.**
- **The impedance of an output device is a few ohms whereas the output impedance of transistor is several hundred times this value. In order to match the impedance, a step-down transformer of proper turn ratio is used.**

4.4 Direct-Coupled Amplifier

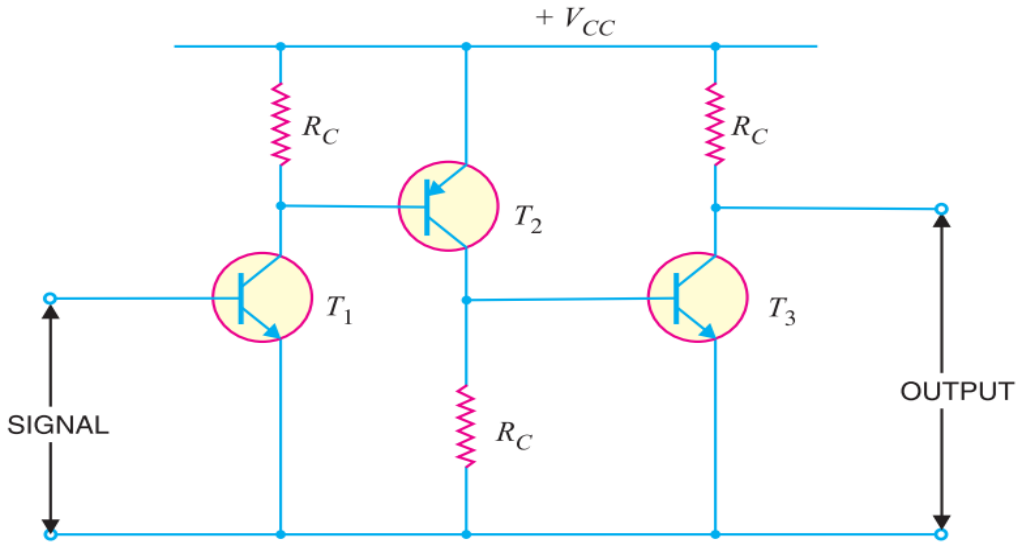


Figure 4.13 Direct coupled amplifier

- **There are many applications in which extremely low frequency (< 10 Hz) signals are to be amplified e.g. amplifying photo-electric current, thermo-couple current etc.**
- **The coupling devices such as capacitors and transformers cannot be used because the electrical sizes of these components become very large at extremely low frequencies.**
- **Under such situations, one stage is directly connected to the next stage without any intervening coupling device.**
- **This type of coupling is known as direct coupling**

Operation

- **It shows the circuit of a three-stage direct-coupled amplifier.**
- **It uses *complementary transistors. This makes the circuit stable w.r.t. temperature changes. In this connection (i.e., npn followed by pnp), when the temperature rises, is opposite for the two transistors. Thus the variation in one transistor tends to cancel that in the other. Thus, the first stage uses npn transistor, the second stage uses pnp transistor and so on.**
- **This arrangement makes the design very simple. The output from the collector of first transistor T1 is fed to the input of the second transistor T2 and so on.**
- **The weak signal is applied to the input of first transistor T1. Due to transistor action, an amplified output is obtained across the collector load RC of transistor T1. This voltage drives the base of the second transistor and amplified output is obtained across its collector load.**
- **In this way, direct coupled amplifier raises the strength of weak signal.**

Advantages

- **The circuit arrangement is simple because of minimum use of resistors.**
- **The circuit has low cost because of the absence of expensive coupling devices.**
    - **Disadvantages**
- **It cannot be used for amplifying high frequencies.**
- **The operating point is shifted due to temperature variations.**

S. No	Particular	*RC* coupling	Transformer coupling	Direct coupling
1.	*Frequency response*	Excellent in the audio frequency range	Poor	Best
2.	*Cost*	Less	More	Least
3.	*Space and weight*	Less	More	Least
4.	*Impedance matching*	Not good	Excellent	Good
5.	*Use*	For voltage amplification	For power amplification	For amplifiying extremely low frequencies

Table 4.1 Comparison between multistage amplifiers

4.5 Miller Theorem

- **The Miller effect is a basic electronic phenomenon associated with feedback circuits.**
- **It can occur undesirably in amplifiers, caused by parasitic capacitance.**
- **It accounts for an increase in the equivalent input capacitance of an inverting voltage amplifier due to amplification of capacitance between the input and output terminals.**
- **Although *Miller effect* normally refers to capacitance, any impedance connected between the input and another node exhibiting high gain can modify the amplifier input impedance via the Miller effect.**
- **In transistor amplifiers, it is necessary to split the capacitance between input and output. It can be achieved by using miller's theorem.**

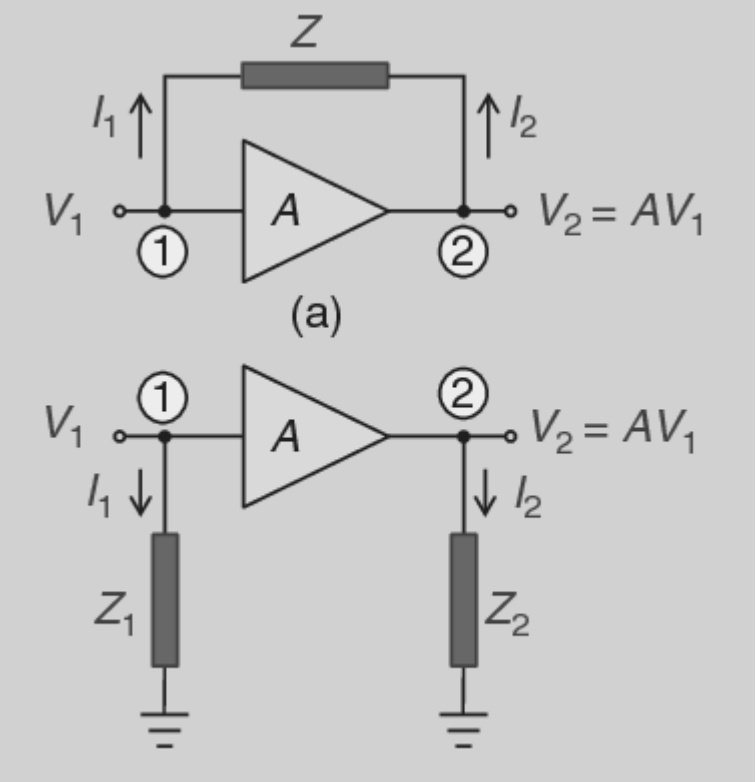


Figure 4.14 Miller feedback circuits

I1= (V1-V2) / Z----(a)

I2 = (V2- V1) / Z----(b)

I1 = V1/ Z1-----(c)

I2=V2 / Z2-----(d)

If (a)= (3)

V1/ Z1 = (V1-V2) / Z

Z1 = (V1*Z)/(V1-V2)

Z1= Z * 1 / (1-V2/V1)

Z1= Z / (1- Av)

If (b) = (d)

(V2- V1) / Z = V2 / Z2

Z2 = Z/(1-(1/Av))

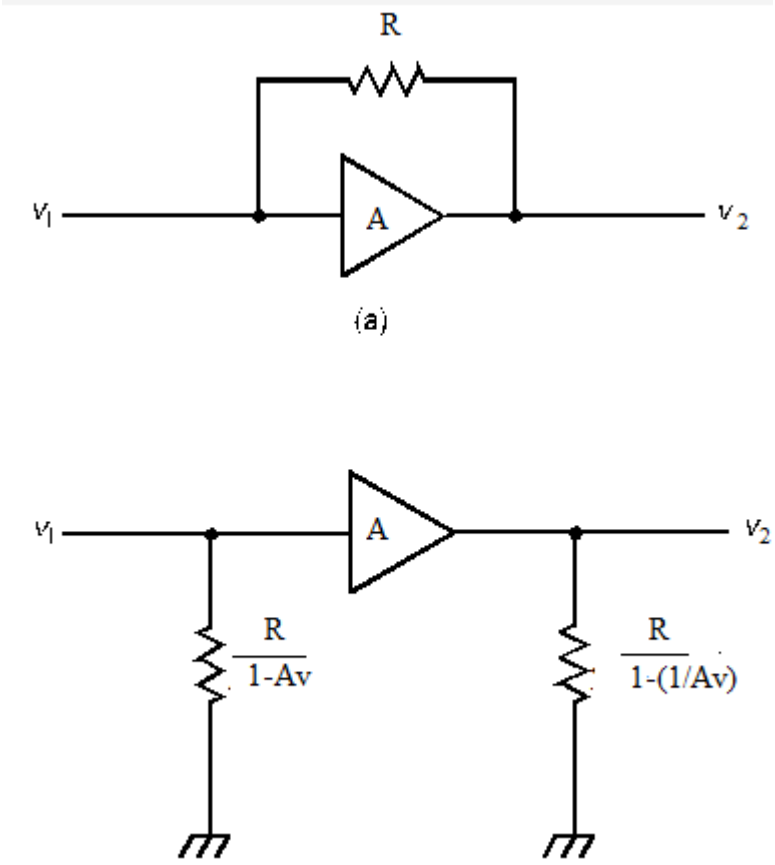
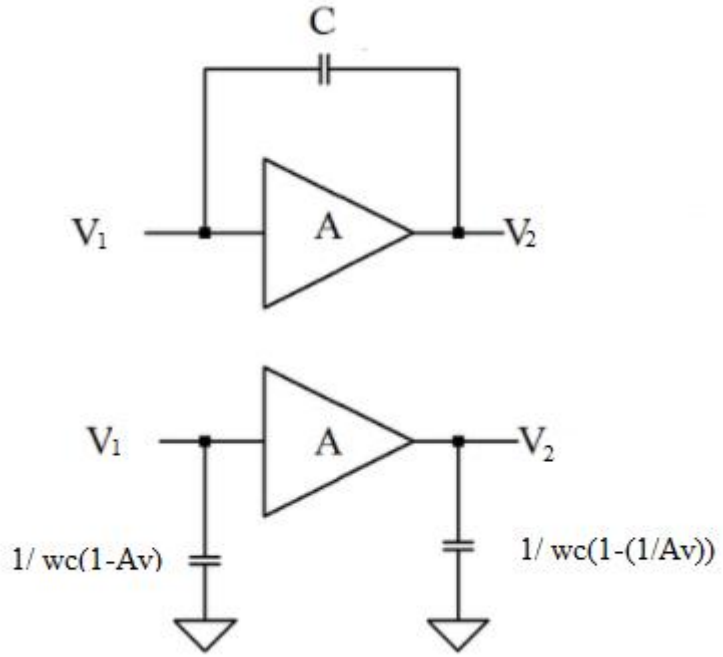


Figure 4.15 Resistive feedback circuits



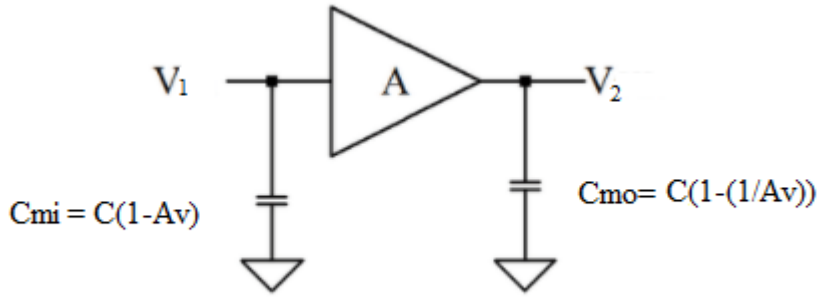


Figure 4.16 Capacitive feedback circuits

Miller Input capacitance

Cmi = C (1-Av)

Cmo = C (1-(1/Av))

Non Inverting Amplifier

(O/P of the amplifier in phase with the I/P)

Inverting Amplifier :Output of the amplifier is 180 degree out of phase with respect to input.

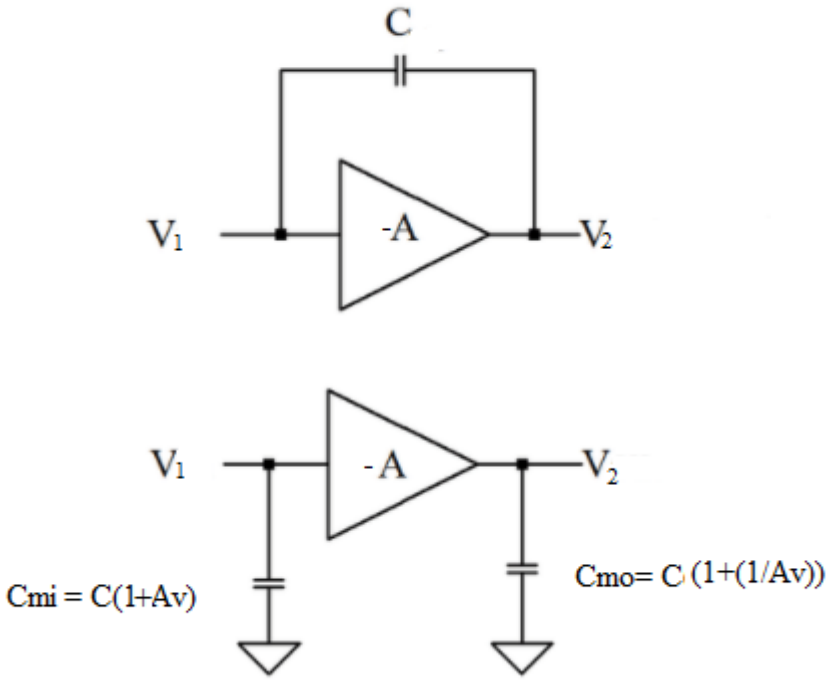


Figure 4.17 Inverting Amplifier-Output of the amplifier is 180 degree out of phase with respect to input.

4.6 Frequency response of transistor amplifiers with capacitor circuit

- **Most amplifiers have relatively constant gain over a certain range (band) of frequencies, this is called the bandwidth (BW) of the amplifier**
- **The gain of an amplifier remains relatively constant across a band of frequencies.**
- **When the operating frequency starts to go outside this frequency range, the gain begins to drop off.**

BW= f_{c2}-f_{c1}

Center frequency $f_o = \sqrt{f_{c1}f_{c2}}$

The ratio of f_o to f_{c1} equals the ratio of f_{c2} to f_o , this is:

$$f_o / f_{c1} = f_{c2} / f_o$$

$$f_{c2} = f_o^{\,2} / f_{c1} \quad \text{(OR)}$$

$$f_{c1} = f_o^{\,2} / f_{c2}$$

- **Frequency response analysis – Cutoff frequencies**
- **The cut-off frequencies of single stage BJT/FET amplifiers are influenced by the RC combinations formed by the network capacitors CC, CE, etc. and the resistive parameters that are present in the network.**

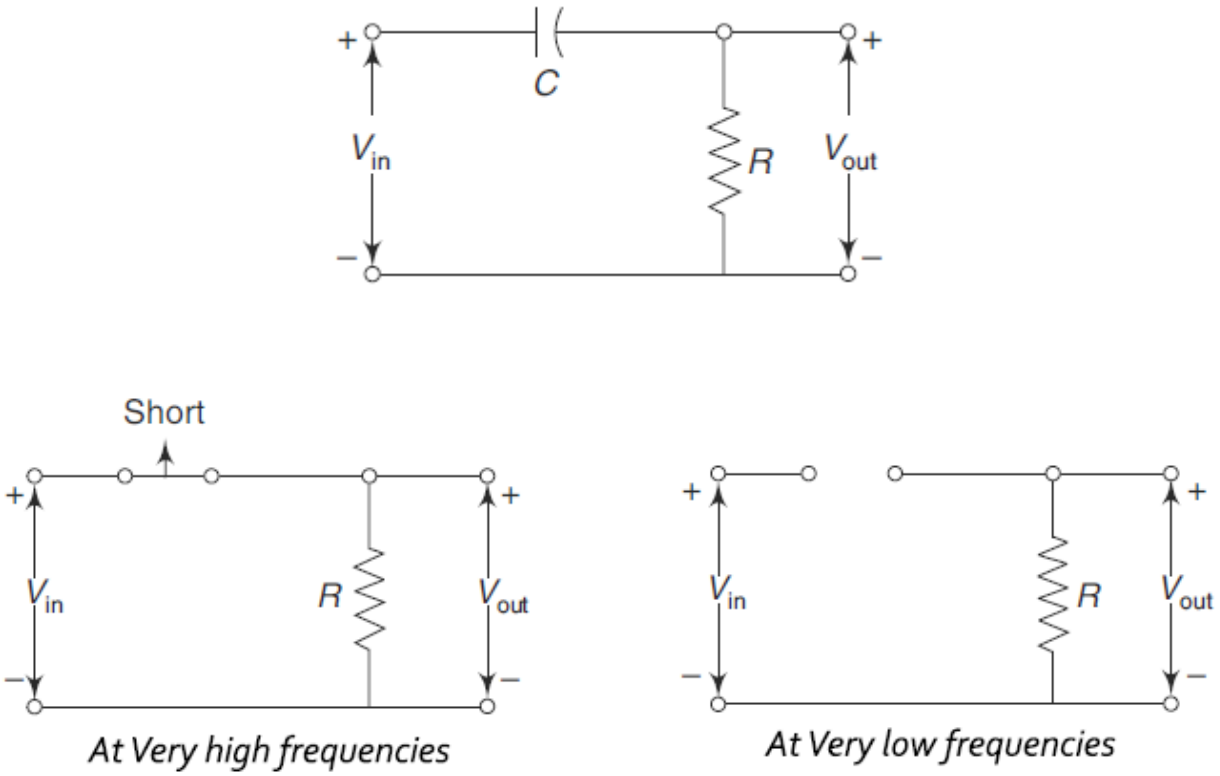


Figure 4.18 Frequency analysis

It is to be recalled that at High frequencies Xc = $1/2\pi fc \approx 0\ \Omega$

At low frequencies Xc = $1/2\pi fc \approx \infty\ \Omega$

Low Frequency	High Frequency
The Change in the reactance of inductors and capacitors could affect the gain of amplifiers	The Change in the reactance of inductors and capacitors could affect the gain of amplifiers
Capacitors can no longer be treated as short circuits - their reactance becomes larger enough to affect the signal	The reactance of intrinsic capacitance of devices becomes low enough -the signals could effectively pass through them and change the response of the circuit
Reactance of the primary of transformer becomes low – Resulting to poor low frequency response.	The stray capacitance of transformer windings reduces the gain of amplifier

Table 4.2 Comparison between Low Frequency and High Frequency

Low Frequency Response of RC circuit

Low frequency , the amplifier circuit behaves like high pass filter

(At low frequencies , Xc tends to ∞ and the capacitance treated as open circuit)

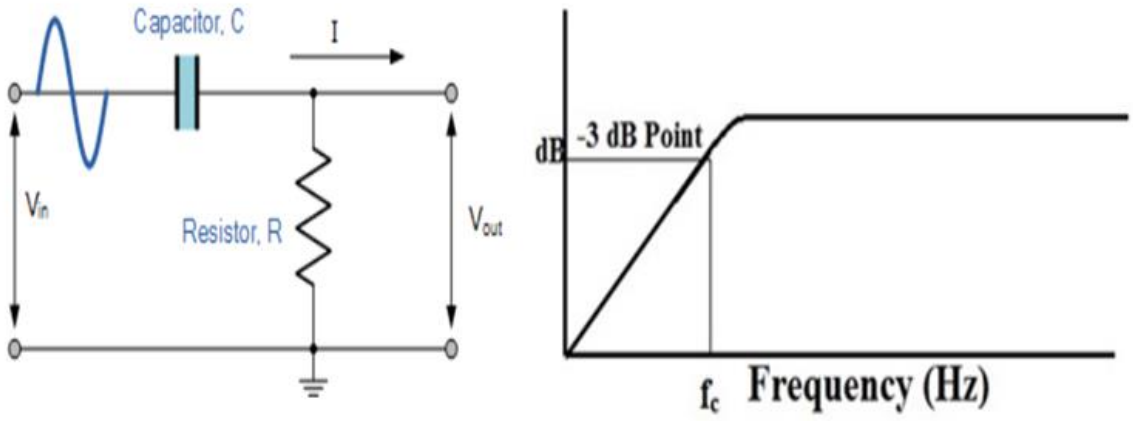


Figure 4.19 LPF Response

Vo = V1 *R / R-jXc

I Vo I = V1*R / $\sqrt{(R^2 + Xc^2)}$

If Xc = R

I Vo I = V1*R / $\sqrt{(2R^2)}$

I Vo I = V1 / $\sqrt{2}$

Av = 0.707

High Frequency Response of RC circuit

- **At high frequencies (Frequency increases, Xc decreases) act as short circuit.**

- **Also the parasitic capacitance comes into effect and defines the 3db point.**
- **At high frequencies, it acts as low pass filter.**

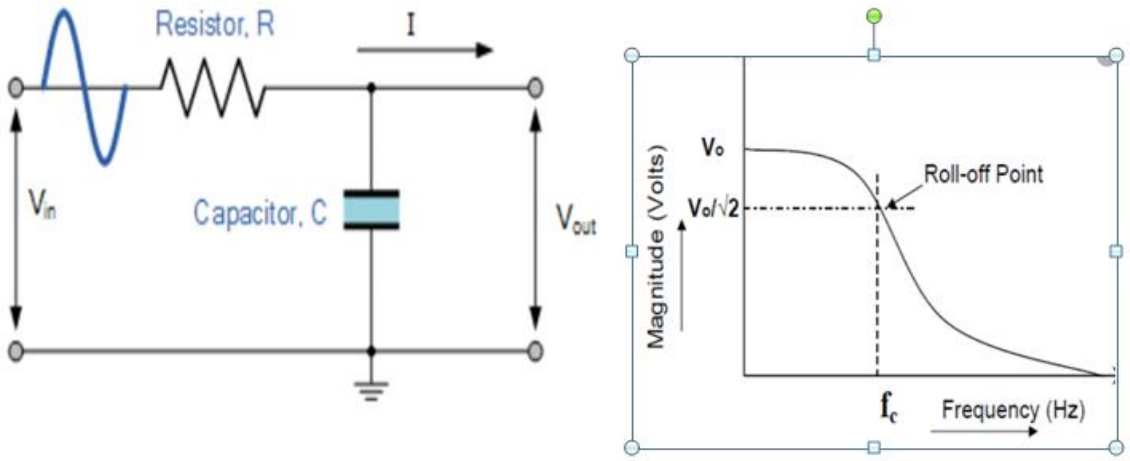


Figure 4.20 HPF Response

The frequency response of an amplifier refers to the frequency range in which the amplifier will operate with negligible effects from capacitors and device internal capacitance. This range of frequencies can be called the mid-range.

At frequencies above and below the midrange, capacitance and any inductance will affect the gain of the amplifier

.•At low frequencies the coupling and bypass capacitors lower the gain.

•At high frequencies stray capacitances associated with the active device lower the gain.

•Also, cascading amplifiers limits the gain at high and low frequencies.

- **At low frequencies, coupling capacitor (CS, CC) and bypass capacitor (CE) reactances affect the circuit impedances.**
- **The capacitive reactance varies inversely with frequency. At lower frequencies the reactance is greater, and it decreases as the frequency increases.**
- **At high frequencies, the coupling and bypass capacitors become effective ac shorts and do not affect an amplifier's response. Internal transistor junction capacitances, however, do come into play, reducing an amplifier's gain and introducing phase shift as the signal frequency increases.**
- **At high and mid frequencies , Vi ≈ V0 voltage across the load , so Vo/Vi =1**
- **At low frequencies Vo=0 voltage across the load and Vo/Vi =0**
- **Between two extremes the ratio between Vo and Vi will vary between 0 and 1 .**

4.7 Low Frequency Analysis of Capacitor Coupled BJT Amplifier

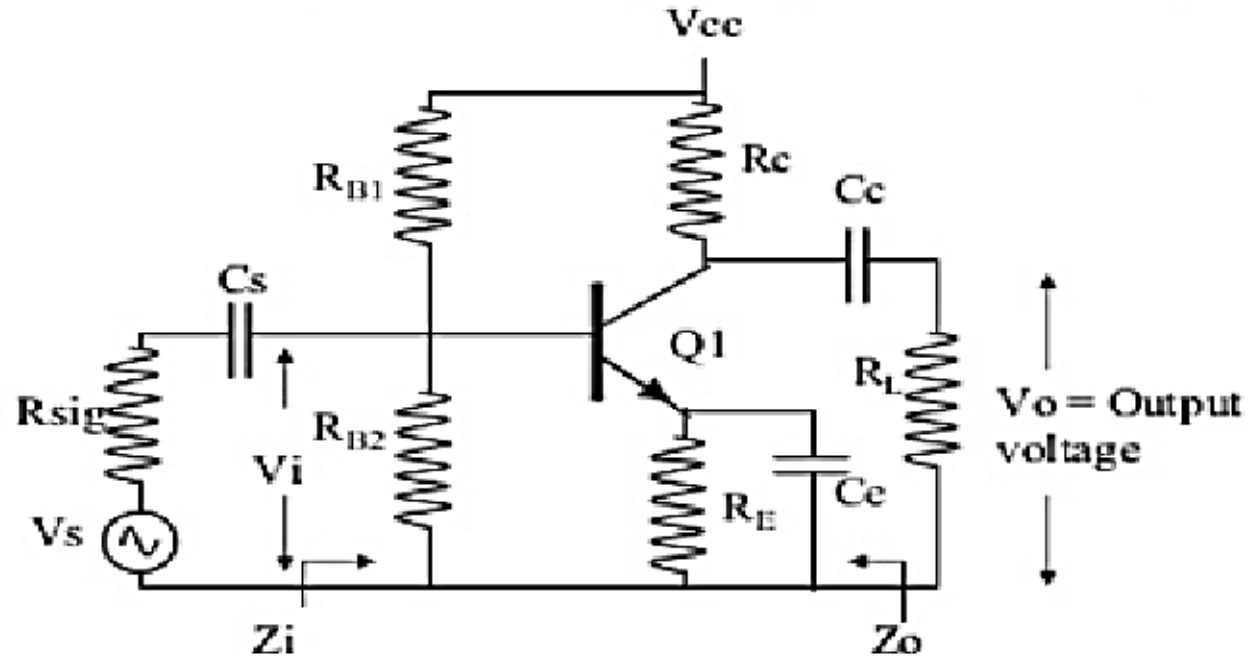


Figure 4.21 RC Coupled amplifiers

Vs = signal source

Rsig = Internal resistance of signal source

Cs = coupling capacitor for Vs

Cc= coupling capacitor for R_L

Cc = bypass capacitor for R_E

- **A capacitor coupled (also called RC coupled) BJT amplifier circuit .**
- **At middle and high frequencies, the capacitors Cc,Cs and Ce can be considered short circuits because their reactance become low enough, that there are no significant voltage drops across the capacitors.**
- **At low frequencies, the coupling capacitors Cc,Cs and Ce could no longer be treated as short circuit because their reactance become high enough that the there are significant voltage drops across the capacitors.**

Coupling Capacitors

– To couple the various stages of a multi-stage amplifier • For AC performance essentially a short circuit and AC current flows from one stage to the next stage – To support the biasing of each stage individually: • For DC performance: open circuit and no biasing current flows from one stage to another

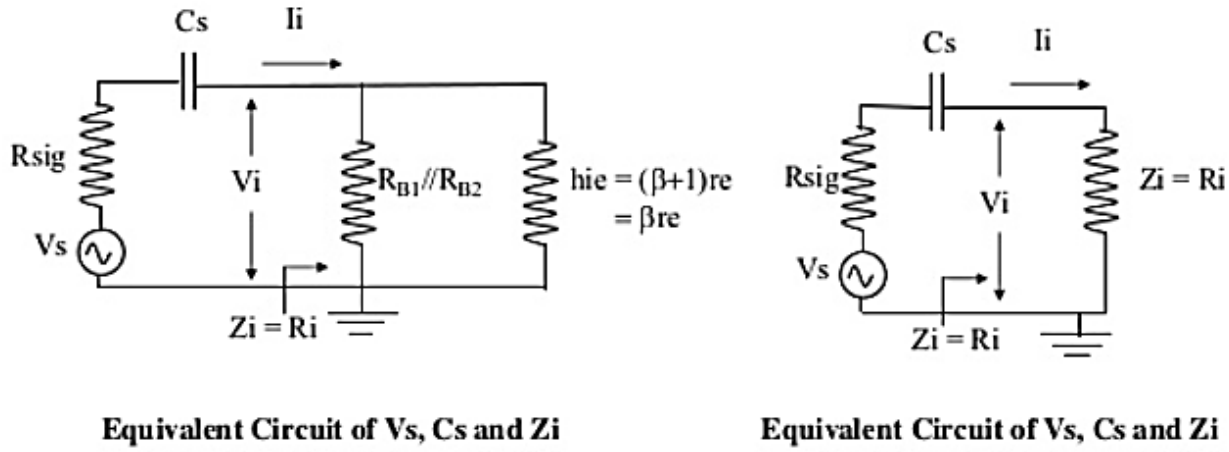
ByPass Capacitors

– To support the addition of a resistor for biasing purposes only • For DC performance: open circuit and current flows through the biasing resistor – Short-circuit the biasing resistor for AC performance. • For AC performance: short circuit and no current flows through the resistor (shorted out/bypassed)

To find Z_i

Case (i) Equivalent Circuit involving Cs capacitor:

$$h_{ie} = \beta r_e$$



Equivalent Circuit of Vs, Cs and Zi **Equivalent Circuit of Vs, Cs and Zi**

Figure 4.22 Equivalent Circuit

The input impedance of the circuit is:

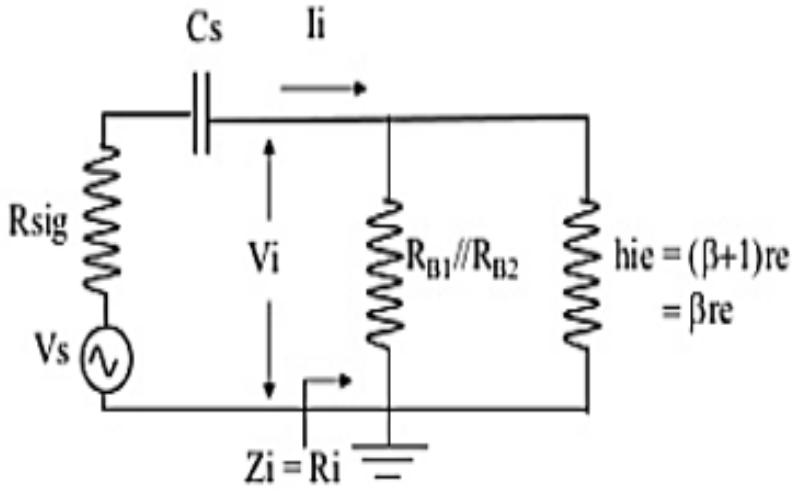


Figure 4.23 Input impedance

$$Zi = Ri = R_{B1} // R_{B2} // hie$$
$$= R_{B1} // R_{B2} // \beta re$$

The Lower cutoff frequency involving Cs capacitor is:

Sub: $R = R_i + R_{sig}$

$C = C_s$

$$f_{Ls} = \frac{1}{2\pi(Rsig + Ri)Cs}$$

To find Output impedance Z_0:

Case (ii)Equivalent Circuit involving Cc capacitor:

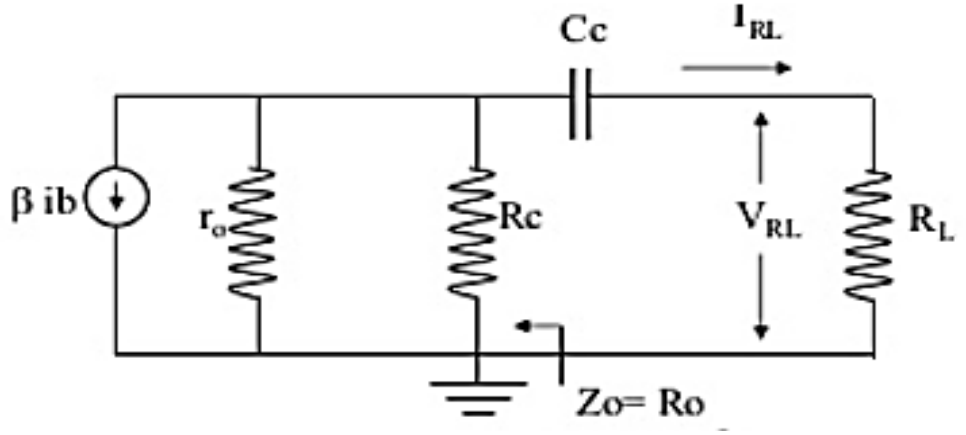


Figure 4.24 Equivalent Circuit

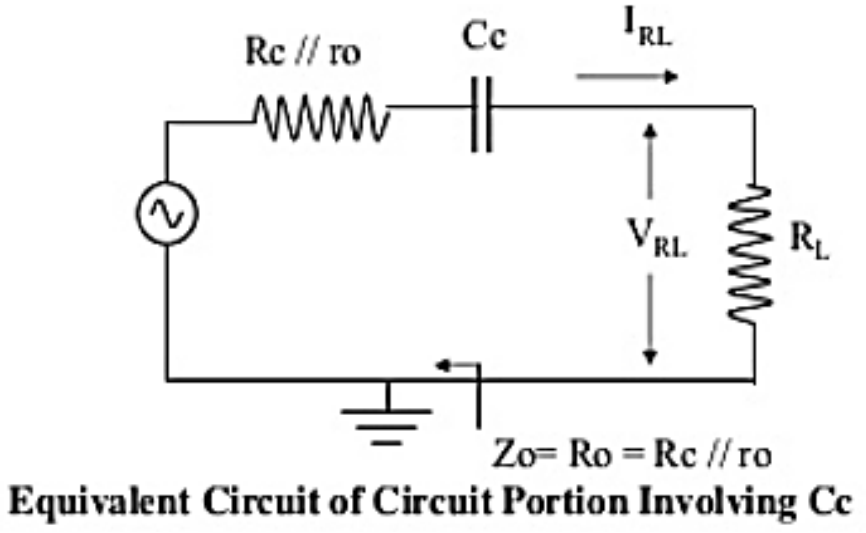


Figure 4.25 Equivalent circuit Cc

The output impedance of the circuit is:

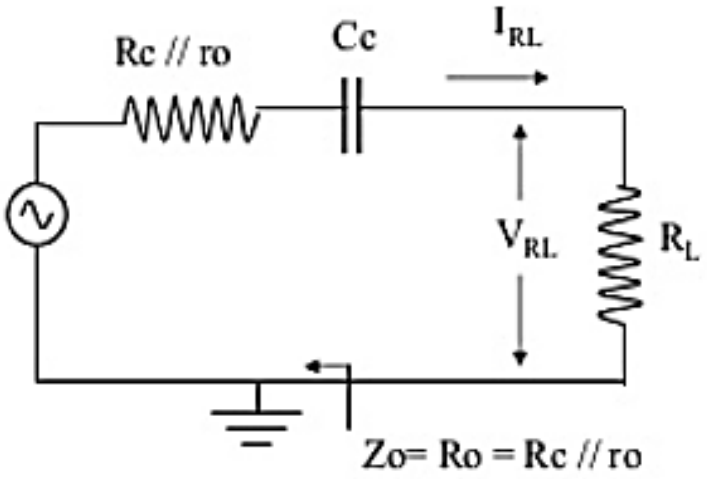


Figure 4.26 Equivalent circuit

$$f_{LC} = \frac{1}{2\pi(R_O + R_L)C_C}$$

$$Z_O = R_O = R_C // r_o$$

Case (iii) Equivalent Circuit involving Ce capacitor:

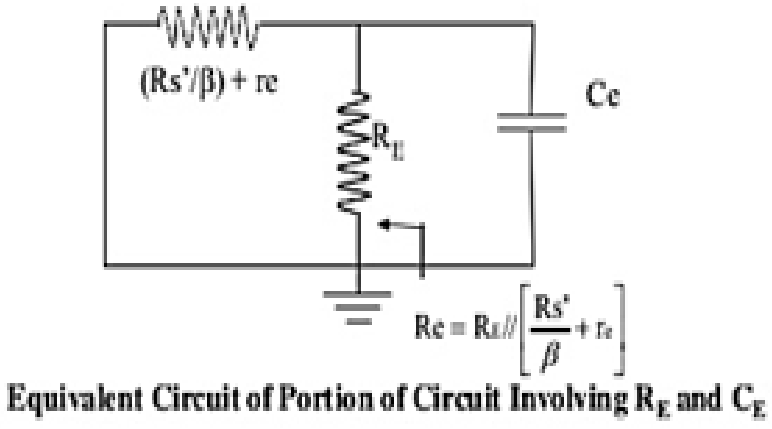


Figure 4.27 Equivalent circuit Ce

- **Cs and Cc shorted.**
- **By calculating the equivalent input resistance (Rs' = Rsig ‖ RB1 ‖ RB2) and reflecting into the emitter circuit (ie ., dividing by β)**
- **The resistance Re seen looking into RE from the output side can be computed as:**

$$Re = R_E // \left[\frac{Rs'}{\beta} + r_e \right]$$

Where : $Rs' = Rsig // R_{B1} // R_{B2}$

$$r_e = \frac{26 \times 10^{-3}}{I_E} \quad \text{(ohms)}$$

I_E = Emitter DC current (Ampere) = Emitter quiescent current (Ampere)

The Lower cutoff frequency involving Ce capacitor is: Sub: R= Re

C= Ce

$f_{LE} = 1/ 2\pi CeRe$

Cutoff frequency= Maximum (F_{LS},F_{LC},F_{LE})

4.8 LOW FREQUENCY RESPONSE OF JFET COMMON SOURCE AMPLIFIER

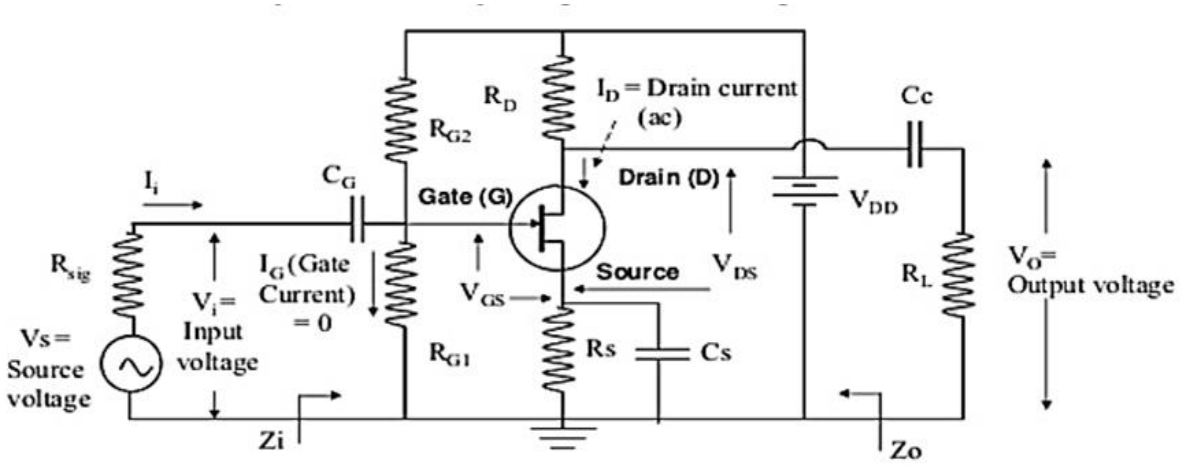


Figure 4.28 Common Source Amplifier JFET

- **The analysis of low frequencies response of FET amplifier is similar to that of BJT amplifiers.**
- **At middle and high frequencies, the capacitors Cc,Csand Cg consider short circuits because their reactance become low enough that the there are no significant voltage drops across the capacitors.**
- **At low frequencies .the coupling capacitors Cc, Cs and Cg could no longer be treated as short circuits because their reactance become high enough that the there are significant voltage drops across the capacitors.**

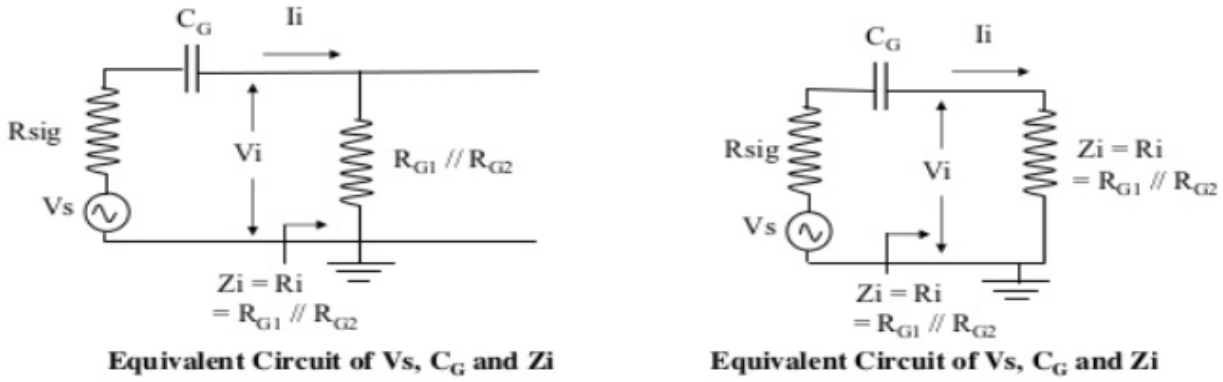


Figure 4.29 Equivalent circuit CG

- **The frequency analysis of high pass RC network can be used for capacitor coupled FET amplifer circuit.**
- **For the portion of the circuit involving the coupling capacitors Cg, the equivalent circuit**
    - **Equivalent circuit assumes that the input impedance of the amplifier (Zi) is purely resistive and is equal to Ri**

Case 1 : Considering C_G and other C_D, C_S are short circuit

The value of the input impedance (resistance) of the amplifier can be computed

$$Zi = Ri = R_{G1} // R_{G2}$$

$Zi = R_{G2}$ if R_{G1} is not present (R_{G1} = infinity)

$R = R_{sig} + R_i$ and $C = C_G$

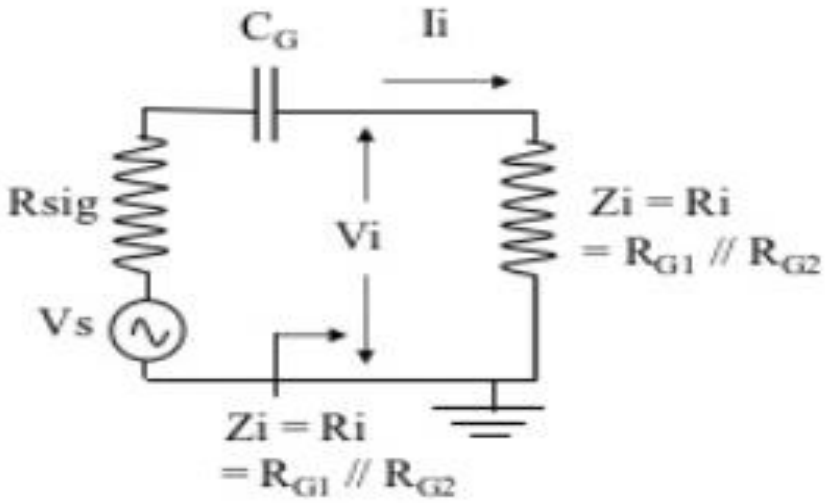


Figure 4.30 Equivalent circuit Ce with Zi

The lower cutoff frequency (half power frequency) can be computed as

$$f_{L_G} = \frac{1}{2\pi(Rsig + Ri)C_G}$$

Case 2 : Considering C_c and other C_G, C_S are short circuit

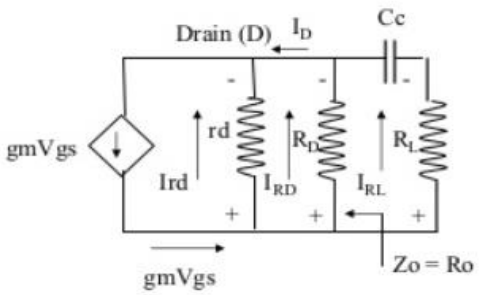


Figure 4.31 Equivalent circuit Zo

- **For the portion of the circuit involving the coupling capacitor Cc, the equivalent circuit is shown Figure 4.31.**
  - **Equivalent circuit assumes that the output impedance of the transistor is purely resistive and is equal to Ro**

The value of the output impedance (resistance) of the amplifier can be computed as

$Zo = Ro = R_D \parallel r_d$

If r_d is equal to unity

$Z_o = R_o = R_D$

The lower cut off frequency can be computed as

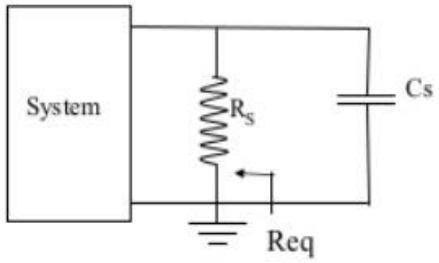
$f_{LC} = 1/2\pi(Ro + RL)Cc$

Case 3 : Considering C_S and other C_G, C_D are short circuit

- **For the portion of the circuit involving the bypass capacitor Cs, the equivalent circuit is shown in Figure.**
  - **The resistance (Req)seen looking into Rs, from the output side can be computed as:**

$R_{eq} = Rs \parallel 1/gm$

$R = R_{eq}$ and $C = C_S$



Equivalent Circuit of Portion of Circuit Involving R_S and C_S

Figure 4.32 Equivalent circuit Cs

- **The low cut off frequency of the portion of the circuit involving the bypass capacitor Cs can be computed as:**
- **$f_{LS} = 1/ 2\pi ReqCs$**

- **Overall , the effect of the capacitor Cg,Cc and Cs must be considered in determined the low cutoff frequency of the amplifier,**
- **The highest lower cutoff frequency among the three cutoff frequencies will have the greatest impact on the low cutoff frequency of the amplifier.**
- **If the cutoff frequencies due to the capacitors are relatively far apart , the highest low cutoff frequencies will essentially determine the low cutoff frequency .**

4.9 HIGH FREQUENCY RESPONSE OF BJT

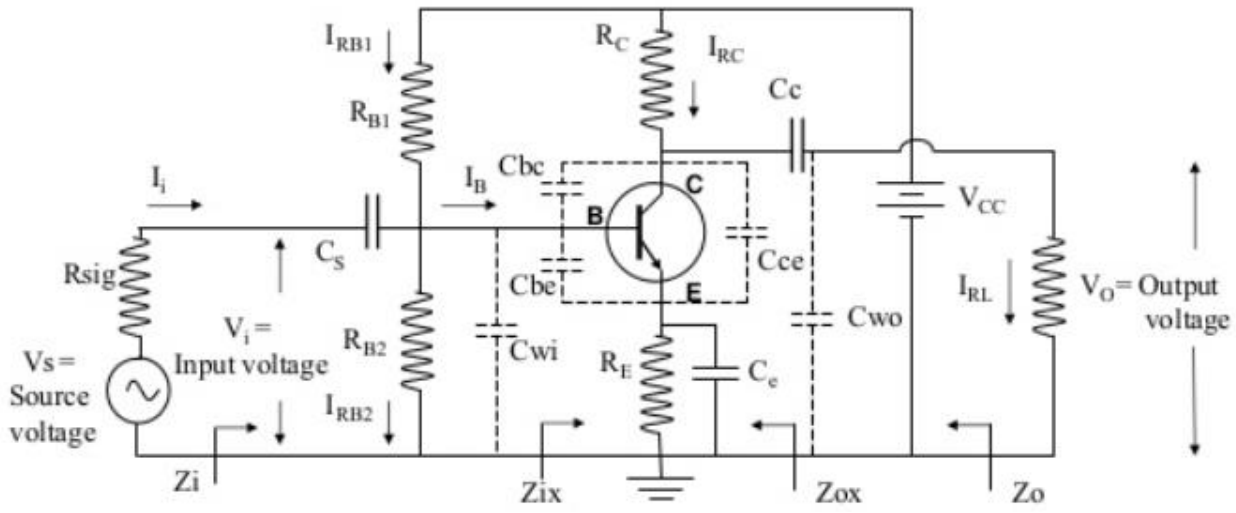


Figure 4.33 High frequency Response of BJT

Cbe =capacitance between the base and emitter of the transistor

Cce= capacitance between the collector and emitter of transistor

Cbc = capacitance between the base and collector of transistor

Cwi= wiring capacitor at input of amplifier

Cwo = wiring capacitor at output of amplifier

- **At the higher frequency end the higher cut off frequency(-3db) of BJT circuits is affected by:**
  - **Network capacitance (parasitic and induced)**
  - **Frequency dependence of the current gain hfe**
- **At high frequencies , the high cutoff frequency of a BJT circuit is affected by:**
  - **The interelectrode capacitance between the base and emitter , base and collector, collector and emitter.**
  - **Wiring capacitor at the input and output of the BJT**
  - **At high frequencies, the reactance of the interelectrode and wiring capacitor become significantly low, resulting to a "shorting" effect across the capacitance .**
  - **The "shorting" effect at the input and output of an amplifier causes a reduction in the gain of the amplifier**

Input and output capacitances are given by

$$Ci = Cwi + Cbe + C_{Mi} \qquad Co = Cwo + Cce + C_{Mo}$$

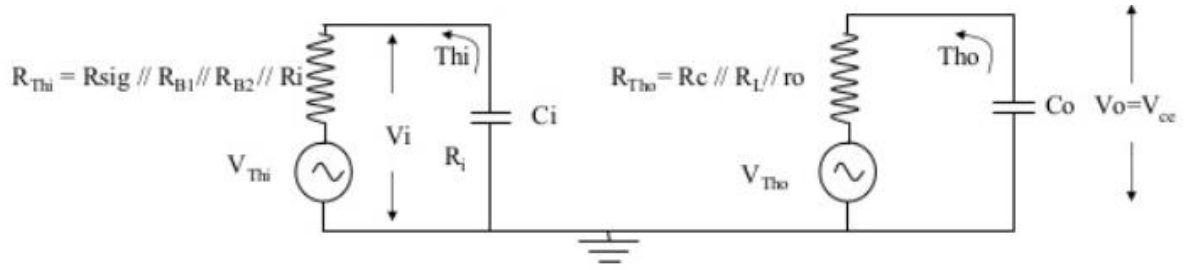


Figure 4.34 High frequency Response – Ci capacitance

- For the ***input side***, the ***-3db high cutoff frequency*** can be computed as:

$$f_{Hi} = \frac{1}{2\pi R_{Thi} Ci} = \text{higher cut off frequency for the input side (-3db frequency)}$$

$$R_{THi} = Rsig // R_{B1} // R_{B2} // Ri = Rsig // R_{B1} // R_{B2} // (\beta + 1)re$$
$$= \text{Thevenin equivalent resistance at input side}$$

$$C_i = C_{wi} + C_{be} + C_{Mi} = C_{wi} + C_{be} + (1 - Av)C_{bc} = \text{input capacitance of circuit}$$

- **At the high frequency end, the reactance of the capacitance Ci will deacrease as frequency increases, resuting to reduction in the total impedance at the input side**
  - **This will result to lower voltage across Ci, resulting to lower base current ,and lower voltage gain**

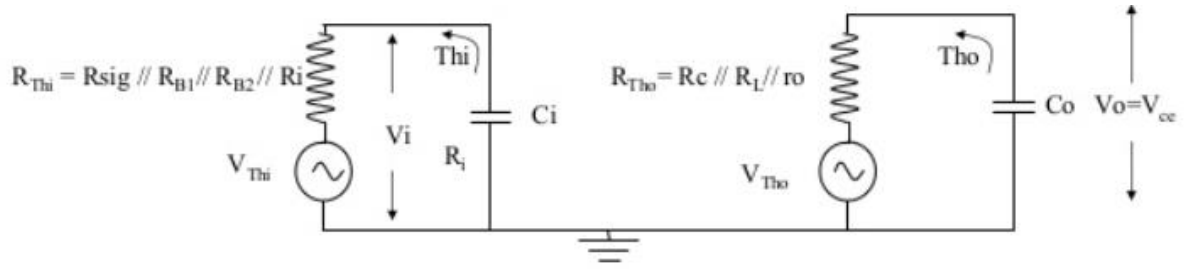


Figure 4.35 High frequency Response – Co capacitance

- For the ***output side***, the ***-3db high cutoff frequency*** can be computed as:

$$f_{Ho} = \frac{1}{2\pi R_{Tho} C_o} = \text{higher cut off frequency for the output side (-3db frequency)}$$

$$R_{Tho} = R_c \,//\, R_L \,//\, r_o = \text{Thevenin equivalent resistance at output side}$$

$$C_o = C_{wo} + C_{ce} + C_{Mo} = C_{wo} + C_{ce} + \left[1 - \frac{1}{A_V}\right] C_{bc} = \text{output capacitance of circuit}$$

- **At the high frequency end , the reactance of capacitance Co will decrease as frequency increases, resulting to reduction in the total impedance at the output side**
  - **This will result to lower output voltage Vo, resulting to lower voltage and power gain .**

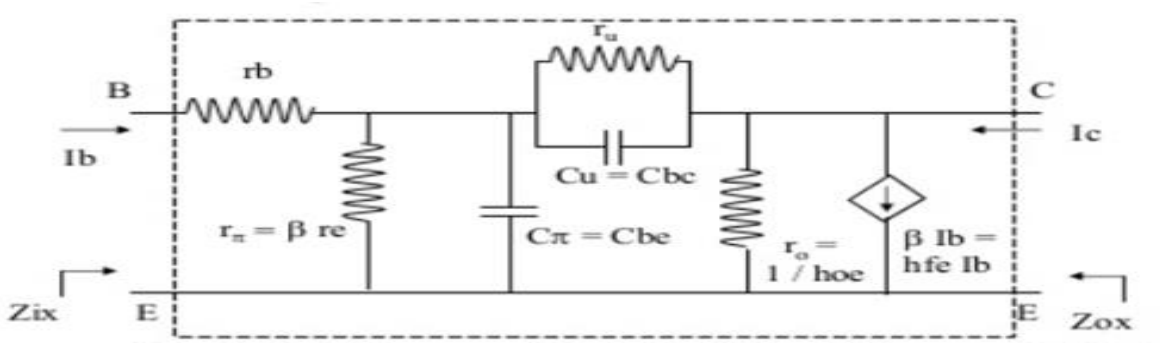


Figure 4.36 High frequency Response – Hybrid pi Model

- **The hybrid π high frequency equivalent circuit for common emitter.**
- **The resistance rb includes the base contact resistance (due to actual connection to the base) base bulk resistance (resistance from external base terminal to the active region of transistor) and base spreading resistance (actual resistance within with active region of transistor)**
- **The resistances rg , r0 and ru are the resistance between the indicated terminals**
- **When the BJT is in the active region**
- **Cbe and Cbc are the capacitance between the indicated terminals**
  - **At the high frequency end, hfe of a BJT will be reduced as frequency increases**

- **The variation of hfe with frequency can approximately be computed as:**

$$hfe = \frac{hfe_{mid}}{1 + j\frac{f}{f_\beta}} = \text{hfe at frequency f}$$

$hfe_{mid} = \beta_{mid} =$ hfe at middle frequency (the one usually given at specs sheet)

$$f_\beta = f_{hfe} = \frac{1}{2\pi\, r_\pi\,(C\pi + Cu)} = \frac{1}{hfe_{mid}} \frac{1}{2\pi\, re\,(C\pi + Cu)}$$

$$f_\beta \cong \frac{1}{\beta_{mid}} \frac{1}{2\pi\, re\,(C\pi + Cu)}$$

$$r_\pi = \beta_{mid}\, r_e = (hfe_{mid})(r_e)$$

$$r_e = \frac{26mV}{I_E}$$

$I_E =$ DC emitter current of transistor

- **The upper cutoff frequency of the entire system (upper limit for the bandwidth) is lower than the lowest upper cutoff frequency (lowest among f_{Hi} , f_{HO} and $f\beta$**
- **The lowest upper cutoff frequency has the greatest impact on the bandwidth of the system. it defines a limit for the bandwidth of the system**
- **The lower is the upper cut off frequency, the greater is its effect on the bandwidth of the entire system**

4.10 GAIN BANDWIDTH PRODUCT:

The Gain-Bandwidth of the circuit (usually amplifier) is the product of the bandwidth and the gain at which the bandwidth is measured. For an operational amplifier, the gain-bandwidth product for one configuration will always equal the gain-bandwidth product for any other configuration of the same amplifier.

- The ***gain-bandwidth product of a transistor*** is defined by the following ***condition***:

$$hfe = \left|\frac{hfe_{mid}}{1 + j\frac{f}{f_\beta}}\right| = 1 \qquad \text{and} \quad hfe_{db} = 20\log\left|\frac{hfe_{mid}}{1 + j\frac{f}{f_\beta}}\right| = 20\log 1 = 0\,db$$

The frequency at which hfe_{db} is equal to 0db is denoted by f_T, and the magnitude of hfe when ($f_T >> f_\beta$) is computed as :

$$\frac{hfe_{mid}}{\sqrt{1+\left(\frac{f_T}{f_\beta}\right)^2}} \cong \frac{hfe_{mid}}{\frac{f_T}{f_\beta}} = 1$$

$f_T \approx (hfe_{mid}) (f\beta) = (\beta_{mid}) (f\beta) =$ Gain bandwidth product , since β_{mid} is gain $f\beta$ bandwidth

Bandwidth $f\beta \approx f_T / \beta_{mid}$

$$\boxed{f_\beta \cong \frac{f_T}{\beta_{mid}} \cong \text{bandwidth}}$$

$$f_T \cong (\beta_{mid})(f_\beta) = (\beta_{mid})\left[\frac{1}{\beta_{mid}}\frac{1}{2\pi re(C\pi + Cu)}\right]$$

$$\boxed{f_T \cong \frac{1}{2\pi re(C\pi + Cu)}} = \text{gain bandwidth product}$$

4.11 FET High Frequency Responses

FET HIGH FREQUENCY RESPONSE

- **The high frequency response analysis for FET is similar to that of BJT.**
- **At the high frequency end, the high cutoff frequency(-3db) of FET circus is affected by the network capacitance (parasitic and induced).**
- **The capacitance that affect the high frequency response of the circuit are composed of:**
  - **The inter-electrode capacitance between the gate and source, gate and drain, and drain and source.**
  - **Wiring capacitance at the input and output of the circuit.**
- **At high frequencies, the reactance of the inter electrode and wiring capacitance because significantly low, resulting to a "shorting" effect across the capacitances.**
- **The shorting effect at the input and out of an amplifier causes a reduction in the gain of the amplifier**
- **For common source FET circuits, the Miller effect will be present, since it is an inverting amplifier.**

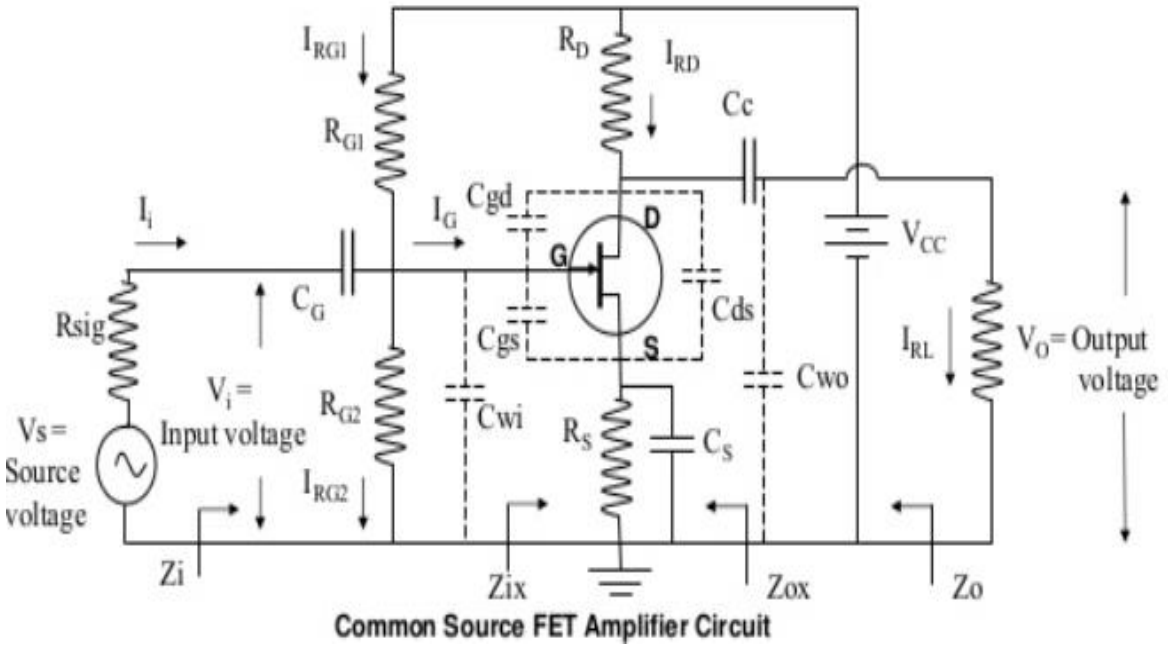


Figure 4.37 Common source FET amplifier circuit

- **Cgs = capacitance between the gate and source of transistor**
- **Cds = capacitance between drain and source of transistor**
- **Cgs = capacitance between gate and source of transistor**
- **Cwi = wiring capacitor at input of amplifier**
- **Cwo = wiring capacitance at output of amplifier**

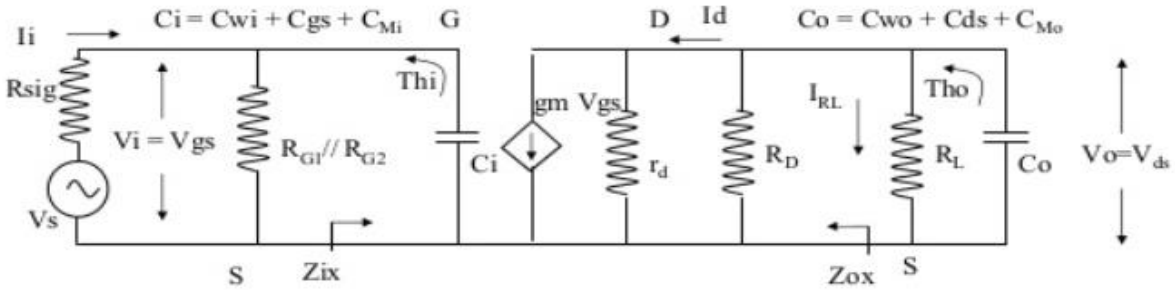


Figure 4.33 Equivalent circuit for Common source FET amplifier

- **At mid and high frequencies, C_G,C_S , and C_C are assumed to be short circuits because Their impedances are very low.**
- **The input capacity C_i includes the input wiring capacitance(Cwi), the transistor capacitance Cgs, and the input Miller capacitance C_{Mi}**
- **The output capacitance Co includes the output wiring capacitance (Cwo),the transistor parasitic capacitance Cds, and the output Miller capacitance C_{MO}.**
- **Typically, Cgs and Cgd are higher than Cds.**

- **At high frequencies ,Ci will approach a short–circuit and Vgs will drop, resulting to reducing in voltage gain.**
- **At high frequencies, Co will approach a short-circuit and Vo will drop, resulting to reduction in voltage gain.**

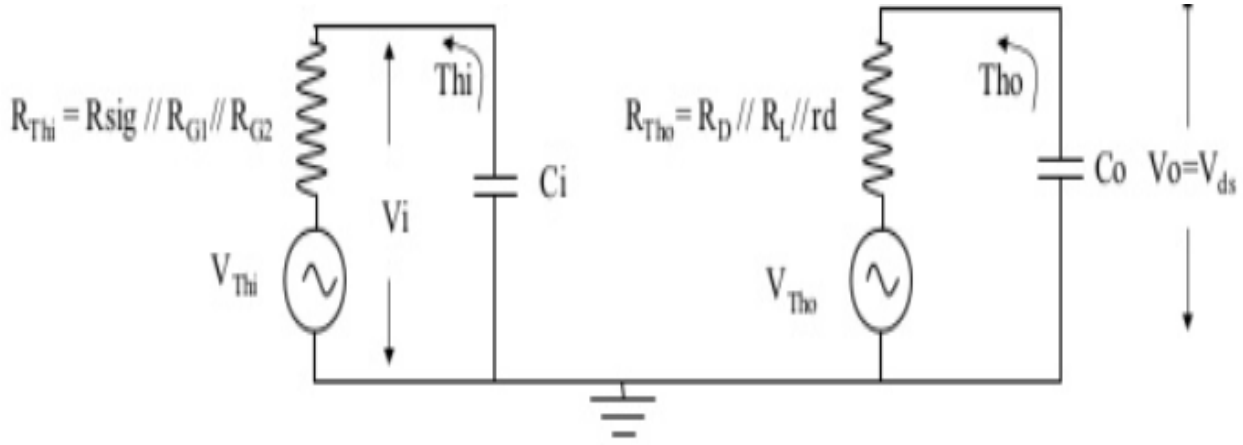


Figure 4.34 Equivalent circuit for Common source FET amplifier- Ci & Co capacitance

- The ***Thevenin equivalent*** circuit of the ac equivalent circuit of the FET amplifier is shown below.
- For the ***input side***, the ***-3db high cutoff frequency*** can be computed as:

$$f_{Hi} = \frac{1}{2\pi R_{Thi} C_i} = \text{high cut off frequency for the input side (-3db frequency)}$$

$$R_{THi} = Rsig // R_{G1} // R_{G2} = \text{Thevenin equivalent resistance at input side}$$

$$C_i = C_{wi} + Cgs + C_{Mi} = \text{input capacitance of circuit}$$

$$C_{Mi} = [1 - Av]Cgd = \text{Miller effect capacitance at input side}$$
where Avmid is used for Av to get the worst case scenario

FET High Frequency Response

- For the ***output side***, the ***-3db high cutoff frequency*** can be computed as:

$$f_{Ho} = \frac{1}{2\pi R_{THo} C_o} = \text{high cut off frequency for the output side (-3db frequency)}$$

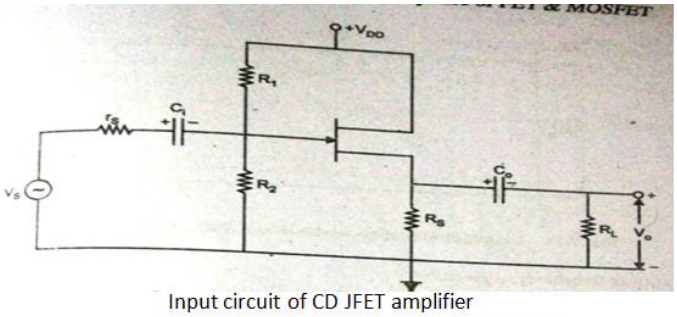
$$R_{THo} = R_D // R_L // rd = \text{Thevenin equivalent resistance at output side}$$

$$C_o = C_{wo} + Cds + C_{Mo} = \text{output capacitance of circuit}$$

$$C_{Mo} = \left[1 - \frac{1}{Av}\right] Cgd = \text{Miller effect capacitance at the output side}$$

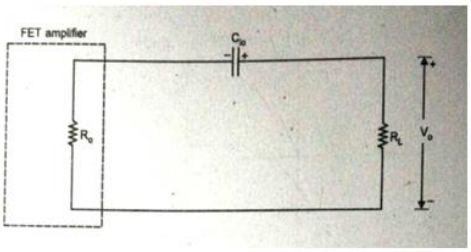
Avmid is used for Av to get the worst case scenario

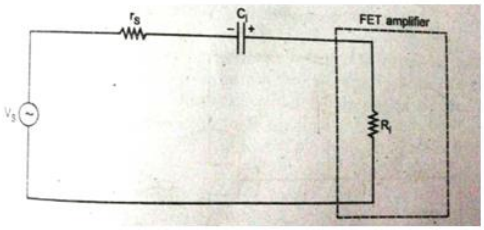
4.12 COMMON DRAIN JFET AMPLIFIER – LOW FREQUENCY RESPONSE



Input circuit of CD JFET amplifier

Output circuit of CD JFET amplifier





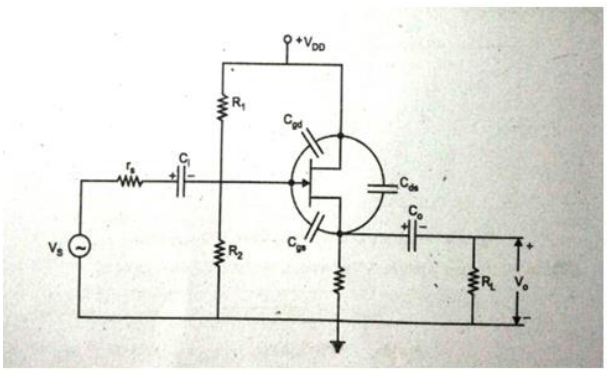
fci = 1/ 2∏(Ri + rs) Ci & Ri = Rs ‖ 1/gm ‖ R1 ‖ R2

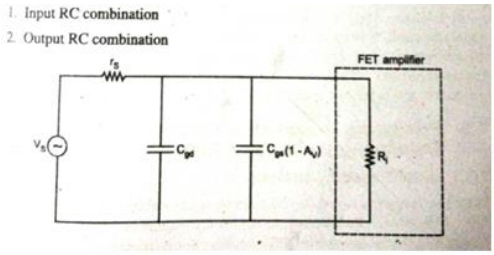
fco= 1/ 2∏(Ro + R_L) Co and Ro= r_D ‖ R_D

r_D - AC resistance or Inbuilt resistance of drain terminal

Figure 4.35 Analysis of Common drain amplifier Low frequency- Ci & Co capacitance

COMMON DRAIN JFET AMPLIFIER- HIGH FREQUENCY RESPONSE





fhi = 1/ 2∏(Ri + rs) Ci

Ci = Cgs + Cgd(1-Av) and Ri = R1 ‖ R2

Inter-electrode capacitance Cgs provides a feedback path from gate to source
Inter-electrode capacitance Cgd provides a feedback path from gate to drain
Inter-electrode capacitance Cds provides a feedback path from drain to source

fho = 1/ 2∏(Ro ‖ R_L) Co

Co = Cds + Cgd(1-1/Av)

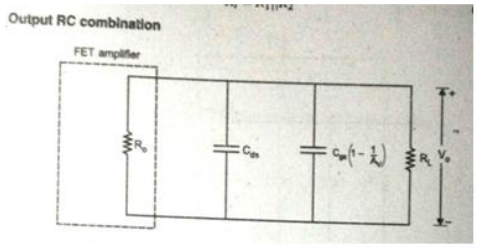
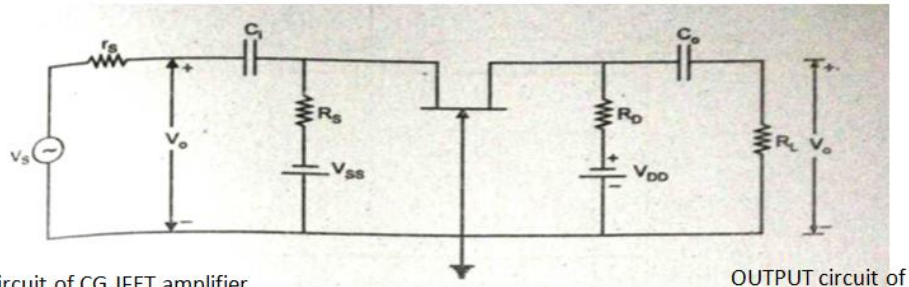


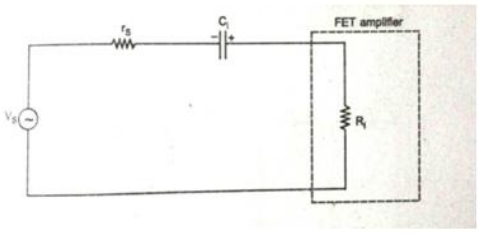
Figure 4.36 Analysis of Common drain amplifier High frequency- Ci & Co capacitance

4.13 COMMON GATE JFET AMPLIFIER – LOW FREQUENCY RESPONSE



Input circuit of CG JFET amplifier

OUTPUT circuit of CG JFET amplifier



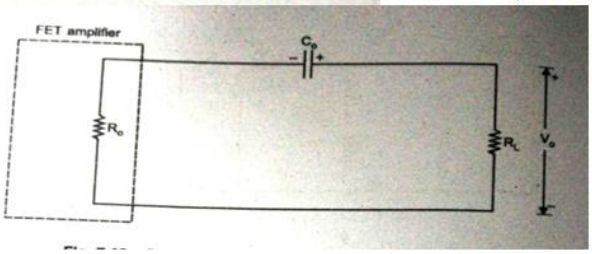


Figure 4.37 Analysis of Common gate amplifier Low frequency- Ci & Co capacitance

fci = 1/ 2∏(Ri + rs) Ci

fco= 1/ 2∏(Ro + R_L) Co and Ro= r_D ‖ R_D

COMMON GATE JFET AMPLIFIER – HIGH FREQUENCY RESPONSE

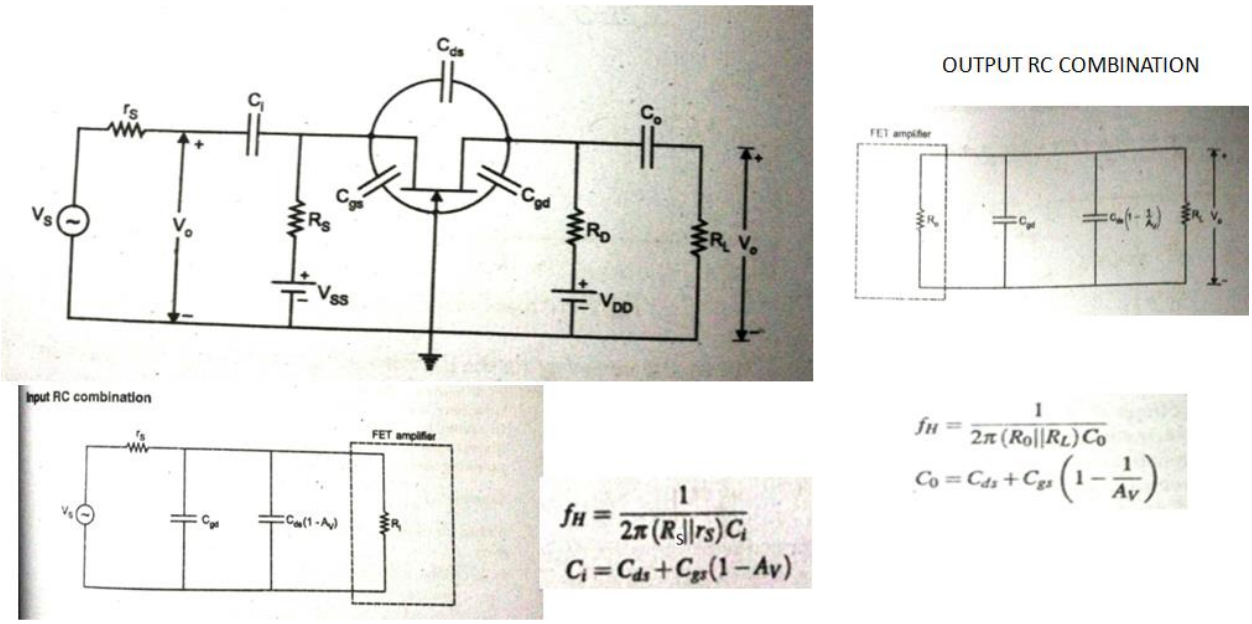
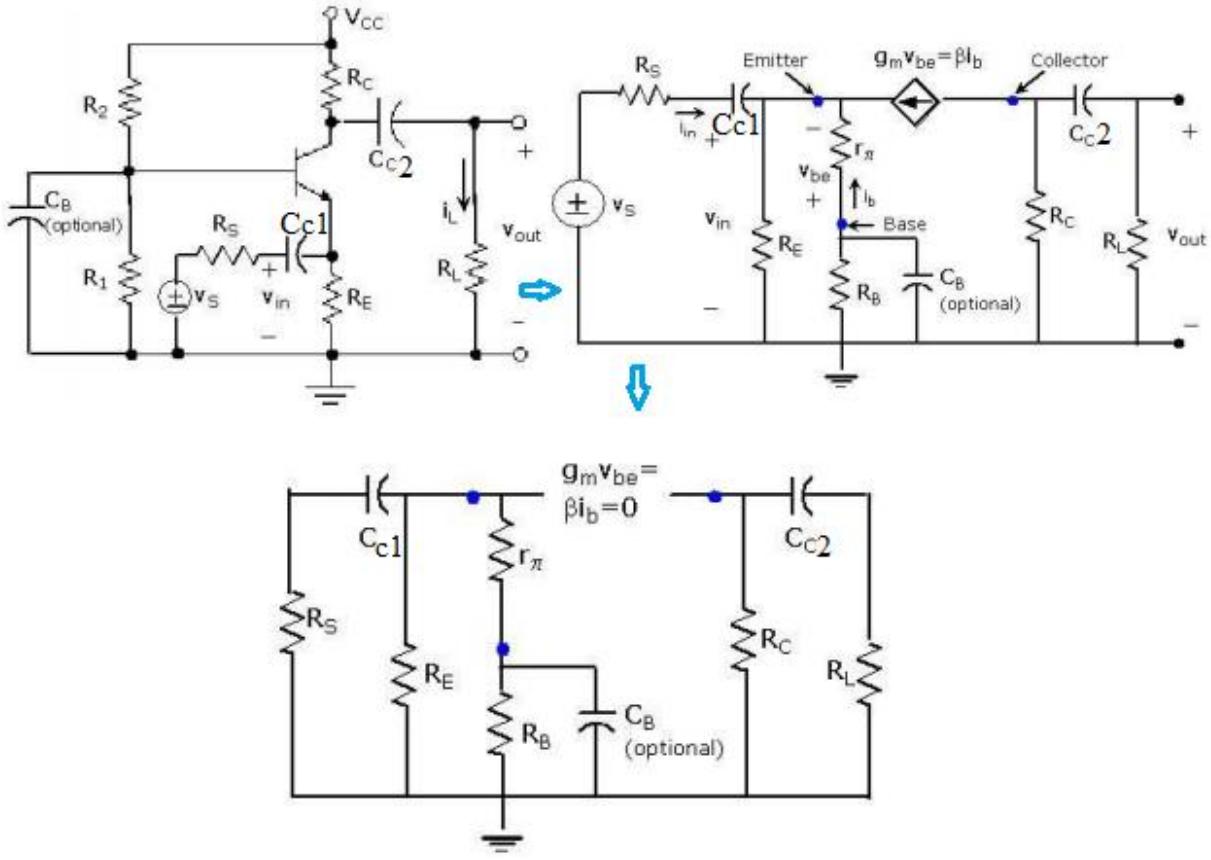


Figure 4.38 Analysis of Common gate amplifier High frequency- Ci & Co capacitance

4.14 COMMON BASE LOW FREQUENCY RESPONSE

Both voltage and current biasing follow the same rules as those applied to the common emitter amplifier. As before, insert a blocking capacitor in the input signal path to avoid disturbing the dc bias. The common base amplifier uses a bypass capacitor – or a direct connection from base to ground to hold the base at ground for the signal only! The common emitter amplifier (except for intentional RE feedback) holds the emitter at signal ground, while the common collector circuit does the same for the collector.



Steps 1: D C voltage sources are replaced by ground
2: D C current sources are open circuited
3: Capacitors are shorted

Case 1: Consider Cc1 and Cc2 shorted

R_B is redundant

$r_{\prod}$ base to emitter junction $r_{\prod / (1+\beta)}$

R1 = $r_{\prod / (1+\beta)}$ is parallel with RE + Rs ; C= Cc1

F1= $1 / 2_{\prod R1Cc1}$

Case 2: Consider CB and Cc1 shorted

Emitter to base $(R_s \parallel R_E) * (1+\beta)$

R2 = $\{ (R_s \parallel R_E) * (1+\beta) + r_{\prod} \} \parallel R_B$

F2 =$1 / 2_{\prod} R_2 C_B$

Case 3

R3= Rc+RL

F3 = 1 / $2_{\prod} R_3C$

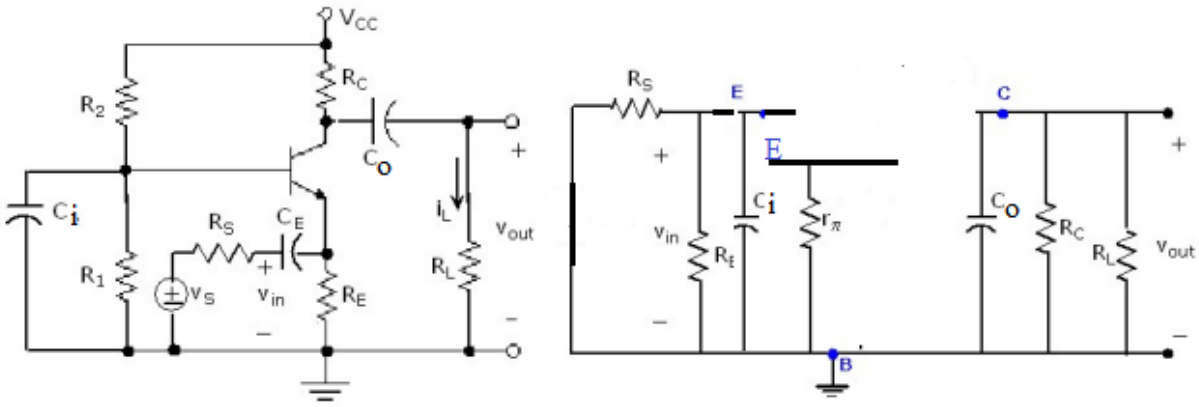
COMMON BASE HIGH FREQUENCY RESPONSE

Note that, unlike the CE/ER amplifier, no internal feedback capacitance exists for the common base configuration. This is the most important characteristic of the CB stage and means that there is no Miller effect, which means that the capacitances are smaller, which means that the cutoff frequency will be higher.

Using the method of open circuit time constants, we can define equivalent resistances for each of the remaining capacitances. With vS=0 and, therefore, gmvbe=0

since Cb'e and re are quite small. At such high frequencies, it is often necessary to take into account effects that may generally be considered negligible.

- **AC & DC Grounded**
- **Capacitance is shorted and RB is redundant**
- **No Miller capacitance**
- **Cπ and Cμ are present**
- **Wire capacitances are present**
- **Vi=0 and gm Vπ = 0 current source is open**



Ci = Cwi + Cπ

Co = Cwo + Cμ

Ri= $R_E \parallel R_S \parallel r_{\prod / (1+\beta)}$

Ro = $R_L \parallel R_C$

Fhi =1 / $2_{\prod} R_iC_i$

Fho =1 / $2_{\prod} R_oC_o$

4.15.High-Frequency Response -MOSFET
(Amplifier gain falls off due to the internal capacitive effects of transistors)

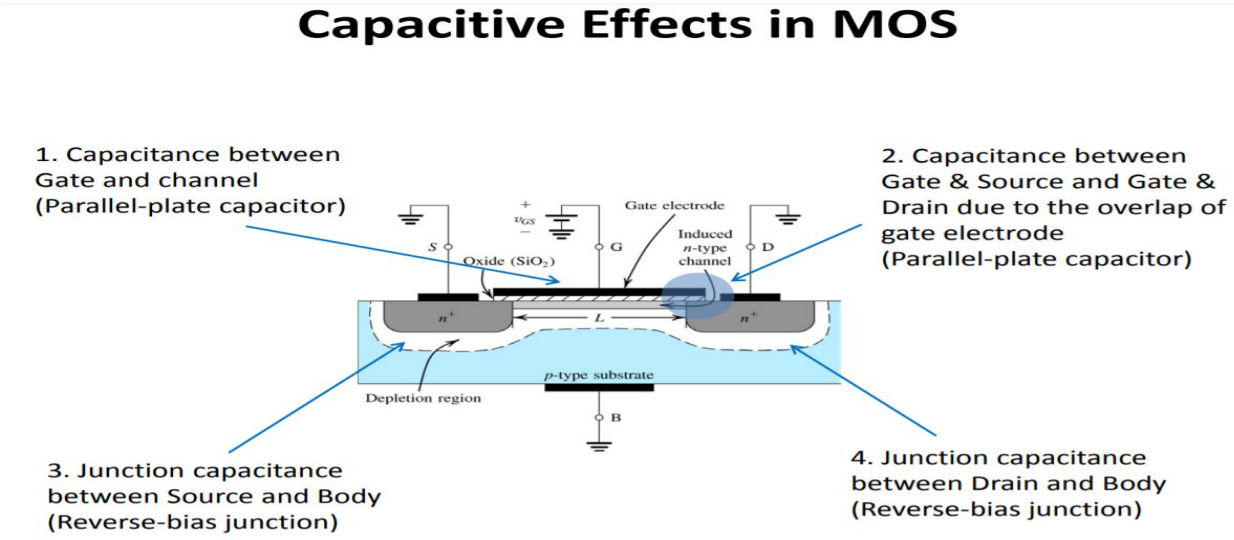


Figure 4.39 Capacitive effects in MOSFET

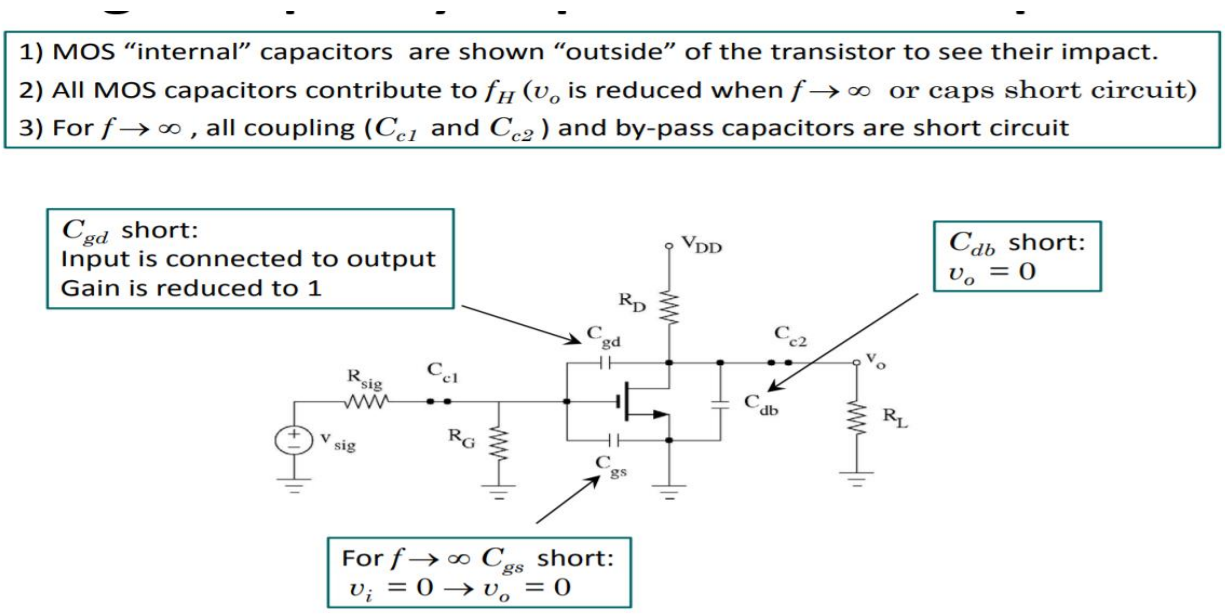


Figure 4.40 Capacitive effects in MOSFET- Cgd,Cdb,Cgs

MOSFET LOW FREQUENCY COMMON SOURCE RESPONSE

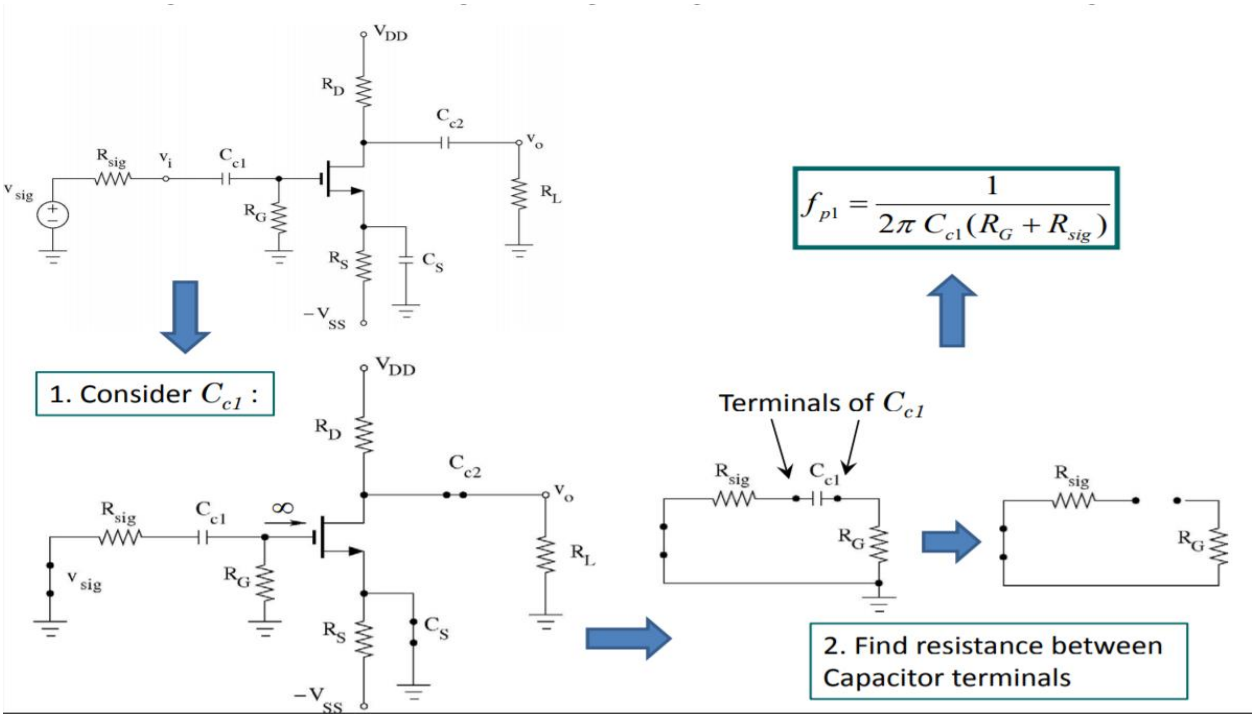


Figure 4.41 MOSFET Low Frequency Common Source Response- Cc1 capacitance

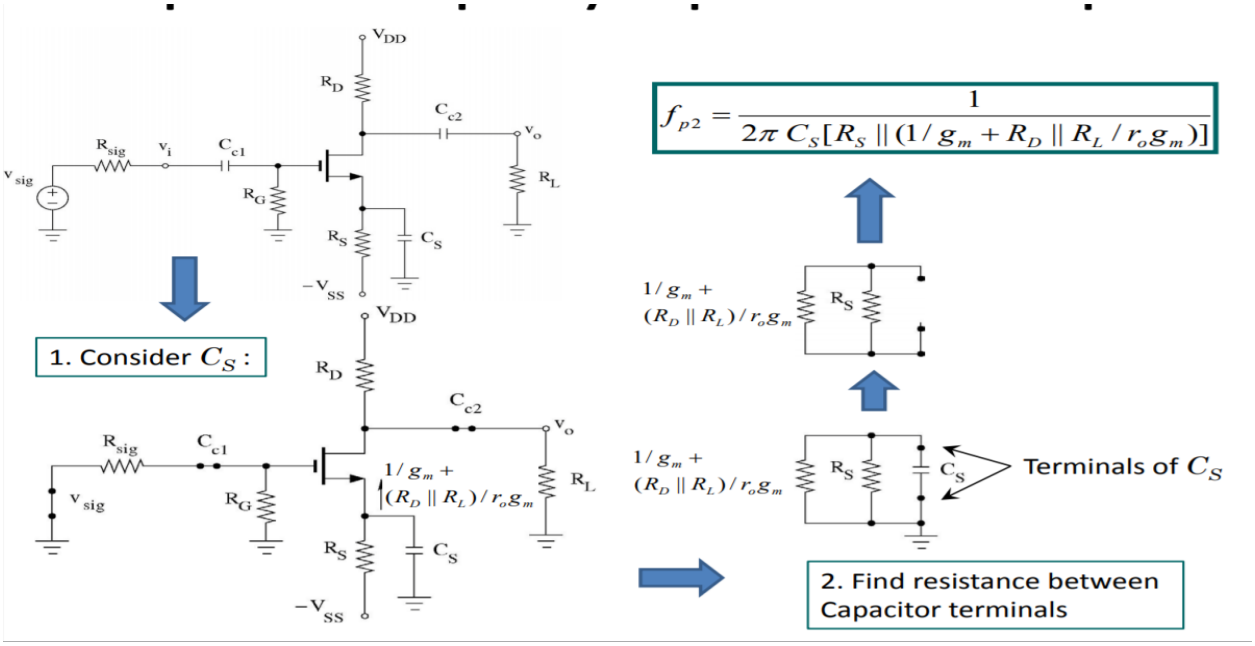


Figure 4.42 MOSFET Low Frequency Common Source Response- Cs capacitance

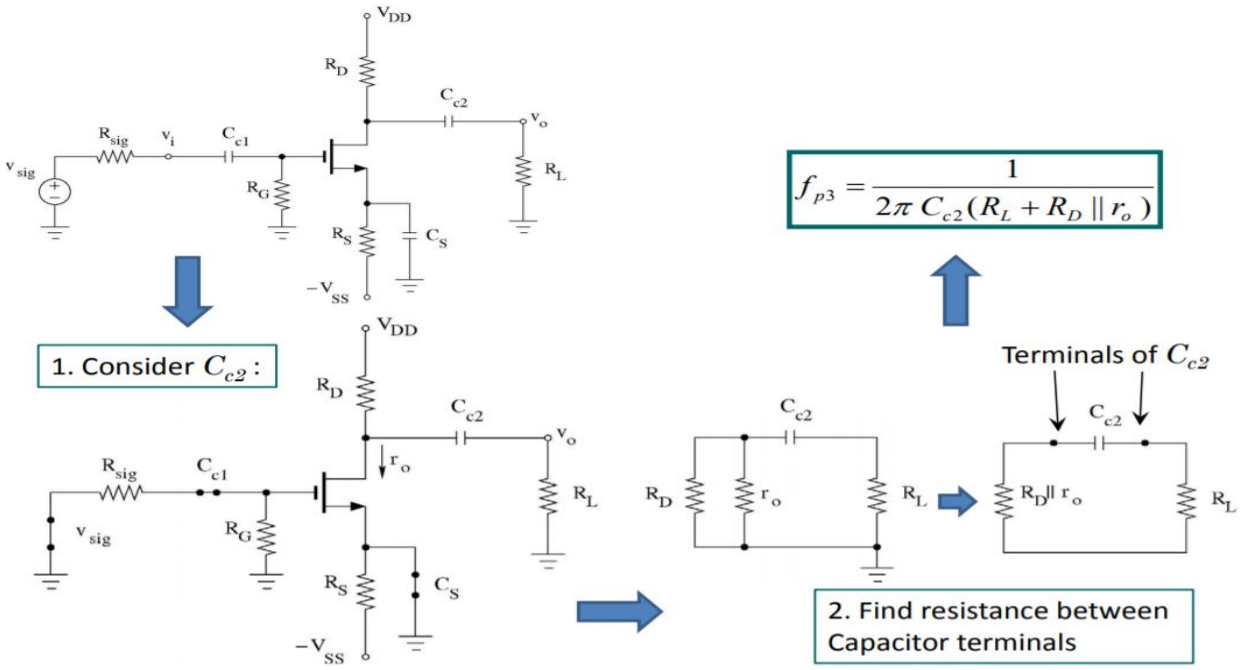


Figure 4.43 MOSFET Low Frequency Common Source Response- Cc2 capacitance

CS High-Frequency Response –MOSFET

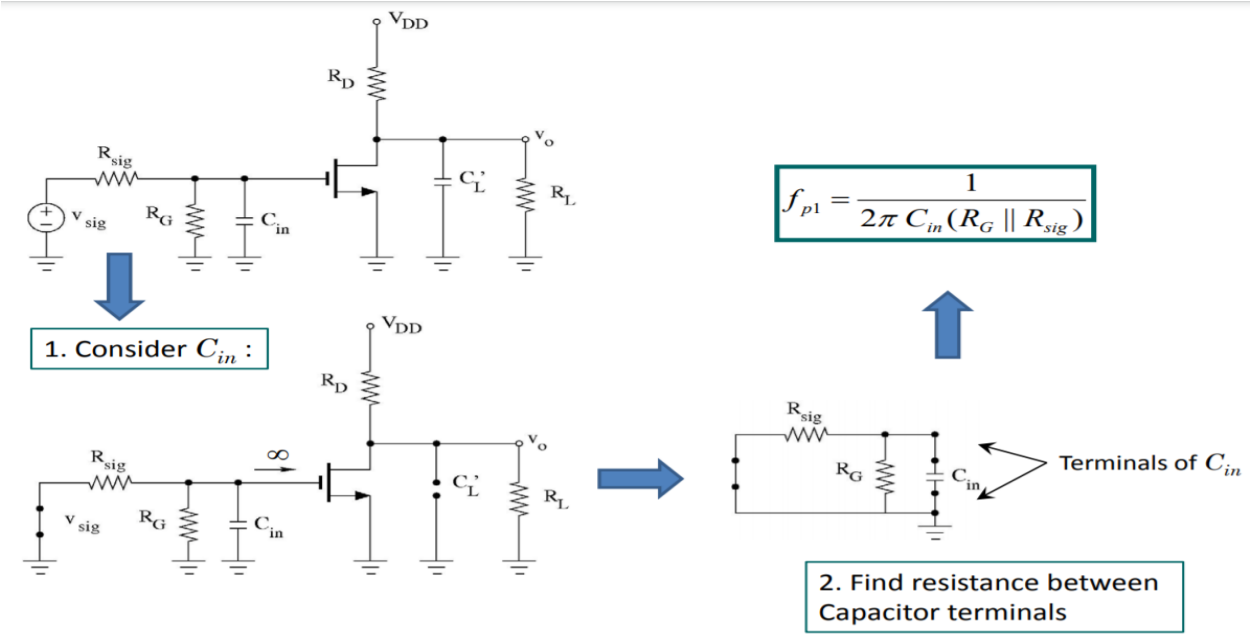


Figure 4.44 MOSFET High Frequency Common Source Response- Cin capacitance

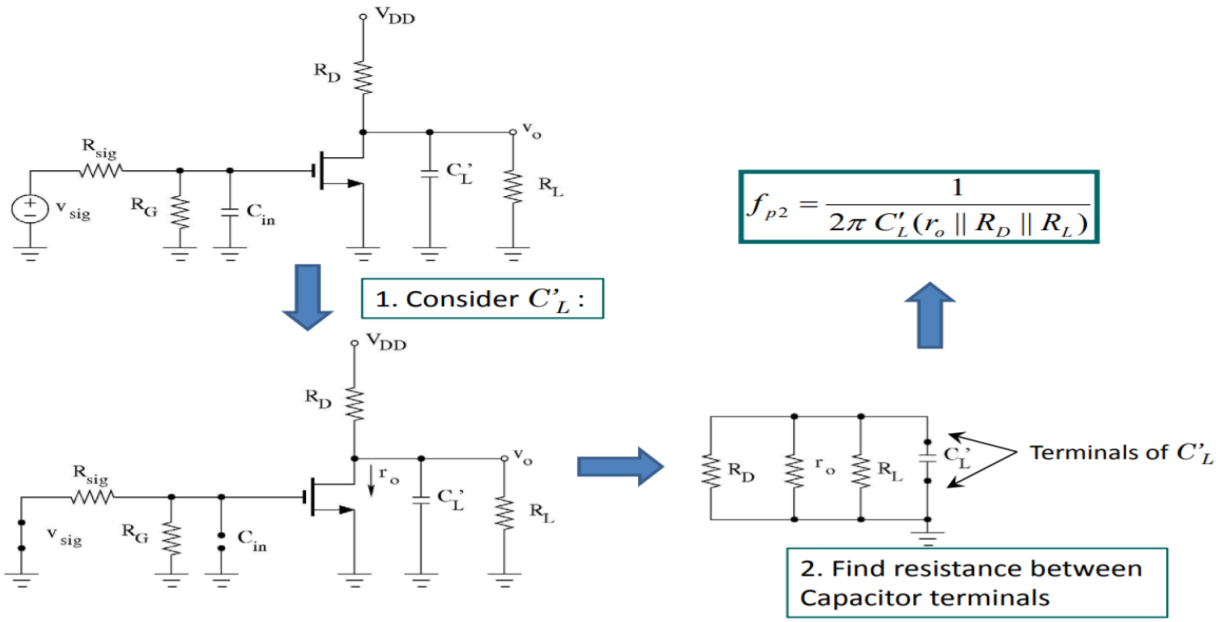


Figure 4.45 MOSFET High Frequency Common Source Response- Cin capacitance

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SCHOOL OF ELECTRICAL AND ELECTRONICS

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

UNIT-V

ELECTRONIC CIRCUITS-I– SECA1302

UNIT 5 POWER SUPPLIES AND POWER AMPLIFIERS 9 Hrs

Linear mode power supply - Rectifiers - Half-Wave Rectifier - Full-Wave Rectifier – Filters - L,C, LC, CLC Filter- Regulators - Zener Diode regulator - Linear series, shunt voltage Regulators - Switched mode power supply (SMPS) - Large Signal Amplifiers - Class A, Class B, Class C, Class D- Distortion in power amplifiers

Linear mode power supply: A regulated DC power supply is also known as a linear power supply; it is an embedded circuit and consists of various blocks. The regulated power supply will accept an AC input and give a constant DC output. The figure below shows the block diagram of a typical regulated DC power supply.

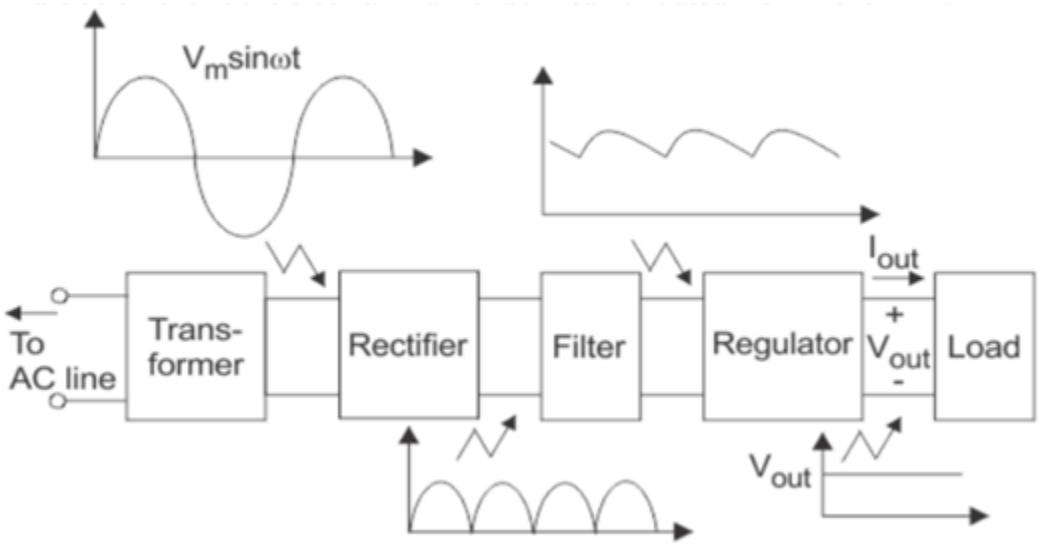


Figure 5.1 Block diagram of linear regulated power supply

- Linear regulated power supplies gain their name from the fact that they use linear, i.e. non-switching techniques to regulate the voltage output from the power supply.
- The term linear power supply implies that the power supply is regulated to provide the correct voltage at the output.
- The voltage is sensed and this signal is fed back, normally into some form of differential amplifier where it is compared with a reference voltage, and resulting signal is used to ensure the output remains on the required voltage.

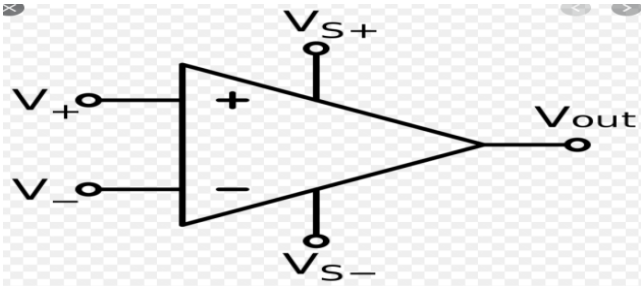


Figure 5.2 Differential Amplifier

Power supply input transformer:

- As many regulated power supplies take their source power from an AC mains input, it is common for linear power supplies to have a step down or occasionally a step up transformer.
- This also serves to isolate the power supply from the mains input for safety.
- The transformer is typically a relatively large electronic component, especially if it is used in a higher power linear regulated power supply.
- The transformer can add significant weight to the power supply, and can also be quite costly, especially for the higher power ones.

Rectifier:

- As the input from an AC supply is alternating, this needs to be **converted to a DC format**. Various forms of rectifier circuit are available.
- The simplest form of rectifier that could be used in a power supply is a single diode, providing **half wave rectification**. This approach is not normally used because it is more difficult to satisfactorily smooth the output.
- Normally **full wave rectification**, using both halves of the cycle is used. This provides a waveform that can be more easily smoothed.
- There are two main approaches to providing half wave rectification. One is to use a **centre tapped transformer and two diodes**. The other is to use a single winding on the power supply transformer and to use a **bridge rectifier with four diodes**.
- As diodes are very cheap, and the cost of providing a centre tapped transformer is more, the most common approach these days is to use **a bridge rectifier**.

Power supply smoothing:

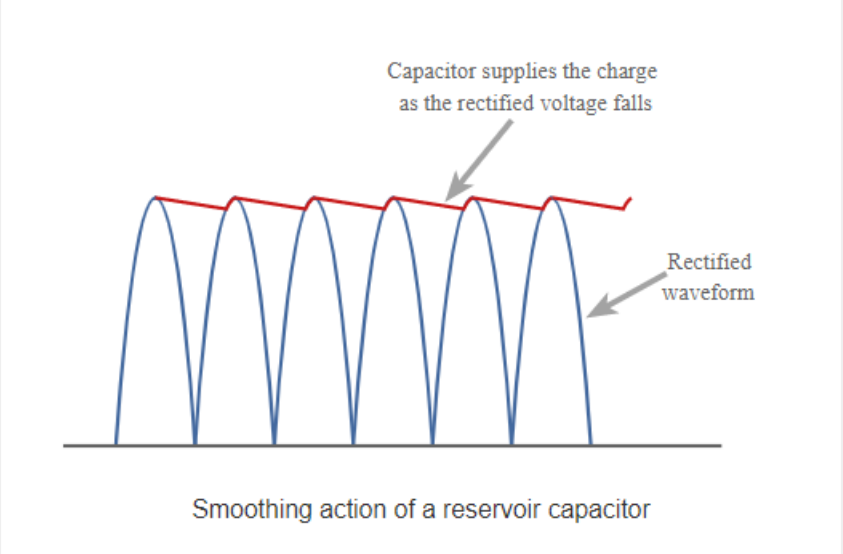


Figure 5.3 Smoothing action of a Capacitor

Once rectified from an AC signal, the DC needs to be smoothed to remove the varying voltage level. **Large reservoir capacitors are used for this**.

The smoothing element of the circuit uses a large capacitor. This charges up as the incoming waveform from the rectifier rises to its peak. As the voltage of the rectified waveform falls away, once the voltage is below that of the capacitor, the capacitor starts to supply charge, holding the voltage up, until the next rising waveform from the rectifier.

Linear power supply regulators:

- There are two main types of linear power supply:

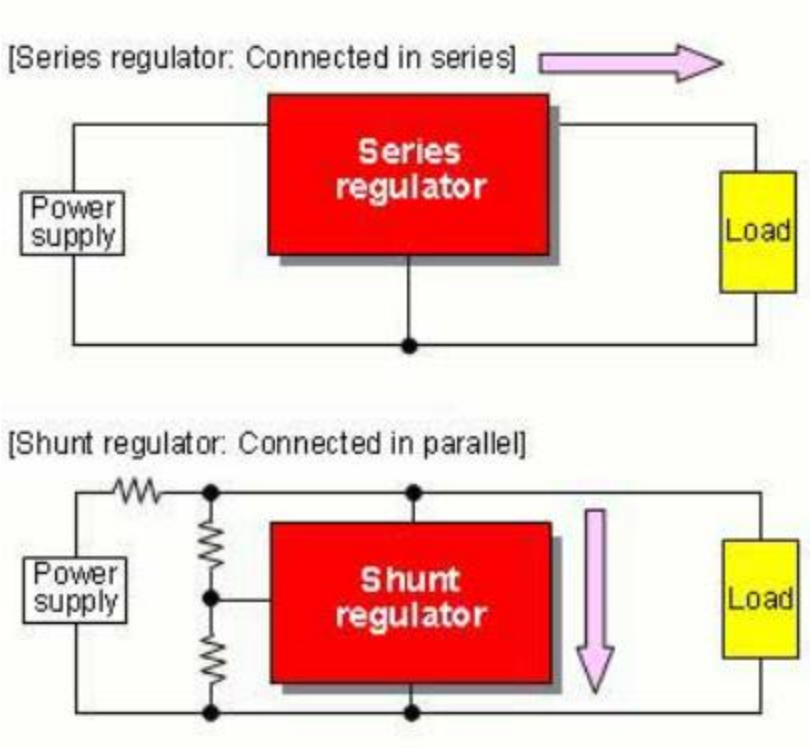


Figure 5.4 Shunt and Series regulator

- ***Shunt regulator:*** The shunt regulator is less widely used as the main element within a linear voltage regulator. For this form of linear power supply, **a variable element is placed across the load**.
- There is a source resistor placed in series with the input, and the shunt regulator is varied to ensure that the voltage across the load remains constant.
- ***Series regulator:*** This is the most widely used format for a linear voltage regulator. As the name implies a series element is placed in the circuit, and its resistance varied via the control electronics to ensure that the correct output voltage is generated for the current taken.
- A reference voltage is used to drive the series pass element which may be a **bipolar transistor or a FET.** The reference may just be a voltage taken from a reference voltage source, e.g. an electronic component such as a Zener diode.

Linear power supply advantages / disadvantages

- The use of any technology is often a careful balance of several advantages and disadvantages. This is true for linear power supplies which offer some distinct advantages, but also have their drawbacks.

Linear PSU advantages Established technology:

Linear power supplies have been in widespread use for many years and their 2 technology is well established and understood. Low noise: The use of the linear technology without any switching element means that noise is kept to a minimum and the annoying spikes found in switching power supplies are now found.

Linear PSU disadvantages Efficiency: In view of the fact that a linear power supply uses linear technology, it is not particularly efficient. Efficiencies of around 50% are not uncommon, and under some conditions they may offer much lower levels.

Heat dissipation: The use of a series or parallel (less common) regulating element means that significant amounts of heat are dissipated and this needs to be removed.

Size: The use of linear technology means that the size of a linear power supply tends to be larger than other forms of power supply. Despite the disadvantages, linear regulated power supply technology is still widely used, although it is more widely used where low noise and good regulation are needed. One typical application is for audio amplifiers where the linear supply is able to provide optimum performance for powering all the stages of the amplifier.

Rectifiers

- The main application of p-n junction diode is in rectification circuits.
- These circuits are used to describe the conversion of A.C signals to D.C in power supplies.
- A rectifier is an electrical device that converts alternating current (AC), which periodically reverses direction, to direct current (DC), which flows in only one direction.
- Diode rectifier gives an alternating voltage which pulsates in accordance with time. The filter smoothes the pulsation in the voltage and to produce D.C voltage, a regulator is used which removes the ripples.
- *There are two primary methods of diode rectification:*

1. Half Wave Rectifier
2. Full Wave Rectifier

Half Wave Rectifier

- In a half-wave rectifier, one half of each a.c input cycle is rectified.
- When the p-n junction diode is forward biased, it gives little resistance and when it is reversing biased it provides high resistance.
- During one-half cycles, the diode is forward biased when the input voltage is applied and in the opposite half cycle, it is reverse biased.

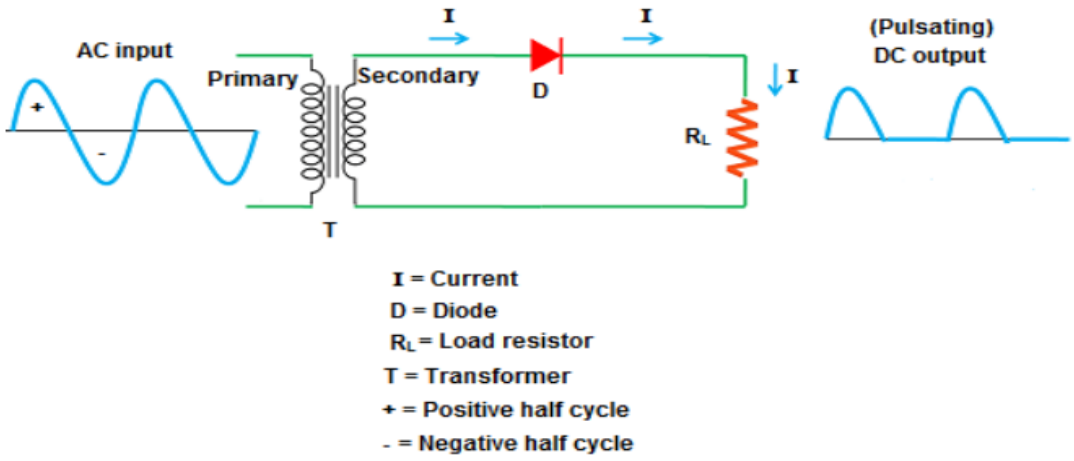


Figure 5.5 Half Wave Rectifier

- When A.C supply is applied to the transformer, the voltage will be decreasing at the secondary winding of the diode. All the variations in the A.C supply will reduce, and we will get the pulsating D.C voltage to the load resistor.
- In the second half cycle, the current will flow from negative to positive and the diode will be reverse biased. Thus, at the output side, there will be no current generated; a small amount of reverse current will flow during reverse bias due to minority carriers.

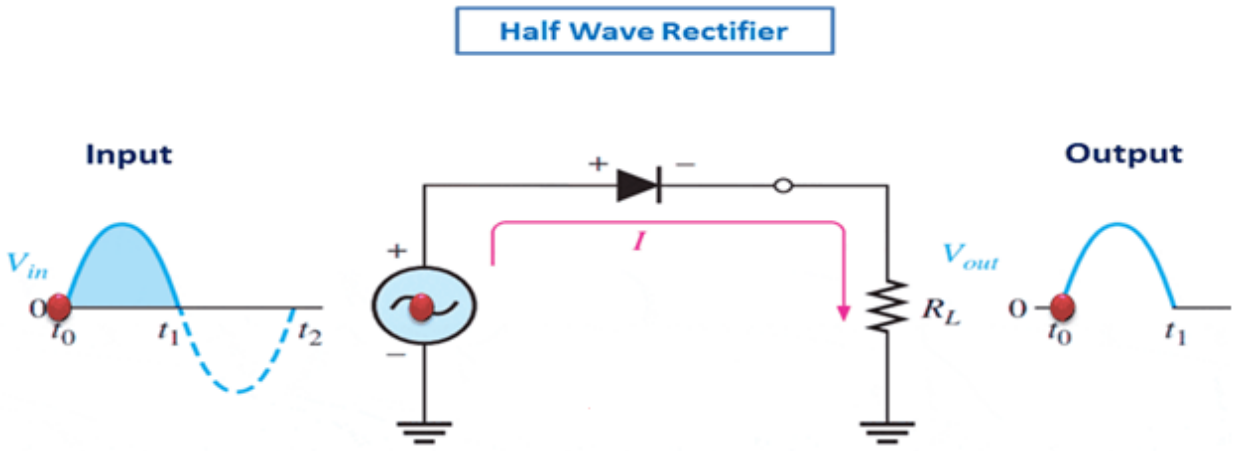


Figure 5.6 Working of Half Wave Rectifier

Average DC Load Current (I_{DC})

Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \qquad \text{for } 0 \le \omega t \le \pi$$

$$i_L = 0 \qquad \text{for } \pi \le \omega t \le 2\pi$$

where I_m = Peak value of load current

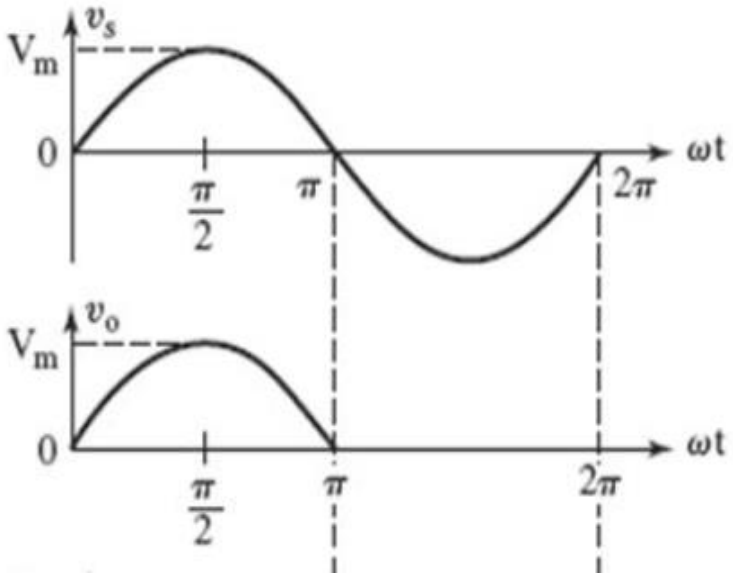


Figure 5.7 Load voltage wave forms for half wave rectifier

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(\omega t)\, d(\omega t)$$

As no current flows during negative half cycle of a.c. input voltage, i.e. between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t) = \frac{I_m}{2\pi}\left[-\cos(\omega t)\right]_0^{\pi}$$

$$= -\frac{I_m}{2\pi}\left[\cos(\pi) - \cos(0)\right] = -\frac{I_m}{2\pi}[-1-1] = \frac{I_m}{\pi}$$

$$\therefore \quad \boxed{I_{DC} = \frac{I_m}{\pi} = \text{average value}}$$

Applying Kirchhoff's voltage law we can write,

$$\boxed{I_m = \frac{E_{sm}}{R_f + R_L + R_s}}$$

where R_s = Resistance of secondary winding of transformer. If R_s is not given it should be neglected while calculating I_m.

Average DC Load Voltage (E_{DC})

It is the product **of average D.C. load current** and the load resistance R_L.

$$E_{DC} = I_{DC} R_L$$

Substituting **value of** I_{DC},

$$E_{DC} = \frac{I_m}{\pi} R_L = \frac{E_{sm}}{(R_f + R_L + R_s)\pi} R_L$$

The winding resistance R_s and forward diode resistance R_f are practically very **small** compared to R_L.

$$\therefore \quad \boxed{E_{DC} = \frac{E_{sm}}{\pi\left[\frac{R_f + R_s}{R_L} + 1\right]}}$$

But as R_f and R_s are small compared to R_L, $(R_f + R_s)/R_L$ is negligibly small compared to 1. So neglecting it we get,

$$\therefore \quad \boxed{E_{DC} \approx \frac{E_{sm}}{\pi}}$$

Note : When R_f and R_s are finite, calculate I_m, then I_{DC} and from that E_{DC} as $I_{DC}R_L$. Do not calculate E_{DC} as E_{sm}/π directly for finite R_f and R_s.

R.M.S value of Load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S. value of load current can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin\omega t)^2 \, d(\omega t)} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} \left(I_m^2 \sin^2 \omega t \, d(\omega t)\right)}$$

$$= I_m \sqrt{\frac{1}{2\pi}\int_0^{\pi} \frac{[1-\cos(2\omega t)]\, d(\omega t)}{2}} = I_m \sqrt{\frac{1}{2\pi}\left\{\frac{\omega t}{2} - \frac{\sin(2\omega t)}{4}\right\}_0^{\pi}}$$

$$= I_m \sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2}\right)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$= \frac{I_m}{2}$$

$$\therefore \quad \boxed{I_{RMS} = \frac{I_m}{2}}$$

DC Power Output (P_{DC})

The d.c. power output can be obtained as,

$$\boxed{P_{DC} = E_{DC} I_{DC} = I_{DC}^2 R_L}$$

$$\text{D.C. Power output} = I_{DC}^2 R_L = \left[\frac{I_m}{\pi}\right]^2 R_L = \frac{I_m^2}{\pi^2} R_L$$

$$\therefore \quad P_{DC} = \frac{I_m^2}{\pi^2} R_L$$

where $$I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

$$\therefore \quad \boxed{P_{DC} = \frac{E_{sm}^2 R_L}{\pi^2 [R_f + R_L + R_s]^2}}$$

AC Power Input (P_{AC})

The power input taken from the secondary of transformer is the power supplied to three resistances namely load resistance R_L, the diode resistance R_f and winding resistance R_s. The a.c. power is given by,

$$\boxed{P_{AC} = I_{RMS}^2 [R_L + R_f + R_s]}$$

but $$I_{RMS} = \frac{I_m}{2}$$ for half wave,

$$\therefore \quad \boxed{P_{AC} = \frac{I_m^2}{4} [R_L + R_f + R_s]}$$

Rectifier Efficiency (η)

The rectifier efficiency is defined as the ratio of output d.c. power to input a.c. power.

$$\therefore \quad \eta = \frac{\text{D.C. output power}}{\text{A.C. input power}} = \frac{P_{DC}}{P_{AC}}$$

$$\therefore \quad \eta = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4}[R_f + R_L + R_s]} = \frac{(4/\pi^2)R_L}{(R_f + R_L + R_s)}$$

$$\therefore \quad \boxed{\eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{R_L}\right)}}$$

If $(R_f + R_s) << R_L$ as mentioned earlier, we get the maximum theoretical efficiency of half wave rectifier as,

$$\boxed{\%\,\eta_{max} = 0.406 \times 100 = 40.6\ \%}$$

Thus in half wave rectifier, maximum 40.6% a.c. power gets converted to d.c. power in the load. If the efficiency of rectifier is 40% then what happens to the remaining 60% power. It is present interms of ripples in the output which is fluctuating component present in the output. Thus more the rectifier efficiency, less are the ripple contents in the output.

Ripple Factor (γ)

- Ripples are the oscillations that are obtained in DC which is corrected by using filters such as inductors and capacitors.
- These ripples are measured with the help of the ripple factor and are denoted by γ.
- Ripple factor tells us the number of ripples presents in the output DC. Higher the ripple factor, more is the oscillation at the output DC and lower is the ripple factor, less is the oscillation at the output DC.
- *Ripple factor is the ratio of RMS value of the AC component of the output voltage to the DC component of the output voltage.*

$$\text{Ripple factor } \gamma = \frac{\text{R.M.S. value of a.c. component of output}}{\text{Average or d.c. component of output}}$$

Now the output current is composed of a.c. component as well as d.c. component.

Let I_{ac} = r.m.s. value of a. c. component present in output

I_{DC} = d.c. component present in output

I_{RMS} = R.M.S. value of total output current

$$\therefore \quad I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$\therefore \quad I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

Now $\text{Ripple factor} = \frac{I_{ac}}{I_{DC}}$ as per definition

$$\therefore \quad \gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}}$$

$$\therefore \quad \boxed{\gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}}$$

Transformer Utilization Factor (TUF)

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (T.U.F.)

The T.U.F. is defined as the ratio of d.c. power delivered to the load to the a.c power rating of the transformer. While calculating the a.c. power rating, it is necessary to consider r.m.s. value of a.c. voltage and current.

The T.U.F. for half wave rectifier can be obtained as,

$$\text{A.C. power rating of transformer} = E_{RMS}\, I_{RMS}$$

$$= \frac{E_{sm}}{\sqrt{2}} \cdot \frac{I_m}{2} = \frac{E_{sm}\, I_m}{2\sqrt{2}}$$

$$\text{D.C. power delivered to the load} = I_{DC}^2\, R_L$$

$$= \left(\frac{I_m}{\pi}\right)^2 R_L$$

$$\text{T.U.F.} = \frac{\text{D.C. Power delivered to the load}}{\text{A.C. Power rating of the transformer}}$$

$$= \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{E_{sm} I_m}{2\sqrt{2}}\right)}$$

Neglecting the drop across R_f and R_s we can write,

$$E_{sm} = I_m R_L$$

$$\therefore \quad \text{T.U.F} = \frac{I_m^2}{\pi^2} \cdot \frac{R_L \cdot 2\sqrt{2}}{I_m^2 R_L} = \frac{2\sqrt{2}}{\pi^2} = 0.287$$

The value of T.U.F. is low which shows that in half wave circuit, the transformer is not fully utilized.

Load Current

The load current i_L which is composed of a.c. and d.c. components can be expressed using Fourier series as,

$$i_L = I_m \left[\frac{1}{\pi} + \frac{1}{2}\sin \omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t \ \ldots\right]$$

This expression shows that the current may be considered to be the sum of an infinite number of current components, according to Fourier series.

The first term of the series is the average or d.c. value of the load current. The second term is a varying component having frequency same as that of a.c. supply voltage. This is called fundamental component of the current having frequency same as the supply. The third term is again a varying component having frequency twice the frequency of supply voltage. This is called second harmonic component. Similarly all the other terms represent the a.c. components and are called harmonics.

Thus ripple in the output is due to the fundamental component alongwith the various harmonic components. And the average value of the total pulsating d.c. is the d.c. value of the load current, given by the constant term in the series, I_m / π

Peak Inverse Voltage (PIV)

The Peak Inverse Voltage is the peak voltage across the diode in the reverse direction i.e. when the diode is reverse biased. In half wave rectifier, the load current is ideally zero when the diode is reverse biased and hence the maximum value of the voltage that can exist across the diode is nothing but E_{sm}.

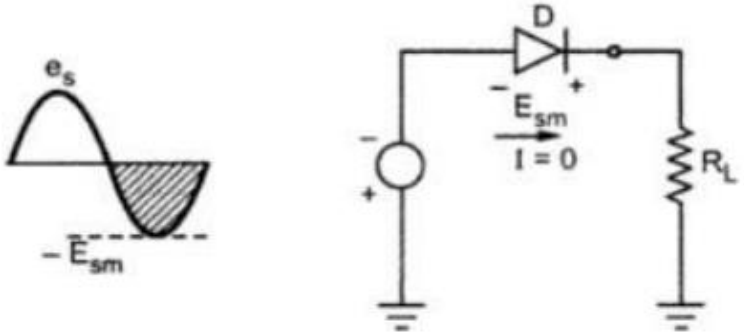


Fig 5.8 PIV rating of a Diode

Thus PIV occurs at the peak of each negative half cycle of the input, when diode is reverse biased and not conducting.

$\therefore$ PIV of diode = E_{sm} = Maximum value of secondary voltage = $\pi E_{DC}|_{IDC=0}$

This is called PIV rating of a diode. So diode must be selected based on this PIV rating and the circuit specifications.

Voltage Regulation

The secondary voltage should not change with respect to the load current. The voltage regulation is the factor which tells us about the change in the d.c. output voltage as load changes from no load to full load condition.

If $(V_{dc})_{NL}$ = D.C. voltage on no load

$(V_{dc})_{FL}$ = D.C. voltage on full load

$$\text{Voltage regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}$$

Disadvantages of Half Wave Rectifier

3. The circuit has low transformer utilization factor, showing that the transformer is not fully utilized.
4. The d.c. current is flowing through the secondary winding of the transformer which may cause dc saturation of the core of the transformer. To minimize the saturation, transformer size have to be increased accordingly. This increases the cost.

The various disadvantages of the half wave rectifier circuit are,

1. The ripple factor of half wave rectifier circuit is 1.21, which is quite high. The output contains lot of varying components.
2. The maximum theoretical rectification efficiency is found to be 40%. The practical value will be less than this. This indicates that half wave rectifier circuit is quite inefficient.

Characteristics of Half Wave Rectifier

Following are the characteristics of half-wave rectifier:

Ripple Factor

- Ripples are the oscillations that are obtained in DC which is corrected by using filters such as inductors and capacitors.
- These ripples are measured with the help of the ripple factor and are denoted by γ.
- Ripple factor tells us the number of ripples presents in the output DC. Higher the ripple factor, more is the oscillation at the output DC and lower is the ripple factor, less is the oscillation at the output DC.
- Ripple factor is the ratio of RMS value of the AC component of the output voltage to the DC component of the output voltage.

$$\gamma = \sqrt{(\frac{V_{rms}}{V_{DC}})^2 - 1}$$

Full wave Rectifier

The full wave rectifier conducts during both positive and negative half cycles of input a.c. supply. In order to rectify both the half cycles of a.c. input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center tap transformer. The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

For the proper operation of the circuit, a **center-tap** on the secondary winding of the transformer is essential.

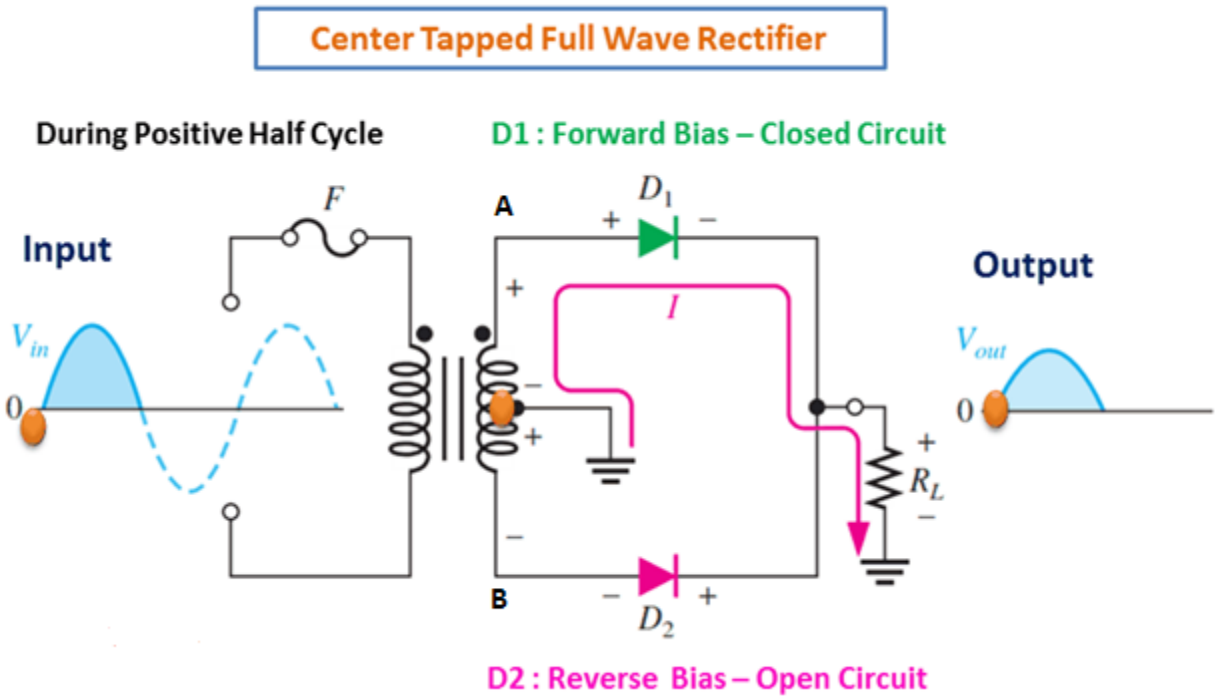


Figure 5.9 Working of Full Wave Rectifier (+ve half cycle)

Consider the positive half cycle of ac input voltage in which terminal (A) is positive and terminal (B) negative. The diode D_1 will be forward biased and hence will conduct; while diode D_2 will be reverse biased and will act as an open circuit and will not conduct.

The diode D_1 supplies the load current, i.e. $i_L = i_{d1}$ .This current is flowing through upper half of secondary winding while the lower half of secondary winding of the transformer carries no current since diode D_2 is reverse biased and acts as an open circuit.

In the next half cycle of ac voltage, polarity reverses and terminal (A) becomes negative and (B) positive. The diode D_2 conducts, being forward biased, while D_1 does not, being reverse biased.

The diode D_2 supplies the load current, i.e. $i_L = i_{d2}$. Now the lower half of the secondary winding carries the current but the upper half does not.

It is noted that the **load current flows in both the half cycles of ac voltage and in the same direction through the load resistance**. Hence we get rectified output across the load. The load current is sum of individual diode currents flowing in corresponding half cycles. It is also noted that the two diodes do not conduct simultaneously but in alternate half cycles.The individual diode currents and the load current are shown in the Fig. 1.9

Thus the full wave rectifier circuit essentially consists of two half-wave rectifier circuits working independently (working in alternate half cycles of a c) of each other but feeding a common load. The output load current is still pulsating d.c. and not pure d.c.

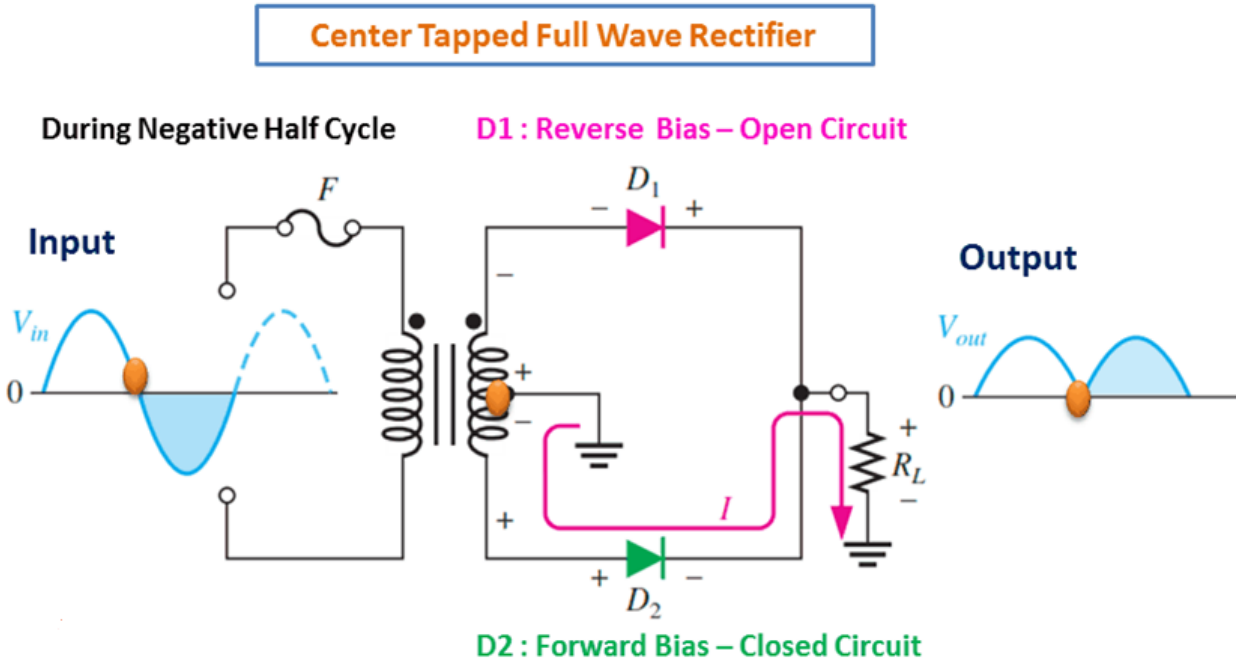


Figure 5.10 Working of Full Wave Rectifier (-ve Half Cycle)

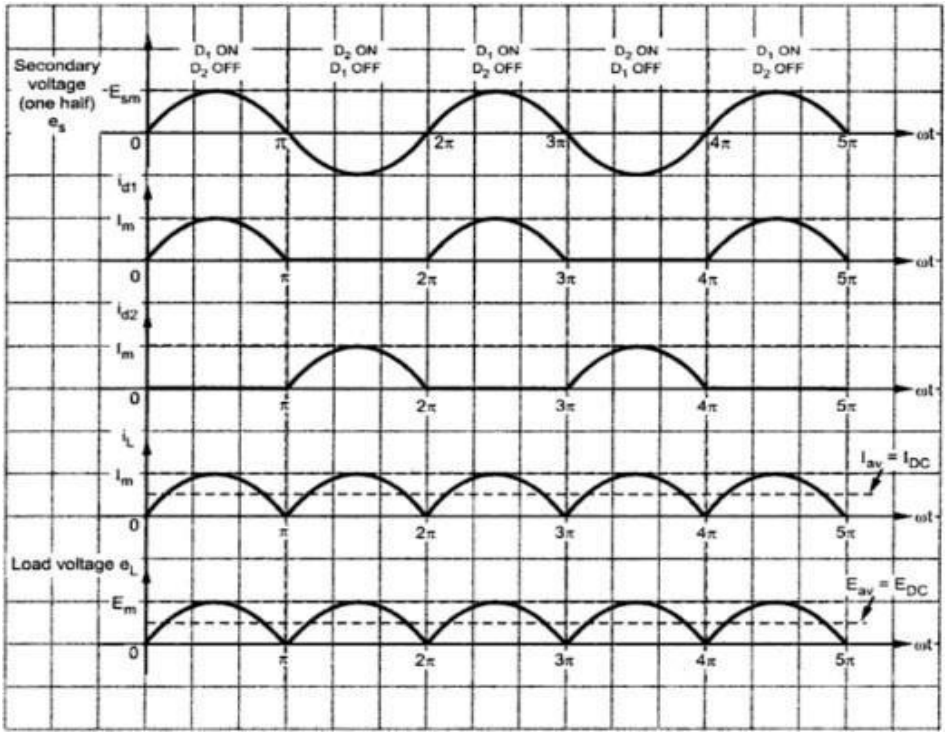
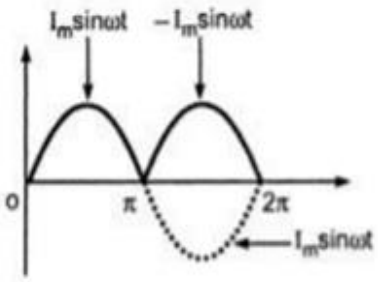


Figure 5.11 Current and voltage wave forms at load for full wave rectifier

Average DC Load Current (I_{DC})



Consider one cycle of load current i_L from 0 to 2π to obtain the average value which is d.c. value of load current.

$$i_L = I_m \sin \omega t \qquad 0 \le \omega t \le \pi$$

But for π to 2π, the current i_L is again positive while sin ω t term is negative during π to 2π . Hence in the region π to 2π the positive i_L can be represented as negative of $I_m \sin(\omega t)$.

$$\therefore \quad i_L = -I_m \sin \omega t \qquad \pi \le \omega t \le 2\pi$$

$$\therefore \quad I_{av} = I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin \omega t \, d(\omega t) + \int_{\pi}^{2\pi} -I_m \sin \omega t \, d(\omega t)\right]$$

$$= \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin \omega t \, d(\omega t) - \int_{\pi}^{2\pi} \sin \omega t \, d(\omega t)\right]$$

$$= \frac{I_m}{2\pi}\left[(-\cos \omega t)_0^{\pi} - (-\cos \omega t)_{\pi}^{2\pi}\right]$$

$$= \frac{I_m}{2\pi}[-\cos \pi + \cos 0 + \cos 2\pi - \cos \pi]$$

but $\cos\pi = -1$

$$= \frac{I_m}{2\pi}[-(-1)+1+1-(-1)] = \frac{4I_m}{2\pi}$$

$$\therefore \quad \boxed{I_{DC} = \frac{2I_m}{\pi}} \quad \text{for full wave rectifier}$$

For half wave it is I_m/π and full wave rectifier is the combination of two half wave circuits acting alternately in two half cycles of input. Hence obviously the d.c. value for full wave circuit is $2\ I_m/\pi$.

Average DC Load Voltage (E_{DC})

The d.c. load voltage is,

$$E_{DC} = I_{DC}R_L = \frac{2I_mR_L}{\pi}$$

Substituting value of I_m,

$$E_{DC} = \frac{2\,E_{sm}\,R_L}{\pi\,[R_f + R_s + R_L]} = \frac{2\,E_{sm}}{\pi\left[1+\frac{R_f+R_s}{R_L}\right]}$$

But as R_f and $R_s << R_L$ hence $\frac{R_f+R_s}{R_L} << 1$

$$\therefore \quad \boxed{E_{DC} = \frac{2E_{sm}}{\pi}}$$

R.M.S value of Load Current (I_{RMS})

The R.M.S. value of current can be obtained as follows :

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 d(\omega t)}$$

Since two half wave rectifier are similar in operation we can write,

$$I_{RMS} = \sqrt{\frac{2}{2\pi}\int_0^{\pi} [I_m \sin \omega t]^2 d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{1-\cos 2\omega t}{2}\right] d(\omega t)} \qquad \text{as } \sin^2 \omega t = \frac{1-\cos 2\omega t}{2}$$

$$\therefore \quad I_{RMS} = I_m \sqrt{\frac{1}{2\pi}\left[[\omega t]_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]} = I_m \sqrt{\frac{1}{2\pi}[\pi - 0]}$$

$$= I_m \sqrt{\frac{1}{2\pi}(\pi)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$\therefore \quad \boxed{I_{RMS} = \frac{I_m}{\sqrt{2}}}$$

DC Power Output (P_{DC})

$$\boxed{\text{D.C. Power output} = E_{DC} I_{DC} = I_{DC}^2 R_L}$$

$$\therefore \quad P_{DC} = I_{DC}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$\therefore \quad P_{DC} = \frac{4}{\pi^2} I_m^2 R_L$$

Substituting value of I_m we get,

$$\boxed{P_{DC} = \frac{4}{\pi^2} \frac{E_{sm}^2}{(R_s + R_f + R_L)^2} \times R_L}$$

Note : Instead of remembering this formula, students can use the expression $E_{DC}I_{DC}$ or $I_{DC}^2 R_L$ to calculate P_{DC} while solving the problems.

AC Power Output (P_{AC})

The a.c. power input is given by,

$$\boxed{P_{AC} = I_{RMS}^2 (R_f + R_s + R_L)}$$

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_s + R_L)$$

$$\therefore \quad P_{AC} = \frac{I_m^2 (R_f + R_s + R_L)}{2}$$

Substituting value of I_m we get,

$$\therefore \quad P_{AC} = \frac{E_{sm}^2}{(R_f + R_s + R_L)^2} \times \frac{1}{2} \times (R_f + R_s + R_L)$$

$$\therefore \quad \boxed{P_{AC} = \frac{E_{sm}^2}{2(R_f + R_s + R_L)}}$$

Rectifier Efficiency (η)

$$\boxed{\eta = \frac{P_{DC} \text{ output}}{P_{AC} \text{ input}}}$$

$$\therefore \quad \eta = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}}$$

$$\therefore \quad \eta = \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)}$$

But if $R_f + R_s << R_L$, neglecting it from denominator

$$\eta = \frac{8 R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2}$$

$$\therefore \quad \boxed{\%\, \eta_{max} = \frac{8}{\pi^2} \times 100 = 81.2\ \%}$$

This is the maximum theoretical efficiency of full wave rectifier.

Ripple Factor (γ)

As derived earlier in case of half wave rectifier the ripple factor is given by a general expression,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

For full wave $I_{RMS} = I_m/\sqrt{2}$ and $I_{DC} = 2I_m/\pi$ so substituting in the above equation,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_m/\sqrt{2}}{2I_m/\pi}\right]^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1}$$

$$\therefore \quad \boxed{\text{Ripple factor} = \gamma = 0.48}$$

Key Point: *This indicates that the ripple contents in the output are 48 % of the d.c. component which is much less than that for the half wave circuit.*

Peak Inverse Voltage (PIV)

$$\therefore \quad \boxed{\text{PIV of diode} = 2\,E_{sm} = \pi\,E_{DC}|_{I_{DC}=0}}$$

where E_{sm} = Maximum value of a.c. voltage across half the secondary of transformer.

If the diode drop is considered to be 0.7 V then the PIV of reverse biased diode is,

$$\boxed{\text{PIV of diode} = 2E_{sm} - 0.7}$$

This is because only one diode conducts at a time.

Transformer Utilization Factor (TUF)

In full wave rectifier, the secondary current flows through each half separately in every half cycle. While the primary of transformer carries current continuously. Hence T.U.F is calculated for primary and secondary windings separately and then the average T.U.F. is determined.

$$\text{Secondary T.U.F} = \frac{\text{D.C. power to the load}}{\text{A.C. power rating of secondary}}$$

$$= \frac{I_{DC}^2 R_L}{E_{RMS} I_{rms}} = \frac{\left(\frac{2}{\pi} I_m\right)^2 R_L}{\frac{E_{sm}}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

Neglecting forward resistance R_f of diode, $E_{sm} \approx I_m R_L$.

$$\therefore \quad \text{Secondary T.U.F.} = \frac{\frac{4}{\pi^2} \times I_m^2 R_L}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2} = 0.812$$

The primary of the transformer is feeding two half-wave rectifiers separately. These two half-wave rectifiers work independently of each other but feed a common load. We have already derived the T.U.F. for half wave circuit to be equal to 0.287. Hence

$$\text{T.U.F. for primary winding} = 2 \times \text{T.U.F. of half wave circuit}$$
$$= 2 \times 0.287 = 0.574.$$

The average T.U.F for fullwave circuit will be

$$\text{Average T.U.F. for full wave rectifier circuit} = \frac{\text{T.U.F of primary} + \text{T.U.F of secondary}}{2}$$

$$= \frac{0.574 + 0.812}{2} = \mathbf{0.693}$$

$\therefore$ Average T.U.F. for full-wave rectifier = 0.693

Key Point: *Thus in full-wave circuit, transformer gets utilized more than the half wave rectifier circuit.*

Example 1 : *A full-wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from either end of secondary to center tap is 30 V. If the diode forward resistance is 2 Ω and that of the half secondary is 8 Ω, for a load of 1 kΩ, calculate, a) Power delivered to load, b) % Regulation at full load, c) Efficiency of rectification, d) TUF of secondary.*

Solution:

Given : $E_s = 30\,V,\ R_f = 2\Omega,\ R_s = 8\Omega,\ R_L = 1k\Omega$

$$E_s = E_{RMS} = 30\ V$$

$$E_{sm} = E_s\sqrt{2} = 30\sqrt{2}\ \text{volt} = 42.426\ V$$

$$I_m = \frac{E_{sm}}{R_f + R_L + R_s} = \frac{30\sqrt{2}}{2+1000+8}\ A$$

$$= 42\ mA$$

$$I_{DC} = \frac{2}{\pi} I_m = 26.74\ mA$$

a) Power delivered to the load $= I_{DC}^2\ R_L = (26.74 \times 10^{-3})^2\ (1k\Omega)$

$$= \mathbf{0.715\ W}$$

b) V_{DC}, no load $= \frac{2}{\pi} E_{sm} = \frac{2}{\pi} \times 30\sqrt{2} = 27\ V$

V_{DC}, full load $= I_{DC}\ R_L = (26.74\ mA)\ (1\ k\Omega)$

$$= 26.74\ V$$

$$\%\ \text{Regulation} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{27 - 26.74}{26.74} \times 100$$

$$= \mathbf{0.97\ \%}$$

c) $$\text{Efficiency of rectification} = \frac{\text{D.C. output}}{\text{A.C. input}}$$

$$= \frac{8}{\pi^2} \times \frac{1}{1 + \frac{R_f + R_s}{R_L}} = \frac{8}{\pi^2} \times \frac{1}{1 + \frac{(2+8)}{1000}}$$

$$= 0.802 \quad \textbf{i.e. 80.2\%}$$

d) Transformer secondary rating $= E_{RMS}\ I_{RMS} = [30\ V]\left[\frac{42\ mA}{\sqrt{2}}\right]$

$$= \mathbf{0.89\ W}$$

$$\therefore \quad \text{T.U.F.} = \frac{\text{D.C. power output}}{\text{A.C. rating}}$$

$$= \frac{0.715}{0.89} = \mathbf{0.802}$$

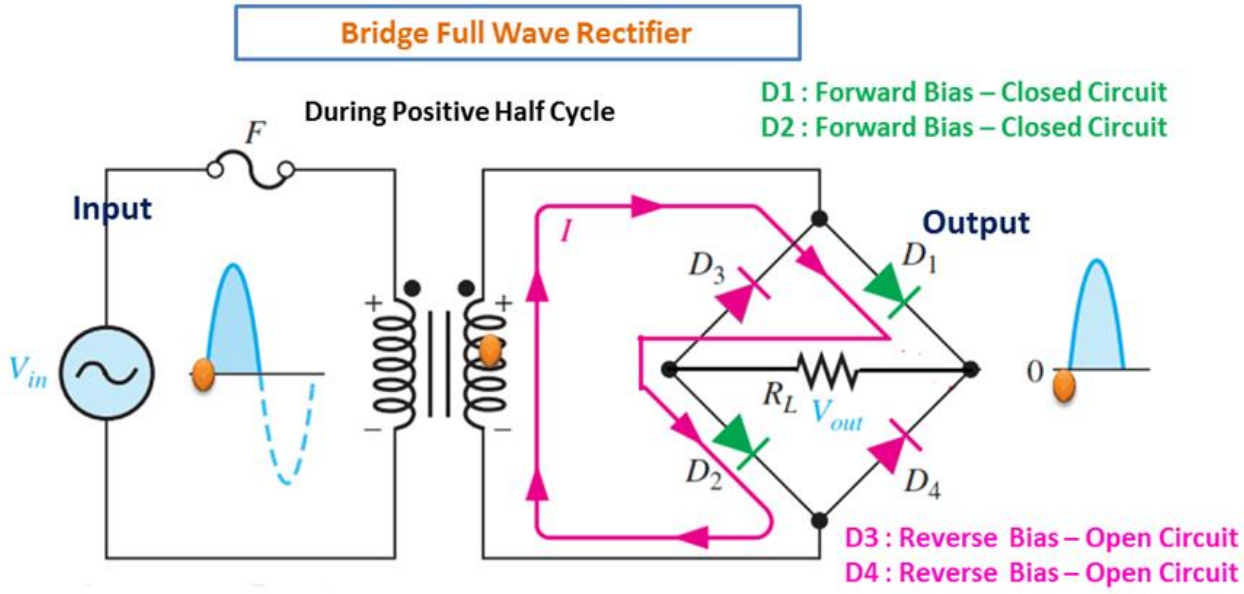


Figure 5.12 Working of Bridge Wave Rectifier (+ve Half Cycle)

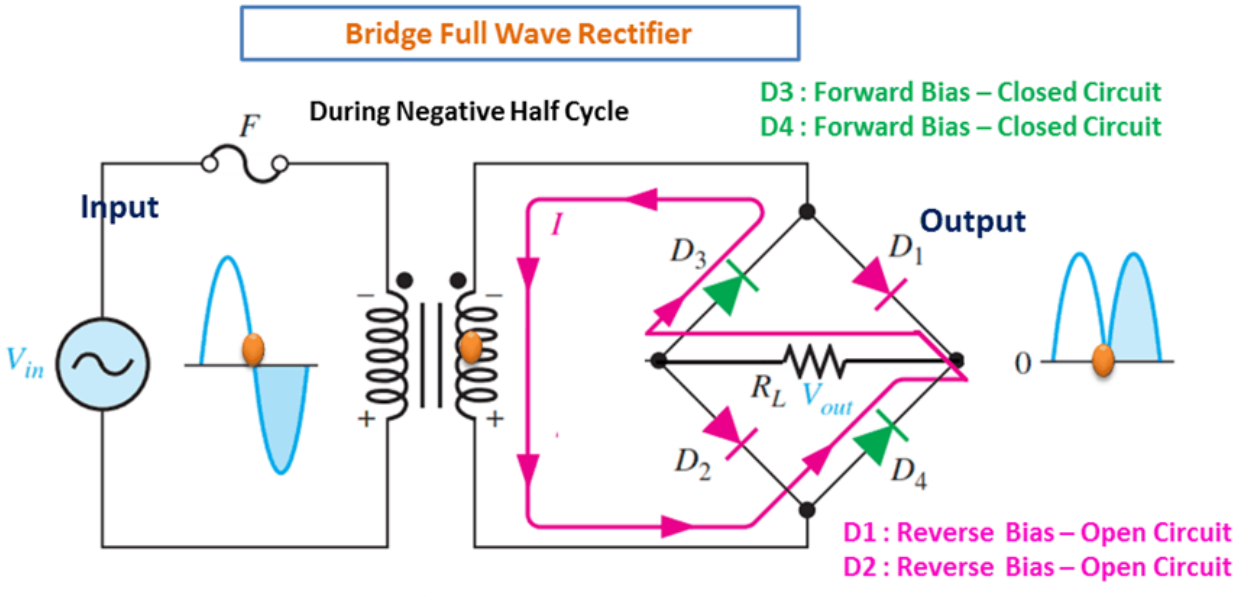
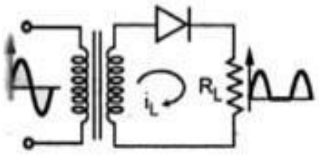
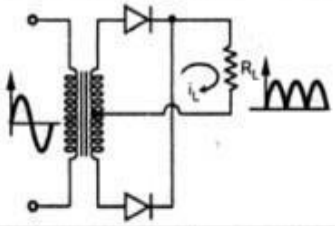
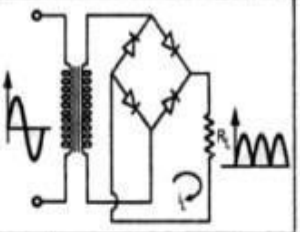


Figure 5.13 Working of Bridge Wave Rectifier (-ve Half Cycle)

Comparison of Rectifier Circuits

Circuit Diagrams		
Half Wave	Full Wave	Bridge
		

S.R.	Parameter	Half Wave	Full Wave	Bridge
1.	Number of diodes	1	2	4
2.	Average D.C. current (I_{DC})	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3.	Average D.C. voltage (E_{DC})	$\frac{E_{sm}}{\pi}$	$\frac{2E_{sm}}{\pi}$	$\frac{2E_{sm}}{\pi}$
4.	R.M.S. current (I_{RMS})	$\frac{I_m}{2}$	$\frac{I_m}{\sqrt{2}}$	$\frac{I_m}{\sqrt{2}}$
5.	D.C. power output (P_{DC})	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4}{\pi^2} I_m^2 R_L$	$\frac{4}{\pi^2} I_m^2 R_L$
6.	A.C. power input (P_{AC})	$\frac{I_m^2(R_L + R_f + R_s)}{4}$	$\frac{I_m^2(R_f + R_s + R_L)}{2}$	$\frac{I_m^2(2R_f + R_s + R_L)}{2}$
7.	Maximum rectifier efficiency (η)	40.6 %	81.2 %	81.2 %
8.	Ripple factor (γ)	1.21	0.482	0.482
9.	Maximum load current (I_m)	$\frac{E_{sm}}{R_s + R_f + R_L}$	$\frac{E_{sm}}{R_s + R_f + R_L}$	$\frac{E_{sm}}{R_s + 2R_f + R_L}$

FILTERS

It is seen that the output a half-wave or full wave rectifier circuit is not pure d.c.; but it contains fluctuations or ripple, which are undesired. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load, as shown in the Fig. 1.13

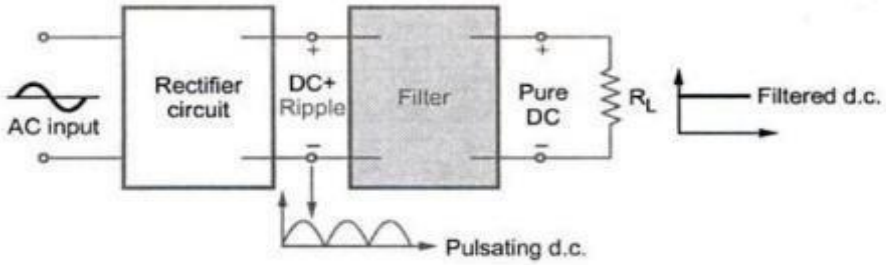


Figure 5.14 Power supply using rectifier and filter

An a.c. input is applied to the rectifier. At the output of the rectifier, there will be d.c. and ripple voltage present, which is the input to the filter. Ideally the output of the filter should be pure d.c. Practically, the filter circuit will try to minimize the ripple at the output, as far as possible.

Basically the ripple is a.c., i.e. varying with time, while d.c. is a constant w.r.t. time. Hence in order to separate d.c. from ripple, the filter circuit should use components which have widely different impedance for a.c. and d.c. Two such components are inductance and capacitance. Ideally, the inductance acts as a short circuit for d.c., but it has a large impedance for a.c.. Similarly, the capacitor acts as open for d.c. and almost short for a.c. if the value of capacitance is sufficiently large enough.

Since ideally, inductance acts as short circuit for d.c., it cannot be placed in shunt arm across the load, otherwise the d.c. will be shorted.

Key Point: *Hence, in a filter circuit, the inductance is always connected in series with the load.*

The inductance used in filter circuits is also called "**choke**".

Similarly, since the capacitance is open for d.c., i.e. it blocks d.c.; hence it cannot be connected in series with the load.

Key Point: *It is always connected in shunt arm, parallel to the load.*

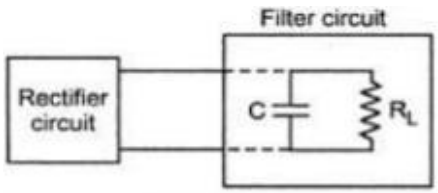
Thus filter is an electronic circuit composed of capacitor, inductor or combination of both and connected between the rectifier and the load so as to convert pulsating d.c. to pure d.c.

There are basically two types of filter circuits,

- Capacitor input filter
- Choke input filter

Looking from the rectifier side, if the first element, in the filter circuit is capacitor then the filter circuit is called **capacitor input filter**. While if the first element is an inductor, it is called **choke input filter**. The choke input filter is not in use now a days as inductors are bulky, expensive and consume more power. Let us discuss the operation of a capacitor input filter.

Capacitor Input Filter



The block schematic of capacitor input filter is shown in the **Fig.5.15** Looking from the rectifier side the first element in filter is a capacitor.

Figure 5.15 Capacitor input filter

Full wave rectifier with capacitor input filter

The same concept can now be extended to the capacitor filter used in full wave rectifier circuit as shown in the Fig. 1.19.

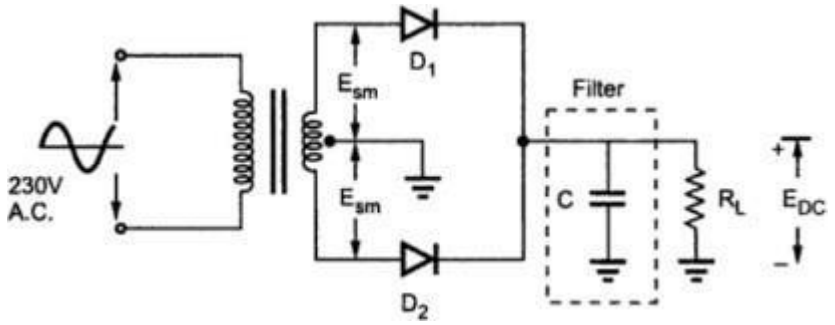


Figure 5.16 Full wave Rectifier with Capacitor input filter

Immediately when power is turned on, the capacitor C gets charged through forward biased diode D_1 to E_{sm}, during first quarter cycle of the rectified output voltage. In the next quarter cycle from $\frac{\pi}{2}$ to π, the capacitor starts discharging through R_L. Once capacitor gets charged to E_{sm}, the diode D_1 becomes reverse biased and stops conducting. So during the period from $\frac{\pi}{2}$ to π, the capacitor C supplies the load current. It discharges to point B shown in the Fig. 1.20. At point B, lying in the quarter π to $\frac{3\pi}{2}$ of the rectified output voltage, the input voltage exceeds capacitor voltage, making D_2 forward biased. This charges capacitor back to E_{sm} at point C.

The time required by capacitor C to charge to E_{sm} is quite small and only for this period, diode D_2 is conducting. Again at point C, diode D_2 stops conducting and capacitor supplies load and starts discharging upto point D in the next quarter cycle of the rectified output voltage as shown in the **Fig.5.17**. At this point, the diode D_1 conducts to charge capacitor back to E_{sm}. The diode currents are shown shaded in the **Fig.5.17**

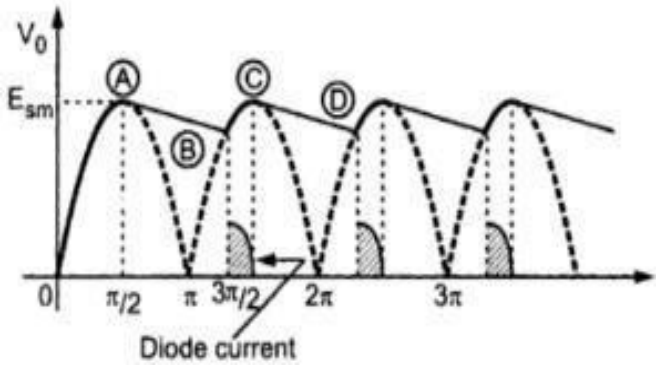


Figure 5.17. Charging and discharging of Capacitor input filter

In this circuit, the two diodes are conducting in alternate half cycles of the output of the rectifier circuit. The diodes are not conducting for the entire half cycle but only for a part of the half cycle, during which the capacitor is getting charged. When the capacitor is discharging through the load resistance R_L, both the diodes are non-conducting. The capacitor supplies the load current. As the time required by capacitor to charge is very small and it discharges very little due to large time constant, hence ripple in the output gets reduced considerably. Though the diodes conduct partly, the load current gets maintained due to the capacitor. This filter is very popularly used in practice.

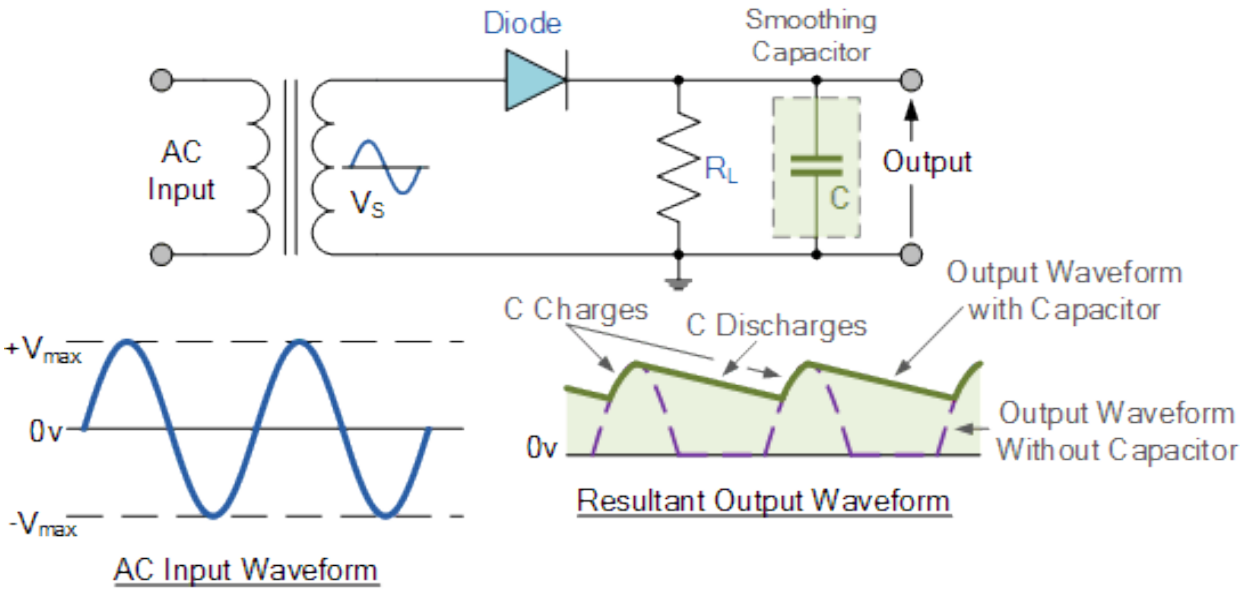


Figure 5.18. Half wave Rectifier with Capacitor filter

Bridge rectifier with capacitor filter

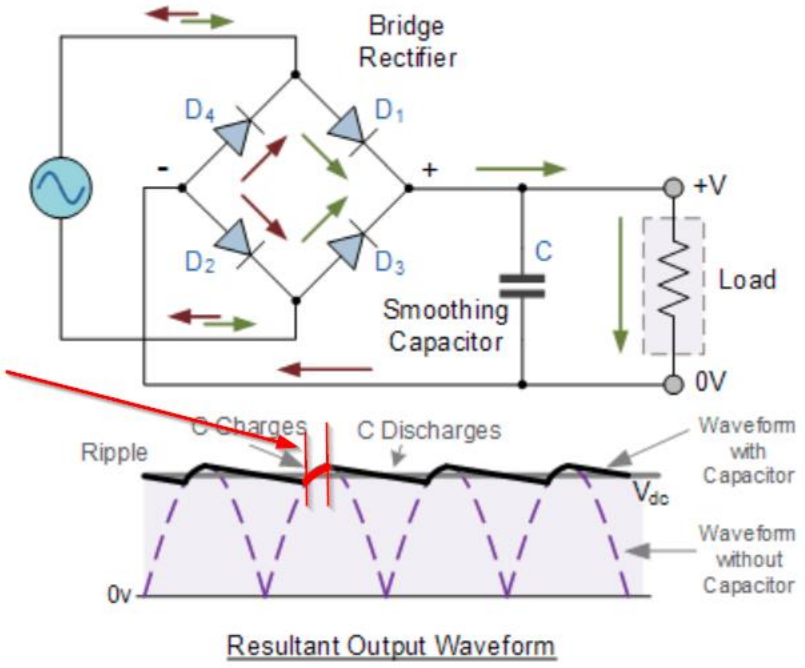


Figure 5.19. Bridge Rectifier with Capacitor filter

Expression for Ripple Factor

Consider an output waveform for a full wave rectifier circuit using a capacitor input filter, as shown in the Fig. 1.21.

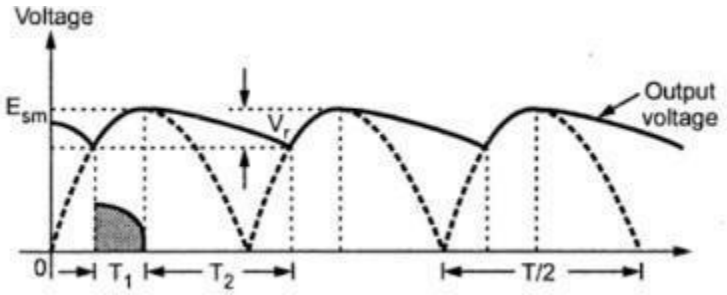


Figure 5.20 Derivation for ripple factor

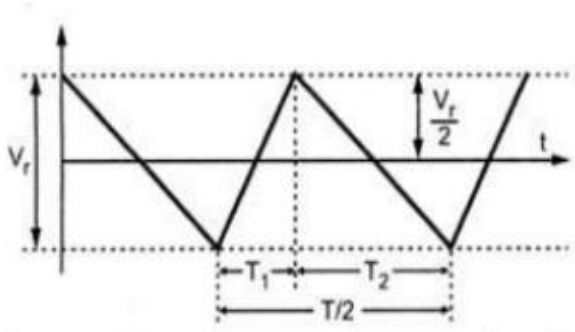
Let

T = Time period of the a.c. input voltage

$\frac{T}{2}$ = Half of the time period

T_1 = Time for which diode is conducting

T_2 = Time for which diode is nonconducting.



During time T_1, capacitor gets charged and this process is quick. During time T_2, capacitor gets discharged through R_L. As time constant R_LC is very large, discharging process is very slow and hence $T_2 >> T_1$.

Let V_r be the peak to peak value of ripple voltage, which is assumed to be triangular as shown in the Fig. 5.19

Figure 5.21.Triangular Approximation of ripple voltage

It is known mathematically that the r.m.s. value of such a **triangular waveform** is,

$$\boxed{V_{rms} = \frac{V_r}{2\sqrt{3}}}$$

During the time interval T_2, the capacitor C is discharging through the load resistance R_L. The charge lost is,

$$Q = CV_r$$

But $$i = \frac{dQ}{dt}$$

$$\therefore \quad Q = \int_0^{T_2} i\,dt = I_{DC}\,T_2$$

As integration gives average or d.c. value

Hence $$I_{DC}\,T_2 = CV_r$$

$$\therefore \quad V_r = \frac{I_{DC}\,T_2}{C}$$

Now, $$T_1 + T_2 = \frac{T}{2}$$ Normally, $T_2 >> T_1$

$$\therefore \quad T_1 + T_2 \approx T_2 = \frac{T}{2} \quad \text{where } T = \frac{1}{f}$$

$$\therefore \quad \boxed{V_r = \frac{I_{DC}}{C}\left[\frac{T}{2}\right] = \frac{I_{DC} \times T}{2C} = \frac{I_{DC}}{2fC}}$$

But $$I_{DC} = \frac{E_{DC}}{R_L}$$

$$\therefore \quad \boxed{V_r = \frac{E_{DC}}{2fCR_L} = \textbf{peak to peak ripple voltage}}$$

$$\text{Ripple factor} = \frac{V_{rms}}{E_{DC}} = \frac{\frac{E_{DC}}{2fCR_L}}{2\sqrt{3}} \times \frac{1}{E_{DC}}, \text{ Since } V_{rms} = \frac{V_r}{2\sqrt{3}}$$

$$\therefore \quad \boxed{\text{Ripple factor} = \frac{1}{4\sqrt{3}\,fCR_L} \text{ for } \textbf{full wave}}$$

For **half wave rectifier** with capacitor input filter the ripple factor is,

$$\boxed{\text{Ripple factor} = \frac{1}{2\sqrt{3}\,fCR_L} \text{ for } \textbf{half wave}}$$

The product CR_L is the time constant of the filter circuit.

Advantages and Disadvantages of Capacitor input filter

The **advantages** of capacitor input filter are,

1. Less number of components.
2. Low ripple factor hence low ripple voltage.
3. Suitable for high voltage at small load currents.

The **disadvantages** of capacitor input filter are,

1. Ripple factor depends on load resistance.
2. Not suitable for variable loads as ripple content increases as R_L decreases.
3. Regulation is poor.
4. Diodes are subjected to high surge currents hence must be selected accordingly.

Example 1 : *A full wave rectifier is operated from 50 Hz supply with 120 V (rms). It is connected to a load drawing 50 mA and using 100 μF filter capacitor. Calculate the d.c. output voltage and the r.m.s. value of ripple voltage. Also calculate the ripple factor.*

Solution : $E_{s(rms)} = 120$ V, f = 50 Hz, $I_{DC} = 50$ mA, C = 100 μF

$$E_{sm} = \sqrt{2}\, E_{s(rms)} = \sqrt{2} \times 120 = 169.7056 \text{ V}$$

For full wave rectifier,

$$E_{DC} = E_{sm} - I_{DC}\left[\frac{1}{4fC}\right]$$

$$= 169.7056 - \frac{50 \times 10^{-3}}{4 \times 50 \times 100 \times 10^{-6}} = \mathbf{167.2056\ V}$$

$$V_{r(rms)} = \frac{I_{DC}}{4\sqrt{3}\, fC} = \frac{50 \times 10^{-3}}{4 \times \sqrt{3} \times 50 \times 100 \times 10^{-6}}$$

$$= \mathbf{1.4433\ V}$$

The ripple factor is given by,

$$\gamma = \frac{V_{r(rms)}}{E_{DC}} = \frac{1.4433}{167.2056}$$

$$= \mathbf{8.63 \times 10^{-3}}$$

Inductor Filter or Choke Filter

In this type of filter, an inductor (choke) is connected in series with the load. It is known that the inductor opposes change in the current. So the ripple which is change in the current is opposed by the inductor and it tries to smoothen the output. Consider a full

wave rectifier with inductor filter which is also called choke filter. Fig. 5.22 (a) shows the circuit diagram while Fig. 5.22 (b) shows the current waveform obtained by using choke filter with full wave rectifier.

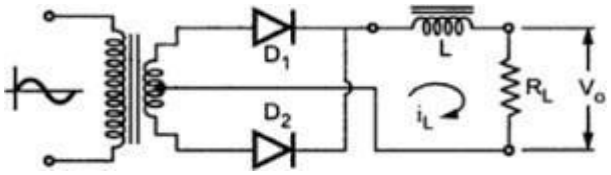


Figure 5.22 (a) Circuit diagram of choke filter

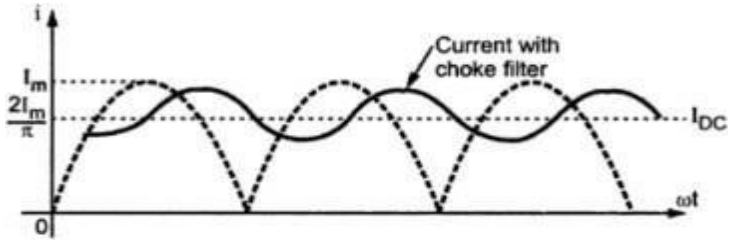


Fig.5.22 (b) Current waveform of choke filter

Operation of Inductor filter

In the positive half cycle of the secondary voltage of the transformer, the diode D_1 is forward biased. Hence the current flows through D_1, L and R_L. While in the negative half cycle, the diode D_1 is reverse biased while diode D_2 is forward biased. Hence the current flows through D_2, L and R_L. Hence we get unidirectional current through R_L. Due to inductor L which opposes change in current, it tries to make the output smooth by opposing the ripple content in the output.

We know that the fourier series for the load current for full wave rectifier as,

$$i_L = I_m \left[\frac{2}{\pi} - \frac{4}{3\pi} \cos 2\omega t - \frac{4}{15\pi} \cos 4\omega t \right]$$

Neglecting higher order harmonics we get,

$$i_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t$$

Neglecting diode forward resistances and the resistance of choke and transformer secondary we can write the d.c. component of current as

$$\frac{2I_m}{\pi} = \frac{2V_m}{\pi R_L}$$

as $$I_m = \frac{V_m}{R_L}$$

While the second harmonic component represents a.c. component or ripple present and can be written as,

$$I_m = \frac{V_m}{Z} \text{ for a.c. component}$$

Now $$Z = R_L + j2X_L = \sqrt{R_L^2 + 4\omega^2 L^2} \angle \phi$$

where $$\phi = \tan^{-1} \frac{2\omega L}{R_L}$$

$\therefore$ $$\boxed{I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}}}$$

The ripple present is the second harmonic component having frequency 2ω.

Key Point: *Hence while calculations the effective inductive reactance must be calculated at 2ω hence represented as $2X_L$ in the above expression.*

Hence equation (1) modifies as,

$$\boxed{i_L = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}} \cos(2\omega t - \phi)}$$

Expression for the ripple factor

Ripple factor is given by ,

$$\text{Ripple factor} = \frac{I_{rms}}{I_{DC}}$$

where $I_{rms} = \frac{I_m}{\sqrt{2}}$ of a.c. component

$$I_{rms} = \frac{4\,V_m}{3\sqrt{2}\,\pi\sqrt{R_L^2 + 4\,\omega^2\,L^2}}$$

while $I_{DC} = \frac{2\,V_m}{\pi\,R_L}$

$$\therefore \text{Ripple factor} = \frac{\frac{4\,V_m}{3\sqrt{2}\,\pi\sqrt{R_L^2 + 4\,\omega^2\,L^2}}}{\frac{2\,V_m}{\pi\,R_L}}$$

$$= \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{1 + \frac{4\,\omega^2\,L^2}{R_L^2}}}$$

Initially on no load condition, $R_L \to \infty$ and hence $\frac{4\,\omega^2\,L^2}{R_L^2} \to 0$.

$\therefore$ Ripple factor $= \frac{2}{3\sqrt{2}} = 0.472$

This is very close to normal full wave rectifier without filtering.

But as load increases, R_L decreases hence $\frac{4\,\omega^2\,L^2}{R_L^2} >> 1$. So neglecting 1 we get,

$$\text{Ripple factor} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{\frac{4\,\omega^2\,L^2}{R_L^2}}}$$

$$\therefore \boxed{\gamma = \frac{R_L}{3\sqrt{2}\,.\,\omega L}}$$

So as load changes, ripple charges which is inversely proportional to the value of the inductor.

Key Point: *Smaller the value of* R_L, *smaller is the ripple hence the filter is suitable for low load resistances i.e. for high load current applications.*

We also know that ripple factor (γ),

$$0.05 = \frac{R_L}{3\sqrt{2} \cdot \omega \cdot L} = \frac{100}{3\sqrt{2} \times (2\pi \times 400) \times L} = \frac{1}{106.6\,L}$$

$\therefore$ $L = 1/(106.6 \times 0.05) = 0.188$ H Ans.

LC Filter or L section Filter

This is also called **choke input filter** as the filter element looking from the rectifier side is an inductance L. The d.c. winding resistance of the choke is R_x . The circuit is also called L-type filter or LC filter. The circuit is shown in the Fig. **5.23**

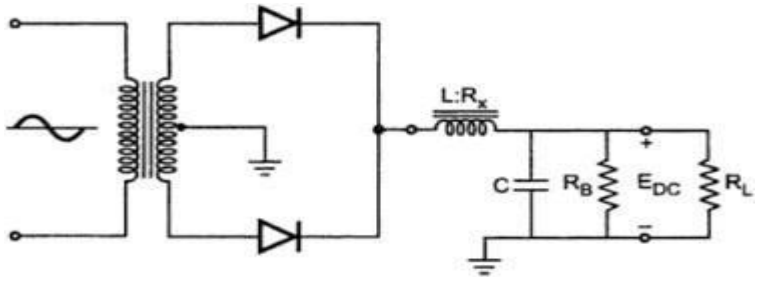


Figure 5.23 Choke Input Filter

The basic requirement of this filter circuit is that the current through the choke must be continuous and not interrupted. An interrupted current through the choke may develop a large back e.m.f. which may be in excess of PIV rating of the diodes and /or maximum voltage rating of the capacitor C. Thus this back e.m.f. is harmful to the diodes and capacitor. To eliminate the back e.m.f. developed across the choke, the current through it must be maintained continuous.

This is assured by connecting a bleeder resistance, R_B across the output terminals.

We have seen that the lowest ripple frequency for a full wave rectifier circuit is twice the supply frequency of a.c. input voltage to the rectifier. Let f, in Hz, be the supply frequency. Then angular supply frequency will be ω rad/s, where $\omega = 2\pi f$. Then the lowest ripple angular frequency will be "2ω" rad/s.

Derivation of Ripple Factor

The analysis of the choke input filter circuit is based on the following assumptions :

Since the filter elements, L and C, are having reasonably large values, the reactance X_L of the inductance of L at 2ω i.e. $X_L = 2\omega L$ is much larger than R_x. Also the reactance X_L is much larger than the reactance of C, X_C at 2ω as,

$$X_C = \frac{1}{2\omega C}$$

Let R be the equivalent resistance of bleeder resistance R_B and the load resistance R_L connected in parallel. Then ,

$$R = R_B \| R_L = \frac{R_B R_L}{R_B + R_L}$$

We will assume that reactance of C at '2ω' is much less than R, i.e. $X_C << R$.

The capacitance C is in parallel with R. Hence the equivalent impedance of X_C and R will be nearly equal to X_C, as per our assumption.

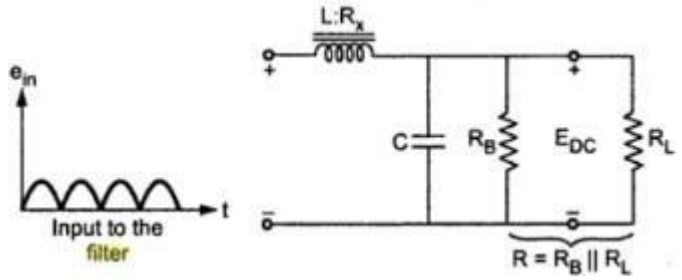


Figure 5.24 Diagram for derivation of ripple factor

The input voltage e_{in}, to the choke-input filter is the output voltage of the full wave rectifier, having the waveform as illustrated in Fig. 1.25. Using Fourier series, the input voltage "e_{in}" can be written as,

$$e_{in} = E_{sm}\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t \ldots\right]$$

where E_{sm} = the maximum value of half secondary voltage of the transformer.

The first term $\frac{2}{\pi} E_{sm}$, in the Fourier series indicates the d.c. output voltage of the rectifier, while the remaining terms ripple. The amplitude of the lowest ripple component, which is the second harmonic component of the supply frequency, is $\frac{4}{3\pi}$ while the amplitude of the fourth harmonic component, 5ω, is $\frac{4}{15\pi}$. The amplitude of the fourth harmonic is just one-fifth or 20% of the amplitude of second harmonic component. The higher harmonics will have still less amplitudes compared to the amplitude of the second harmonic component. Hence all harmonics, except the second harmonic, can be neglected. The equation for "e_{in}" can now be approximately written as,

$$e_{in} \approx E_{sm}\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t\right]$$

The d.c. current in the circuit will be,

$$I_{DC} = \frac{\frac{2}{\pi} E_{sm}}{R_x + R}$$

$$R = R_B \| R_L$$

$$\therefore \quad E_{DC} \text{ across the load} = I_{DC} R = \frac{2}{\pi} \frac{E_{sm}}{R_x + R} \times R$$

$$\therefore \quad E_{DC} = \frac{2}{\pi} \frac{E_{sm}}{1 + \frac{R_x}{R}}$$

Normally, R_x is much less than R, i.e. $R_x << R$

Then, $$E_{DC} \approx \frac{2}{\pi} E_{sm}$$

Thus the choke input filter circuit gives approximately constant d.c. voltage across the load. In other words, this filter circuit is having better load regulation compared to that of capacitor input filter in which case the d.c. load voltage depends upon the d.c. load current drawn. Let us calculate the ripple factor for choke input filter, based on the assumptions already made.

The impedance Z_2 of the filter circuit for second harmonic component of input, i.e. at 2ω, will be,

$$Z_2 = (R_x) + (j\,2\omega L) + \left[\frac{1}{j2\omega C} \| R \right]$$

Hence, $$|Z_2| \approx 2\omega L$$

Second harmonic component of the current in the filter circuit, will be

$$I_{2m} = \frac{\frac{4}{3\pi} E_{sm}}{Z_2} \approx \frac{\frac{4}{3\pi} E_{sm}}{2\omega L}$$

The second harmonic voltage across the load is

$$E_{2m} = I_{2m} \times \left[\frac{1}{2\omega C} \| R \right] \approx I_{2m} \times \frac{1}{2\omega C}$$

Since , But, $\frac{1}{2\omega C} << R$, and $2\omega L >> R_x$, as per assumptions.

$$\therefore \quad E_{2m} = I_{2m} \times \frac{1}{2\omega C} = \frac{\frac{4}{3\pi} E_{sm}}{2\omega L} \times \frac{1}{2\omega C}$$

$$\therefore \quad E_{2m} = \frac{4}{3\pi} \frac{E_{sm}}{4\omega^2 LC} = \frac{E_{sm}}{3\pi\omega^2 LC}$$

$$\therefore \quad E_{2rms} = \frac{E_{2m}}{\sqrt{2}} = \frac{E_{sm}}{3\sqrt{2}\,\pi\,\omega^2 LC}$$

Hence the ripple factor is given by,

$$\text{Ripple factor} = \frac{E_{2rms}}{E_{DC}}$$

$$= \frac{E_{sm}}{3\sqrt{2}\,\pi\,\omega^2 LC} \times \frac{1}{\frac{2}{\pi} \frac{E_{sm}}{1+\frac{R_x}{R}}}$$

$$= \frac{1}{6\omega^2 LC\sqrt{2}} \left(1+\frac{R_x}{R}\right) \qquad \text{but } R_x << R$$

$$\therefore \quad \text{Ripple factor} \approx \frac{1}{6\sqrt{2}\,\omega^2 LC}$$

It is seen that the ripple factor for choke-input filter does not depend upon the load resistance unlike the capacitor input filter.

Advantages of Bleeder Resistor

1. It maintains the minimum current necessary for optimum operation of the inductor.
2. It improves voltage regulation of the supply by acting as preload on the supply.
3. It provides safety to the persons handling the equipment, by acting as a discharging path for capacitors.

Ex. 1 : *Determine the ripple factor of an L-type choke input filter comprising of a 10 H choke and 8 μF capacitor, used with a full-wave rectifier. Compare the above result with a simple 8 μ F capacitor input filter with a load current of 50 mA and also 150 mA, assuming the d.c. output voltage to be 50 V.*
Neglect d.c. resistance of choke and assume supply frequency of 50 Hz.

Sol. : The given values are

$$L = 10\ H,\ C = 8\ \mu F,\ I_{DC} = 50\ mA \text{ and } 150\ mA,\ E_{DC} = 50\ V$$

i) For choke input filter

$$\gamma = \frac{1}{6\sqrt{2}\ \omega^2\ LC} = \frac{1}{6\sqrt{2}\ (2\pi f)^2\ LC}$$

$$= \frac{1}{6\sqrt{2}\ (2\pi \times 50)^2 \times 10 \times 8 \times 10^{-6}}$$

$$= 0.01492$$

ii) For capacitor input filter

$$\gamma = \frac{1}{4\sqrt{3}\ f C R_L}$$

$$\text{For } I_{DC} = 50\ mA,\ R_L = \frac{E_{DC}}{I_{DC}} = \frac{50}{50 \times 10^{-3}} = 1 \times 10^3\ \Omega$$

$$\gamma = \frac{1}{\sqrt{3} \times 50 \times 8 \times 10^{-6} \times 1 \times 10^3}$$

$$= 0.36$$

$$\text{For } I_{DC} = 150\ mA,\ R_L = \frac{E_{DC}}{I_{DC}} = \frac{50}{150 \times 10^{-3}} = \frac{1}{3} \times 10^3\ \Omega$$

$$\gamma = \frac{1}{4\sqrt{3} \times 50 \times 8 \times 10^{-6} \times \left(\frac{1}{3}\right) \times 10^3}$$

$$= 1.082$$

It can be seen that as load current increases, the ripple content also increases in case of capacitor input filter.

CLC Filter or π Filter

This is a capacitor filter followed by a L section filter. The ripple rejection capability of π filter is very good. It is shown in the Fig. 5.25

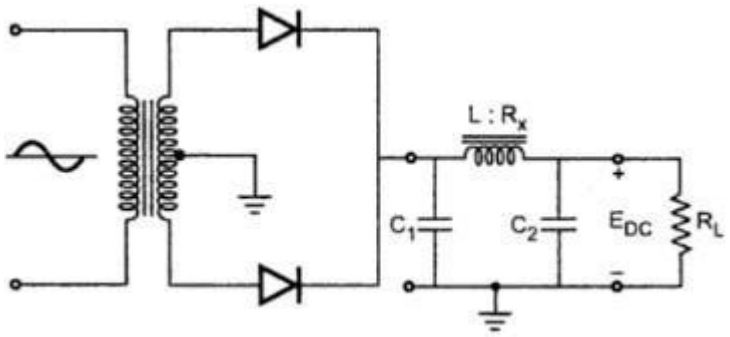


Figure 5.25 π type filter

It consists of an inductance L with a d.c. winding resistance as R_x and two capacitors C_1 and C_2. The filter circuit is fed from full wave rectifier. Generally two capacitors are selected equal. This circuit is basically a capacitor input filter since the first element looking from the rectifier side is a capacitor. All the features, advantages, disadvantages discussed previously for the capacitor input filter using single capacitor are applicable equally to the π filter.

The rectifier output is given to the capacitor C_1. This capacitor offers very low reactance to the a.c. component but blocks d.c. component. Hence capacitor C_1 bypasses most of the a.c. component. The d.c. component then reaches to the choke L. The choke L offers very high reactance to a.c. component and low reactance to d.c. So it blocks a.c. component and does not allow it to reach to load while it allows d.c. component to pass through it. The capacitor C_2 now allows to pass remaining a.c. component and almost pure d.c. component reaches to the load. The circuit looks like a π hence called π filter. To obtain almost pure d.c. to the load, more such π sections may be used one after another.

The output voltage is given by,

$$E_{DC} = E_{sm} - \frac{V_r}{2} - I_{DC} R_x$$

where V_r = Peak to peak ripple voltage

R_x = D.C. resistance of choke

Now $V_r = \frac{I_{DC}}{2fC}$ for full wave

and $= \frac{I_{DC}}{fC}$ for half wave

Ripple factor for π filter

The ripple factor for this filter is given by ,

$$\text{Ripple factor} = \frac{\sqrt{2} \times X_{C1} \times X_{C2}}{X_L R_L}$$

The various reactances X_{C_1}, X_{C_2}, X_L are to be calculated at twice the supply frequency since the circuit is fed from a full wave rectifier circuit.

Hence,

$$X_{C_1} = \frac{1}{2\omega C_1}$$

$$X_{C_2} = \frac{1}{2\omega C_2}$$

$$X_L = 2\omega L$$

$$\therefore \quad \text{Ripple factor} = \frac{\sqrt{2}\left(\frac{1}{2\omega C_1}\right)\left(\frac{1}{2\omega C_2}\right)}{(2\omega L)(R_L)}$$

$$\therefore \quad \boxed{\gamma = \frac{\sqrt{2}}{8\omega^3 LC_1 C_2 R_L}}$$

Since this π type filter employes three fitering elements, the riple is reduced to the great extent.

If C_1 and C_2 are expressed in microfarads and frequency f is assumed to be 50 Hz then we get,

$$\gamma = \frac{\sqrt{2}}{8(2\pi \times 50)^3 \times \left(C_1 \times 10^{-6} \times C_2 \times 10^{-6} \times L \times R_L\right)}$$

$$\therefore \quad \boxed{\gamma \approx \frac{5700}{L C_1 C_2 R_L}}$$

where C_1 and C_2 are in μF, L in henries and R_L in ohms.

Advantages and Disadvantages of π Filter

Advantages

The various advantages of π filter are,

1. For a same total value of L and C, the ripple factor of π filter is much smaller than multiple LC section filter.
2. Higher d.c. output voltage at high load currents can be achieved.
3. The output is very much smoother.

Disadvantages

The various disadvantages of π filter are,

1. The voltage regulation is poor.
2. Higher values of PIV rating for the diodes.

Example 1 : *Calculate the ripple factor for a π type filter, employing 10 H choke and two equal capacitors 16 μF each and fed from a full wave rectifier and 50 Hz mains. The load resistance is 4 k Ω.*

Solution : The given values are,

$C_1 = C_2 = 16\ \mu F, \quad L = 10\ H, \quad R_L = 4\ k\Omega = 4000\ \Omega, \quad f = 50\ Hz$

$$\therefore \quad \gamma = \frac{\sqrt{2}}{8\omega^3 LC_1C_2R_L} = \frac{\sqrt{2}}{8(2\pi f)^3 LC_1C_2R_L}$$

$$= \frac{\sqrt{2}}{8(2\pi\times 50)^3 \times 10\times 16\times 10^{-6}\times 16\times 10^{-6}\times 4000} = 5.56\times 10^{-4}$$

Thus the ripple is 0.055% which shows that with π filter the output is almost pure d.c.

Comparison of Filter Circuits

Parameter	Type of filter			
	L	C	LC	π
E_{DC} (no load)	0.636 E_{sm}	E_{sm}	E_{sm}	E_{sm}
E_{DC} (load I_{DC})	0.636 E_{sm}	$E_{sm} - \frac{I_{DC}}{4fC}$	0.636 E_{sm}	$E_{sm} - \frac{I_{DC}}{4fC}$
Ripple factor (γ)	$\frac{R_L}{3\sqrt{2}\omega L}$	$\frac{1}{4\sqrt{3}\,fRC}$	$\frac{1}{6\sqrt{2}\omega^2 LC}$	$\frac{\sqrt{2}}{8\omega^3 LC_1C_2R_L}$
PIV	2 E_{sm}	2 E_{sm}	2 E_{sm}	2 E_{sm}

Key Point: *Above comparison is for full wave rectifiers with filters and diode, transformer and filter element resistances are neglected.*

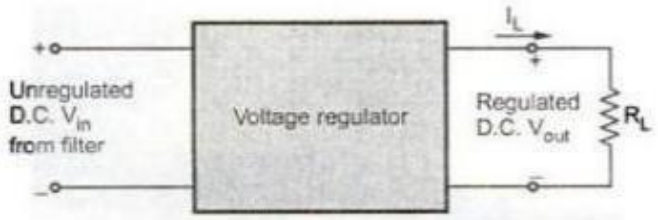
Regulators

None of the electronic circuits work properly with unregulated power supply. They require constant voltage supply regardless of the variations in the input voltage or load current. In order to ensure this, a voltage stabilizing device, called voltage regulator is used.

Key Point: *The **voltage regulator** circuit keeps the output voltage constant inspite of changes in load current or input voltage.*

Thus a voltage regulator is a must for every electronic circuit. But it is also necessary to build an unregulated supply before a voltage regulator is connected to a given circuit.

A voltage regulator is a device designed to keep the output voltage of a power supply as nearly constant as possible.



As shown in the Fig.5.26, the input to a voltage regulator circuit is unregulated d.c. input voltage, while the output of the voltage regulator circuit is regulated d.c. output voltage, V_{out}, which is almost constant.

Figure 5.26 Voltage Regulator

Voltage Regulator Characteristics

Load Regulation:

The load regulation is the change in the regulated output voltage when the load current is changed from minimum (no load) to maximum (full load).

The load regulation is denoted as LR and mathematically expressed as,

$$LR = V_{NL} - V_{FL}$$

where V_{NL} = load voltage with no load current

V_{FL} = load voltage with full load current

The load regulation is often expressed as percentage by dividing the LR by full load voltage and multiplying result by 100.

$$\therefore \quad \% \ LR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

Line Regulation or Source Regulation:

The SR is defined as the change in the regulated load voltage for a specified range of line voltage, typically 230 V ± 10 %.

Mathematically it is expressed as,

$$SR = V_{HL} - V_{LL}$$

where V_{HL} = load voltage with high line voltage

V_{LL} = load voltage with low line voltage

The percentage source regulation is defined as,

$$\% \ SR = \frac{SR}{V_{nom}} \times 100$$

where V_{nom} = nominal load voltage

Basic Voltage Regulator

The basic voltage regulator in its simplest form consists of,

1. Voltage reference, V_R
2. Error amplifier
3. Feedback network
4. Active series or shunt control element

The voltage reference generates a voltage level which is applied to the comparator circuit, which is generally error amplifier. The second input to the error amplifier is obtained through feedback network. Generally using the potential divider, the feedback signal is derived by sampling the output voltage. The error amplifier converts the difference between the output sample and the reference voltage into an error signal. This error signal inturn controls the active element of the regulator circuit, in order to compensate the change in the output voltage. Such an active element is generally a transistor.

Types of Voltage Regulators

Depending upon where the control element is connected in the regulator circuit, the regulators are basically classified as,

1. Series voltage regulator
2. Shunt voltage regulator

Each type provides a constant d.c. output voltage which is regulated.

Shunt Voltage Regulator

The heart of any voltage regulator circuit is a control element. If such a control element is connected in shunt with the load, the regulator circuit is called shunt voltage regulator. The Fig.1.28 shows the block diagram of shunt voltage regulator circuit.

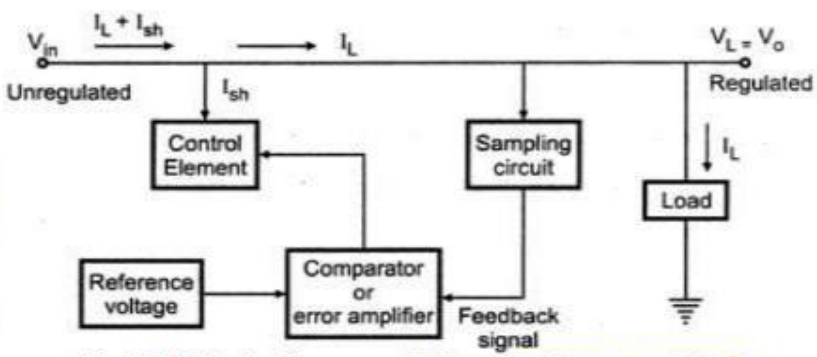


Fig.5.27 Block diagram of shunt voltage regulator

The unregulated input voltage V_{in}, tries to provide the load current. But part of the current is drawn by the control element, to maintain the constant voltage across the load. If there is any change in the load voltage, the sampling circuit provides a feedback signal to the comparator circuit. The comparator circuit compares the feedback signal with the reference voltage and generates a control signal which decides the amount of current required to be shunted to

keep the load voltage constant. For example if the load voltage increases then the comparator circuit decides the control signal based on the feedback information, which draws the increased shunt current I_{sh}. Due to this the load current I_L decreases, hence the load voltage decreases to its normal value.

Key Point: *Thus the control element maintains the constant output voltage by shunting the current, hence the circuit is called shunt voltage regulator.*

Series Voltage Regulator

If in a voltage regulator circuit, the control element is connected in series with the load, the circuit is called series voltage regulator circuit. Fig.5.28 shows the block diagram of series voltage regulator circuit.

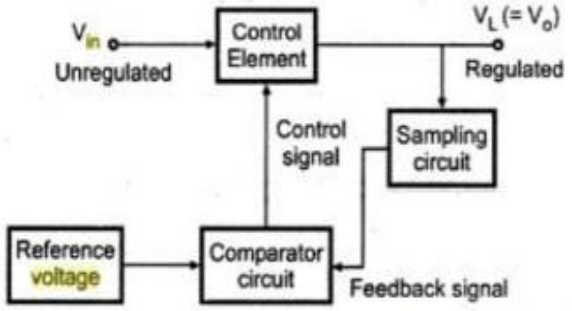


Fig.5.28 **Block diagram of series voltage regulator**

The unregulated d.c. voltage is the input to the circuit. The control element, controls the amount of the input voltage, that gets to the output. The sampling circuit provides the necessary feedback signal. The comparator circuit compares the feedback with the reference voltage to generate the appropriate control signal.

For example, if the load voltage tries to increase, the comparator generates a control signal based on the feedback information. This control signal causes the control element to decrease the amount of the output voltage. Thus the output voltage is maintained constant.

Key Point: *Thus, control element which regulates the load voltage based on the control signal is in series with the load and hence the circuit is called series voltage regulator circuit.*

Zener diode as a shunt regulator

The simplest shunt voltage regulator circuit uses a zener diode, to regulate the load voltage. The Fig.5.29 shows the arrangement of zener diode in a regulator circuit.

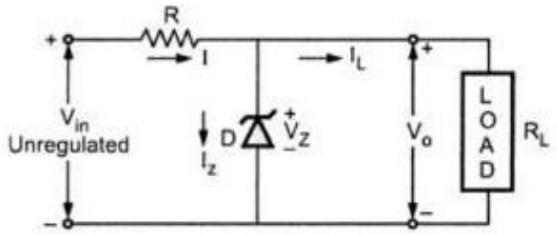


Figure. 5.29 Zener diode as a shunt regulator

Regulation with varying input voltage

The Fig. 5.30 shows a zener regulator under varying input voltage condition.

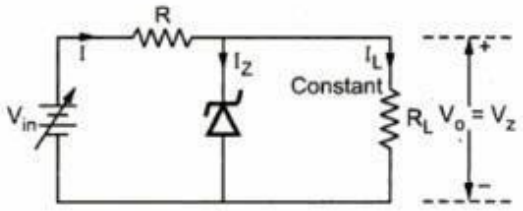


Figure 5.30 Varying input condition

It can be seen that the output is

$V_o = V_Z$ is constant.

$$\therefore \quad I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{constant}$$

And $I = I_Z + I_L$

Now if V_{in} increases, then the total current I increases. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L constant.

But as long as I_Z is between I_{Zmin} and I_{Zmax}, the V_Z i.e. output voltage V_o is constant. Thus the changes in input voltage get compensated and output is maintained constant.

Similarly if V_{in} decreases, then current I decreases. But to keep I_L constant, I_Z decreases. As long as I_Z is between I_{Zmax} and I_{Zmin}, the output voltage remains constant.

Steps to Analyse Zener Regulator with Varying Input

The steps are,

1. Calculate the load current which is constant

$$\therefore \quad I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L}$$

2. To find $V_{in(min)}$, the current through zener must be I_{Zmin} to keep it reverse biased.

$$\therefore \quad I = I_L + I_{Zmin}$$

$$\therefore \quad V_{in}(min) = V_Z + I \times R$$

3. To find $V_{in}(max)$, the current through zener must be maximum equal to I_{Zmax}.

$$\therefore \quad I = I_L + I_{Zmax}$$

$$\therefore \quad V_{in(max)} = V_Z + I \times R$$

4. Hence the range of input is $V_{in(min)}$ to $V_{in(max)}$ for which output will be constant equal to V_Z.

Using the same steps, for given V_{in} range the resistance values can be obtained and zener regulator can be designed.

The maximum power dissipation in the zener diode is given by,

$$P_D = V_Z I_{Z(max)}$$

The zener diode must be selected with power dissipating rating higher than P_D.

Regulation with varying Load

The Fig.5.31 shows a zener regulator under varying load condition and constant input voltage.

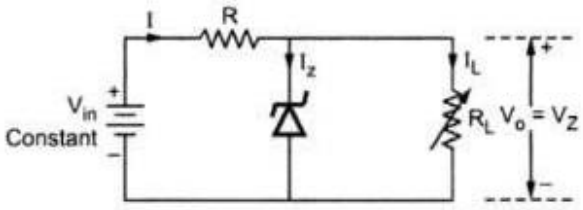


Figure 5.31 Varying load condition

The input voltage is constant while the load resistance R_L is variable. As V_{in} is constant and
$V_o = V_Z$ is constant, then for constant R the current I is constant.

$$\therefore \quad I = \frac{V_{in} - V_Z}{R} \text{ constant } = I_L + I_Z$$

Now if R_L decreases so I_L increases, to keep I constant I_Z decreases. But as long as it is between I_{Zmin} and I_{Zmax}, output voltage V_o will be constant. Similarly if R_L increases so I_L decreases, to keep I constant I_Z increases. But as long as it is between I_{Zmin} and I_{Zmax}, output voltage V_o will be constant.

Steps to Analyse Zener Regulator with Varying Load

The steps are,

1. Calculate total current I which is constant.

$$\therefore \quad I = \frac{V_{in} - V_Z}{R}$$

2. To find $I_{L(min)}$, $I_Z = I_{Zmax}$

$$\therefore \quad I_{L(min)} = I - I_{Zmax}$$

3. To find $I_{L(max)}$, $I_Z = I_{Zmin}$

$$\therefore \quad I_{L(max)} = I - I_{Zmin}$$

4. Thus $I_{L(min)}$ to $I_{L(max)}$ is the range of load current for which output voltage remains constant.

The maximum power dissipation in zener remains same as,

$$P_D = V_Z I_{Zmax}$$

Advantages of IC Voltage Regulators

The various advantages of IC voltage regulators are,

1. Easy to use.
2. It greatly simplifies power supply design.
3. Due to mass production, low in cost.
4. IC voltage regulators are versatile.
5. Conveniently used for local regulation.
6. These are provided with features like built in protection, programmable output, current/voltage boosting, internal short circuit current limiting etc.

Classification of IC Voltage Regulators

The IC voltage regulators are classified as shown in the Fig.1.33 .

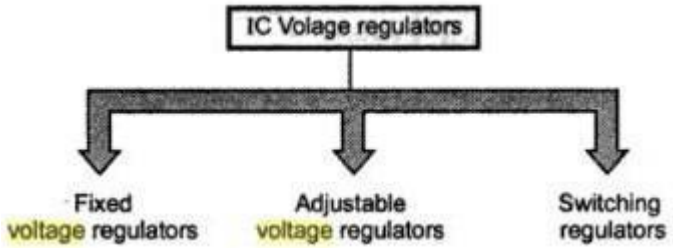


Figure 5.32 Classification of IC regulators

Three terminal fixed voltage regulators

As the name suggests, three terminal voltage regulators have three terminals namely input which is unregulated (V_{in}), regulated output (V_o) and common or a ground terminal. These regulators do not require any feedback connections. The Fig. 1.34 shows the basic three terminal voltage regulator.

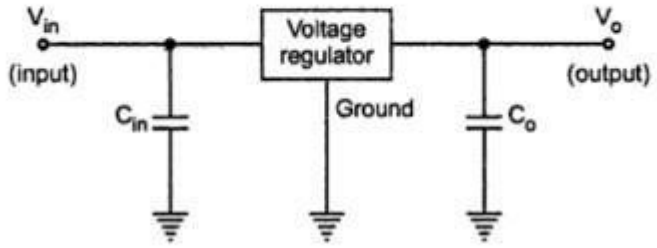


Figure 5.33 Three terminal voltage regulators

The capacitor C_{in} is required if regulator is located at appreciable distance, more than 5 cm from a power supply filter. The output capacitor C_o may not be needed but if used it improves the transient response of the regulator i.e. regulator response to the transient changes in the load. This capacitor also reduces the noise present at the output. The difference between V_{in} and V_o ($V_{in} - V_o$) is called as dropout voltage and it must be typically 2.0 V even during the low point on the input ripple voltage, for the proper functioning of the regulator.

IC series of 3 terminal fixed voltage regulators

The popular IC series of three terminal regulators is μA78XX and μA79XX. The series μA78XX is the series of three terminal **positive** voltage regulators while μA79XX is the series of three terminal **negative** voltage regulators. The last two digits denoted as XX, indicate the output voltage rating of the IC.

Such series is available with seven voltage options as indicated in Table 1

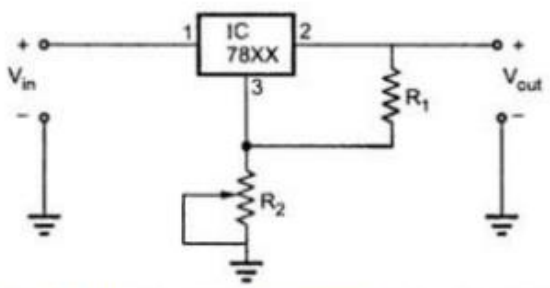
Device type	Output Voltage	Device type	Output Voltage
7805	5.0 V	7905	– 5.0 V
7806	6.0 V	7906	– 6.0 V
7808	8.0 V	7908	– 8.0 V
7812	12.0 V	7912	– 12.0 V
7815	15.0 V	7915	– 15.0 V
7818	18.0 V	7918	– 18.0 V
7824	24.0 V	7924	– 24.0 V

Table 1

The 79XX series voltage regulators are available with same seven options as 78XX series, as indicated in Table 13.3. In addition, two extra voltages –2 V and –5.2 V are also available with ICs 7902 and 7905.2 respectively.

These ICs are provided with adequate heat sinking and can deliver output currents more than 1 A. These ICs do not require external components. These are provided with internal thermal protection, overload and short circuit protection.

Adjustable regulator using 78XX series



Though IC 78XX series regulators have fixed value of the regulated output voltage, by connecting two resistances externally, an adjustable output voltage can be obtained.

The typical connection of 78XX IC regulator to obtain variable output voltage is shown in the Fig. **5.34**

Figure 5.34 Adjustable regulator using IC 78XX

$$V_{out} = V_{reg}\left[1+\frac{R_2}{R_1}\right]$$

where V_{reg} = Regulated fixed voltage of IC

By varying R_2, variable output voltage can be obtained.

Need of Switched Mode Power Supply

A linear regulator power supply has following limitations :

1. The required input step down transformer is bulky and expensive.
2. Due to low line frequency (50 Hz), large values of filter capacitors are required.
3. The efficiency is very low.
4. Input must be greater than the output voltage.
5. As large is the difference between input and output voltage, more is the power dissipation in the series pass transistor.
6. For higher input voltages, efficiency decreases.
7. The need for dual supply, is not economical and feasible to achieve with the help of linear regulators.

Thus in modern days, to overcome all these limitations Switched Mode Power Supplies (SMPS) are needed.

Block diagram of SMPS

A switching power supply is shown in Fig. 1.36 . The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type.

Its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits. The current drawn from V_{ref} is usually very small (~ 10 mA), so the power loss in the series pass regulator does not affect the overall efficiency of the switched mode power supply (SMPS). Transistors Q_1 and Q_2 are alternately switched ***off*** and ***on*** at 20 kHz. These transistors are either fully ***on*** ($V_{CE\ sat}$ ~ 0.2V) or cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer.

The secondary is centre-tapped and full wave rectification is achieved by diodes D_1 and D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_0.

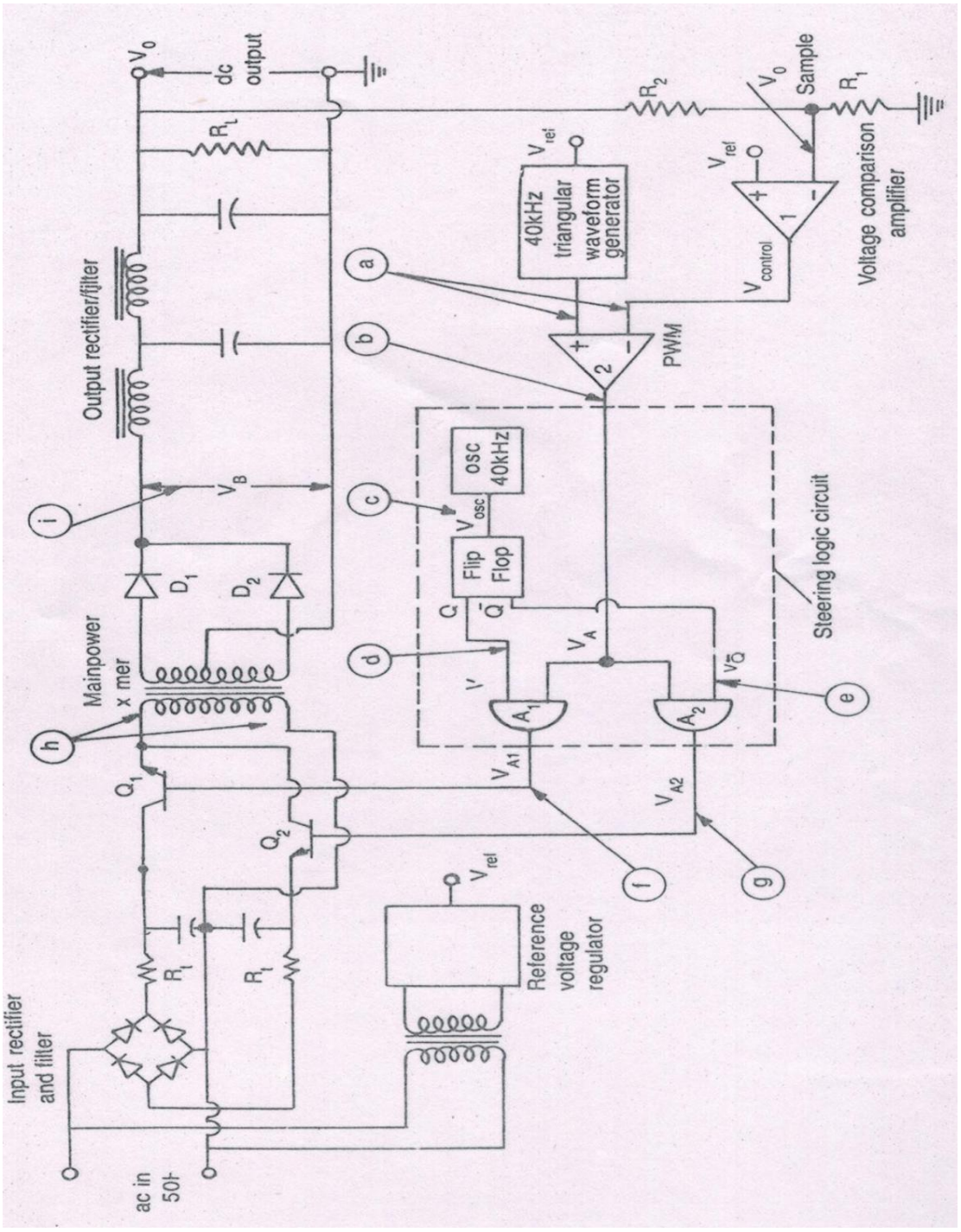


Figure 5.35 Block diagram of switched mode power supply

The regulation of V_o is achieved by the feedback circuit consisting of a pulse-width modulator and steering logic circuit. The output voltage V_o is sampled by a R_1R_2 divider and a fraction $R_1/(R_1+R_2)$ is compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is shown in Figure 5.36

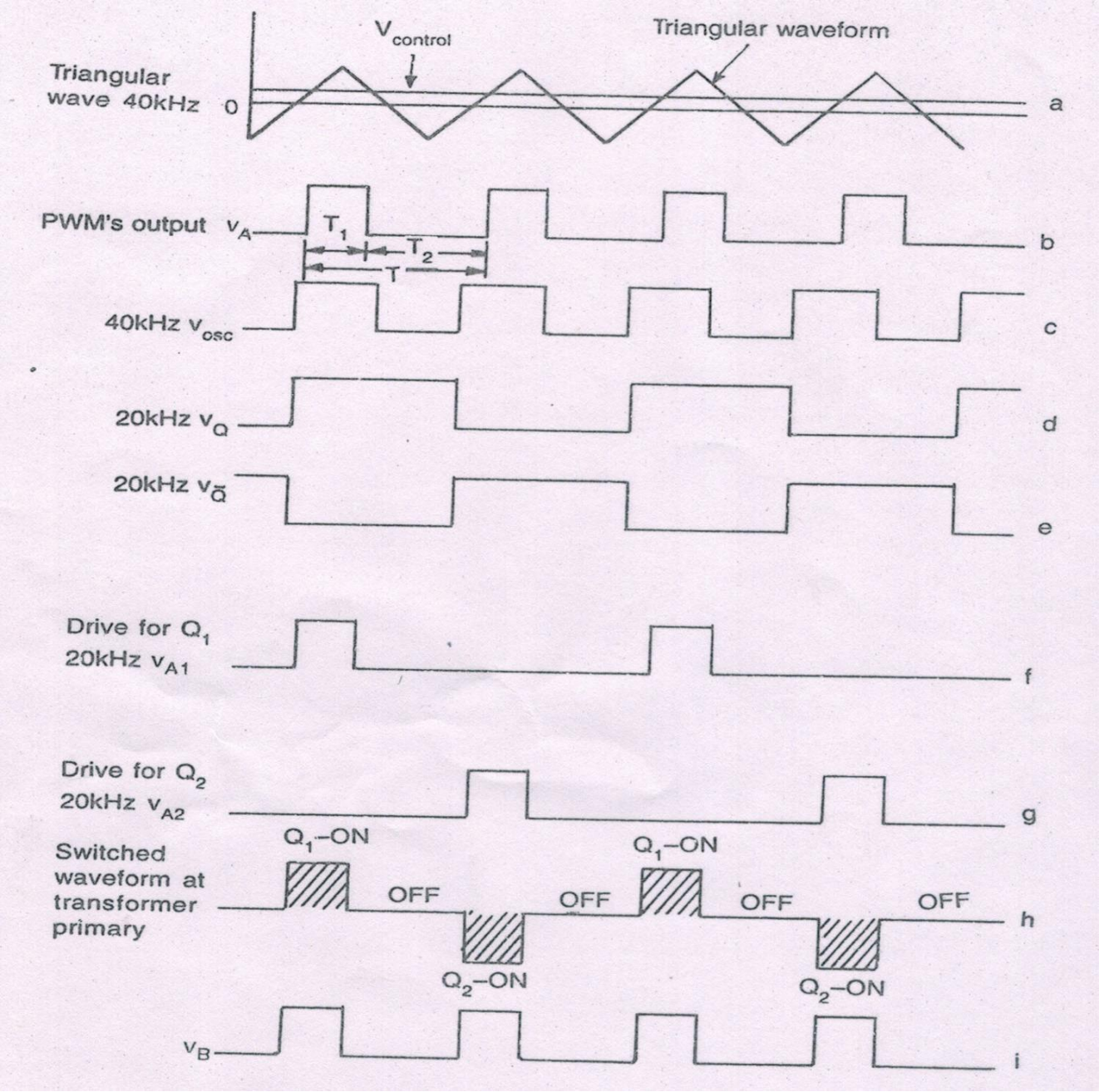


Figure 5.36 Waveforms of switched mode power supply

$V_{control}$ is applied to the (–) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz (also shown in Figure 5.36 (a) is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave v_A (Figure 5.36 (b)) of period $T(f = 40$ kHz). The duty cycle of the square wave is $T_1/(T_1 + T_2)$ and varies with $V_{control}$ which in turn varies with the variation of v_o.

The output v_A drives a steering logic circuit shown in the dashed block. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce two complementary outputs v_Q and $v_{\overline{Q}}$ shown in Figure 5.36 (d) and (e). The output v_{A1} and v_{A2} of AND gates A_1 and A_2 are shown in Figure 5.36 (f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is *on*, the waveform at the input of the transformer will be a square wave as shown in Figure 5.36 (h). The rectified output v_B is shown in Figure 5.36 (i).

If there is a rise in dc output voltage V_o, the voltage control $V_{control}$ of the comparator 1 also rises. This changes the intersection of the $V_{control}$ with the triangular waveform and in this case decreases the time period T_1 in the waveform of Figure 5.36 This in turn decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_o. Thus the initial rise in the dc output voltage V_o has been nullified.

An inspection of Fig. 5.35 shows that the output current passes through the power switch consisting of transistors Q_1 and Q_2, inductor having low resistance and the load. Hence using a switch with low losses (transistor with small $V_{CE\,(sat)}$ and high switching speed) and a filter with high quality factor, the conversion efficiency can easily exceed 90%.

Power Amplifiers/Large signal Amplifiers

One method used to distinguish the electrical characteristics of different types of amplifiers is by "class", and as such amplifiers are classified according to their circuit configuration and method of operation. Then Amplifier Classes is the term used to differentiate between the different amplifier types. Amplifier Classes represent the amount of the output signal which varies within the amplifier circuit over one cycle of operation when excited by a sinusoidal input signal. The classification of amplifiers range from entirely linear operation (for use in high-fidelity signal amplification) with very low efficiency, to entirely nonlinear (where a faithful signal reproduction is not so important) operation but with a much higher efficiency, while others are a compromise between the two.

Amplifier classes are mainly lumped into two basic groups. The first are the classically controlled conduction angle amplifiers forming the more common amplifier classes of A, B, AB and C, which are defined by the length of their conduction state over some portion of the output waveform, such that the output stage transistor operation lies somewhere between being "fully- ON" and "fully-OFF".

The second set of amplifiers are the newer so called "switching" amplifier classes of D, E, F, G, S, T etc, which use digital circuits and pulse width modulation (PWM) to constantly switch the signal between "fully-ON" and "fully-OFF" driving the output hard into the transistors saturation and cutoff regions.

Class A Amplifier

A Class A power amplifier is one in which the output current flows for the entire cycle of the AC input supply. Hence the complete signal present at the input is amplified at the output.

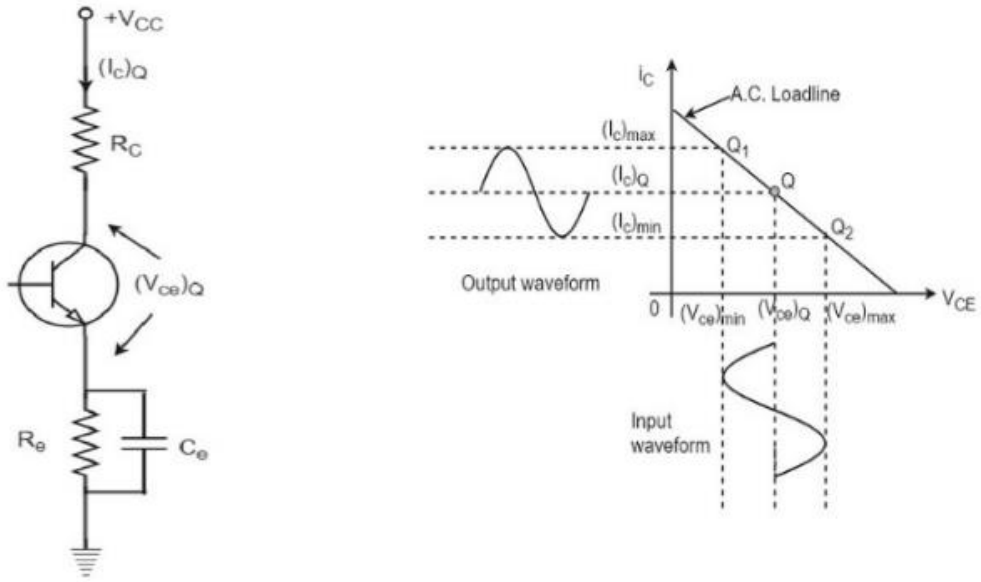


Figure 5.37 Class A Amplifier and its output characteristics

To achieve high linearity and gain, the output stage of a class A amplifier is biased "ON" (conducting) all the time. Then for an amplifier to be classified as "Class A" the zero signal idle current in the output stage must be equal to or greater than the maximum load current (usually a loudspeaker) required to produce the largest output signal. As a class A amplifier operates in the linear portion of its characteristic curves, the single output device conducts through a full 360 degrees of the output waveform. Then the class A amplifier is equivalent to a current source.

The output characteristics with operating point Q is shown in the figure above. Here (Ic)Q and (Vce)Q represent no signal collector current and voltage between collector and emitter respectively. When signal is applied, the Q-point shifts to Q1 and Q2.

The output current increases to (Ic)max and decreases to (Ic)min. Similarly, the collector-emitter voltage increases to (Vce)max and decreases to (Vce)min.

D.C Power drawn from collector battery Vcc is given by

$$P_{in} = voltage \times current = V_{CC}(I_C)_Q$$

This power is used in the following two parts −

- Power dissipated in the collector load as heat is given by

$$P_{RC} = (current)^2 \times resistance = (I_C)_Q^2 R_C$$

- Power given to transistor is given by

$$P_{tr} = P_{in} - P_{RC} = V_{CC} - (I_C)_Q^2 R_C$$

When signal is applied, the power given to transistor is used in the following two parts −

- A.C. Power developed across load resistors RC which constitutes the a.c. power output.

$$(P_O)_{ac} = I^2 R_C = \frac{V^2}{R_C} = \left(\frac{V_m}{\sqrt{2}}\right)^2 \frac{1}{R_C} = \frac{V_m^2}{2R_C}$$

Where **I** is the R.M.S. value of a.c. output current through load, **V** is the R.M.S. value of a.c. voltage, and $\mathbf{V_m}$ is the maximum value of V.

Expression for overall efficiency

$$(P_O)_{ac} = V_{rms} \times I_{rms}$$

$$= \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] \times \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right]$$

$$= \frac{[(V_{ce})_{max} - (V_{ce})_{min}] \times [(I_C)_{max} - (I_C)_{min}]}{8}$$

Therefore

$$(\eta)_{overall} = \frac{[(V_{ce})_{max} - (V_{ce})_{min}] \times [(I_C)_{max} - (I_C)_{min}]}{8 \times V_{CC}(I_C)_Q}$$

Overall Efficiency

The overall efficiency of the amplifier circuit is given by

$$(\eta)_{overall} = \frac{a.c\ power\ delivered\ to\ the\ load}{total\ power\ delivered\ by\ d.c\ supply}$$

$$= \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

Collector Efficiency

The collector efficiency of the transistor is defined as

$$(\eta)_{collector} = \frac{average\ a.c\ power\ output}{average\ d.c\ power\ input\ to\ transistor}$$

$$= \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Advantages of Class A Amplifiers

The advantages of Class A power amplifier are as follows −

The current flows for complete input cycle

It can amplify small signals

The output is same as input

No distortion is present

Disadvantages of Class A Amplifiers

Low power output

Low collector efficiency

Transformer coupled class A power amplifier

The circuit in which the output current flows for the entire cycle of the AC input supply.

The disadvantage is that it has low output power and efficiency.

In order to minimize those effects, the transformer coupled class A power amplifier has been introduced.

It is similar to the normal amplifier circuit but connected with a transformer in the collector load.

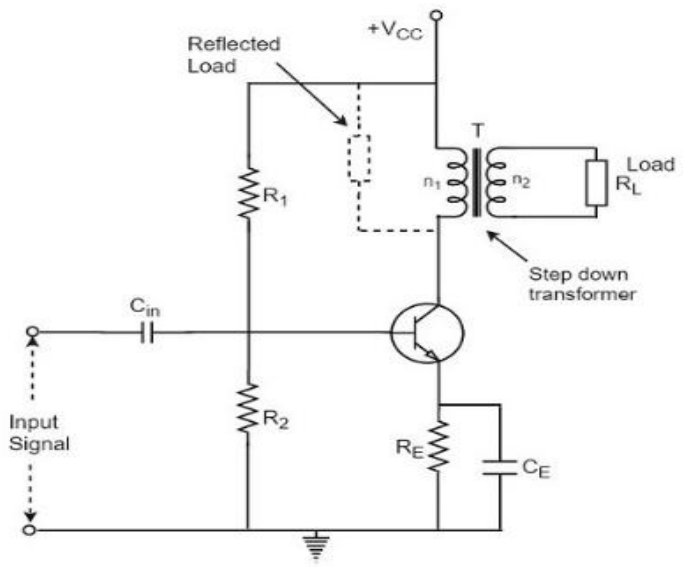


Figure 5.38 Transformer coupled Class A Amplifier

Here R1 and R2 provide potential divider arrangement. The resistor Re provides stabilization, Ce is the bypass capacitor and Re to prevent a.c. voltage.

The transformer used here is a step-down transformer.

The high impedance primary of the transformer is connected to the high impedance collector circuit. The low impedance secondary is connected to the load (generally loud speaker).

Transformer Action

The transformer used in the collector circuit is for impedance matching. RL is the load connected in the secondary of a transformer. RL' is the reflected load in the primary of the transformer.

The number of turns in the primary are n1 and the secondary are n2. Let V1 and V2 be the primary and secondary voltages and I1 and I2 be the primary and secondary currents respectively.

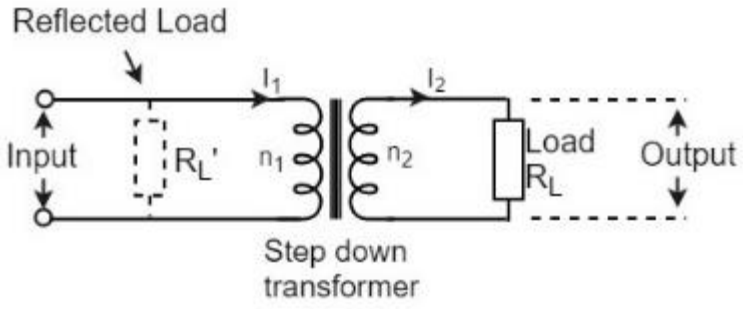


Figure 5.39 Transformer action

$$\frac{V_1}{V_2} = \frac{n_1}{n_2} \; and \; \frac{I_1}{I_2} = \frac{n_1}{n_2} \qquad V_1 = \frac{n_1}{n_2} V_2 \; and \; I_1 = \frac{n_1}{n_2} I_2$$

$$\frac{V_1}{I_1} = \left(\frac{n_1}{n_2}\right)^2 \frac{V_2}{I_2}$$

But $V_1/I_1 = R_L'$ = effective input resistance

And $V_2/I_2 = R_L$ = effective output resistance

Therefore,

$$R_L' = \left(\frac{n_1}{n_2}\right)^2 R_L = n^2 R_L$$

Where

$$n = \frac{number\ of\ turns\ in\ primary}{number\ of\ turns\ in\ secondary} = \frac{n_1}{n_2}$$

A power amplifier may be matched by taking proper turn ratio in step down transformer.

Circuit Operation

If the peak value of the collector current due to signal is equal to zero signal collector current, then the maximum a.c. power output is obtained. So, in order to achieve complete amplification, the operating point should lie at the center of the load line.

The operating point obviously varies when the signal is applied. The collector voltage varies in opposite phase to the collector current. The variation of collector

voltage appears across the primary of the transformer.

Circuit Analysis

The power loss in the primary is assumed to be negligible, as its resistance is very small.

The input power under dc condition will be

$$(P_{in})_{dc} = (P_{tr})_{dc} = V_{CC} \times (I_C)_Q$$

Under maximum capacity of class A amplifier, voltage swings from $(V_{ce})_{max}$ to zero and current from $(I_c)_{max}$ to zero.

Hence

$$V_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max} - (V_{ce})_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(V_{ce})_{max}}{2}\right] = \frac{2V_{CC}}{2\sqrt{2}} = \frac{V_{CC}}{\sqrt{2}}$$

$$I_{rms} = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max} - (I_C)_{min}}{2}\right] = \frac{1}{\sqrt{2}}\left[\frac{(I_C)_{max}}{2}\right] = \frac{2(I_C)_Q}{2\sqrt{2}} = \frac{(I_C)_Q}{\sqrt{2}}$$

Advantages

The advantages of transformer coupled class A power amplifier are as follows.

No loss of signal power in the base or collector resistors.

Excellent impedance matching is achieved.

Gain is high.

DC isolation is provided.

Disadvantages

The disadvantages of transformer coupled class A power amplifier are as follows.

Low frequency signals are less amplified comparatively.

Hum noise is introduced by transformers.

Transformers are bulky and costly.

Poor frequency response.

Applications

The applications of transformer coupled class A power amplifier are as follows.

This circuit is where impedance matching is the main criterion.

These are used as driver amplifiers and sometimes as output amplifiers.

Therefore,

$$(P_O)_{ac} = V_{rms} \times I_{rms} = \frac{V_{CC}}{\sqrt{2}} \times \frac{(I_C)_Q}{\sqrt{2}} = \frac{V_{CC} \times (I_C)_Q}{2}$$

Therefore,

$$\text{Collector Efficiency} = \frac{(P_O)_{ac}}{(P_{tr})_{dc}}$$

Or,

$$(\eta)_{collector} = \frac{V_{CC} \times (I_C)_Q}{2 \times V_{CC} \times (I_C)_Q} = \frac{1}{2}$$

$$= \frac{1}{2} \times 100 = 50\%$$

The efficiency of a class A power amplifier is nearly than 30% whereas it has got improved to 50% by using the transformer coupled class A power amplifier.

Push-Pull Class A Power Amplifier

The main problems that should be dealt with are low power output and efficiency. It is possible to obtain greater power output and efficiency than that of the Class A amplifier by using a combinational transistor pair called as Push-Pull configuration.

two complementary transistors in the output stage with one transistor being an NPN or N-channel type while the other transistor is a PNP or P-channel (the complement) type connected in order to operate them like PUSH a transistor to ON and PULL another transistor to OFF at the same time. This push-pull

configuration can be made in class A, class B, class C or class AB amplifiers.

Construction of Push-Pull Class A Power Amplifier

The construction of the class A power amplifier circuit in push-pull configuration is shown as in the figure below. This arrangement mainly reduces the harmonic distortion introduced by the non-linearity of the transfer characteristics of a single transistor amplifier.

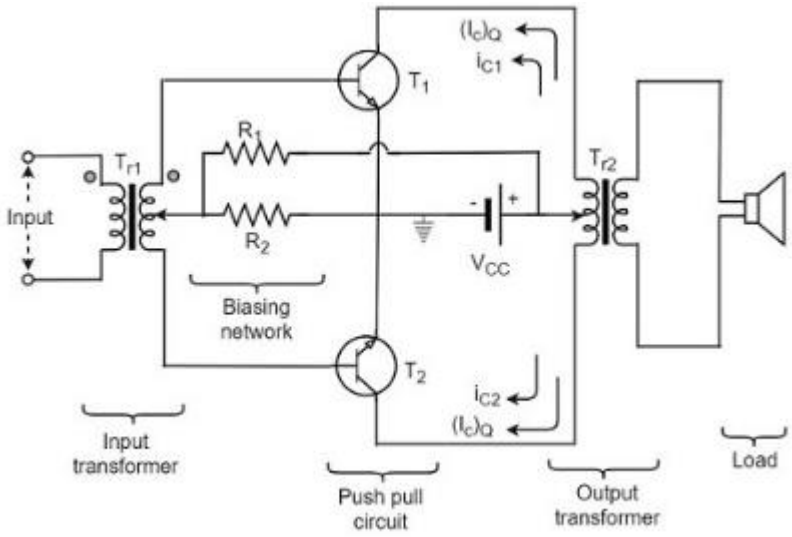


Figure.5.40 Push-Pull Class A Power Amplifier

In Push-pull arrangement, the two identical transistors T1 and T2 have their emitter terminals shorted. The input signal is applied to the transistors through the transformer Tr1 which provides opposite polarity signals to both the transistor bases. The collectors of both the transistors are connected to the primary of output transformer Tr2. Both the transformers are center tapped. The VCC supply is provided to the collectors of both the transistors through the primary of the output transformer.

The resistors R1 and R2 provide the biasing arrangement. The load is generally a loudspeaker which is connected across the secondary of the output transformer. The turns ratio of the output transformer is chosen in such a way that the load is well matched with the output impedance of the transistor. So maximum power is

delivered to the load by the amplifier.

Circuit Operation

The output is collected from the output transformer Tr2. The primary of this transformer Tr2 has practically no dc component through it. The transistors T1 and T2 have their collectors connected to the primary of transformer Tr2 so that their currents are equal in magnitude and flow in opposite directions through the primary of transformer Tr2.

When the a.c. input signal is applied, the base of transistor T1 is more positive while the base of transistor T2 is less positive. Hence the collector current ic1 of transistor T1 increases while the collector current ic2 of transistor T2 decreases. These currents flow in opposite directions in two halves of the primary of output transformer. Moreover, the flux produced by these currents will also be in opposite directions.

Hence, the voltage across the load will be induced voltage whose magnitude will be proportional to the difference of collector currents i.e.

$$(i_{c1} - i_{c2})$$

Similarly, for the negative input signal, the collector current i_{c2} will be more than i_{c1}. In this case, the voltage developed across the load will again be due to the difference

$$(i_{c1} - i_{c2})$$

$$\text{As} \quad i_{c2} > i_{c1}$$

The polarity of voltage induced across load will be reversed.

$$i_{c1} - i_{c2} = i_{c1} + (-i_{c2})$$

The overall operation results in an a.c. voltage induced in the secondary of output transformer and hence a.c. power is delivered to that load.

It is understood that, during any given half cycle of input signal, one transistor is being driven (or pushed) deep into conduction while the other being non-conducting (pulled out). Hence the name Push-pull amplifier. The harmonic distortion in Push-pull amplifier is minimized such that all the even harmonics are eliminated.

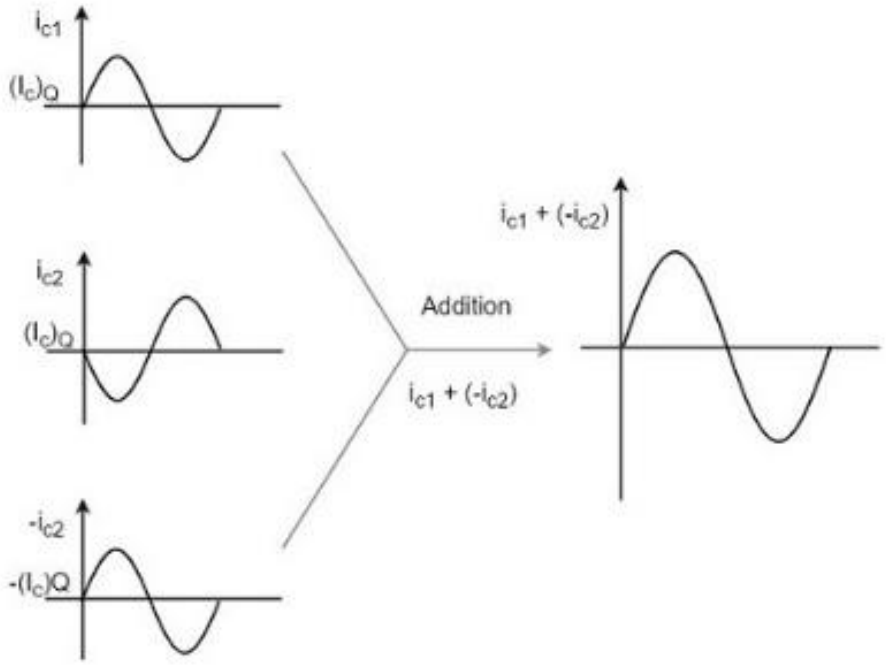


Figure.5.41 Output Waveform in Push-Pull Class A Power Amplifier

Advantages

High a.c. output is obtained.

The output is free from even harmonics.

The effect of ripple voltages are balanced out. These are present in the power supply due to inadequate filtering.

Disadvantages

The transistors are to be identical, to produce equal amplification.

Center-tapping is required for the transformers.

The transformers are bulky and costly.

Class B Amplifier

Class B amplifiers were invented as a solution to the efficiency and heating problems associated with the previous class A amplifier. The basic class B amplifier uses two complimentary transistors either bipolar of FET for each half of the waveform with its output stage configured in a "push-pull" type arrangement, so that each transistor device amplifies only half of the output waveform.

When the input signal goes positive, the positive biased transistor conducts while the negative transistor is switched "OFF". Likewise, when the input signal goes negative, the positive transistor switches "OFF" while the negative biased transistor turns "ON" and conducts the negative portion of the signal. Thus the transistor conducts only half of the time, either on positive or negative half cycle of the input signal. Then we can see that each transistor device of the class B amplifier only conducts through one half or 180 degrees of the output waveform in strict time alternation, but as the output stage has devices for both halves of the signal waveform the two halves are combined together to produce the full linear output waveform.

More clearly, when the collector current flows only during the positive half cycle of the input signal, the power amplifier is known as class B power amplifier.

The biasing of the transistor in class B operation is in such a way that at zero signal condition, there will be no collector current. The operating point is selected to be at collector cut off voltage. So, when the signal is applied, only the positive half cycle is amplified at the output.

When the signal is applied, the circuit is forward biased for the positive half cycle of the input and hence the collector current flows. But during the negative half cycle of the input, the circuit is reverse biased and the collector current will be

absent. Hence only the positive half cycle is amplified at the output.

As the negative half cycle is completely absent, the signal distortion will be high. Also, when the applied signal increases, the power dissipation will be more. But when compared to class A power amplifier, the output efficiency is increased. Well, in order to minimize the disadvantages and achieve low distortion, high efficiency and high output power, the push-pull configuration is used in this class B amplifier.

Class B Push-Pull Amplifier

Though the efficiency of class B power amplifier is higher than class A, as only one half cycle of the input is used, the distortion is high. Also, the input power is not completely utilized. In order to compensate these problems, the push-pull configuration is introduced in class B amplifier.

Construction

The circuit of a push-pull class B power amplifier consists of two identical transistors T1 and T2 whose bases are connected to the secondary of the center-tapped input transformer Tr1. The emitters are shorted and the collectors are given the VCC supply through the primary of the output transformer Tr2.

The circuit arrangement of class B push-pull amplifier, is same as that of class A push-pull amplifier except that the transistors are biased at cut off, instead of using the biasing resistors. The figure below gives the detailing of the construction of a push-pull class B power amplifier.

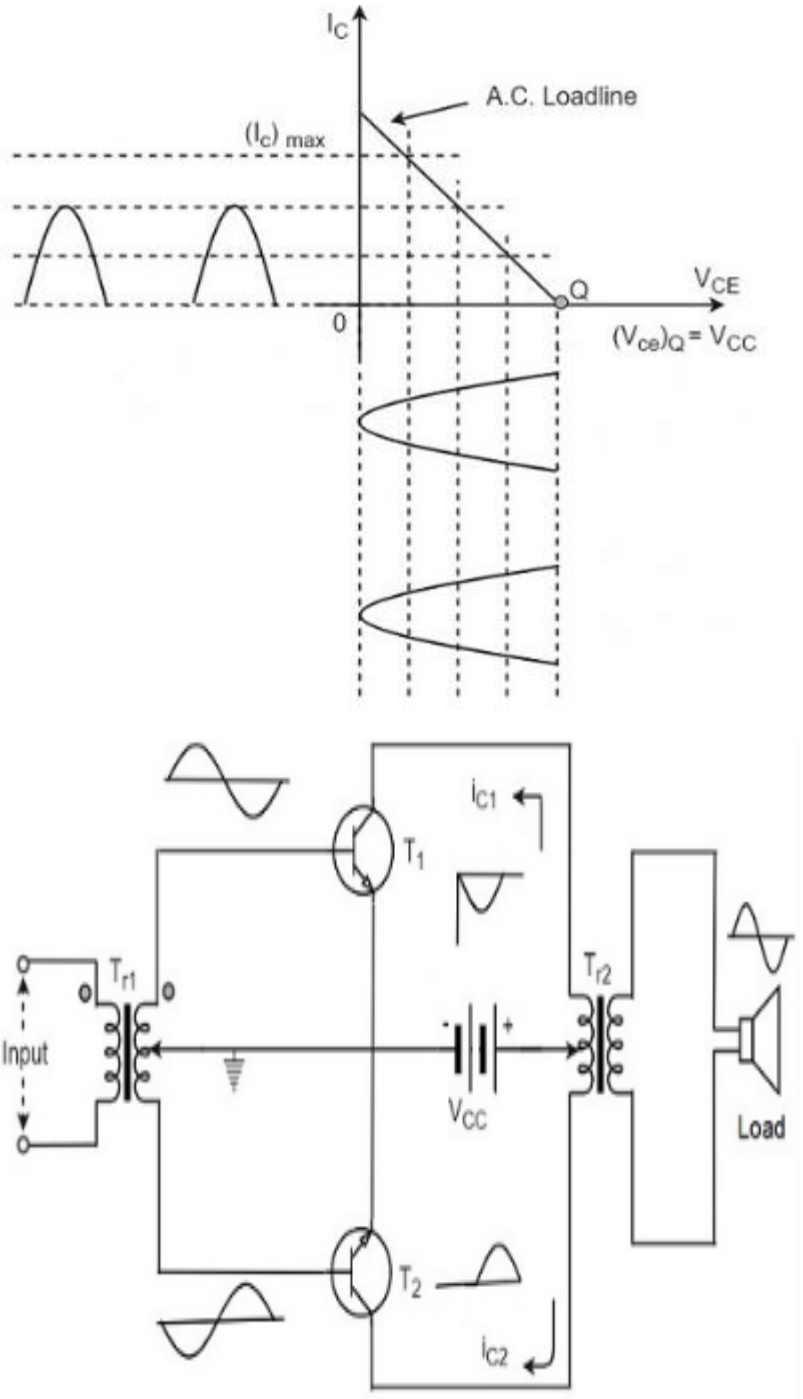


Figure 5.42 Class B Amplifier

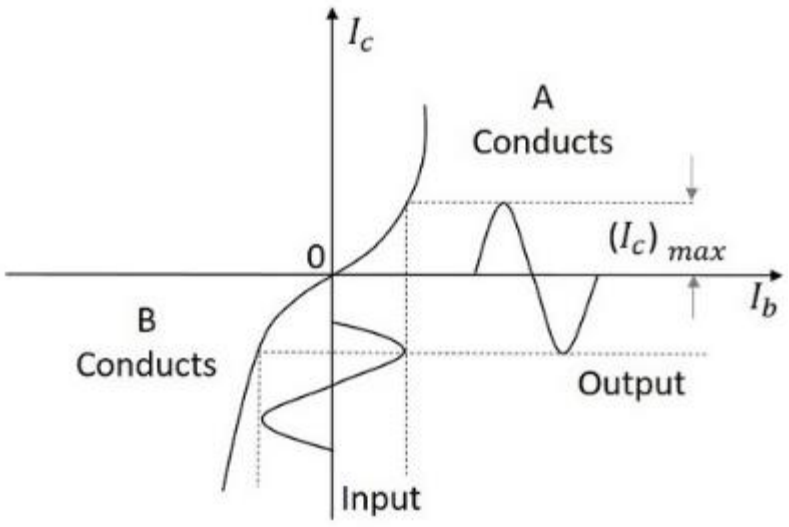


Figure 5.43 Output wave forms of Class B Amplifier

The transformers are center-tapped. When no signal is applied at the input, the transistors T1 and T2 are in cut off condition and hence no collector currents flow. As no current is drawn from VCC, no power is wasted.

When input signal is given, it is applied to the input transformer Tr1 which splits the signal into two signals that are 180o out of phase with each other. These two signals are given to the two identical transistors T1 and T2. For the positive half cycle, the base of the transistor T1 becomes positive and collector current flows. At the same time, the transistor T2 has negative half cycle, which throws the transistor T2 into cutoff condition and hence no collector current flows.

For the next half cycle, the transistor T1 gets into cut off condition and the transistor T2 gets into conduction, to contribute the output. Hence for both the cycles, each transistor conducts alternately. The output transformer Tr3 serves to join the two currents producing an almost undistorted output waveform.

Power Efficiency of Class B Push-Pull Amplifier

The current in each transistor is the average value of half sine loop.

For half sine loop, I_{dc} is given by

$$I_{dc} = \frac{(I_C)_{max}}{\pi}$$

Therefore,

$$(p_{in})_{dc} = 2 \times \left[\frac{(I_C)_{max}}{\pi} \times V_{CC}\right]$$

Here factor 2 is introduced as there are two transistors in push-pull amplifier.

R.M.S. value of collector current = $(I_C)_{max}/\sqrt{2}$

R.M.S. value of output voltage = $V_{CC}/\sqrt{2}$

Under ideal conditions of maximum power

Therefore,

$$(P_O)_{ac} = \frac{(I_C)_{max}}{\sqrt{2}} \times \frac{V_{CC}}{\sqrt{2}} = \frac{(I_C)_{max} \times V_{CC}}{2}$$

Now overall maximum efficiency

$$\eta_{overall} = \frac{(P_O)_{ac}}{(P_{in})_{dc}}$$

$$= \frac{(I_C)_{max} \times V_{CC}}{2} \times \frac{\pi}{2(I_C)_{max} \times V_{CC}}$$

$$= \frac{\pi}{4} = 0.785 = 78.5\%$$

The collector efficiency would be the same.

Hence the class B push-pull amplifier improves the efficiency than the class A push-pull amplifier.

Complementary Symmetry Push-Pull Class B Amplifier

The push pull amplifier which was just discussed improves efficiency but the usage of center-tapped transformers makes the circuit bulky, heavy and costly. To make the circuit simple and to improve the efficiency, the transistors used can be complemented

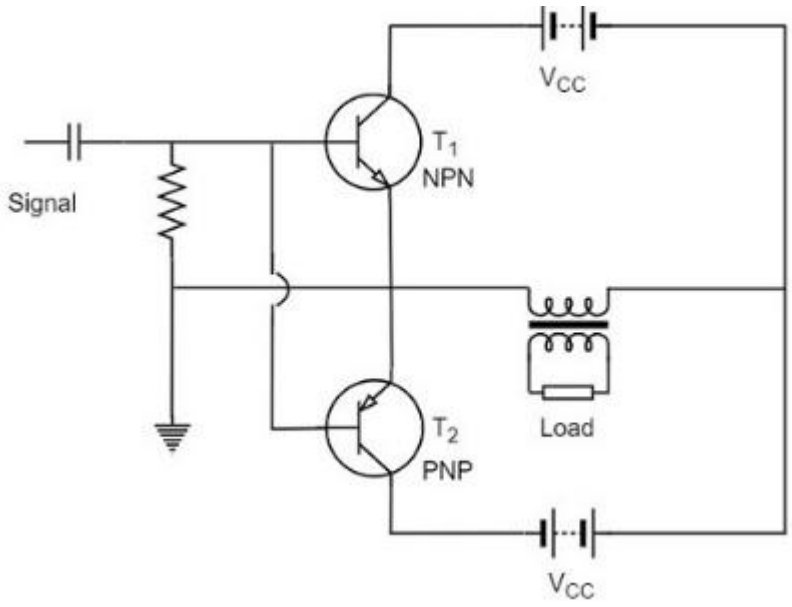


Figure 5.44 Complementary Symmetry Push-Pull Class B Amplifier

The above circuit employs a NPN transistor and a PNP transistor connected in push pull configuration. When the input signal is applied, during the positive half cycle of the input signal, the NPN transistor conducts and the PNP transistor cuts off. During the negative half cycle, the NPN transistor cuts off and the PNP transistor conducts.

In this way, the NPN transistor amplifies during positive half cycle of the input, while PNP transistor amplifies during negative half cycle of the input. As the transistors are both complement to each other, yet act symmetrically while being connected in push pull configuration of class B, this circuit is termed as Complementary symmetry push pull class B amplifier.

Advantages

As there is no need of center tapped transformers, the weight and cost are reduced.

Equal and opposite input signal voltages are not required.

Disadvantages

It is difficult to get a pair of transistors (NPN and PNP) that have similar characteristics.

We require both positive and negative supply voltages.

Class AB Amplifier

As its name suggests, the Class AB Amplifier is a combination of the "Class A" and the "Class B" type amplifiers. The AB classification of amplifier is currently one of the most common used types of audio power amplifier design. The class AB amplifier is a variation of a class B amplifier as described above, except that both devices are allowed to conduct at the same time around the wave forms crossover point eliminating the crossover distortion problems of the previous class B amplifier.

****a new circuit which would have all the advantages of both class A and class B**

Cross-over Distortion

In the push-pull configuration, the two identical transistors get into conduction, one after the other and the output produced will be the combination of both.

When the signal changes or crosses over from one transistor to the other at the zero voltage point, it produces an amount of distortion to the output wave shape. For a transistor in order to conduct, the base emitter junction should cross 0.7v, the cut off voltage. The time taken for a transistor to get ON from OFF or to get OFF from ON state is called the transition period.

At the zero voltage point, the transition period of switching over the transistors from one to the other, has its effect which leads to the instances where both the transistors are OFF at a time. Such instances can be called as Flat spot or Dead band on the output wave shape

This cross over distortion effect also reduces the overall peak to peak value of the output waveform which in turn reduces the maximum power output.

It is understood that this cross-over distortion is less pronounced for large input signals, where as it causes severe disturbance for small input signals. This cross over distortion can be eliminated if the conduction of the amplifier is more than one half cycle, so that both the transistors won't be OFF at the same time.

This idea leads to the invention of class AB amplifier, which is the combination of both class A and class B amplifiers.

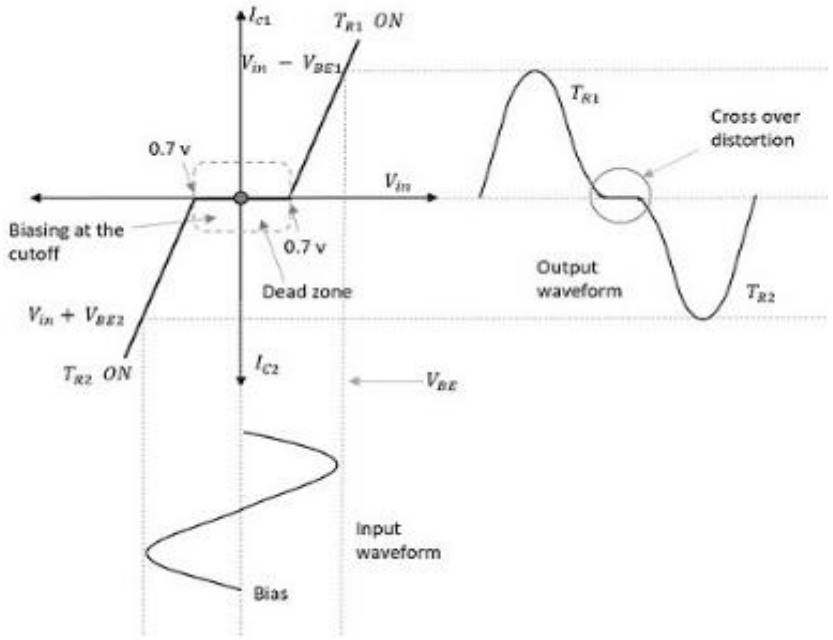


Figure 5.45 Cross over Distortion

As the name implies, class AB is a combination of class A and class B type of amplifiers. As class A has the problem of low efficiency and class B has distortion problem, this class AB is emerged to eliminate these two problems, by utilizing the advantages of both the classes.

The cross over distortion is the problem that occurs when both the transistors are OFF at the same instant, during the transition period. In order to eliminate this, the condition has to be chosen for more than one half cycle. Hence, the other transistor gets into conduction, before the operating transistor switches to cut off state. This is achieved only by using class AB configuration.

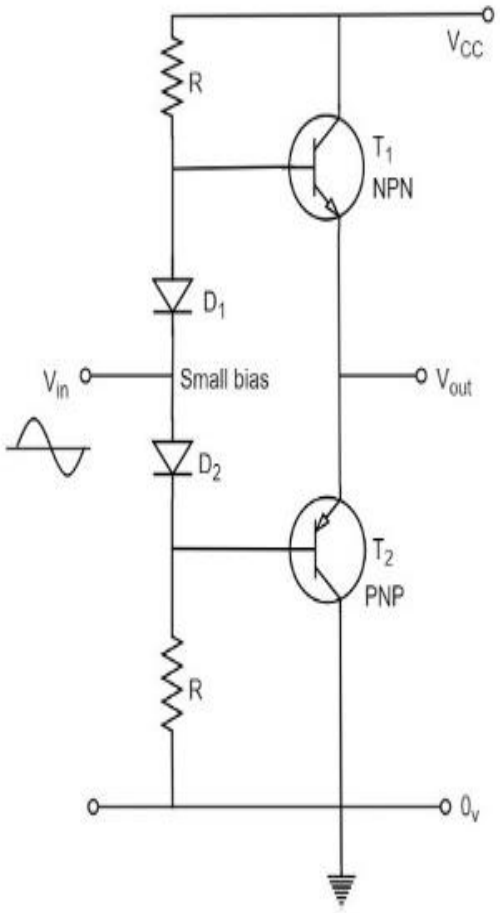


Figure 5.46 Class AB Amplifier

Therefore, in class AB amplifier design, each of the push-pull transistors is conducting for slightly more than the half cycle of conduction in class B, but much less than the full cycle of conduction of class A.

The conduction angle of class AB amplifier is somewhere between 180o to 360o depending upon the operating point selected.

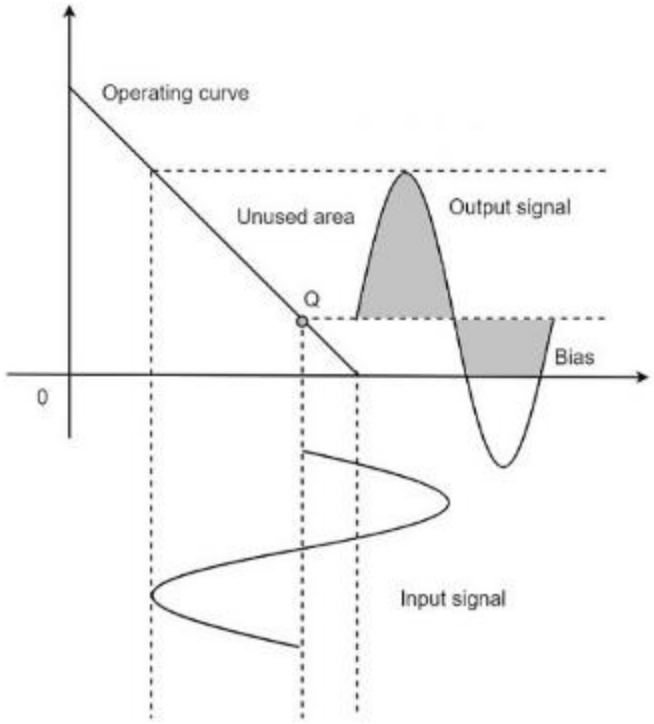


Figure 5.47 Output wave forms of Class AB Amplifier

The small bias voltage given using diodes D1 and D2, as shown in the above figure, helps the operating point to be above the cutoff point. Hence the output waveform of class AB results as seen in the above figure. The crossover distortion created by class B is overcome by this class AB, as well the inefficiencies of class A and B don't affect the circuit.

So, the class AB is a good compromise between class A and class B in terms of efficiency and linearity having the efficiency reaching about 50% to 60%. The class A, B and AB amplifiers are called as linear amplifiers because the output signal amplitude and phase are linearly related to the input signal amplitude and phase.

The advantage of this small bias voltage, provided by series diodes or resistors, is that the crossover distortion created by the class B amplifier characteristics is overcome, without the inefficiencies of the class A amplifier design. •So the class AB amplifier is a good compromise between class A and class B in terms of efficiency and linearity, with conversion efficiency reaching about 50% to 60%

Class C Power Amplifier

Class C Power Amplifier design has the greatest efficiency but the poorest linearity of the classes of amplifiers mentioned here. The previous classes, A, B and AB are considered linear amplifiers, as the output signals amplitude and phase are linearly related to the input signals amplitude and phase. However, the class C amplifier is heavily biased so that the output current is zero for more than one half of an input sinusoidal signal cycle with the transistor idling at its cut-off point.

When the collector current flows for less than half cycle of the input signal, the power amplifier is known as class C power amplifier.

The efficiency of class C amplifier is high while linearity is poor. The conduction angle for class C is less than 180o. It is generally around 90o, which means the transistor remains idle for more than half of the input signal. So, the output current will be delivered for less time compared to the application of input signal.

This kind of biasing gives a much improved efficiency of around 80% to the amplifier, but introduces heavy distortion in the output signal. Using the class C amplifier, the pulses produced at its output can be converted to complete sine wave of a particular frequency by using LC circuits in its collector circuit.

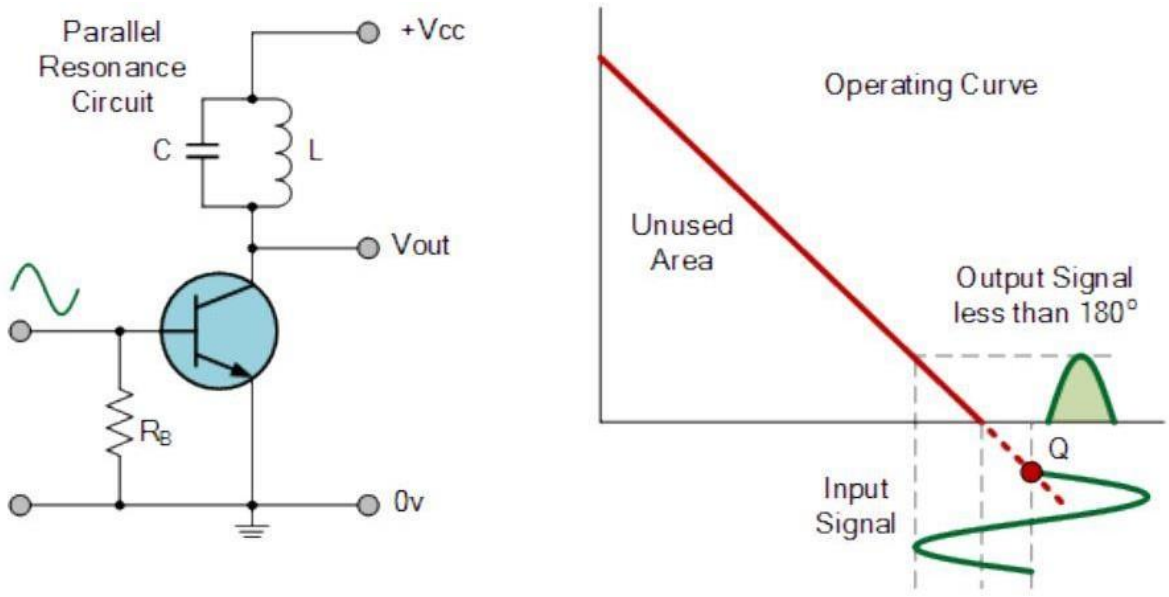


Figure 5.48.Class C Amplifier

Due to its heavy audio distortion, class C amplifiers are commonly used in high frequency sine wave oscillators and certain types of radio frequency amplifiers, where the pulses of current produced at the amplifiers output can be converted to complete sine waves of a particular frequency by the use of LC resonant circuits in its collector circuit.

Class D Power Amplifier

A Class D audio amplifier is basically a non-linear switching amplifier or PWM amplifier. Class-D amplifiers theoretically can reach 100% efficiency, as there is no period during a cycle were the voltage and current wave forms overlap as current is drawn only through the transistor that is on.

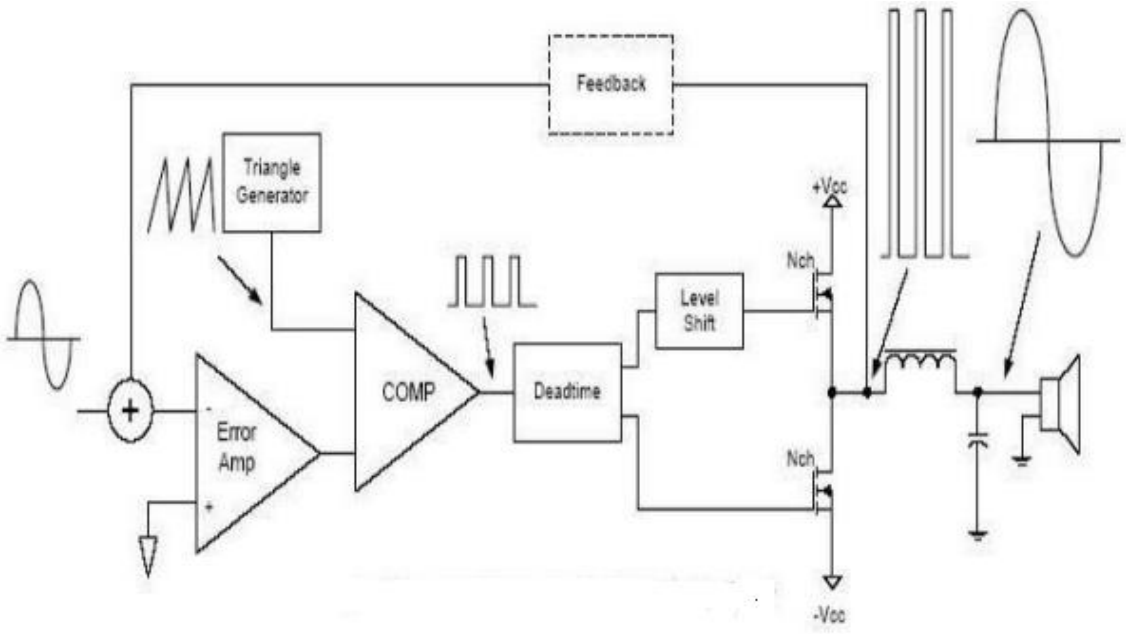


Figure 5.49.Block Diagram of Class D Amplifier

Amplifier Classes and Efficiency

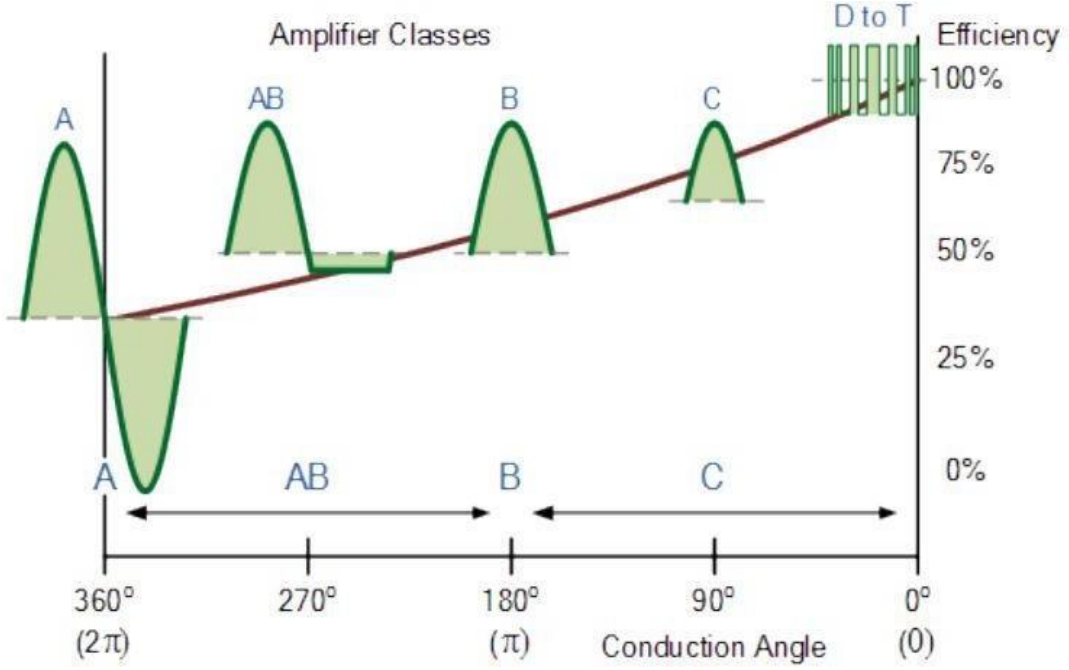


Figure 5.50. Amplifier classes and their efficiency

Amplifier Class by Conduction Angle

Amplifier Class	Description	Conduction Angle
Class-A	Full cycle 360° of Conduction	$\theta = 2\pi$
Class-B	Half cycle 180° of Conduction	$\theta = \pi$
Class-AB	Slightly more than 180° of conduction	$\pi < \theta < 2\pi$
Class-C	Slightly less than 180° of conduction	$\theta < \pi$
Class-D to T	ON-OFF non-linear switching	$\theta = 0$

Crossover Distortion

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed VBE before a transistor conducts. Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting, as shown in Figure. The resulting distortion in the output waveform is called crossover distortion.

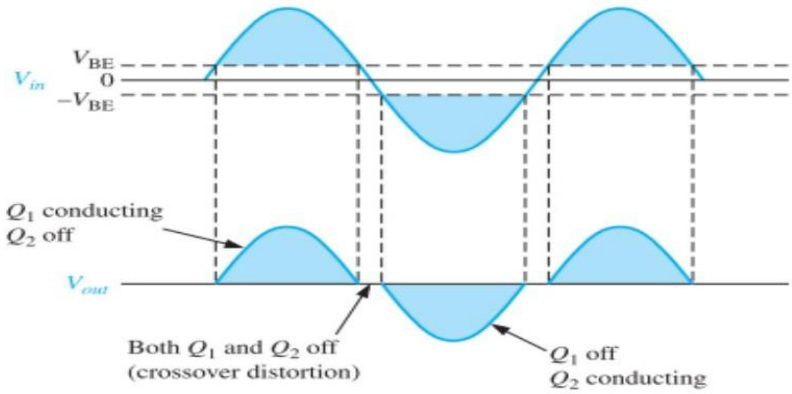


Figure 5.51. Cross over distortion