SATHYABAMA
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SCHOOL OF BIO AND CHEMICAL ENGINEERING

DEPARTMENT OF BIOMEDICAL ENGINEERING

UNIT – I –BIOSIGNAL CONDITIONING– SBMA1504

1. Introduction to OPAMP

Signal conditioning is the manipulation of an analog signal in such a way that it meets the requirements of the next stage for further processing.

- Signal conditioning is stage of instrumentation system used for modifying the transducer signal into a usable format for the final.

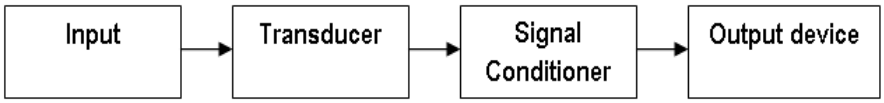

Fig: 1.1 Signal Conditioning Process

Need of Signal Conditioner

- Drive the output device connected at the output of system
- It is required to perform following operations.
    1. Amplification 2. Modulation/Demodulation 3. Attenuation 4. Sampling
    5. Integration 6. Differentiation 7. Addition/ Subtraction
- An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon.
- The active components are transistors and diodes and passive components are resistors and capacitors.
- OP-AMP is basically a multistage amplifier which uses a number of amplifier stages interconnected to each other.
- The integrated op amp offers all the advantage of monolithic integrated circuit such as small size, high reliability, reduced cost, less power consumption.
- It is a versatile device that can be used to amplify AC as well as DC input signals & designed for computing mathematical functions such as addition, subtraction ,multiplication, integration & differentiation

1.1 Integrated Circuits

An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon. The active components are transistors and diodes and passive components are resistors and capacitors.

Advantages of integrated circuits

- Miniaturization and hence increased equipment density.
- Cost reduction due to batch processing.

- Increased system reliability due to the elimination of soldered joints.
- Improved functional performance.
- Matched devices.
- Increased operating speeds.
- Reduction in power consumption

Classification

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip). Based upon above requirement two different IC technologies namely Monolithic Technology and Hybrid Technology have been developed. In monolithic IC, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bounds.

Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimetres. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level integration. These digital ICs, typically microprocessors, DSPs, and micro controllers work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, mixing, etc. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such circuits offer smaller size and lower cost, but must carefully account for signal interference

1.2 Introduction to Operational Amplifier OP AMP

- An integrated circuit (IC) is a miniature, low cost electronic circuit consisting of active and passive components fabricated together on a single crystal of silicon.
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- OP-AMP is basically a multistage amplifier which uses a number of amplifier stages

interconnected to each other.

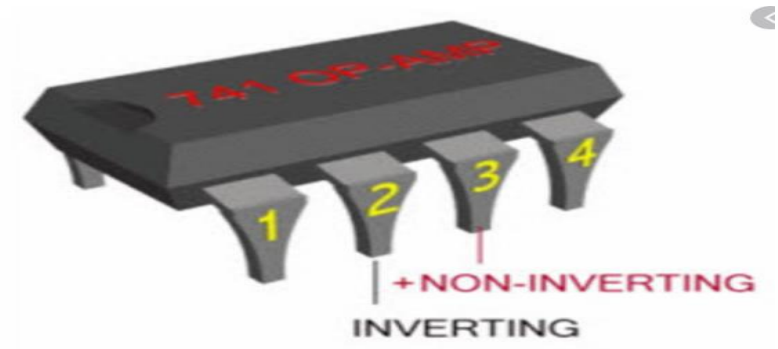
- The integrated op amp offers all the advantage of monolithic integrated circuit such as small size, high reliability, reduced cost, less power consumption.
- It is a versatile device that can be used to amplify AC as well as DC input signals & designed for computing mathematical functions such as addition, subtraction, multiplication, integration & differentiation
- The term "operational amplifier" denotes a special type of amplifier that, by proper selection of its external components, could be configured for a variety of operations.

HISTORY

- First developed by John R. Ragazzine in 1947 with vacuum tube.
- In 1960 at FAIRCHILD SEMICONDUCTOR CORPORATION, Robert J. Widlar fabricated op amp with the help of IC fabrication technology.
- In 1968 FAIRCHILD introduces the op-amp that was to become the industry standard.

What is OP-AMP?

- An operational amplifier (op-amp) is a DC-coupled high-gain electronic voltage amplifier. Direct-coupled high gain amplifier usually consisting of one or more differential amplifiers
- Output stage is generally a push-pull or push-pull complementary-symmetry pair.
- Op amps are differential amplifiers, and their output voltage is proportional to the difference of the two input voltages.



Op-Amp Symbol

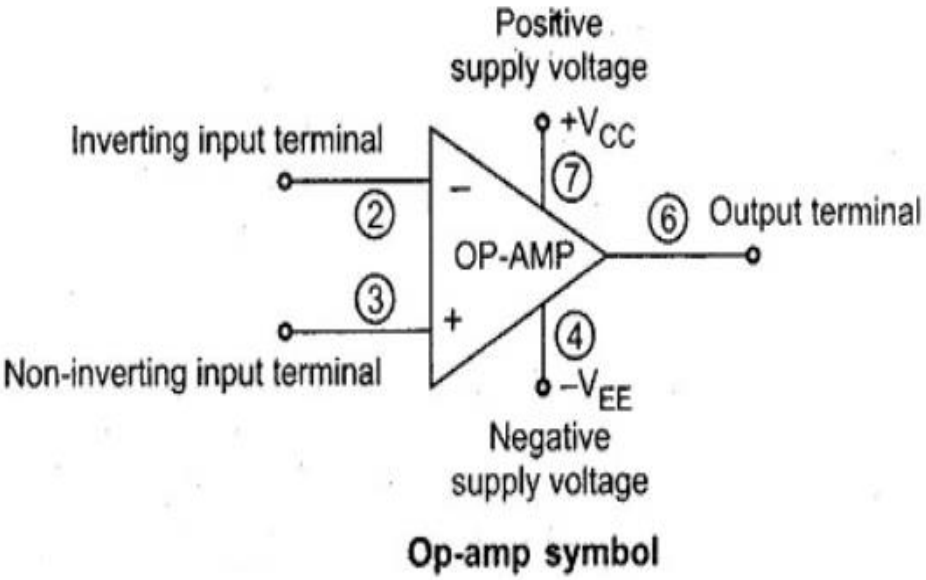


Fig: 1.2 Opamp Symbol

Pin Diagram

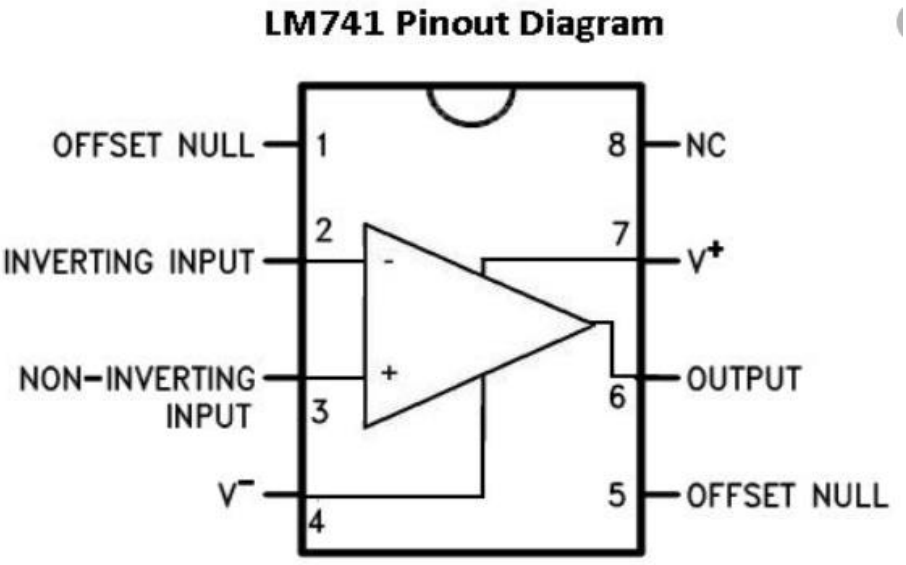


Fig: 1.3 Pin Diagram

Block Diagram of OP-AMP

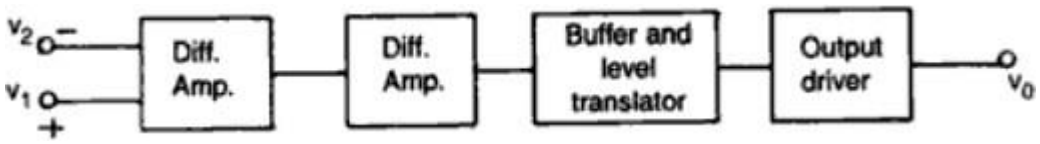


Fig: 1.4 Block Diagram of OP-AMP

The input stage is a differential amplifier. The differential amplifier used as an input stage provides differential inputs and a frequency response down to DC. Special techniques are used to provide the high input impedance necessary for the operational amplifier. The second stage is a high-gain voltage amplifier. This stage may be made from several TRANSISTORs to provide high gain. A typical operational amplifier could have a voltage gain of 200,000. Most of this gain comes from the voltage amplifier stage. The final stage of the OP AMP is an output amplifier. The output amplifier provides low output impedance. The actual circuit used could be an emitter follower. The output stage should allow the operational amplifier to deliver several mill amperes to a load.

1.3 Ideal op-amp characteristics

- Infinite voltage gain A.
- Infinite input resistance Ri, so that almost any signal source can drive it and there is no loading of the proceeding stage.
- Zero output resistance Ro, so that the output can drive an infinite number of other devices.
- Zero output voltage, when input voltage is zero.
- Infinite bandwidth, so that any frequency signals from o to ∞ HZ can be amplified without attenuation.
- Infinite common mode rejection ratio, so that the output common mode noise voltage is zero.
- Infinite slew rate, so that output voltage changes occur simultaneously with input voltage changes.

1.4 OP-AMP characteristics

The OP-AMP characteristics (parameters) are important in practice because, we can use them to compare the performance of various op amp ICs and select the best suitable from them for the required application.

OP-AMP characteristics are classified into two categories namely AC characteristic and DC characteristic.

Open loop voltage gain - It is the differential gain of an OP-AMP in the open loop mode of operation.

Input resistance - It is defined as the equivalent resistance which can be measured at either at inverting or non- inverting terminal with the other terminal connected to ground.

Output resistance - It is the resistance measured by looking into the output terminal of OP-AMP, with the input source short circuited.

Bandwidth - It is the range over which all signal frequencies are amplified almost equal.

Common mode rejection ratio - It is defined as the ratio of differential gain to common mode gain.

Slew rate - It is defined as the maximum rate of change of output voltage per unit time.

Power supply rejection ratio - It is the change in an OP-AMPs input offset voltage caused by variation in the supply voltage.

Input offset voltage - Ideally, for a zero input voltage output should be zero. But practically it is not so. This is due to unavoidable unbalances inside the OP- AMP.

Input bias current - It is the average of the currents flowing into the two input terminal of the OP-AMP.

Input offset current - It is the algebraic difference between the currents flowing into the inverting and non-inverting terminal of OP-AMP.

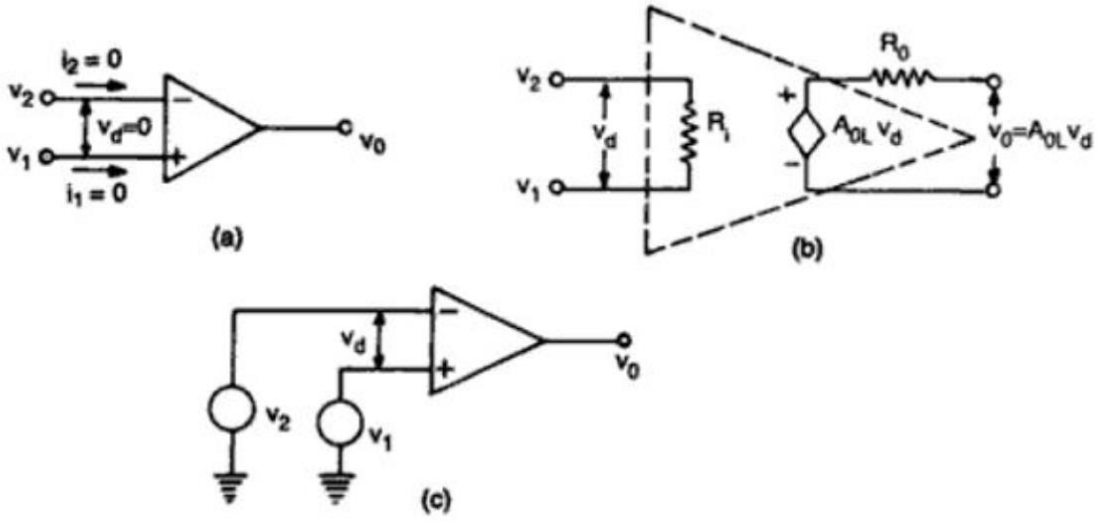


Fig: 1.5 a) Ideal opamp, b) Equivalent circuit of opamp c) open loop circuit

1.5 Open Loop circuit

The magnitude of A_{OL} is typically very large—100,000 or more for integrated circuit op-amps—and therefore even a quite small difference between V_+ and V_- drives the amplifier output nearly to the supply voltage. Situations in which the output voltage is equal to or greater than the supply voltage are referred to as saturation of the amplifier. The magnitude of A_{OL} is not well controlled by the manufacturing process, and so it is impractical to use an open loop amplifier as a stand-alone differential amplifier.

Without negative feedback, and perhaps with positive feedback for regeneration, an op-amp acts as a comparator. If the inverting input is held at ground (0 V) directly or by a resistor R_g, and the input voltage V_{in} applied to the non-inverting input is positive, the output will be maximum positive; if V_{in} is negative, the output will be maximum negative. Since there is no feedback from the output to either input, this is an open loop circuit acting as a comparator.

1.6 Close loop configuration

- In close loop configuration, a feedback is introduced i.e. a part of output is fed back to the input.
- The feedback can be of the following two types:
    1. Positive feedback/regenerative feedback
    2. Negative feedback/degenerative feedback

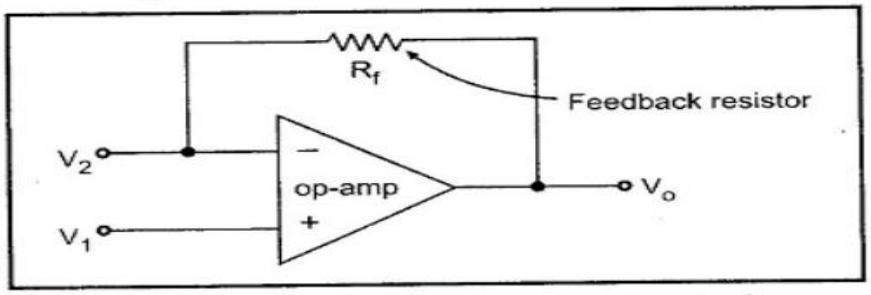


Fig: 1.6 Opamp with negative feedback

Positive feedback

- If the feedback signal and the input signal are in phase with each other then it is called as the positive feedback.
- It is used in application such as oscillators and schmitt trigger or regenerative comparators.

Negative feedback

- If the signal fed back to the input and the original input signal are 180º out of phase, then it is called as the negative feedback
- In application of op amp as an amplifier, the negative feedback is used.

Advantages of negative feedback

- It stabilizes gain
- Reduces the distortion
- Increases the bandwidth
- Reduces the effect of variations in temperature and supply voltage on the output of op amp
- The only disadvantage of negative feedback is low gain

1.7 Inverting Amplifier

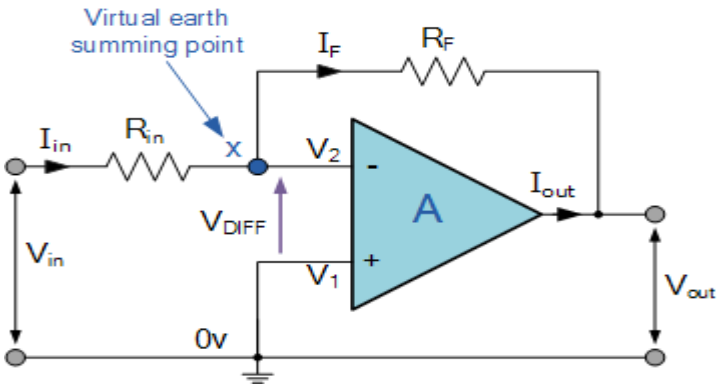


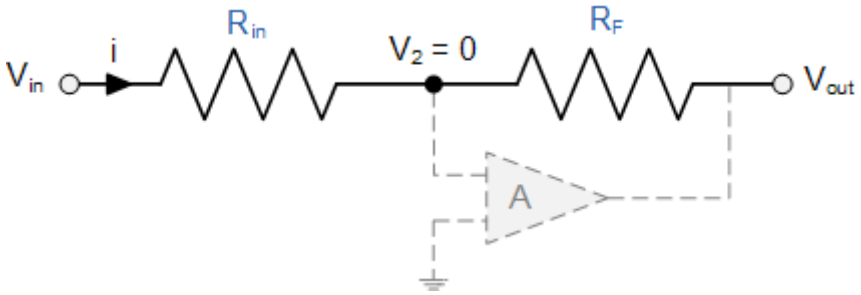
Fig: 1.7 Inverting Amplifier

In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V1 always equals V2". However, in real world op-amp circuits both of these rules are slightly broken. This is because the junction of the input and feedback signal (X) is at the same potential as the positive (+) input which is at zero volts or ground then, the junction is a **"Virtual Earth"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

Then by using these two rules we can derive the equation for calculating the closed-loop gain of an inverting amplifier, using first principles.

Current (i) flows through the resistor network as shown.



$$\frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

1.8 Non-Inverting Amplifier

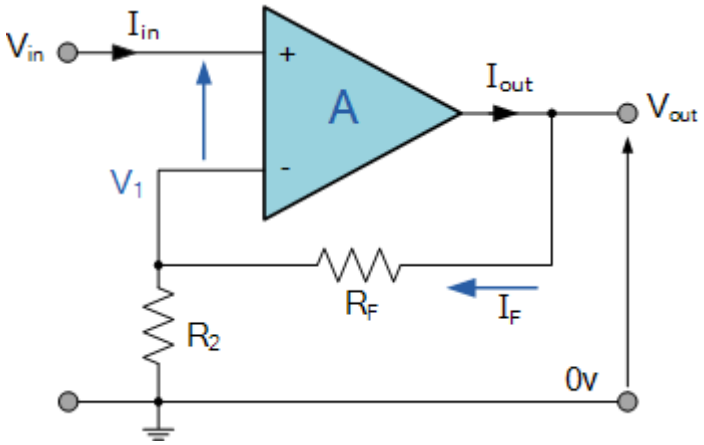


Fig: 1.8 Non-Inverting Amplifier

In this configuration, the input voltage signal, (V_{IN}) is applied directly to the non-inverting (+) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (–) input terminal via a Rf – R2 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance.

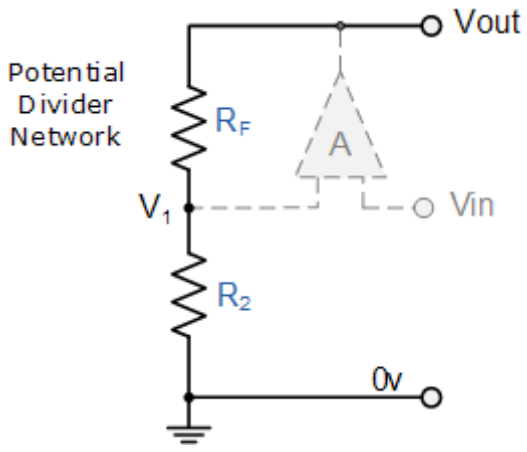


Fig:1.9 Equivalent Potential Divider Network

Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain (A_V) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

$$\text{Ideal Summing Point: } V_1 = V_{IN}$$

$$\text{Voltage Gain, } A_{(V)} \text{ is equal to: } \frac{V_{OUT}}{V_{IN}}$$

$$\text{Then, } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$$

$$\text{Transpose to give: } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$$

1.9 Voltage follower

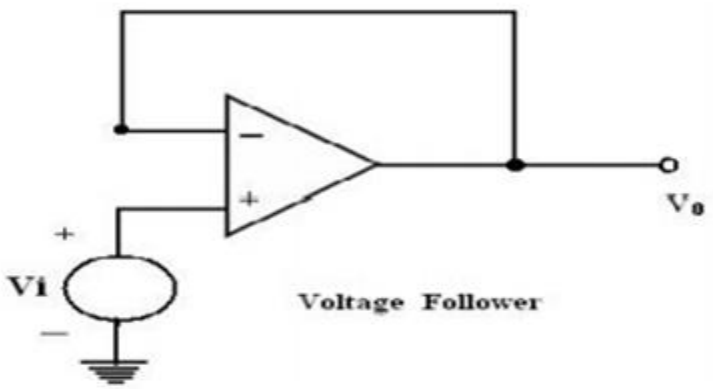


Fig: 1.9 b Voltage Follower

If R1=∞ and Rf =0 in the non inverting amplifier configuration. The amplifier act as a unity-gain amplifier or voltage follower.

The circuit consists of an op -amp and a wire connecting the output voltage to the input, i.e. the output voltage is equal to the input voltage, both in magnitude and phase. $V_0 = V_i$. Since the output voltage of the circuit follows the input voltage, the circuit is called voltage follower. It offers very high input impedance of the order of MΩ and very low output impedance.

Therefore, this circuit draws negligible current from the source. Thus, the voltage follower can be used as a buffer between a high impedance source and a low impedance load for impedance matching applications.

1.10 Summing Amplifier

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer or adder.

Inverting Summing Amplifier

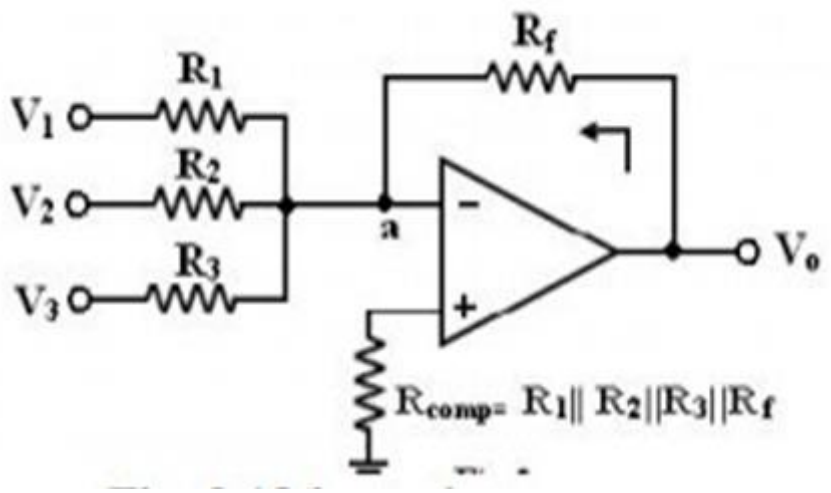


Fig: 1.10 Inverting Summing Amplifier

A typical summing amplifier with three input voltages V_1, V_2 and V_3 three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in figure 2.The following analysis is carried out assuming that the op-amp is an ideal one, AOL= ∞. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor Rcomp and hence the non-inverting input terminal is at ground potential.

$$I = V_1/R1 + V_2/R2\ldots. + Vn/Rn$$

$$Vo = - R_f\, I = R_f / R\,(V_1+V_2+\ldots V_n).$$

To find Rcomp, make all inputs $V1 = V_2 = V_3 = 0$.

So the effective input resistance $R_i = R_1 \parallel R_2 \parallel R_3$.

Therefore, $Rcomp = R_i \parallel R_f = R_1 \parallel R_2 \parallel R_3 \parallel R,f$.

Non-Inverting Summing Amplifier

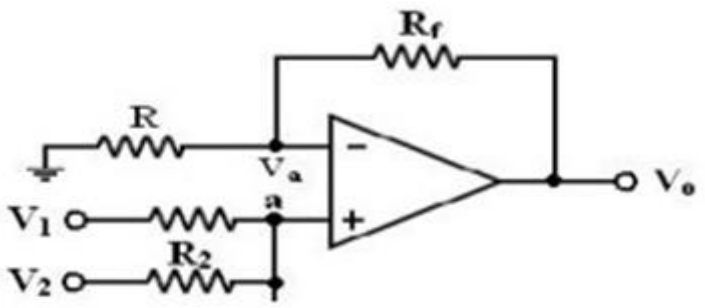


Fig: 1.11 Non-Inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier of figure. Let the voltage at the (-) input terminal be Va. which is a non-inverting weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$,

$$V_o = V_1+V_2+V_3$$

1.11 Integrator

A circuit in which the output voltage waveform is the integral of the input voltage waveform is the integrator or Integration Amplifier. Such a circuit is obtained by using a basic inverting amplifier configuration if the feedback resistor R_F is replaced by a capacitor C_F. The expression for the output voltage V0 can be obtained by KVL eqn. at node V_2.

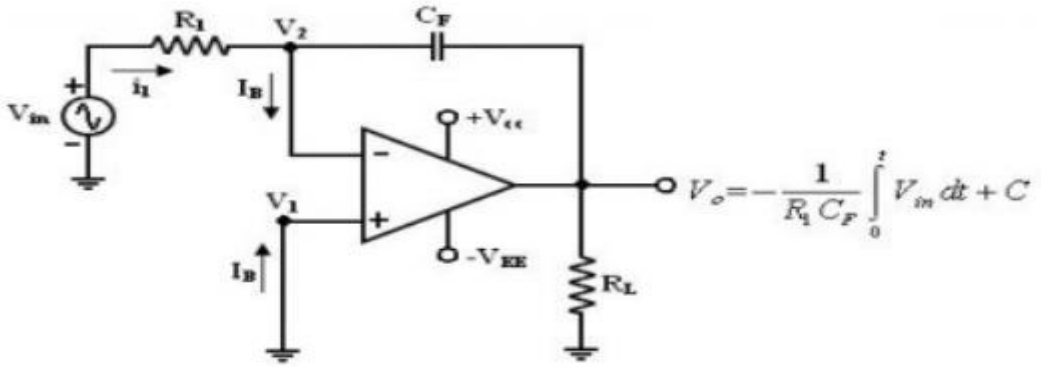


Fig: 1.12 Integrator

$$I_1 = I_B + i_f$$

Since I_B is negligible small, $i_1 = i_F$

Relation between current through and voltage across the capacitor is

$$i_{C(t)} = C dv_c(t)/dt$$

$V_1 = 0$ because A is very large,

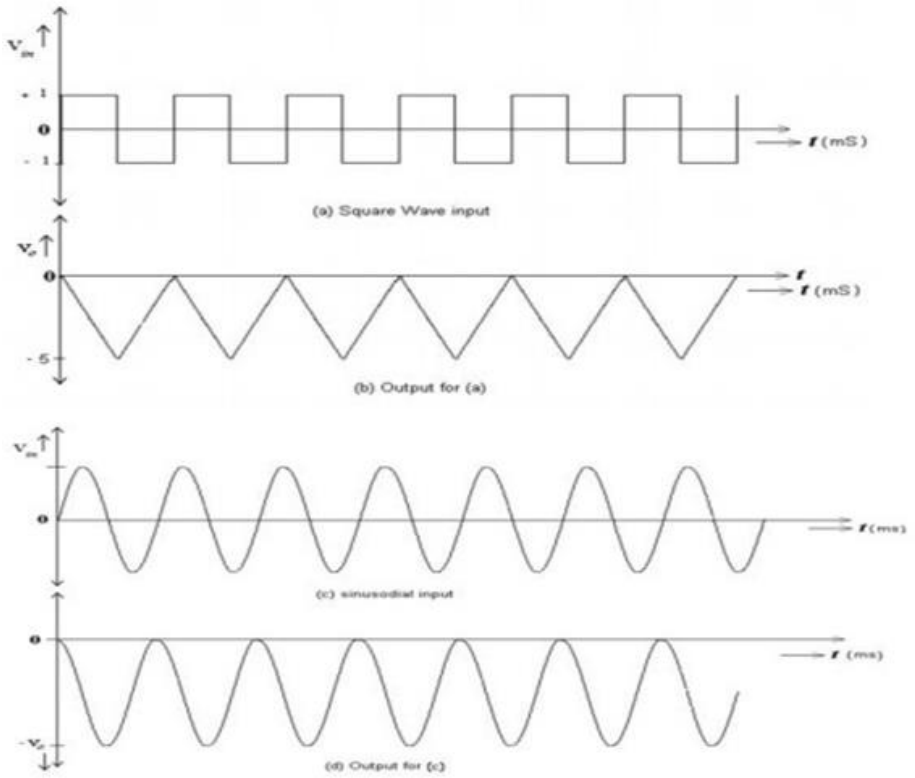
The output voltage can be obtained by integrating both sides with respect to time

$$V_0(jw) = [1 / jwR_1C_f]\ V_i(jw)$$

Indicates that the output is directly proportional to the negative integral of the input volts and inversely proportional to the time constant R_1C_F.

Ex: If the input is sine wave -> output is cosine wave.

If the input is square wave -> output is triangular wave.



These waveform with assumption of $R_1C_f = 1$, Vout =0V (i.e) C =0.

When V_{in} = 0 the integrator works as an open loop amplifier because the capacitor C_F acts an open circuit to the input offset voltage V_{io}.

The Input offset voltage V_{io} and the part of the input is charging capacitor C_F produce the error voltage at the output of the integrator.

1.12 Differentiator

The basic operational amplifier differentiator circuit produces an output signal which is the first derivative of the input signal.

Here, the position of the capacitor and resistor have been reversed and now the reactance, X_C is connected to the input terminal of the inverting amplifier while the resistor, R*f* forms the negative feedback element across the operational amplifier as normal.

This operational amplifier circuit performs the mathematical operation of **Differentiation** that is it "*produces a voltage output which is directly proportional to the input voltage's rate-of-change with respect to time*". In other words the faster or larger the change to the input voltage signal, the greater the input current, the greater will be the output voltage change in response, becoming more of a "spike" in shape.

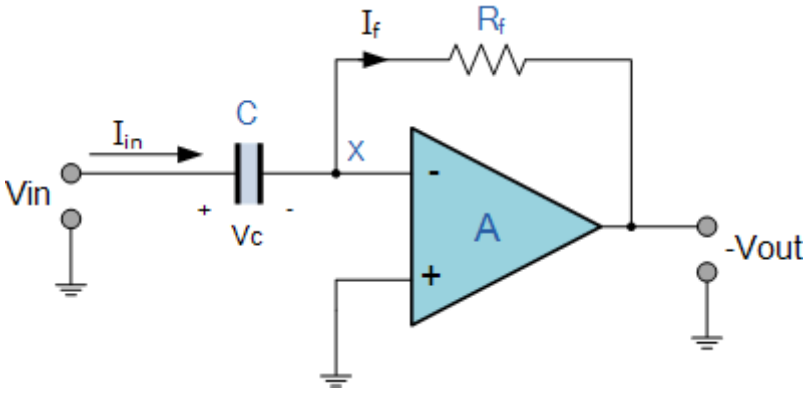


Fig: 1.13 Differentiator

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \text{ and } I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

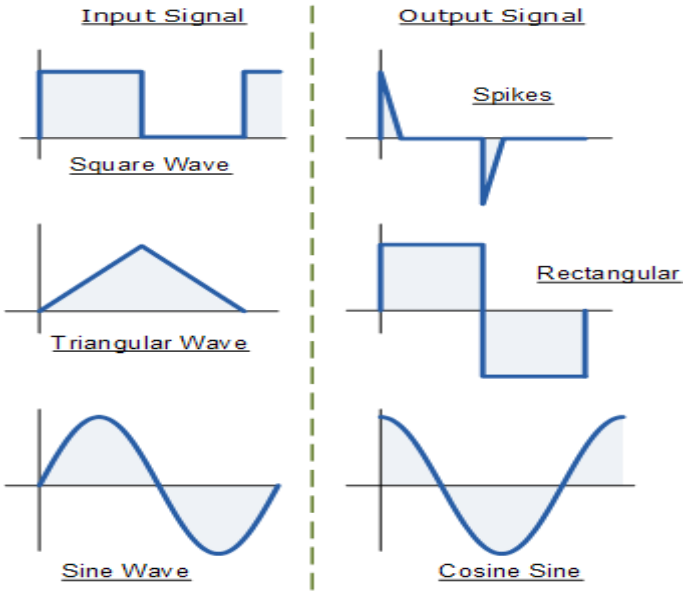
from which we have an ideal voltage output for the op-amp differentiator is given as:

$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

Therefore, the output voltage Vout is a constant –R*f**C times the derivative of the input voltage Vin with respect to time. The minus sign (–) indicates a 180^o phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

Op-amp Differentiator Waveforms

If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependent upon the RC time constant of the Resistor/Capacitor combination.



1.13 Log Amplifier

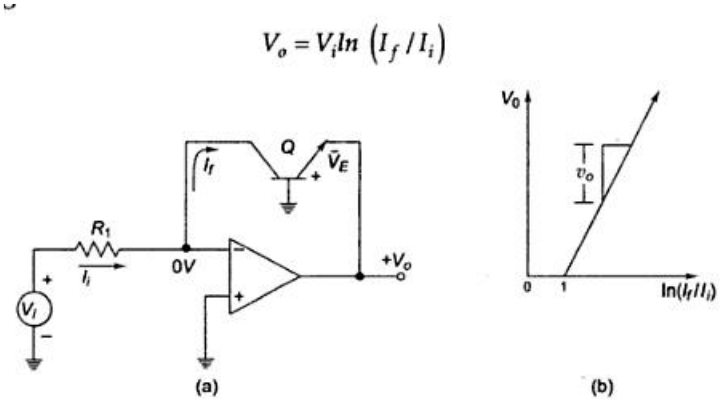


Fig: 1.14 Log Amplifier

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or sin hx.

Uses:

Direct dB display on a digital Voltmeter and Spectrum analyzer.

Log-amp can also be used to compress the dynamic range of a signal.
A grounded base transistor is placed in the feedback path. Since the collector is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor‘s= voltage [-current−1] relationship becomes that of a diode and is given by,

$$I_E = I_s[e^{\frac{qV_{BE}}{kT}} - 1]$$

and since $I_c = I_E$ for a grounded base transistor $I_C = I_s\, e^{kT}$

Is-emitter saturation current $\approx 10^{-13}$A

k=Boltzmann‘s constant

T=absolute temperature (in^{o}K)

$$V_o = -\frac{kT}{q} ln\left(\frac{V_i}{R_1 I_S}\right) = -\frac{kT}{q} ln\left(\frac{V_i}{V_R}\right)$$

where $V_{ref} = R_1 I_s$

The output voltage is thus proportional to the logarithm of input voltage.

Although the circuit gives natural log (ln), one can find log10, by proper scaling

$$Log10X = 0.4343 \ln X$$

1.14 Antilog Amplifier

A circuit to convert logarithmically encoded signal to real signals. Transistor in inverting input converts input voltage into logarithmically varying currents.

The circuit is shown in figure below. The input Vi for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output of A2 is fed back to R_1 at the inverting input of op amp A_1. The non-inverting inputs are grounded.

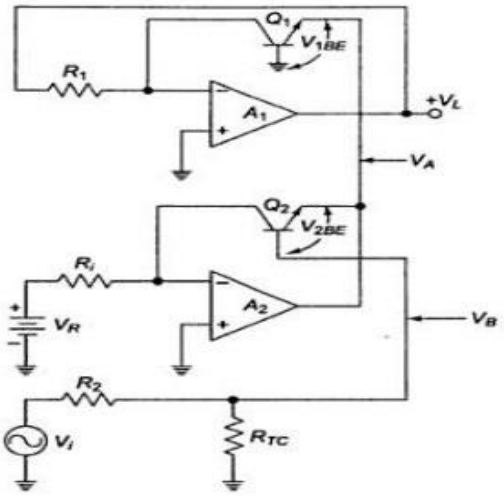


Fig 2.32 Antilog amplifier

$V_{1BE} = \frac{kT}{q} \ln[\frac{V_L}{R_1 I_S}]$ and $V_{2BE} = \frac{kT}{q} \ln[\frac{V_B}{R_1 I_S}]$ and $V_A = -V_{1BE}$ and $V_B = R_{TC}/(R_2+R_{TC})\ V_i$

$V_{Q2E} = V_B + V_{2BE} = R_{TC}/(R_2+R_{TC})\ V_i - \frac{kT}{q} \ln[\frac{V_B}{R_1 I_S}]$

$V_{Q2E} = V_A$

Therefore, $$-\frac{kT}{q}ln\left(\frac{V_L}{R_1 I_S}\right)=\frac{R_{TC}}{R_2+R_{TC}}V_i+\frac{kT}{q}ln\left(\frac{V_R}{R_1 I_S}\right)$$

Rearranging, we get

$$\frac{R_{TC}}{R_2+R_{TC}}V_i=-\frac{kT}{q}ln\left(\frac{V_L}{R_1 I_S}\right)-\frac{kT}{q}ln\left(\frac{V_R}{R_1 I_S}\right)$$

$$=-\frac{kT}{q}ln\left(\frac{V_L}{V_R}\right)$$

We know that $\log_{10} x = 0.4343 \ln x$.

Therefore, $$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)V_i=0.4343\ ln\left(\frac{V_L}{V_R}\right)$$

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)V_i=\log_{10}\left(\frac{V_L}{V_R}\right)$$

$$-KV_i=\log\left(\frac{V_L}{V_R}\right)$$

$$K=0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)$$

$$V_L=V_R 10^{-KV_i}$$

The output V_o of the antilog- amp is fed back to the inverting input of A_1 through the resistor R_1. Hence an increase of input by one volt causes the output to decrease by a decade.

1.15 Differential Amplifier

A difference amplifier or differential amplifier amplifies the difference between the two input signals. An operational amplifier is a difference amplifier; it has an inverting input and a non-inverting input. But the open loop voltage gain of an operational amplifier is too high (ideally infinite), to be used without a feedback connection. So, a practical difference amplifier uses a negative feedback connection to control the voltage gain of the amplifier.

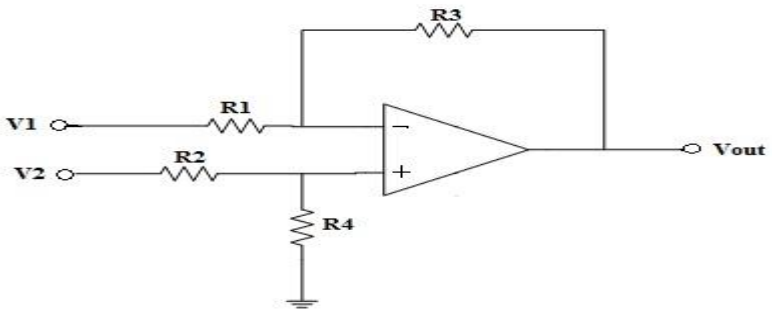


Fig.- Differential Amplifier Circuit

The difference amplifier shown in the above circuit is a combination of both inverting and non-inverting amplifiers. If the non-inverting terminal is connected to ground, the circuit operates as an inverting amplifier and the input signal V_1 is amplified by $-(R_3 / R_1)$.

Similarly, if the inverting input terminal is connected to ground, the circuit behaves as a non-inverting amplifier. With the inverting input terminal grounded, R_3 and R_1 function as the feedback components of a non-inverting amplifier. Input V_2 is potentially divided across resistors R_2 and R_4 to give V_{R4}, and then V_{R4} is amplified by $(R_3 + R_1) / R_1$.

With $V_2 = 0$,

$$V_{O1} = - (R_3 / R_1) * V_1$$

With $V_1 = 0$,

$$V_{R4} = \{R_4 / (R_2+R_4)\}*V_2$$

and

$$V_{O2} = \{(R_1+R_3)/R_1\}*V_{R4}$$

Therefore,

$$V_{O2} = \{(R_1 + R_3) / R_1\} * \{R_4 / (R_2 + R_4) \} * V_2$$

If the input resistances are chosen such that, $R_2 = R_1$ and $R_4 = R_3$, then

$$V_{O2} = \{R_3 / R_1\} * V_2$$

Now, according to superposition principle if both the input signals V_1 and V_2 are present, then the output voltage is

$$V_O = V_{O1} + V_{O2}$$

$$= \{-(R_3 / R_1) * V_1\} + \{R_3 / R_1\} * V_2$$

Which results in,

$$V_O = (R_3 / R_1) * \{V_2 – V_1\}$$

When the resistors R_3 and R_1 are of the same value, the output is the direct difference of the input voltages applied. By selecting R_3 greater than R_1, the output can be made an amplified version of the difference of the input voltages.

Differential Gain

The differential gain of a difference amplifier is defined as the gain obtained at the output signal with respect to the difference in the input signals applied.

The output voltage of a difference amplifier is given as,

$$V_O = A_D (V_1 – V_2)$$

where, $A_D = – (R_3 / R_1)$ is the differential gain of the amplifier.

Common Mode Input

A difference amplifier amplifies the difference between the two input voltages. Ideally, a common mode input V_{cm} would make the inputs $(V_1 + V_{cm})$ and $(V_2 + V_{cm})$, which will result in V_{cm} being cancelled out when the difference of the two input voltages is amplified.

Since the output of a practical difference amplifier depends upon the ratio of the input resistances, if these resistor ratios are not exactly equal, then one input voltage is amplified by a greater amount than the other input.

Consequently, the common mode voltage V_{cm} will not be completely cancelled. Because it is practically impossible to match resistor ratios perfectly, there is likely to be some common mode output voltage.

With the common mode input voltage present, the output voltage of the differential amplifier is given as,

$$V_O = A_d V_d + A_c V_c$$

Where Vd = the difference voltage V_1-V_2

Vc = the common mode voltage $(V_1+V_2)/2$

Common Mode Rejection Ratio (CMRR)

The ability of a differential amplifier to reject common mode input signals is expressed in terms of common mode rejection ratio (CMRR). The common mode rejection ratio of a differential amplifier is mathematically given as the ratio of differential voltage gain of the differential amplifier to its common mode gain.

$$CMRR = | A_d / A_c|$$

Ideally, the common mode voltage gain of a differential amplifier is zero. Hence the CMRR is ideally infinite.

Characteristics of a Differential Amplifier

- High Differential Voltage Gain
- Low Common Mode Gain
- High Input Impedance
- Low Output Impedance
- High CMRR
- Large Bandwidth
- Low offset voltages and currents

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UNIT 2 APPLICATION OF OPAMPS

2.1 Comparator

The change in the output state takes place with an increment in input V_i , of only 2 mV. This is the uncertainty region where output cannot be directly defined.

There are basically two types of comparators

- Non inverting comparator
- Inverting comparator

Non inverting comparator

- A Fixed reference voltage Vref is applied to (-) input and a time varying signal V_i is applied to (+) input.

The output voltage

- Vo is at - Vsat for V_i <Vref.
- Vo is at +Vsat for Vi > Vref.
- The diodes D1 and D2 are connected to protect the op-amp from excessive input voltages of Vref as shown in Fig.a.

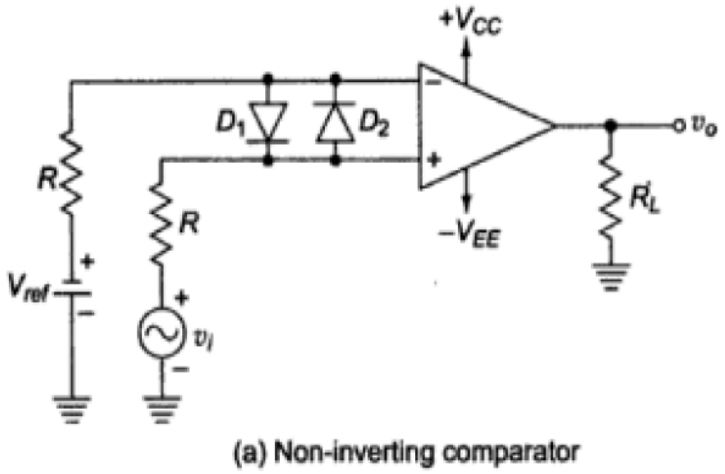
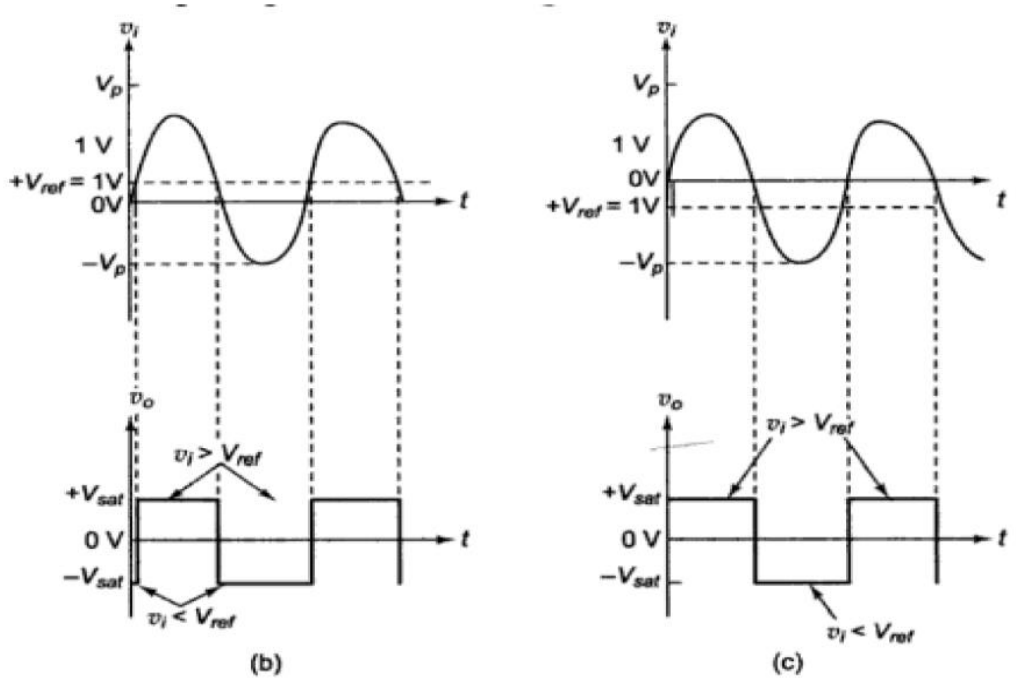


Fig: 2.1 Non-inverting Comparator

- The output waveform for a sinusoidal input signal applied to the (+) input is shown in Fig.
- Fig. for positive and negative Vref respectively
- In a practical circuit (Fig. d),

Vref is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages V+ and V- with the wiper connected to (-) input terminal.

Thus a Vref of desired amplitude and polarity is obtained by simply adjusting the 10 kΩ potentiometer.



(b) Input and Output wave-forms when V_{ref} is +ve
(c) Input and Output wave-forms when V_{ref} is –ve

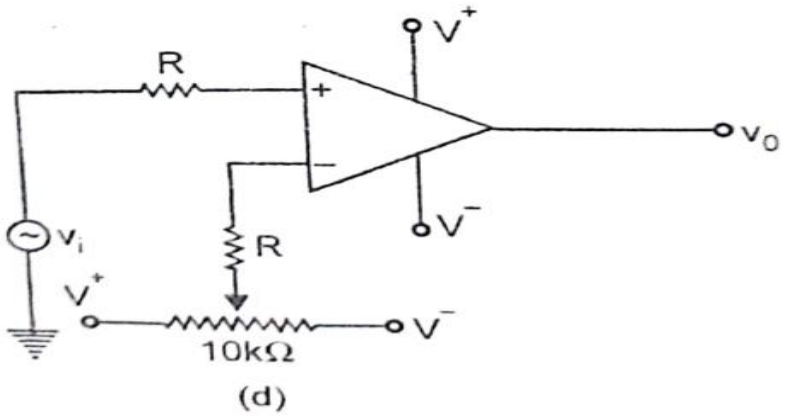


Fig: 2.2 Non-inverting Comparator Waveforms

Inverting comparator

- In inverting comparator, reference voltage Vref is applied to the (+) input and V_i is applied to input.

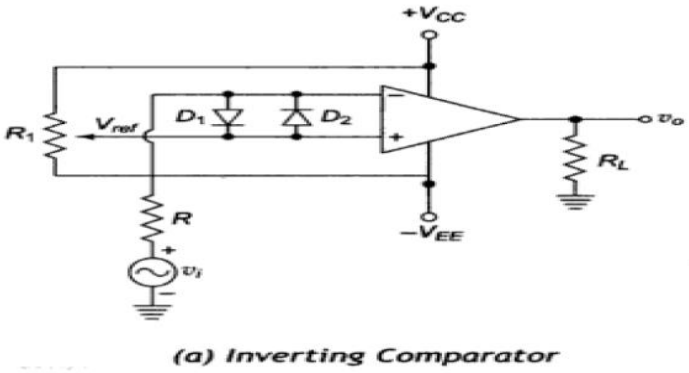


Fig: 2.3 Inverting Comparator

For a sinusoidal input signal, the output waveform is shown in Fig. (b) and (c) for Vref positive and negative respectively.

The output voltage

Vo is at +Vsat for V_i <Vref.

Vo is at - Vsat for Vi > Vref.

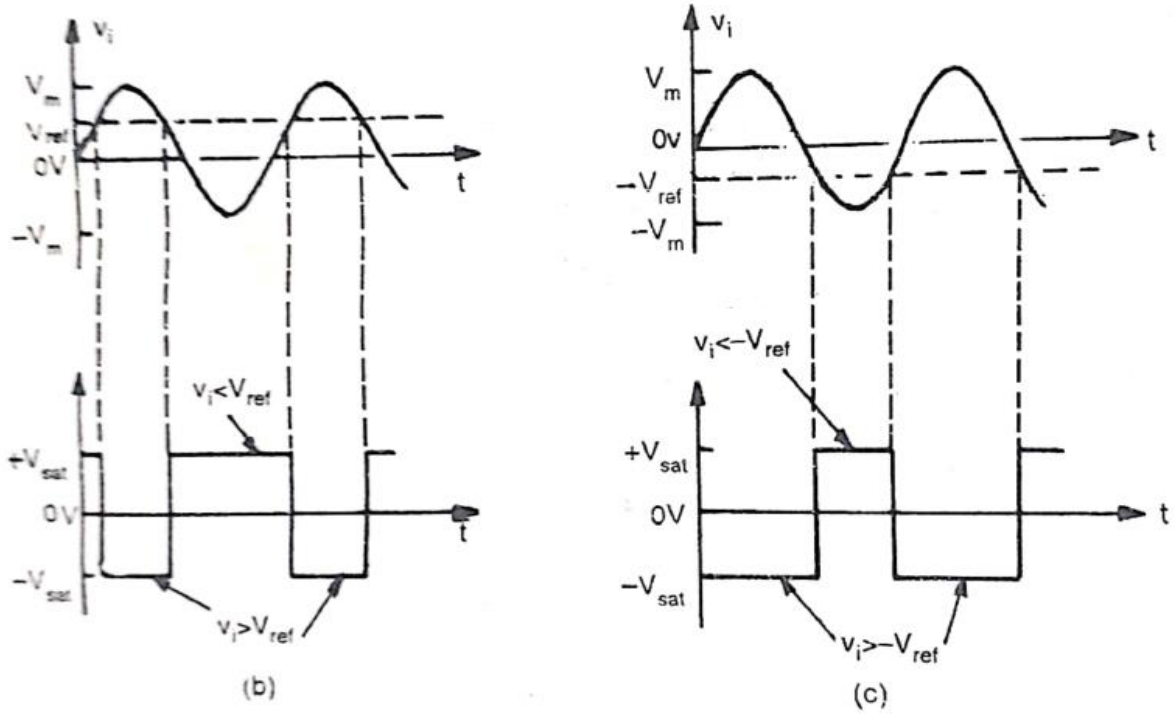


Fig: 2.4 Inverting Comparator Waveforms

- Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in Fig.(d).

- The value of resistance R is chosen so the zener diodes operate at the recommended current.
- It can be seen that the limiting voltages of Vo, are (V_{Z1} + V_D) and - (V_{Z1} + V_D) where V_D (- 0.7 V) is the diode forward voltage.

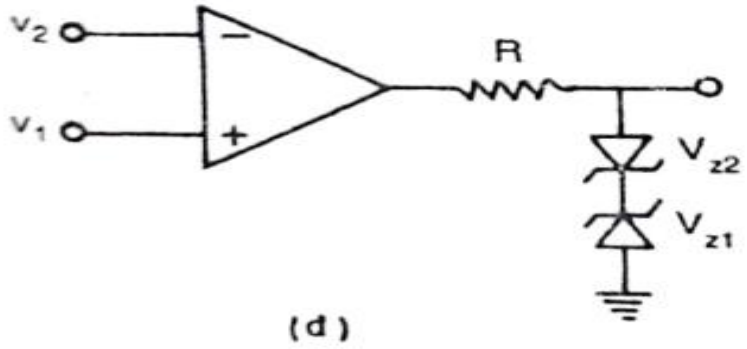


Fig: 2.5 Inverting Comparator

2.2 Zero Crossing Detectors

Some important applications of comparator

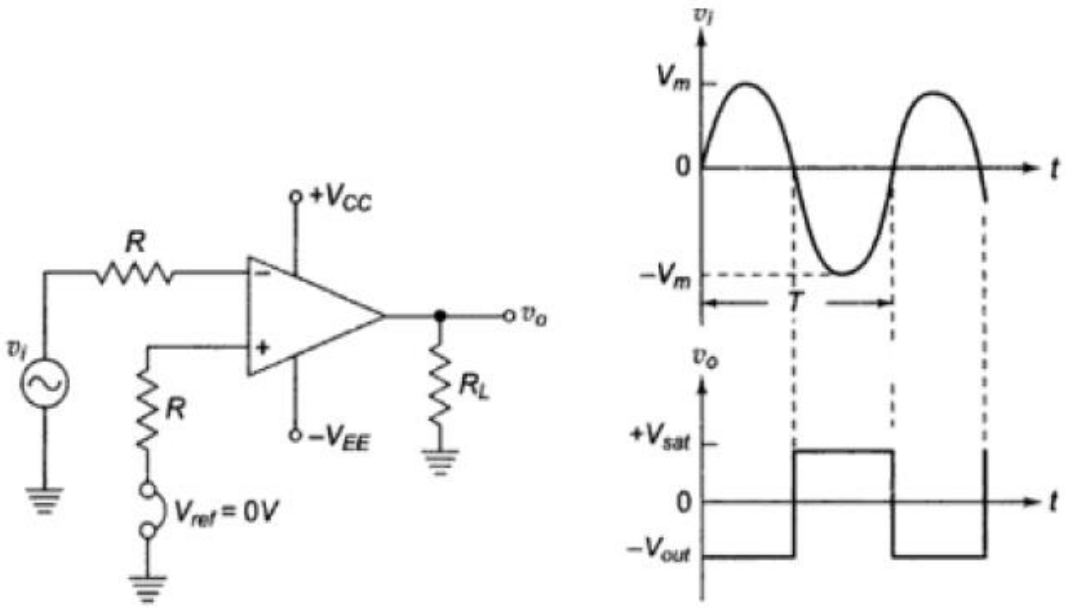
- Zero crossing
- Window detector
- Time marker generator
- Phase meter
-

The basic comparators of can be used as a zero crossing detector provided that Vref in set to zero. An inverting zero- crossing detector is shown in Fig. (a) .The output waveform for a sinusoidal input signal is shown in Fig.(b). The circuit in also called a sine to square wave generator.

The output voltage

Vo is at +Vsat for V_i positive

Vo is at - Vsat for Vi negative

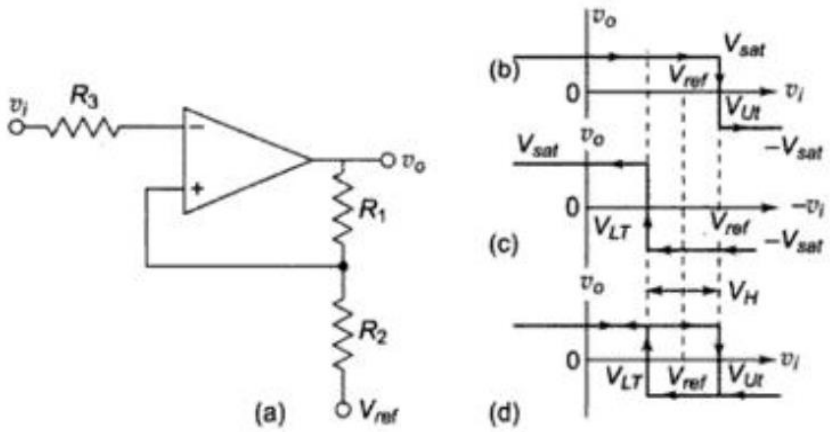


(a) Zero crossing detector and (b) Input and output waveforms

Fig: 2.6 Zero Crossing detector

2.3 Regenerative Comparator (Schmitt Trigger)

- If positive feedback is added to the comparator circuit, gain can be increased greatly.
- Consequently, the transfer curve of comparator becomes more close to ideal curve.
- Theoretically, if the loop gain $-\beta A_{0L}$ is adjusted to unity, then the gain with feedback A_{Vf} becomes infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage.
- In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for Long time because of supply voltage and temperature variations.
- So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous at the comparison voltage. This circuit, however now exhibits a phenomenon called hysteresis or backlash.



(a) Inverting Schmitt Trigger circuit (b), (c) and (d) Transfer Characteristics of Schmitt Trigger

Fig: 2.7 Schmitt Tigger

- Fig. (a) shows such a regenerative comparator. The circuit is also known as **Schmitt Trigger.**
- The input voltage is applied to the (-) input terminal and feedback voltage to the (+) input terminal.
- The input voltage V_i triggers the output V_o every time it exceeds certain voltage level.
- These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}).
- The hysteresis width is the difference between these two threshold voltages **ie. V_{UT} - V_{LT}** .
- These threshold voltages are calculated as follows:
- Suppose the output V_o = + V_{sat} The voltage at (+) input terminal will be

$$V_{ref} + \frac{R_2}{R_1 + R_2}\left(V_{sat} - V_{ref}\right) = V_{UT}$$

- This voltage is called upper threshold voltage (V_{UT}). As long as V_i is less than V_{UT}, the output Vo, remains constant at + V_{sat}
- When V_i is just greater than V_{UT}, the output Vo regenerative switches to - V_{sat} and remains at this level as long as $V_i > V_{UT}$ Or as shown in Fig.(b).
- For , Vo = - V_{sat} , the voltage at the (+) input terminal is,

$$V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = V_{LT}$$

- This voltage is referred to as lower threshold voltage V_{LT}.
- The input voltage V_i must become lesser than V_{LT} in order to cause Vo to switch from - V_{sat} to + V_{sat}.
- A regenerative transition takes place as shown in Fig.(c) and the output Vo returns from - V_{sat} to + V_{sat} almost instantaneously. The complete transfer characteristics are shown in Fig (d).
- Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2R_2 V_{sat}}{R_1 + R_2}$$

- Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones.
- Further, note that if peak-to-peak input signal V_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, i.e, once the output has jumped to say. +Vsat it would remain at this level and never return to -V_{sat} .
- It may be seen from Eq. V_H that hysteresis width V_H is independent of Vref.
- When Vref = 0V Then,

$$V_{UT} = -V_{LT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

- A non inverting Schmitt trigger is obtained if Vi and Vref are interchanged in Fig. a.
- The most important application of Schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output as shown in Fig. (e).

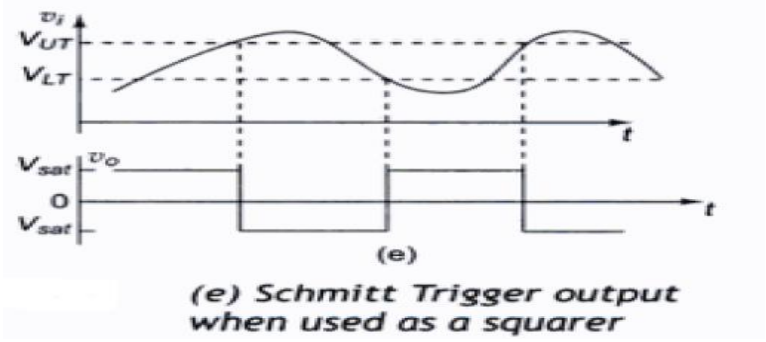


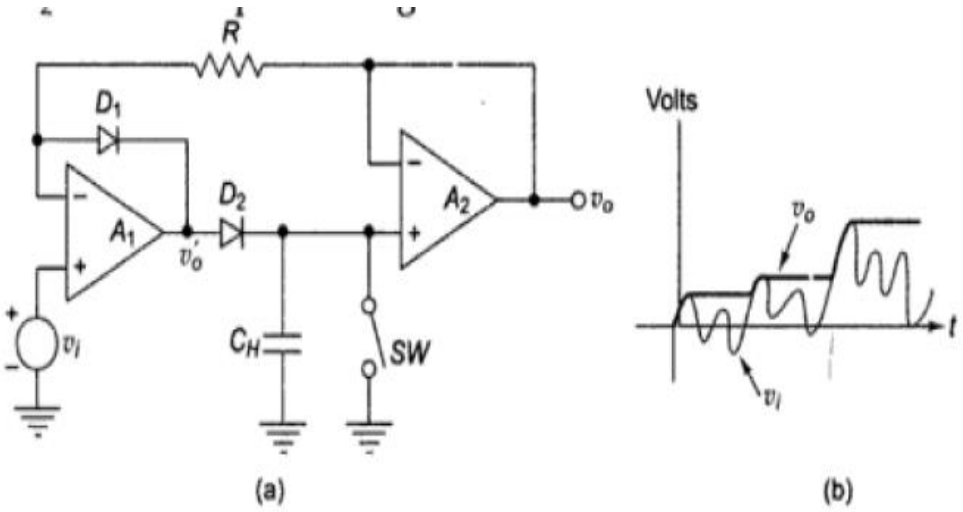
Fig: 2.8 Schmitt Tigger output

2.4 Peak Detectors

- A peak detector is a circuit that produces an output voltage equal to the positive or negative peak value of the input voltage.
- A positive peak detector detects the positive peak magnitude of the input and a negative peak detector identifies the negative peak magnitude of the input.

The basic blocks required for the peak detector circuit are:

- an analog memory such as a capacitor to store the charge proportional to the peak value
- a unidirectional switch such as a diode to charge the capacitor when a new peak arrives at the input
- a device such as a voltage follower circuit for making the capacitor charge to the input voltage and a switch to periodically reinitialize the output to zero



(a) Peak detector circuits and (b) Input and output waveforms

Fig: 2.9 Peak detectors

Figure (b) shows the voltage waveforms for the positive peak detector for a certain input signal v_i. The circuit can be reset at any time by closing the switch *SW*. The switch *SW* can be a low leakage MOSFET. Negative peak detectors can be obtained by reversing the diode connections.

- Figure (a) shows the circuit of a positive peak detector.
- The capacitor C_H, diode D_2, op-amp A_1, and switch SW perform the four functions listed above in order.
- The op-amp A_2, acts as a buffer. This prevents discharging of the capacitor C_H.

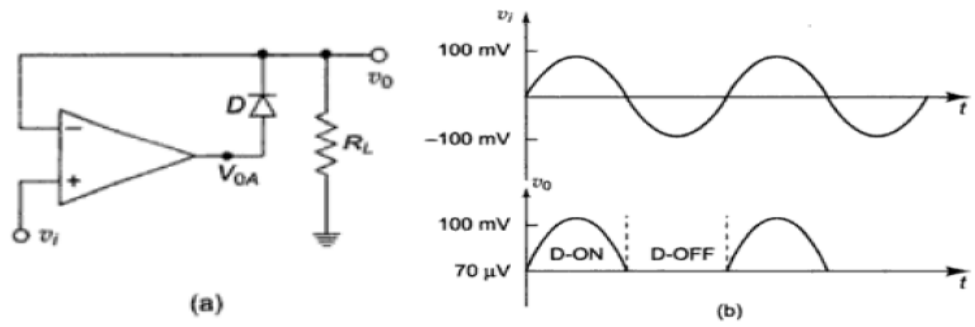
- The diode D2 is preferred to be of very low leakage current.
- The diode D_1, and resistance R avoids saturation of op-amp when a peak is detected.
- When the input signals $V_i > 0$, the output V'_O of op amp A_1 is positive.
- The diode D_2 is hence forward-biased and diode D_1 is reverse-biased. The capacitance C_H then gets charged.
- The feedback path provided by diode D_2, op-amp A_2 and resistor R maintain the virtual short between the input terminals of A_1.
- In other words, the voltages at the inverting and non-inverting terminals of A_1 are equal.
- Then, the voltage V_i, during this phase is $v_i = v_o + V_{D2(ON)}$.
- The output V_O tracks V_i, and this phase is called the track mode.
- The op-amp A_1 sources current to charge C_H through diode D_2.
- When V_i, begins to decrease, D_2, becomes reverse-biased and D_1, becomes forward-biased and conducts.
- The output of V'_O of op amp A_1 is now $v_o = v_i - V_{D1\,(ON)}$
- The feedback path from Vo, to V_i through diode D_2 and R is now open. During this phase, the capacitor voltage remains constant. Hence it is called the hold mode, and the output of op-amp A_2, retains the peak voltage.

2.5 Precision Rectifier

- The ordinary diodes cannot rectify voltages below the cut-in -voltage of the diode.
- A circuit which can act as an ideal diode or precision signal – processing rectifier circuit for rectifying voltages which are below the level of cut-in voltage of the diode can be designed by placing the diode in the feedback loop of an op-amp.

Precision Diodes

- It is a single diode arrangement and functions as a non-inverting precision half– wave rectifier circuit.
- If Vi in the circuit of figure is positive, the op-amp output V_O also becomes positive. Then the closed loop condition is achieved for the op-amp and the output voltage V_0 = Vi.
- When Vi < 0, the voltage V_0 becomes negative and the diode is reverse biased. The loop is then broken and the output $V_0 = 0$.



(a) Precision diode and (b) input and output waveforms

Fig: 2.10 Precision Diode

- Consider the open loop gain AOL of the op-amp is approximately 10^4 and the cut-in voltage Vγ for silicon diode is ≈ 0.7V.
- When the input voltage Vi > Vγ / AOL, the output of the op-amp V_O exceeds Vγ and the diode D conducts.
- Then the circuit acts like a voltage follower for input voltage level $V_i > V_\gamma / AOL$,(i.e. when $V_i > 0.7/10^4 = 70\mu V$),
- The output voltage V_0 follows the input voltage during the positive half cycle for input voltages higher than 70μV as shown in figure.

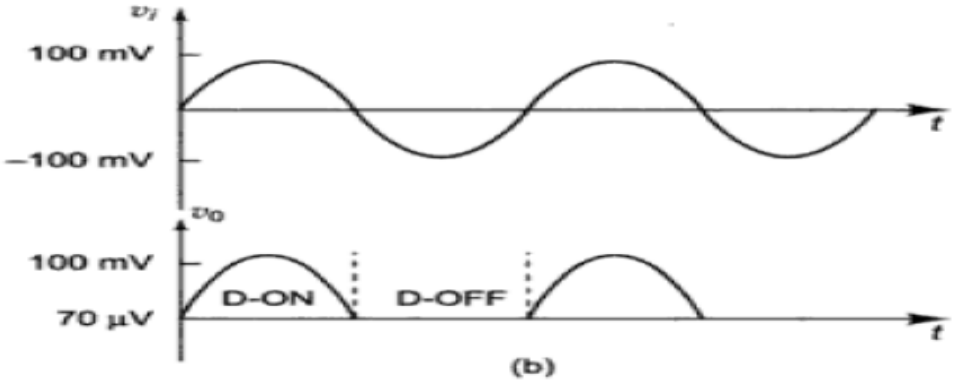


Fig: 2.11 Precision Diode Waveform

- When Vi is negative or less than V_γ / A_{OL}, the output of op-amp V_{OA} becomes negative, and the diode becomes reverse biased.
- The loop is then broken, and the op-amp swings down to negative saturation.
- However, the output terminal is now isolated from both the input signal and the output of the op-amp terminal thus V_0 =0.
- No current is then delivered to the load RL except for the small bias current of the op-amp and the reverse saturation current of the diode.

- This circuit is an example of a non-linear circuit, in which linear operation is achieved over the remaining region ($V_i < 0$).
- Since the output swings to negative saturation level when $V_i < 0$, the circuit is basically of saturating form. Thus the frequency response is also limited.

Applications: The precision diodes are used in

Half wave rectifier, Full-wave rectifier,

Peak value detector, Clipper and clamper circuits.

Disadvantage:

- It can be observed that the precision diode as shown in figure operated in the first quadrant with Vi > 0 and $V_0 > 0$. The operation in third quadrant can be achieved by connecting the diode in reverse direction.

2.6 Half – wave Rectifier

- A non-saturating half wave precision rectifier circuit is shown in figure.
- When $V_i > 0V$, the voltage at the inverting input becomes positive, forcing the output V_{OA} to go negative.
- This results in forward biasing the diode D_1 and the op-amp output drops only by ≈ 0.7V below the inverting input voltage. Diode D_2 becomes reverse biased.
- The output voltage V_0 is zero when the input is positive.
- When $V_i < 0$, the op-amp output V_{OA} becomes positive, forward biasing the diode D_2 and reverse biasing the diode D_1.
- The circuit then acts like an inverting amplifier circuit with a non-linear diode in the forward path.
- The gain of the circuit is unity when $R_f = R_i$.

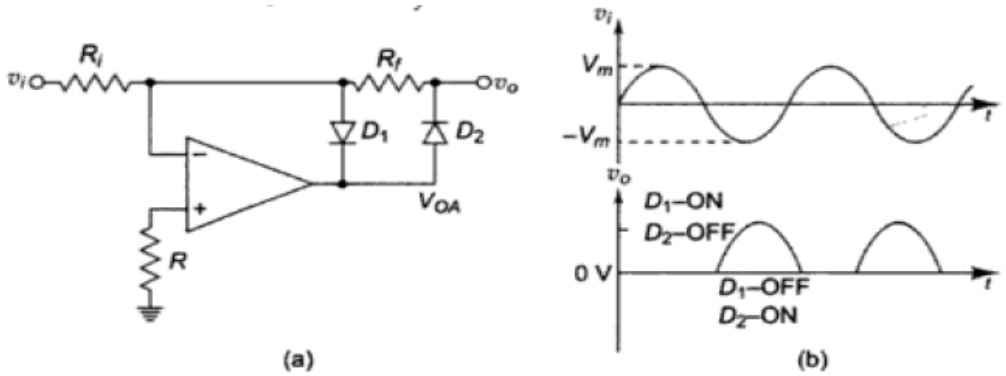


Fig: 2.12 Half wave Rectifier

The circuit operation can mathematically be expressed as

$$v_o = 0 \text{ when } v_i > 0$$

and

$$v_o = -\frac{R_f}{R_i} v_i \text{ for } v_i < 0$$

The voltage V_{OA} at the op-amp output is

$$V_{OA} \cong -0.7 \text{ for } v_i > 0\text{V}$$

and

$$V_{OA} \cong \frac{R_f}{R_i} v_i + 0.7\,\text{V} \text{ for } v_i < 0\text{V}.$$

- The op-amp is a high speed and this accommodates the abrupt changes in the value of V_{OA} when V_i changes sign and improves the frequency response characteristics of the circuit.

2.7 Full wave Rectifier

The fullwave rectifier circuits accept an ac signal at the input, inverts either the negative or the positive half, and delivers both the inverted and noninverted halves at the output, as shown in the Fig.

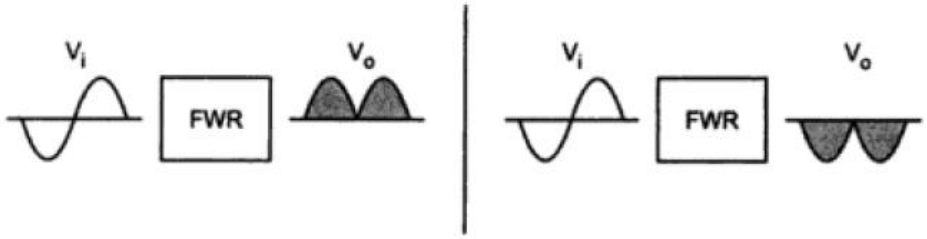


Fig. Positive and negative full wave rectifiers

The operation of the positive full wave rectifier is expressed as

$$V_o = |V_i| \quad \ldots (1)$$

and that of the negative rectifier as

$$V_o = -|V_i| \quad \ldots (2)$$

Looking at equations 1 and 2 we can say that precision full wave rectifier circuits are precision absolute value circuits.

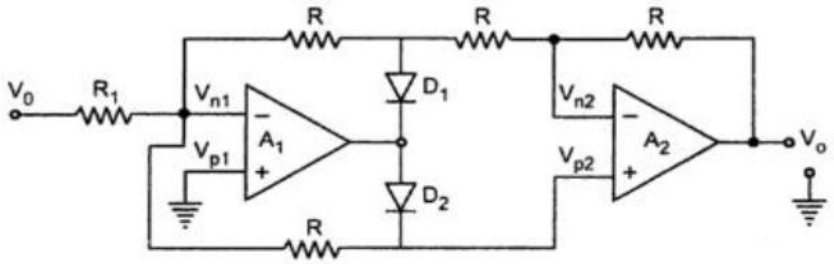
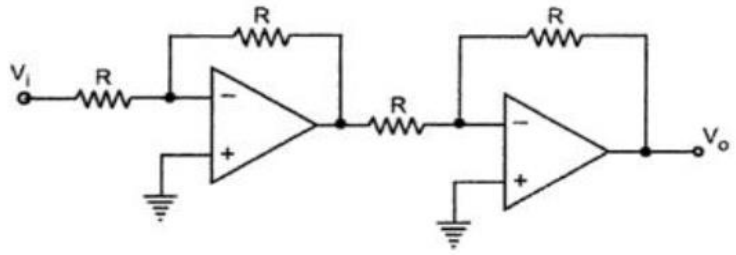


Fig. Full wave rectifier

CASE 1 : $V_i > 0$: When $V_i > 0$, inverting side of A_1 will force its output to swing negative, thus forward biasing D_1 and reverse biasing D_2. Since no current flows through resistance R connected between V_{n1} and V_{p2}, both are equipotential.



i.e. $V_{n1} = V_{p2} = 0V$.

The Fig. shows the equivalent circuit.

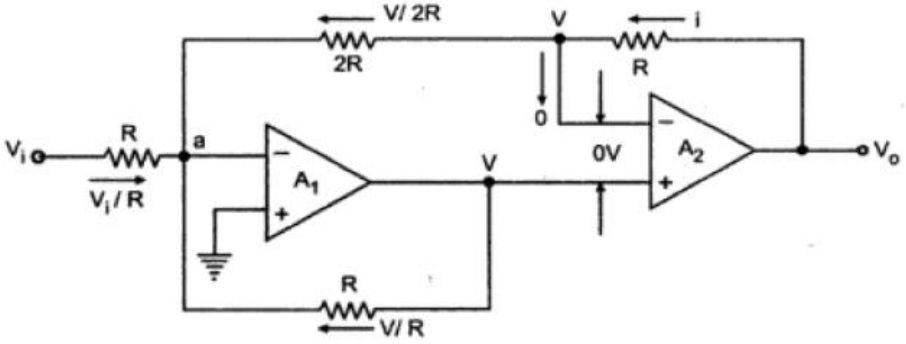
From equivalent circuit, the output voltage can be given as

$$V_o = \left(\frac{-R}{R}\right) - \left(\frac{R}{R}\right) V_i = V_i \qquad \ldots(3)$$

CASE 2 : $V_i < 0$: When $V_i < 0$, negative, the output voltage of A_1 swings to positive, making diode D_1 reverse biased and diode D_2 forward biased.

The Fig. shows the equivalent circuit.

Let the output voltage of op-amp A_1 be V. Since the differential input to A_2 is zero, the inverting input terminal is also at voltage V, as shown in the Fig.

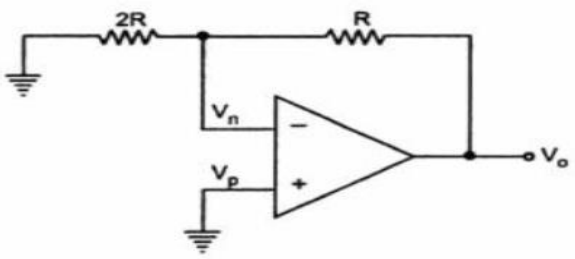


Applying KCL at node 'a' we have

$$\frac{V_i}{R} + \frac{V}{2R} + \frac{V}{R} = 0$$

$$\frac{3V}{2R} = \frac{-V_i}{R}$$

$$\therefore \quad V = \frac{-2}{3} V_i \qquad \ldots (4)$$



To find V_o in terms of V we concentrate on the equivalent circuit of A_2 , as shown in the Fig.

$$\therefore V_o = \left(1 + \frac{R}{2R}\right) V = \left(\frac{2R + R}{2R}\right) V = \frac{3}{2} V \quad \ldots (5)$$

Substituting value of V in above equation we get,

$$V_o = \frac{3}{2}\left(\frac{-2}{3} V_i\right) = -V_i \quad \ldots (6)$$

Hence for $V_i < 0$ the output is positive. This is illustrated in Fig.

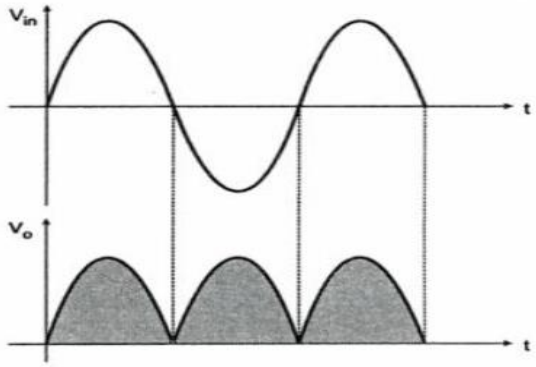


Fig. Input and output waveforms for full wave rectifier

2.8 Monostable Multivibrator

- The **monostable multivibrator** is also called as **the one-shot multivibrator**.
- The circuit produces a single pulse of specified duration in response to each **external trigger** signal. For such a circuit, only one **stable state** exists.
- When an external trigger is applied, the output changes its state. The new state is called as **a quasi-stable state**.
- The circuit remains in this state for a fixed interval of time. After some time it returns back to its original stable state.
- In fact, an internal trigger signal is generated which drives the circuit back to its original stable state.
- Usually, the **charging and discharging of a capacitor** provide this internal trigger signal.

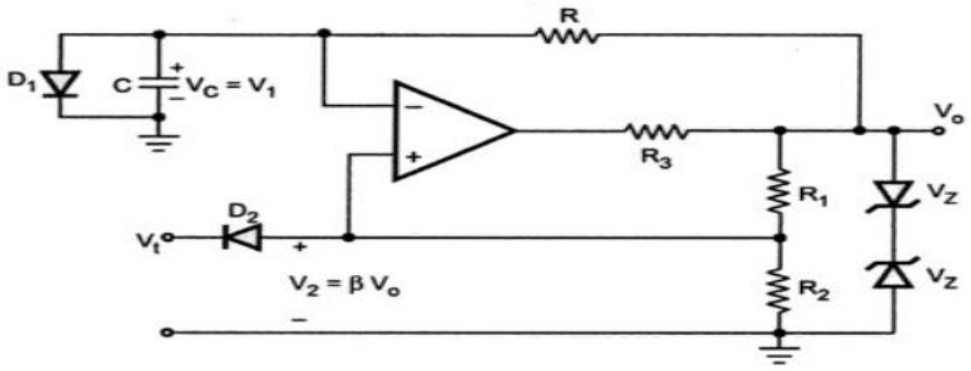


Fig: 2.13 Monostable Multivibrators

- The diode D_1 connected across the capacitor is called clamping diode. It clamps the capacitor voltage to 0.7 V when the output is at + V_{sat}.
- A negative triggering pulse is applied to the Non-inverting terminal of Op-amp through RC differentiator circuit and diode D_2.

Operation of the Circuit

(i).To understand the operation of the circuit, let us assume that the output Vo is at + $V_{sat,}$ i.e. in its stable state.

(ii). The diode D_1 (Connected across Capacitor) conducts and the voltage across the capacitor C = V_C gets clamped to 0.7 Volts.

(iii). The voltage at the non-inverting terminal is controlled by voltage divider circuit of R_1 and R_2

- Voltage at non-inverting terminal $(V_2) = +\beta V_0$

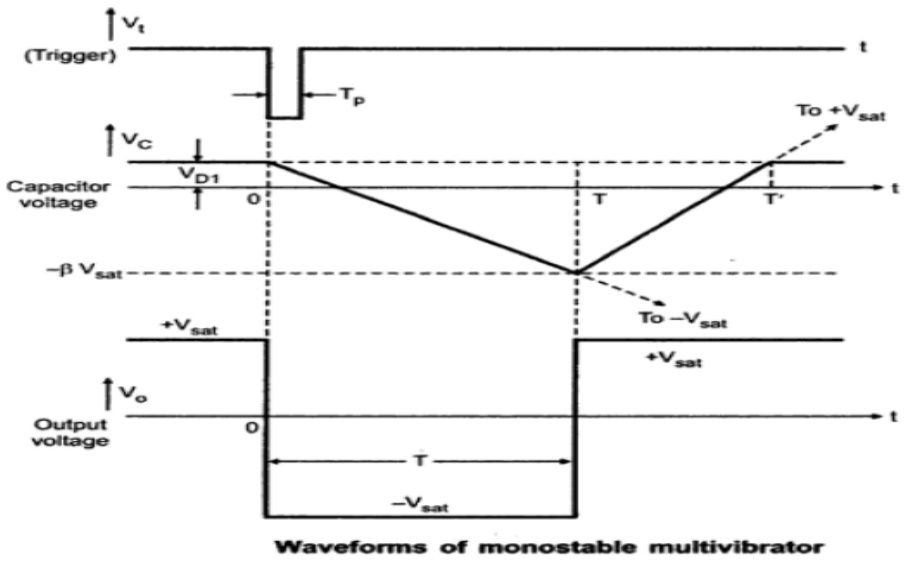
$$\beta = \frac{R_2}{R_1 + R_2}$$

(iv). If V_T, a negative trigger of amplitude V_T is applied to the non-inverting terminal, so that the effective voltage at this terminal is less than 0.7 V=>then the output of the Op-amp changes its state from + V_{sat} to - $V_{sat.}$

(v). The diode is now reverse biased and the capacitor starts charging exponentially to - V_{sat} through resistance R. The voltage at the non-inverting terminal is now - βV_{sat}. When the capacitor voltage becomes just slightly more negative than - $\beta V_{sat,}$ the output of the Op-amp changes its state back to + V_{sat}.

(vi).The capacitor now starts charging towards + V_{sat} through R until V_C reaches 0.7V as capacitor gets clamped to the voltage.

The waveforms are shown in the Fig.



Waveforms of monostable multivibrator

Fig: 2.14 Monostable Multivibrator Waveform

Expression for Pulse Width T

For a low pass RC circuit let,

V_i = initial value of the voltage

V_f = final value of the voltage

Then the general solution is given by,

$$V_o = V_f + (V_i - V_f)\, e^{-t/RC} \quad \ldots (1)$$

Now for the monostable multivibrator discussed above, the values of V_f and V_i are,

$$V_f = -V_{sat} \text{ and } V_i = V_{D1} \text{ (diode forward voltage)}$$

while V_o = output = capacitor voltage = V_C

$$\therefore \quad V_C = -V_{sat} + (V_{D1} - [-V_{sat}])\, e^{-t/RC} \quad \ldots (2)$$

at t = T, $V_C = -\beta V_{sat}$ ... (3)

$$\therefore \quad -\beta V_{sat} = -V_{sat} + (V_{D1} + V_{sat})\, e^{-T/RC} \quad \ldots (4)$$

$$\therefore \quad (V_{D1} + V_{sat})\, e^{-T/RC} = V_{sat}(1 - \beta)$$

$$\therefore \quad e^{-T/RC} = \frac{V_{sat}(1-\beta)}{(V_{D1} + V_{sat})}$$

$$\therefore \quad \boxed{T = RC\, ln\left[\frac{1 + V_{D1}/V_{sat}}{1-\beta}\right]} \quad \ldots (5)$$

This is obtained by absorbing negative sign inside the natural logarithm.

The potential divider decides the value of β given by,

$$\beta = \frac{R_2}{R_1 + R_2} \quad \ldots (6)$$

If $V_{sat} >> V_{D1}$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$\boxed{T = 0.69\ RC} \quad \ldots (7)$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator.

2.9 ASTABLE MULTIVIBRATOR

- A simple op-amp square wave generator is shown in Fig (a). Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region.
- In Fig. (a) Fraction $\beta = R_2/(R_1+R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage Vref is βVo, and may take values as + βVsat or - βVsat.
- The output is also fed back to the (-) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (-) input terminal just exceeds Vref switching takes place resulting in a square wave output.
- In Astable multivibrator, both the states are quasi stable.
- Consider an instant of time when the output is at +Vsat. The capacitor now starts charging towards +Vsat through resistance R, as shown in Fig (b).
- The voltage at the (+) input terminal in held at +βVsat by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded + βVsat the reference voltage.
- When the voltage at the (-) input terminal becomes just greater than this reference voltage, the output is driven to - Vsat.

- At this instant, the voltage on the capacitor is +βVsat. It begins to discharge through R. that is charges toward – Vsat.
- When the output voltage switches to -Vsat, the capacitor charges more and more negatively until its voltage just exceeds - BVsat. The output switches back to +Vsat. The cycle repeats itself as shown in Fig.

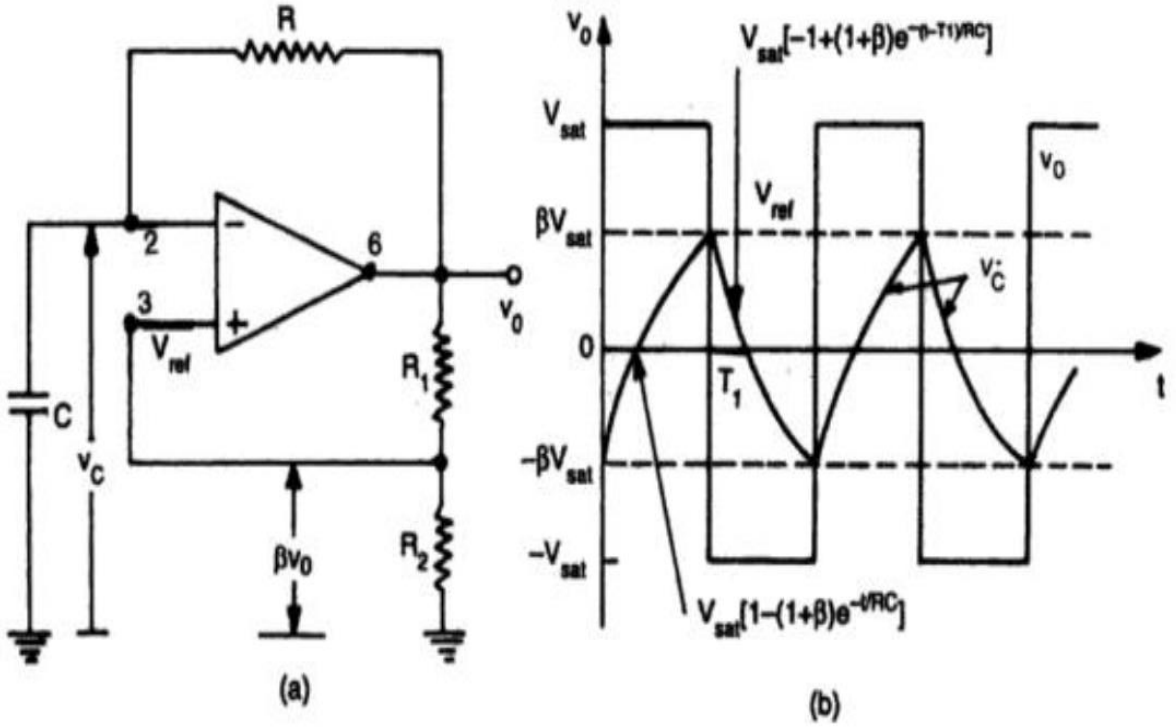


Fig. (a) Simple op-amp square wave generator (b) waveforms

Fig: 2.15 Astable Multivibrator

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC}$$

2.10 TRIANGULAR WAVE GENERATOR

It consists of a comparator (A) and an integrator (B) as shown in Figure 1.1. The output of comparator A is a square wave of amplitude $\pm$Vsat and is applied to the inverting (-) input terminal of the integrator B. The output of integrator is a triangular wave and it is feedback as input to the comparator A through a voltage divider R_2R_3.

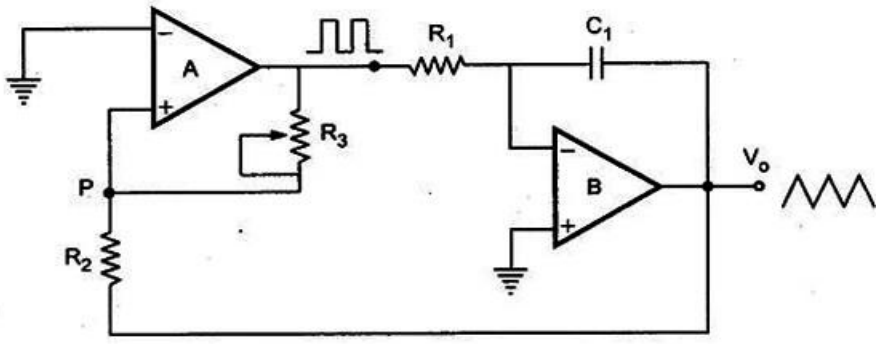


Fig: 2.16 Triangular Wave Generator

To understand circuit operation, assume that the output of comparator A is at + V_{sat} . This forces a constant current (+ V_{sat} / R_1) through C to give a negative going ramp at the output of the integrator, as shown in the Fig. Therefore, one end of voltage divider is at a voltage +V_{sat} and the other at the negative going ramp. When the negative going ramp reaches a certain value -V_{ramp}, the effective voltage at point p becomes slightly below 0V.

As a result, the output of comparator A switches from positive saturation to negative saturation (-V_{sat}). This forces a reverse constant current (right to left) through C to give a positive going ramp at the output of the integrator, as shown in the Fig. 2.89. When positive going ramp reaches + V_{ramp}, the effective voltage at point p becomes slightly above 0V. As a result, the output of comparator A switches from negative saturation to positive saturation (+V_{sat}). The sequence then repeats to give triangular wave at the output of integrator B.

Amplitude and Frequency Calculations:

The frequency and amplitude of the Triangular Wave Generator Using Op amp wave can be determined as follows:

When comparator output is at +V_{sat}, the effective voltage at point P is given by

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \qquad \ldots (1)$$

When effective voltage at P becomes equal to zero, we can write above equation

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}[+V_{sat} - (-V_{ramp})] = 0$$

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}(V_{ramp}) + \frac{R_2}{R_2 + R_3}(+V_{sat}) = 0$$

$$\frac{-R_3}{R_2 + R_3}(V_{ramp}) = -\frac{R_2}{R_2 + R_3}(+V_{sat})$$

$$\therefore \quad -V_{ramp} = \frac{-R_2}{R_3}(+V_{sat}) \qquad \ldots (2)$$

Similarly, when comparator output is at $-V_{sat}$, we can write,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) \qquad \ldots (3)$$

The peak to peak amplitude of the triangular wave can be given as

$$V_{o(pp)} = +V_{ramp} - (-V_{ramp}) \qquad \ldots (4)$$

$$= \frac{-R_2}{R_3}(-V_{sat}) - \left(\frac{-R_2}{R_3}\right)(+V_{sat})$$

If $|+V_{sat}| = |-V_{sat}|$ then, we can write

$$V_{o(pp)} = \frac{R_2}{R_3}V_{sat} + \frac{R_2}{R_3}V_{sat} = \frac{2R_2}{R_3}V_{sat} \qquad \ldots (5)$$

The time taken by the output to swing from $-V_{ramp}$ to $+V_{ramp}$ (or from $+V_{ramp}$ to $-V_{ramp}$) is equal to half the time period T/2. Refer Fig. 2.89. This time can be calculated from the integrator output equation as follows :

$$V_{o(pp)} = -\frac{1}{R_1 C_1}\int_0^{T/2}(-V_{sat})\,dt = \left(\frac{V_{sat}}{R_1 C_1}\right)\frac{T}{2} \qquad \ldots (6)$$

$$T = \frac{2R_1 C_1 V_{o(pp)}}{V_{sat}} \qquad \ldots . (7)$$

Substituting value of $V_{o(pp)}$ we get,

$$T = \frac{2R_1 C_1\left(\frac{2R_2}{R_3}V_{sat}\right)}{V_{sat}} = \frac{4R_1 C_1 R_2}{R_3} \qquad \ldots (8)$$

Therefore, the frequency of oscillation can be given as,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1 C_1 R_2} \qquad \ldots (9)$$

2.11 SAWTOOTH WAVE GENERATOR

- Saw tooth waveform can be also generated by an asymmetrical astable multivibrator followed by an integrator.
- The saw tooth wave generators have wide application in time-base generators and pulse width modulation circuits.
- The difference between the triangular wave and saw tooth waveform is that the rise time of triangular wave is always equal to its fall of time
- while in saw tooth generator; rise time may be much higher than its fall of time, vice versa.

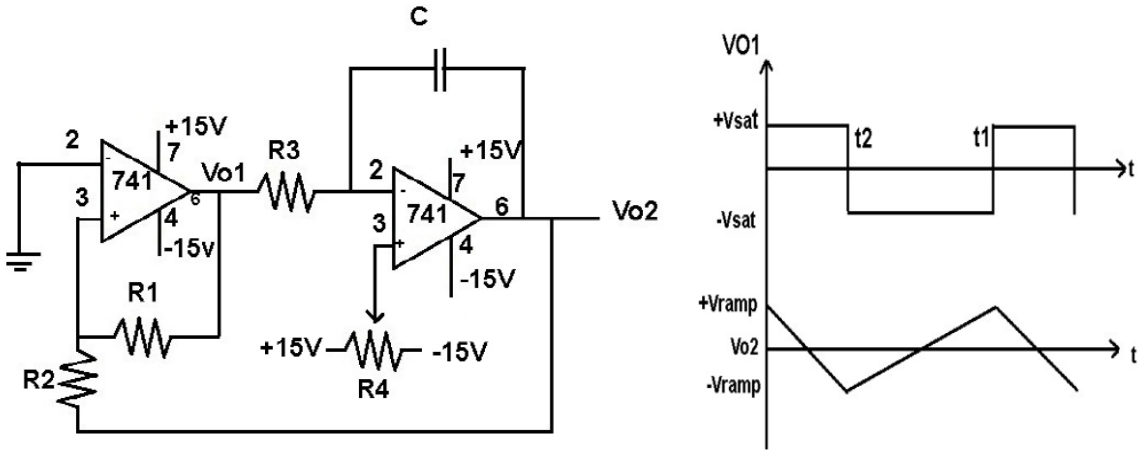


Fig: 2.17 Saw tooth Wave Generator

- The triangular wave generator can be converted in to a saw tooth wave generator by injecting a variable dc voltage into the non inverting terminal of the integrator. In this circuit a potentiometer is used (47K).
- when the wiper moves towards -V, the rise time of the saw tooth become longer than the fall time. If the wiper moves towards +V, the fall time becomes more than the rise time.
- Reason is when comparator output is at -ve saturation. When wiper moves to -ve supply, a negative voltage is added to inverting terminal.
- This causes the potential difference across R1 decreases and hence the current through the resistor and capacitor decreases. Then slope of the output, I/C decreases and in turn rise time decreases.
- When the comparator output goes positive, due to presence of negative voltage at the inverting terminal, potential difference of across the resistor R1 increases and hence current increases. Then slope increases and fall time decreases. And obtained output as saw tooth wave.

2.12 SINE WAVE GENERATORS

R-C phase shift oscillator

- R-C phase shift oscillator using op-amp uses an op-amp in inverting amplifier mode. Thus it introduces the phase shift of 180° between input and output.
- The feedback network consists of 3 RC sections each producing 60° phase shift. Such an RC phase shift oscillator using op-amp is shown in Fig.
- The output of the amplifier is given to the feedback network. The output of the feedback network drives the amplifier.
- The total phase shift around a loop is 180° of the amplifier and 180° due to 3 RC sections, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

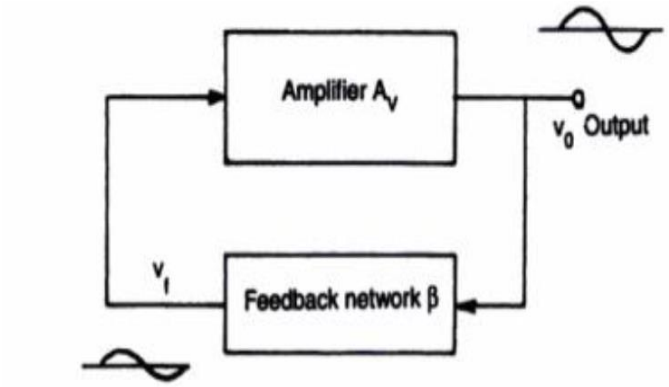


Fig. Block diagram of a feedback oscillator

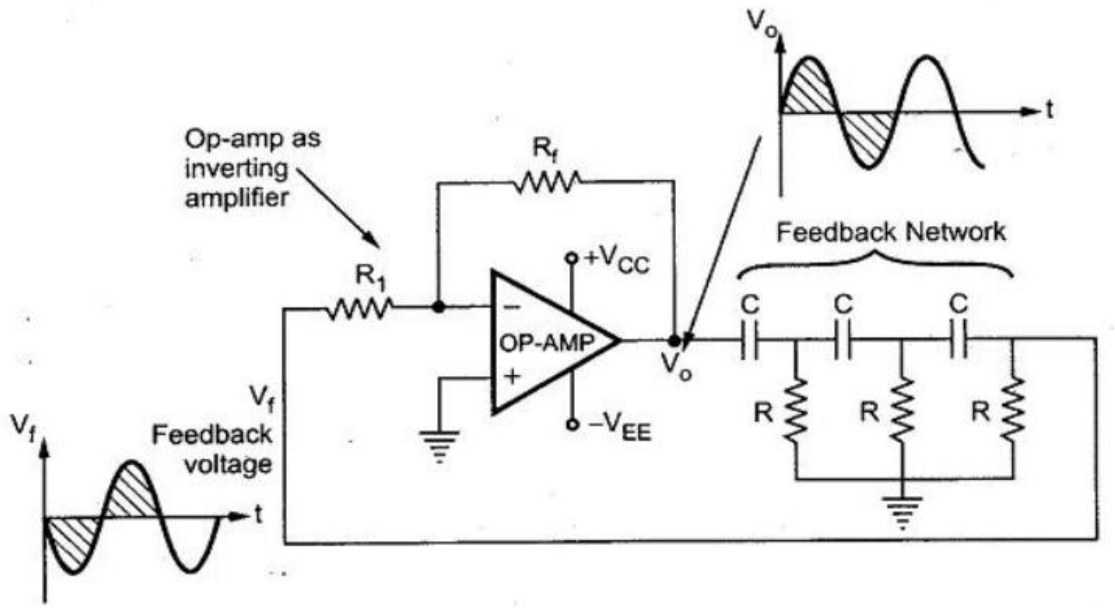


Fig: 2.18 **R-C Phase shift oscillator using op-amp**

Let us find the transfer function of the RC feedback network :

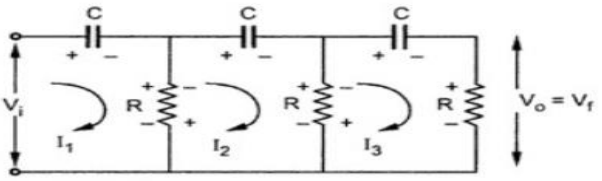


Fig. 2.

Applying KVL to various loops we get,

$$I_1\left(R+\frac{1}{j\omega C}\right) - I_2 R = V_i \quad \ldots (15)$$

$$-I_1 R + I_2\left(2R+\frac{1}{j\omega C}\right) - I_3 R = 0 \quad \ldots (16)$$

$$0 - I_2 R + I_3\left(2R+\frac{1}{j\omega C}\right) = 0 \quad \ldots (17)$$

Replacing $j\omega$ by s and writing the equations in the matrix form,

$$\begin{vmatrix} R+\frac{1}{sC} & -R & 0 \\ -R & 2R+\frac{1}{sC} & -R \\ 0 & -R & 2R+\frac{1}{sC} \end{vmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_i \\ 0 \\ 0 \end{bmatrix} \quad \ldots (18)$$

Using the Crammer's rule to obtain I_3

$$D = \begin{vmatrix} \frac{1+sRC}{sC} & -R & 0 \\ -R & \frac{1+2sRC}{sC} & -R \\ 0 & -R & \frac{1+2sRC}{sC} \end{vmatrix}$$

$$= \frac{(1+sRC)(1+2sRC)^2}{s^3C^3} - \frac{R^2(1+2sRC)}{sC} - \frac{R^2(1+sRC)}{sC}$$

$$= \frac{(1+sRC)(1+4sRC+4s^2C^2R^2) - R^2s^2C^2[1+2sRC+1+sRC]}{s^3C^3}$$

$$= \frac{1+5sRC+8s^2C^2R^2+4s^3C^3R^3-3s^3R^3C^3-2R^2s^2C^2}{s^3C^3}$$

$$= \frac{1+5sRC+6s^2C^2R^2+s^3C^3R^3}{s^3C^3} \quad \ldots (19)$$

$$D_3 = \begin{vmatrix} \frac{1+sRC}{sC} & -R & V_i \\ -R & \frac{1+2sRC}{sC} & 0 \\ 0 & -R & 0 \end{vmatrix}$$

$$= V_i R^2 \quad \ldots (20)$$

$$\therefore \quad I_3 = \frac{D_3}{D} = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3}$$

Now $$V_o = V_f = I_3 R = \frac{V_i R^2 s^3 C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \quad \ldots (21)$$

$$\therefore \quad \beta = \frac{V_o}{V_i} = \frac{R^3 s^3 C^3}{1+5sCR+6s^2C^2R^2+s^3C^3R^3} \quad \ldots (22)$$

Replacing s by $j\omega$, s^2 by $-\omega^2$, s^3 by $-j\omega^3$

$$\therefore \quad \beta = \frac{-j\omega^3 R^3 C^3}{1+5j\omega CR-6\omega^2C^2R^2-j\omega^3C^3R^3}$$

Dividing numerator and denominator by $-j\omega^3R^3C^3$ and replacing $\frac{1}{\omega RC}$ by α we get,

$$\therefore \quad \beta = \frac{1}{1+6j\alpha-5\alpha^2-j\alpha^3}$$

$$\therefore \quad \boxed{\beta = \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)}} \quad \ldots (23)$$

To have phase shift of 180°, the imaginary part in the denominator must be zero.

$$\alpha(6-\alpha^2) = 0$$
$$\alpha^2 = 6$$
$$\alpha = \sqrt{6}$$
$$\frac{1}{\omega RC} = \sqrt{6}$$
$$\omega = \frac{1}{RC\sqrt{6}}$$

$$\therefore \quad \boxed{f = \frac{1}{2\pi RC\sqrt{6}}} \quad \ldots (10)$$

This is the frequency with which circuit oscillates.

At this frequency,

$$\beta = \frac{1}{1-5\times(\sqrt{6})^2} = -\frac{1}{29}$$

Negative sign indicates phase shift of 180°

$$\therefore \quad \boxed{|\beta| = \frac{1}{29}} \quad \ldots (11)$$

Now to have the oscillations, $|A\beta| \geq 1$

$$\therefore \quad |A|\,|\beta| \geq 1$$

$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{\left(\frac{1}{29}\right)}$$

$$\boxed{|A| \geq 29} \quad \ldots (12)$$

Key Point: *For the oscillations to occur, the gain of the op-amp must be equal to or greater than 29, which can be adjusted using the resistances* R_f *and* R_i.

- Thus circuit will work as an oscillator which will produce a sinusoidal waveform if the gain is 29 and total phase shift around a loop is 360°.
- This satisfies the Barkhausen criterion for the oscillator. These oscillators are used over the audio frequency range i.e. about 20 Hz up to 100 kHz.

Advantages

- The advantages of R-C phase shift oscillator are,
- The circuit is simple to design.
- Can produce output over the audio frequency range.
- Produces sinusoidal output waveform.
- It is a fixed-frequency oscillator.

Disadvantages

- By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.
- And the frequency stability is poor due to the changes in the values of various components, due to the effect of temperature, ageing etc.

2.13 Wien Bridge Oscillator Using Opamp

- An oscillator is a circuit that produces periodic electric signals such as sine wave or square wave. The application of oscillator includes sine wave generator, local oscillator for synchronous receivers etc.

An oscillator consists of an amplifier and a feedback network.

1. Active device i.e. opamp is used as an amplifier.

2. Passive components such as R-C or L-C combinations are used as feedback network.

To start the oscillation with the constant amplitude, positive feedback is not the only sufficient condition. Oscillator circuit must satisfy the following two conditions known as **Barkhausen conditions:**

1. Magnitude of the loop gain ($Av\ \beta$) = 1,

where, Av = Amplifier gain and

β = *Feedback gain.*

2. Phase shift around the loop must be 360°or 0°.

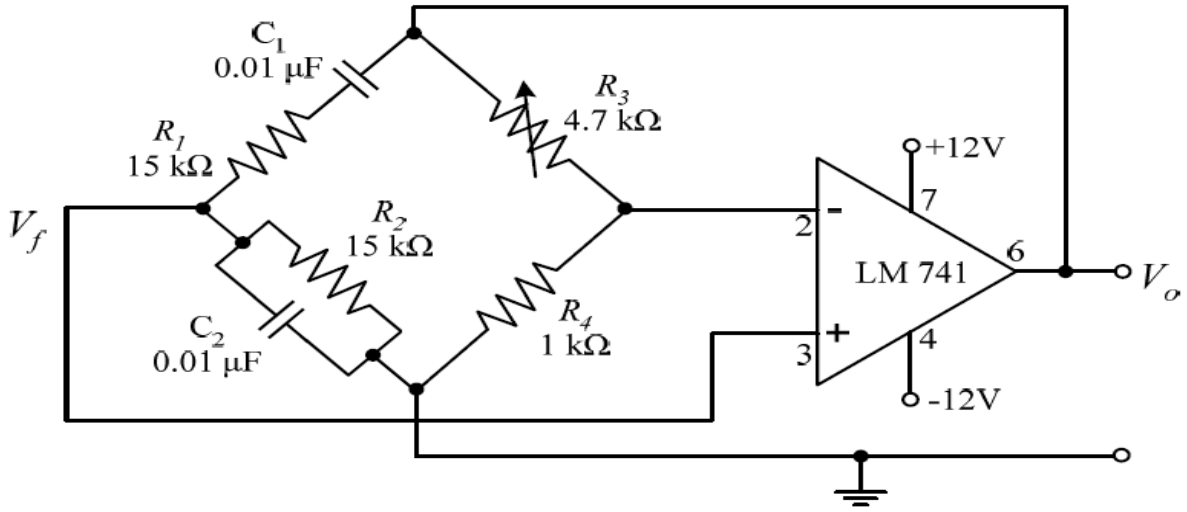


Fig 2 Circuit diagram of Wien bridge oscillator using opamp.

- Wien bridge oscillator is an audio frequency sine wave oscillator of high stability and simplicity.
- The feedback signal in this circuit is connected to the non-inverting input terminal. so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift.
- The circuit can be viewed as a Wien bridge with a series combination of R1 and C1 in one arm and parallel combination of R2 and C2 in the adjoining arm. Resistors R3 and R4 are connected in the remaining two arms.
- The condition of zero phase shift around the circuit is achieved by balancing the bridge.
- The series and parallel combination of RC network form a lead-lag circuit.
- **At high frequencies,** the reactance of capacitor C1 and C2 approaches zero. This causes C1 and C2 appears short. Here, capacitor C2 shorts the resistor R2. Hence, the output voltage Vo will be zero since output is taken across R2 and C2 combination. So, at high frequencies, circuit acts as a '**lag circuit'.**
- **At low frequencies, both capacitors act as open because capacitor offers** very high reactance. Again, output voltage will be zero because the input signal is dropped across the R1 and C1 combination. Here, the circuit acts like a **'lead circuit'.**
- But at one particular frequency between the two extremes, the output voltage reaches to the maximum value. At this frequency only, resistance value becomes equal to capacitive reactance and gives maximum output. Hence, this frequency is known as oscillating frequency (*f*).

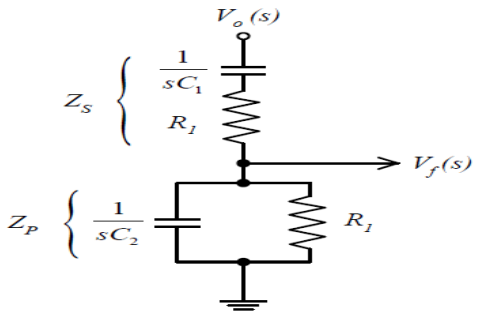
Consider the feedback circuit shown in fig 3 On applying voltage divider rule,

$$V_f(s) = \frac{V_o(s) \times Z_P(s)}{Z_P(s) + Z_S(s)}$$

where, $Z_S(s) = R_1 + \frac{1}{sC_1}$ and $Z_P(s) = R_2 \parallel \frac{1}{sC_2}$

Let, $R_1 = R_2 = R$ and $C_1 = C_2 = C$. On solving,

$$\text{feedback gain, } \beta = \frac{V_f(s)}{V_o(s)} = \frac{RsC}{(RsC)^2 + 3RsC + 1} \tag{1}$$



Since the op-amp is operated in the non-inverting configuration the voltage gain,

$$A_v = \frac{V_o(s)}{V_f(s)} = 1 + \frac{R_3}{R_4} \tag{2}$$

Applying the condition for sustained oscillations, $A_v\beta = 1$

Substitute equations (1) & (2), we get,

$$\left(1 + \frac{R_3}{R_4}\right)\left(\frac{RsC}{(RsC)^2 + 3RsC + 1}\right) = 1$$

Substitute $s = j\omega$

$$\left(1 + \frac{R_3}{R_4}\right)\left(\frac{j\omega RC}{-R^2C^2\omega^2 + 3j\omega RC + 1}\right) = 1$$

$$\left(1 + \frac{R_3}{R_4}\right) j\omega RC = \left(-R^2C^2\omega^2 + 3j\omega RC + 1\right)$$

$$j\omega\left[\left(1 + \frac{R_3}{R_4}\right)RC - 3RC\right] = 1 - R^2C^2\omega^2$$

To obtain the frequency of oscillation equate the real part to zero.

$$1 - R^2C^2\omega^2 = 0$$

$$\omega = \frac{1}{RC}$$

$$f = \frac{1}{2\pi RC}$$

SIMPLIFIED DESIGN:

Frequency of oscillation, $f = \dfrac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$

Let, $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$f = \frac{1}{2\pi RC}$$

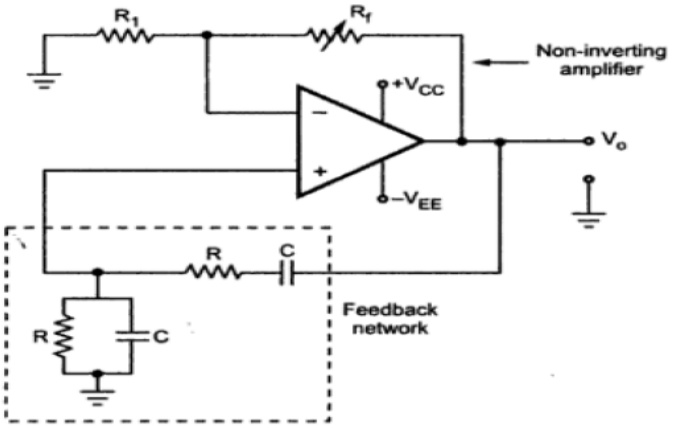
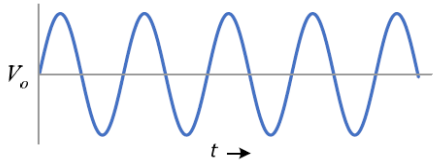


Fig. Simplified diagram of Wien bridge oscillator

OUTPUT (TO BE OBTAINED):



f = 1 kHz

Advantages

The various advantages of Wien bridge oscillator are,

1. By varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be obtained.
2. The perfect sine wave output is possible.
3. It is useful audio frequency range i.e. 20 Hz to 100 kHz.

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SCHOOL OF BIO AND CHEMICAL ENGINEERING

DEPARTMENT OF BIOMEDICAL ENGINEERING

UNIT – III –BIOSIGNAL CONDITIONING– SBMA1504

Unit 3 Filters

3.1 Introduction

A filter is a frequency selective circuit that, passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. Filter may be classified on a number of ways.

1. Analog or digital
2. Passive or active
3. Audio or radio frequency

Analog filters are designed to process only signals while digital filters process analog signals using digital technique. Depending on the type of elements used in their consideration, filters may be classified as passive or active.

Elements used in passive filters are resistors, capacitors and inductors.

Active filters, on the other hand, employ transistors or OPAMPs, in addition to the resistor and capacitors. Depending upon the elements the frequency range is decided. RC filters are used for audio or low frequency operation. LC filters are employed at RF or high frequencies.

The most commonly used filters are these:

1. Low pass filters
2. High pass filter
3. Band pass filter
4. Band reject filter.
5. All pass filter

A low pass filter has a constant gain from 0 Hz to a high cut-off frequency f_H. Therefore, the bandwidth is f_H. At f_H the gain is down by 3db. After that the gain decreases as frequency increases. The frequency range 0 to f_H Hz is called pass band and beyond f_H is called stop band.

Similarly, a high pass filter has a constant gain from very high frequency to a low cut-off frequency f_L. Below f_L the gain decreases as frequency decreases. At f_L the gain is down by 3db. The frequency range f_L Hz to ∞ is called pass band and below f_L is called stop band.

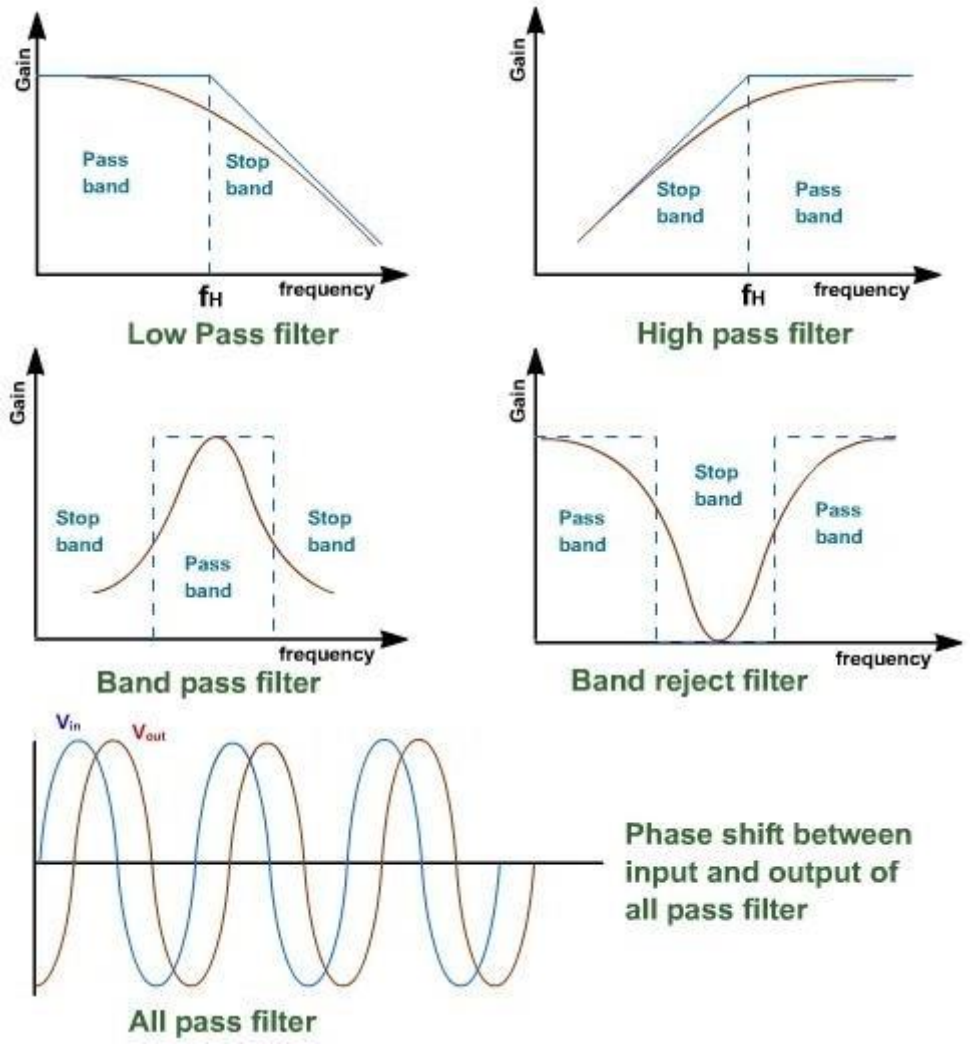


Fig. 1, shows the frequency response characteristics of the five types of filter. The ideal response is shown by dashed line. While the solid lines indicates the practical filter response.

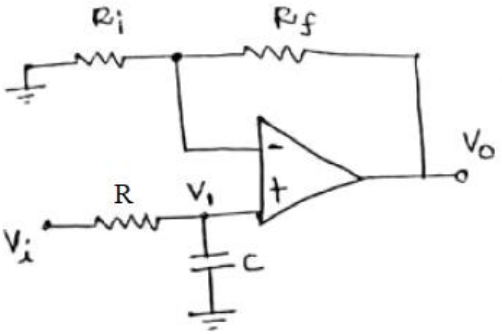
3.2 Low Pass filter

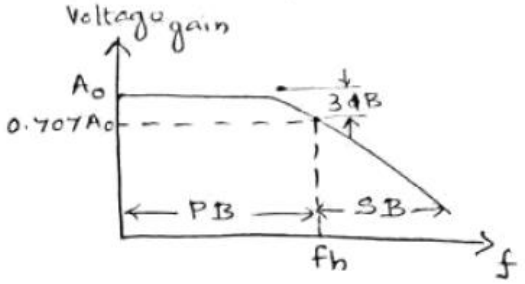
A **low-pass filter** (LPF) is a **filter** that **passes** signals with a **frequency lower** than a selected cut off **frequency** and attenuates signals with frequencies higher than the cut off **frequency**.

LOWPASS FILTER:

→ Active filters may be different orders and types

(*) A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-amp amplifier.





By applying voltage divider Rule,

V_1 across the capacitor C in the s domain is

$$V_1(s) = V_i(s) \frac{\frac{1}{sC}}{R + \frac{1}{sC}}$$

$\frac{C}{R+C}$ $C = \frac{1}{sC}$

$\frac{\frac{1}{sC}}{\frac{sCR+1}{sC}}$

$$V_1(s) = \frac{V_i(s)}{1+sCR}$$

$$\frac{V_1(s)}{V_i(s)} = \frac{1}{1+RCs} \quad \text{①}$$

The closed loop gain A_o of the op-amp is

$$A_o = \frac{V_o(s)}{V_1(s)} = \left[1 + \frac{R_f}{R_1}\right] \quad \text{②}$$

Transfer function

$$\frac{V_o}{V_i} = \frac{V_o}{V_1} \times \frac{V_1}{V_i} \quad \text{③}$$

Sub ①, ② in ③

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right]\left[\frac{1}{1+RCs}\right]$$

$$= \left[\frac{1 + R_f/R_1}{1+RCs}\right]$$

$$\frac{V_o}{V_i} = \frac{A_o}{1+RCs}$$

Using Laplace Transform

$$\frac{V_o(s)}{V_i(s)} = \frac{A_o}{1+RCs}$$

$\omega_h = \frac{1}{RC}$ $\therefore H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{1+\frac{s}{\omega_h}} = \frac{A_o \omega_h}{s+\omega_h}$ — (4)

Sub $s = j\omega$ in (4)

$$H(j\omega) = \frac{A_o}{1+j\omega/\omega_h} = \frac{A_o}{1+j(f/f_h)}$$

$$= \frac{A_o}{1+j\omega RC}$$ where

$$f = \frac{\omega}{2\pi}$$

$$f_h = \frac{1}{2\pi RC}$$

1) At very low frequency
(ie) $f << f_h$ $|H(j\omega)| \simeq A_o$

2) At $f = f_h$ $|H(j\omega)| = \frac{A_o}{1+(j\, f_h/f_h)} = \frac{A_o}{1+j}$

$$|H(j\omega)| = \frac{A_o}{\sqrt{2}} = 0.707 A_o$$

3) At very high frequency $f >> f_h$

$|H(j\omega)| = << A_o \simeq 0$

$\frac{A_o}{1+j} \times \frac{1-j}{1-j}$

$= \frac{A_o(1-j)}{1-j+j-j^2} = \frac{A_o(1-j)}{1-j^2}$

$= \frac{A_o(1-j)}{1-(-1)}$

$= \frac{A_o(1-j)}{2}$

$\frac{A_o(1-j)}{2} = \frac{A_o}{2} - j\frac{A_o}{2}$

$= \sqrt{\frac{A_o^2}{4} + \frac{A_o^2}{4}}$

$= \sqrt{\frac{2A_o^2}{4}} = \sqrt{\frac{A_o^2}{2}}$

$= \frac{A_o}{\sqrt{2}}$

→ LPF has maximum gain, A_o at $f = 0$ Hz

→ At f_h the gain falls to 0.707 time the maximum gain A_o.

→ The frequency range from 0 to f_h is called the pass band

→ At $f > f_h$ gain decreases at a constant rate of −20dB/decade.

→ The frequency range $f > f_h$ is called the stop band.

3.3 Second Order Low Pass Filter

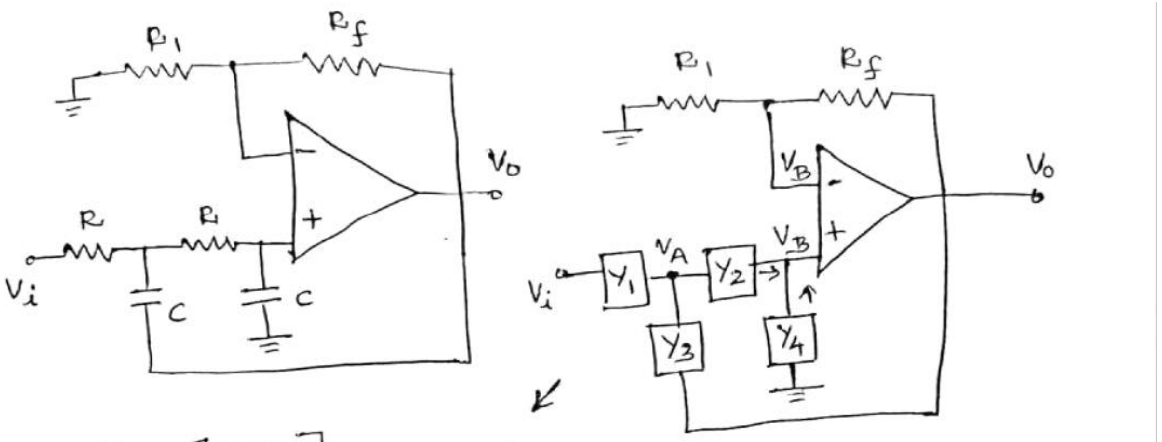
A second order LPF having a gain 40dB/decade in stop band. A First order LPF can be converted into a II order type simply by using an additional RC network.

SECOND ORDER LOW PASS FILTER: [Sallen-Key filter]

(*) An improved filter response can be obtained by using a second order active filter.

(*) A second order filter consists of two RC pairs and has a roll-off rate of -40dB/decade.

(*) The op-amp is connected as non-inverting amplifier.



$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_B = A_o V_B$$

$$V_o = A_o V_B \; ; \; V_B = \frac{V_o}{A_o}$$

Applying KCL Law At node B.

$$(V_A - V_B) Y_2 - V_B Y_4 = 0 \quad -(2)$$

$$V_A Y_2 - V_B Y_2 - V_B Y_4 = 0$$

$$V_A Y_2 = [Y_2 + Y_4] V_B$$

$$V_A = \left[\frac{Y_2 + Y_4}{Y_2}\right] V_B \quad -(3)$$

Applying KCL at node A

$$(V_i - V_A) Y_1 + (V_B - V_A) Y_2 + (V_o - V_A) Y_3 = 0 \quad -(1)$$

Replace $V_B = \frac{V_o}{A_o}$; $V_A = \left[\frac{Y_2 + Y_4}{Y_2}\right] V_B$ in (4)

$$V_i Y_1 + V_B Y_2 + V_o Y_3 = V_A (Y_1 + Y_2 + Y_3) \quad -(4)$$

$$V_i Y_1 + \frac{V_o}{A_o} Y_2 + V_o Y_3 = \left(\frac{Y_2 + Y_4}{Y_2}\right)\left(\frac{V_o}{A_o}\right)(Y_1 + Y_2 + Y_3)$$

$$V_i Y_1 + \frac{V_o Y_2}{A_o} + V_o Y_3 = \frac{V_o}{A_o Y_2}\left[(Y_2+Y_4)(Y_1+Y_2+Y_3)\right]$$

$$V_i Y_1 = V_o\left[\frac{(Y_2+Y_4)(Y_1+Y_2+Y_3)}{A_o Y_2} - \frac{Y_2}{A_o} - Y_3\right]$$

$$V_i Y_1 = V_o\left[\frac{(Y_2+Y_4)(Y_1+Y_2+Y_3) - A_o Y_2 Y_3 - Y_2 Y_2}{A_o Y_2}\right]$$

$$\frac{V_o}{V_i} = \left[\frac{A_o Y_1 Y_2}{(Y_2+Y_4)(Y_1+Y_2+Y_3) - A_o Y_2 Y_3 - Y_2 Y_2}\right]$$

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1+Y_2+Y_3) + (1-A_o) Y_2 Y_3} \quad \text{--- (1)}$$

Sub $Y_1 = Y_2 = 1/R$

$Y_3 = Y_4 = sC$

$$= \frac{A_o (1/R)^2}{(1/R)^2 + sC\left[2/R + sC\right] + (1-A_o)\frac{sC}{R}}$$

$$= \frac{A_o (1/R)^2}{(1/R)^2 + \frac{2sC}{R} + (1-A_o)\frac{sC}{R} + s^2C^2}$$

$$= \frac{A_o (1/R)^2}{(1/R)^2 + \frac{sC}{R}(3-A_o) + s^2C^2}$$

Multiply R^2 in Numr & Deno

$$H(s) = \frac{A_o}{1 + (3-A_o)sCR + s^2C^2R^2}$$

$$H(s) = \frac{A_o}{s^2C^2R^2 + (3-A_o)sCR + 1}$$

Let $\omega_n = RC$

$$H(s) = \frac{A_o}{s^2/\omega_n^2 + (3-A_o)s/\omega_n + 1} \quad \text{--- (2)}$$

$$H(s) = \frac{A_0 \omega_h^2}{s^2 + (3 - A_0) s \omega_h + \omega_h^2} \quad \text{---} (3)$$

Sub $s = j\omega$ in eqn (2)

$$H(j\omega) = \frac{A_0}{(j\omega/\omega_h)^2 + (3 - A_0) j(\omega/\omega_h) + 1}$$

$$H(j\omega) = \frac{A_0}{s^2 + \alpha s + 1} \quad \text{---} (4)$$

where $s = j\omega/\omega_h$; $\alpha = 3 - A_0$

$$\text{Gain} = 20 \log |H(j\omega)|$$

$$= 20 \log \left| \frac{A_0}{1 + j\alpha(\omega/\omega_h) + (j\omega/\omega_h)^2} \right|$$

$$= 20 \log \frac{A_0}{\sqrt{[1 - \omega^2/\omega_h^2]^2 + [\alpha\omega/\omega_h]^2}}$$

For any Butterworth filter

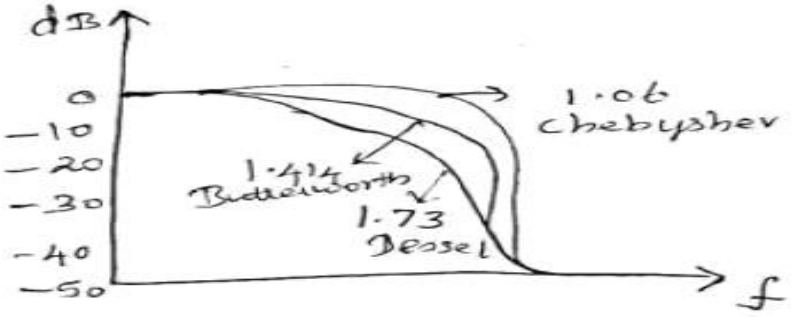
$$\alpha = 1.414$$

α is called damping coefficient

$$= 20 \log \frac{A_0}{\sqrt{1 + \frac{\omega^4}{\omega_h^4} - \frac{2\omega^2}{\omega_h^2} + \frac{\alpha\omega^2}{\omega_h^2}}}$$

$$= 20 \log \frac{A_0}{\sqrt{1 + (\omega/\omega_h)^4}}$$

$$20 \log \left| \frac{H(j\omega)}{A_0} \right| = \frac{1}{\sqrt{1 + (\omega/\omega_h)^{2n}}}$$



Pb 1. Design a second order Butterworth Low Pass filter having upper cut off frequency 1kHz.

$f = \frac{1}{2\pi RC}$; $C = 0.1\mu F$; $A_0 = 1 + \frac{R_f}{R_1}$

$\alpha = 3 - A_0$ let $\alpha = 1.414$

$1.414 - 3 = -A_0$; $\boxed{A_0 = 1.586}$

$A_0 = 1 + \frac{R_f}{R_1}$

$1.586 = 1 + \frac{R_f}{10}$

$1.586 = \frac{10 + R_f}{10}$

$1.586 = 10 + R_f$

$\boxed{R_f = 5.860}$

Sub $f = 1kHz$ & C is $f = \frac{1}{2\pi R}$.

$1 = \frac{1}{2\pi R(0.1)}$

$1 = \frac{1}{0.6280R}$

$0.6280R = 1$

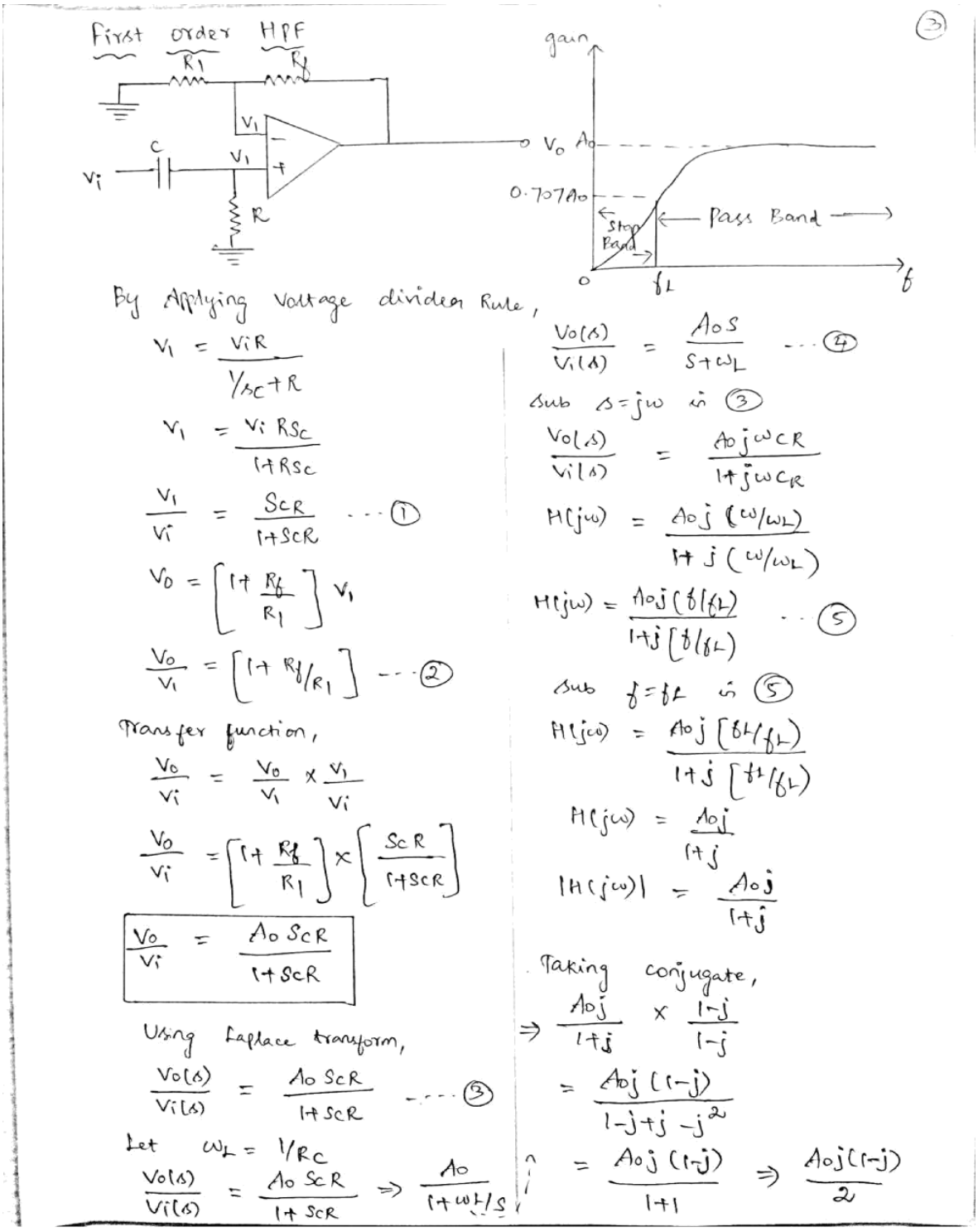
$R = 1.5924$

$\boxed{R = 1.6K}$

3.4 HIGH PASS FILTER

First Order HPF

A High Pass Filter is the exact opposite to the low pass filter. High pass filters are often formed simply by interchanging frequency-determining resistors and capacitors in low-pass filters.



$$= \frac{A_0 j - A_0 j^2}{2}$$

$$= \frac{A_0 j + A_0}{2}$$

$$|H(j\omega)| = \frac{A_0}{2} + \frac{jA_0}{2}$$

$$= \sqrt{\left[\frac{A_0}{2}\right]^2 + \left[\frac{A_0}{2}\right]^2}$$

$$= \sqrt{\frac{A_0^2}{4} + \frac{A_0^2}{4}}$$

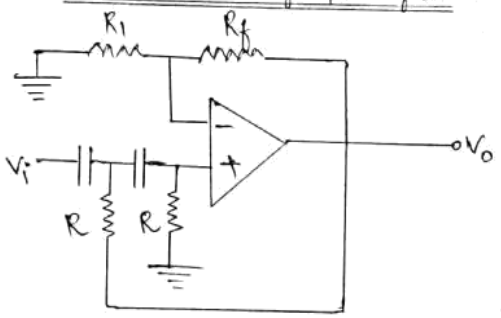
$$= \sqrt{\frac{2A_0^2}{4}}$$

$$= \sqrt{\frac{A_0^2}{2}}$$

$$= A_0/\sqrt{2}$$

magnitude at $f = f_L$, $|H(j\omega)| = A_0/\sqrt{2}$

* Second order High pass filter:-



$$\frac{V_o(s)}{V_i(s)} = H(s) = \frac{A_0 Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + (1 - A_0) Y_2 Y_3}$$

HPF

$Y_1 = Y_2 = sc$

$Y_3 = Y_4 = 1/R$

$$= \frac{A_0 sc\, sc}{sc\, sc + \frac{1}{R}[sc + sc + 1/R] + (1 - A_0)(sc)(1/R)}$$

$$= \frac{A_0 sc^2}{sc^2 + \frac{1}{R}\left[\frac{Rsc + Rsc + 1}{R}\right] + \frac{(1 - A_0)(sc)}{R}}$$

$$= \frac{A_0 sc^2}{sc^2 + \frac{1}{R}\left[\frac{2Rsc + 1}{R}\right] + \frac{sc - A_0 sc}{R}}$$

$$= \frac{A_0 sc^2}{sc^2 + \frac{2sc}{R} + \frac{1}{R^2} + \frac{sc}{R} - \frac{A_0 sc}{R}}$$

$$= \frac{A_0 (sc)^2}{(sc)^2 + \frac{sc}{R}[3 - A_0] + 1/R^2}$$

Taking LCM,

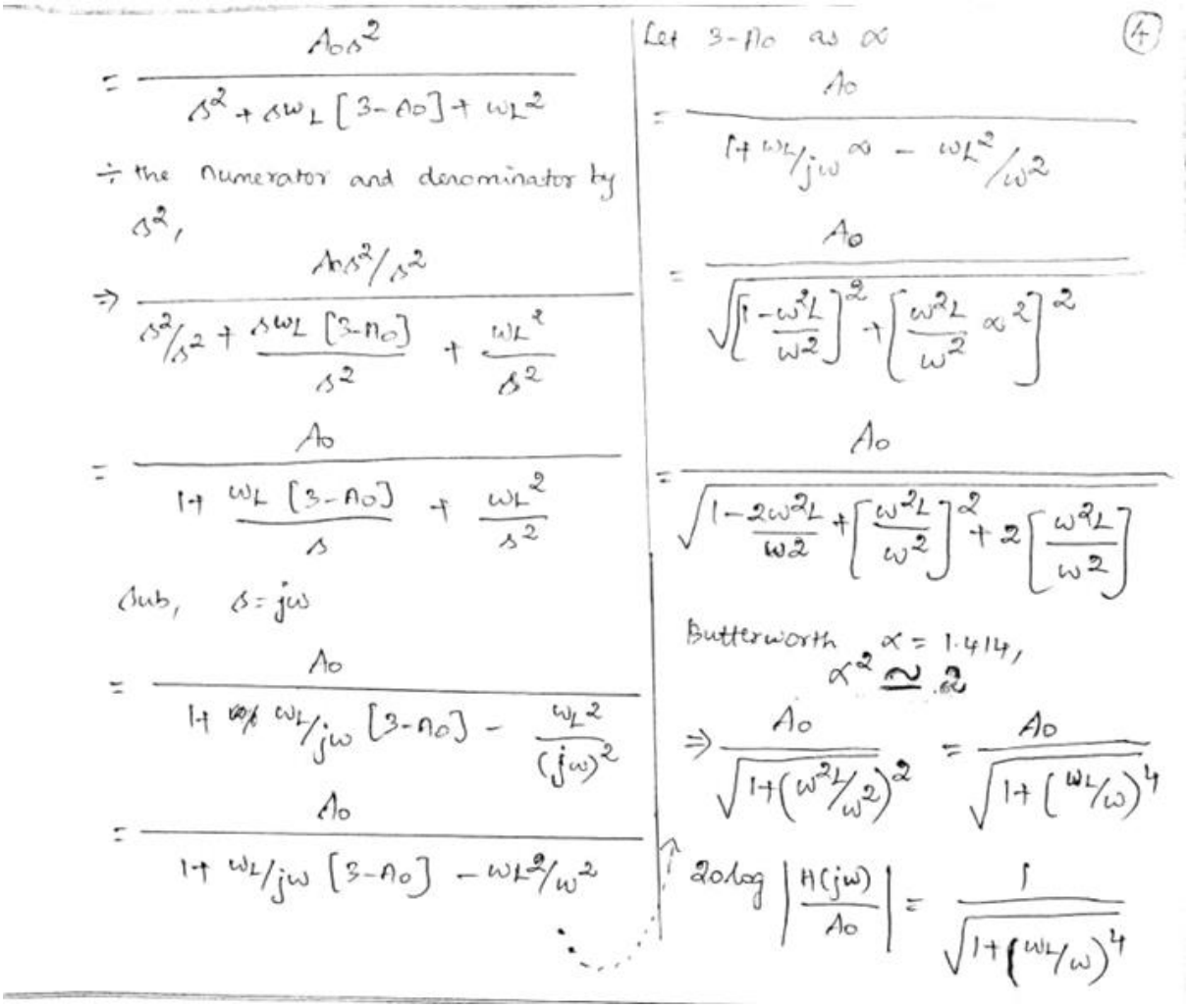
$$= \frac{A_0 (sc)^2 R^2}{s^2 c^2 R^2 + scR[3 - A_0] + 1}$$

$$= \frac{A_0 s^2/\omega_L^2}{1/\omega_L^2 \cdot s^2 + \frac{s}{\omega_L}[3 - A_0] + 1}$$

$$= \frac{A_0 s^2/\omega_L^2}{s^2/\omega_L^2 + s/\omega_L[3 - A_0] + 1}$$

$$= \frac{A_0 s^2/\omega_L^2}{\frac{s^2 + s\omega_L[3 - A_0] + \omega_L^2}{\omega_L^2}}$$

$$= \frac{A_0 s^2}{\omega_L^2} \times \frac{\omega_L^2}{s^2 + s\omega_L[3 - A_0] + \omega_L^2}$$



3.5 Band Pass Filter

Band pass filter pass a certain range of frequencies (called as **pass band**) while attenuate all other frequencies. Such band pass filters can be obtained by connecting low pass filter sections in cascade with high pass filter sections as shown in Fig.

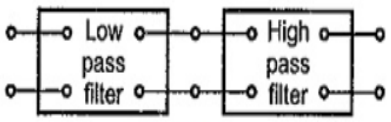


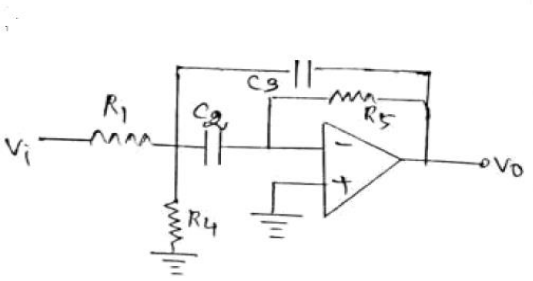
Fig.

In above type of connection, the cut-off frequency of low pass filter section must be selected higher than that of high pass filter section.

Although cascade connection of low pass filter and high pass filter sections functions properly as band pass filter, it is more economical to combine both sections in one single filter section.

- **Narrow Band Pass Filter Q > 10**
- **Wide Band Pass Filter Q< 10**

Second Order Narrow Band Pass Filter



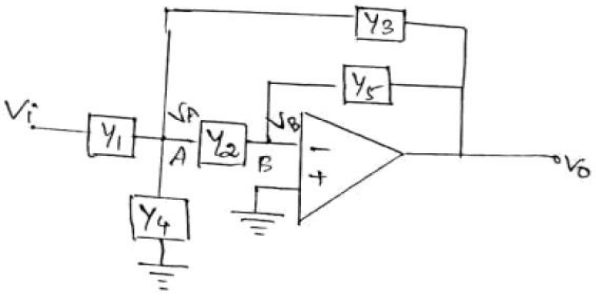


Figure of merit (Q) = $\frac{f_0}{f_H + f_L}$

$= \frac{f_0}{BW}$

$f_0 = \sqrt{f_H f_L}$

At node A:

$(V_i - V_A)Y_1 + (V_B - V_A)Y_2 + (V_o - V_A)Y_3 - V_A Y_4 = 0 \quad \cdots (1)$

$V_i Y_1 - V_A Y_1 + V_B Y_2 - V_A Y_2 + V_o Y_3 - V_A Y_3 - V_A Y_4 = 0$

$V_i Y_1 + V_B Y_2 + V_o Y_3 = V_A [Y_1 + Y_2 + Y_3 + Y_4] \quad \cdots (2)$

At node B,

$(V_A - V_B)Y_2 + (V_o - V_B)Y_5 = 0 \quad \cdots (3)$

Since $V_B = 0$

$V_A Y_2 + V_o Y_5 = 0$

$V_A = -\frac{V_o Y_5}{Y_2}$

Sub $V_A = -\frac{V_o Y_5}{Y_2}$ in (2)

$V_i Y_1 + 0 + V_o Y_3 = -\frac{V_o Y_5}{Y_2} [Y_1 + Y_2 + Y_3 + Y_4]$

$V_i Y_1 + V_o Y_3 = -\frac{V_o Y_5 [Y_1 + Y_2 + Y_3 + Y_4]}{Y_2}$

$\frac{V_o}{V_i} = \frac{-Y_1 Y_2}{Y_1 Y_5 + Y_2 Y_5 + Y_3 Y_5 + Y_2 Y_3 + Y_4 Y_5} \quad \cdots (4)$

$Y_1 = G_1, \; Y_2 = SC_2, \; Y_3 = SC_3,$

$Y_4 = G_4, \; Y_5 = G_5$

Transfer function,

Sub these values in (4),

$H(s) = \frac{V_o}{V_i} \Rightarrow$

$= \frac{-G_1 SC_2}{G_1 G_5 + SC_2 G_5 + SC_3 G_5 + SC_2 SC_3 + G_4 G_5}$

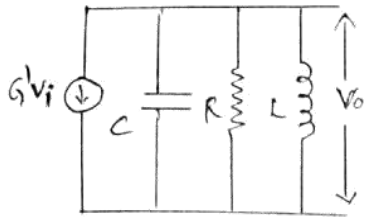
$= \frac{-G_1 SC_2}{s^2 C_2 C_3 + SC_2 G_5 + SC_3 G_5 + G_1 G_5 + G_4 G_5}$

$= \frac{-G_1 SC_2}{s^2 C_2 C_3 + S(C_2 + C_3) G_5 + G_5 (G_1 + G_4)}$

÷ Numerator and Denominator by SC_2,

$H(s) = \frac{-G_1}{SC_3 + G_5 \left[\frac{C_2 + C_3}{C_2}\right] + G_5 \left[\frac{G_1 + G_4}{SC_2}\right]} \quad \cdots (5)$

Parallel RLC circuit



For RLC circuit,

Transfer function is,

$$\frac{V_o(s)}{V_i(s)} = \frac{-G'}{Y} = \frac{-G'}{sC + G + \frac{1}{j\omega L}}$$

$\therefore$ ---> (6)

Compare (5) & (6),

$$G' = G_1$$

$$G = \frac{G_5(C_2 + C_3)}{C_2}$$

$$C = C_3$$

$$L = \frac{C_2}{G_5(G_1 + G_4)}$$

At resonance,

$$sC + \frac{1}{sL} = 0$$

$$sC = -1/sL$$

$$j\omega C = \frac{-1}{j\omega L}$$

$$\boxed{\omega_o = \frac{1}{\sqrt{LC}}} \rightarrow \text{Angular frequency}$$

When the frequency is maximum,

$$\text{Gain } \frac{V_o(s)}{V_i(s)} = \frac{-G'}{G}$$

Similarly for a Band pass filter at resonance gain, (5)

$$H(s) = \frac{-G_1}{\frac{G_5(C_2 + C_3)}{C_2}}$$

$$H(s) = \frac{-G_1 C_2}{G_5(C_2 + C_3)}$$

$$H(s) = -\left[\frac{G_1}{G_5}\right] \frac{C_2}{C_2 + C_3}$$

* Quality factor :-

$$Q = \frac{\omega_o L}{R} = \omega_o RC$$

For a Band pass filter, Replace R by G_1,

$$Q = \omega_o L G$$

$$Q = \frac{\omega_o C}{G}$$

$$Q = \frac{\omega_o C_2 (C_2 + C_3) G_5}{G_5 (G_1 + G_4) C_2}$$

$$Q = \left[\frac{(C_2 + C_3)}{(G_1 + G_4)}\right] \omega_o$$

$$Q = \frac{\omega_o C}{G} = \frac{\omega_o C_3}{\frac{G_5(C_2 + C_3)}{C_2}}$$

$$Q = \frac{\omega_o C_3 \cdot C_2}{G_5(C_2 + C_3)}$$

Bandwidth:

$$BW = \frac{f_0}{Q_0} = \frac{\omega_0}{2\pi\omega_0 RC} = \frac{1}{2\pi RC}$$

$$BW = \frac{G}{2\pi C} = \frac{G_5(C_2+C_3)}{2\pi C_2 C_3}$$

$$C_2 = C_3 = C$$

$$\text{Gain, } = H(s) = \frac{-\left[\frac{G_1}{G_5}\right]C_2}{(C_2+C_3)}$$

$$= \frac{-[G_1/G_5]\,C}{C+C}$$

$$H(s) = \frac{-[G_1/G_5]\,C}{2C}$$

$$= \frac{-[G_1/G_5]}{2}$$

$$H(s) = \left[\frac{-R_5}{2R_1}\right]$$

$$\text{BW for BPF}_1 = \frac{G}{2\pi C}$$

$$\Rightarrow \frac{G_5(C_2+C_3)}{2\pi C_2 C_3} = \frac{G_5(C+C)}{2\pi C\,C}$$

$$= \frac{G_5(2C)}{2\pi C^2} \Rightarrow \frac{1}{\pi R_5 C}$$

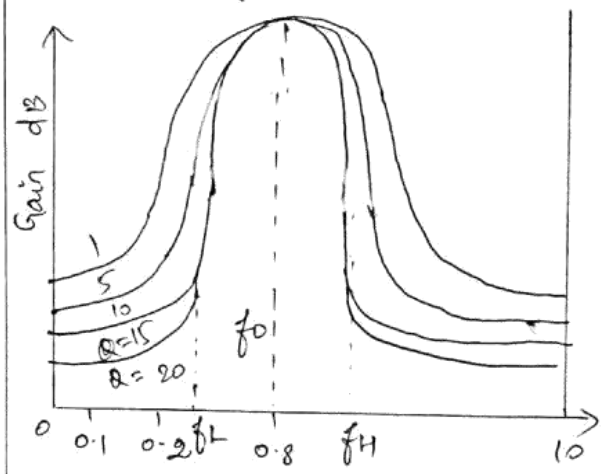
$$\omega_0 = \frac{1}{\sqrt{LC}}$$

$$\omega_0 = \frac{1}{\sqrt{\frac{C_2}{G_5(G_1+G_4)}\cdot C_3}}$$

$$\omega_0 = \frac{1}{\sqrt{\frac{C_2\cdot C_3}{G_5(G_1+G_4)}}}$$

$$\omega_0 = \frac{1}{\sqrt{\frac{C\cdot C}{G_5(G_1+G_4)}}}$$

$$\omega_0 = \sqrt{\frac{G_5(G_1+G_4)}{C}}$$



$$H(s) = \frac{-A_0(\omega_0/Q)\,s}{s^2+(\omega_0/Q)s+\omega_0^2}$$

$$= \frac{-A_0\alpha s}{s^2+\alpha s+\omega_0^2}$$

$$\therefore \boxed{\alpha = \omega_0/Q}$$

$$|H(j\omega)| = \frac{-A_0\alpha j\omega}{(j\omega)^2+\alpha j\omega+\omega_0^2}$$

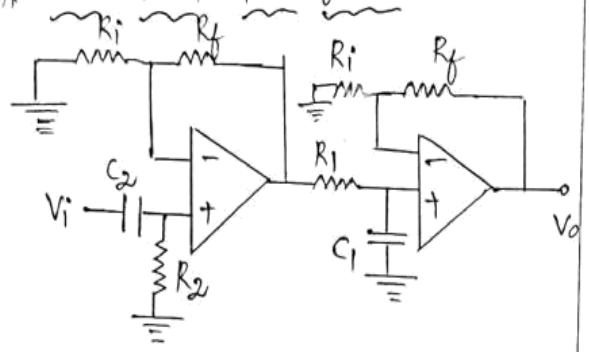
$$= \frac{-jA_0\alpha\omega}{-\omega^2+\alpha\omega j+\omega_0^2}$$

$$= \sqrt{\left[\frac{A_0 \alpha\omega}{(\omega_0^2 - \omega^2 + j\alpha\omega)}\right]^2}$$

$$|H(j\omega)| = \frac{A_0 \alpha\omega}{\omega_0^2 - \omega^2 + j\alpha\omega}$$

---

* Wide Band Pass filter



Since it is a cascaded Reaction, High pass filter + Low pass filter, so it is a cascade reaction

$$H(j\omega) = \frac{Aj\, f/f_L}{1 + j\, f/f_L} \times \frac{A_0}{(1-j)(f/f_h)}$$

$$\left|\frac{V_0}{V_i}\right| = \left| \frac{\left[Aj\ [f/f_L]\right]}{\left[1 + jf/f_L\right]^2 \left[1 + f/f_h\right]^2} \right|$$

Example Problem:

1. Design a wide band pass filter having $f_L = 400$ Hz, $f_h = 2$ KHz and pass band gain of 4. Find the value of Q of the filter.

(6)

$$A_0 = 1 + \frac{R_f}{R_i} = 2$$

$$R_f = R_i = 10\,k\Omega$$

For LPF, $f_h = 2$ KHz

$$= \frac{1}{2\pi R_1 C_1}$$

$C_1 = 0.01\,\mu F$, $R_1 = 7.9\,k\Omega$

For HPF, $f_L = 400$ Hz

$$= \frac{1}{2\pi R_2 C_2}$$

$C_2 = 0.01\,\mu F$, $R_2 = 39.8\,k\Omega$

$$f_0 = \sqrt{f_h f_L}$$

$$= \sqrt{2000 \times 400} = 894.4$$

$$Q = \frac{f_0}{BW} = \frac{f_0}{(f_h - f_L)}$$

$$Q = \frac{894.4}{(2000 - 400)} = 0.56$$

$Q < 10$, it is a wide Band pass filter.

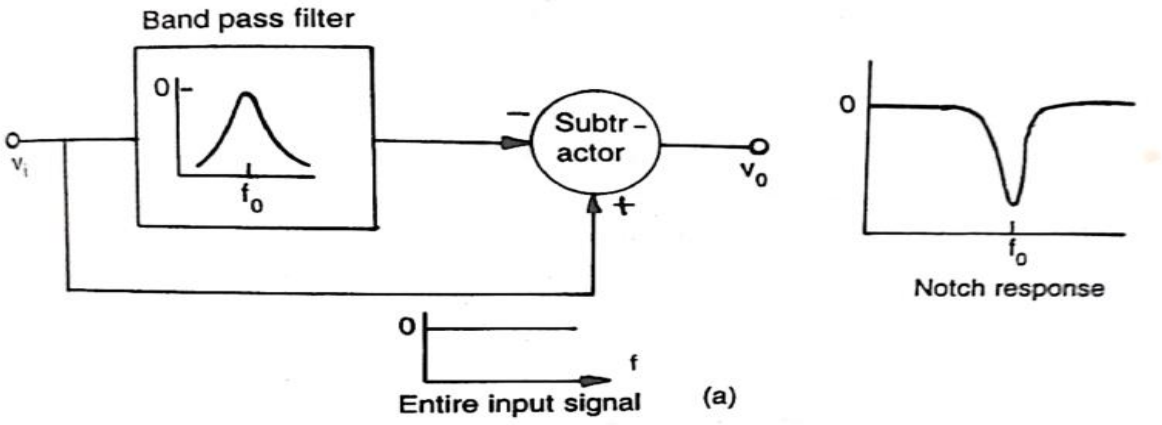
3.6 Band Stop / Reject Filter

A band Stop Filter known also as a Notch Filter, blocks and rejects frequencies that lie between its two cut-off frequency points passes all those frequencies either side of this range

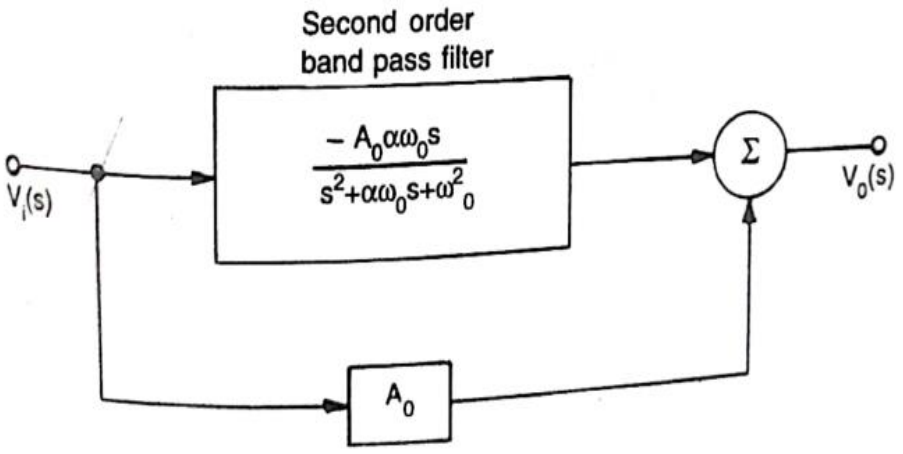
- Also called a band stop or band elimination
- 1. Narrow band reject (Q>10)
- 2. Wide band reject (Q<10)

Narrow band reject filter

- Narrow band reject filter is commonly called a notch filter- useful for the rejection of a single frequency such as 50Hz power line frequency.



(a) Notch filter block diagram

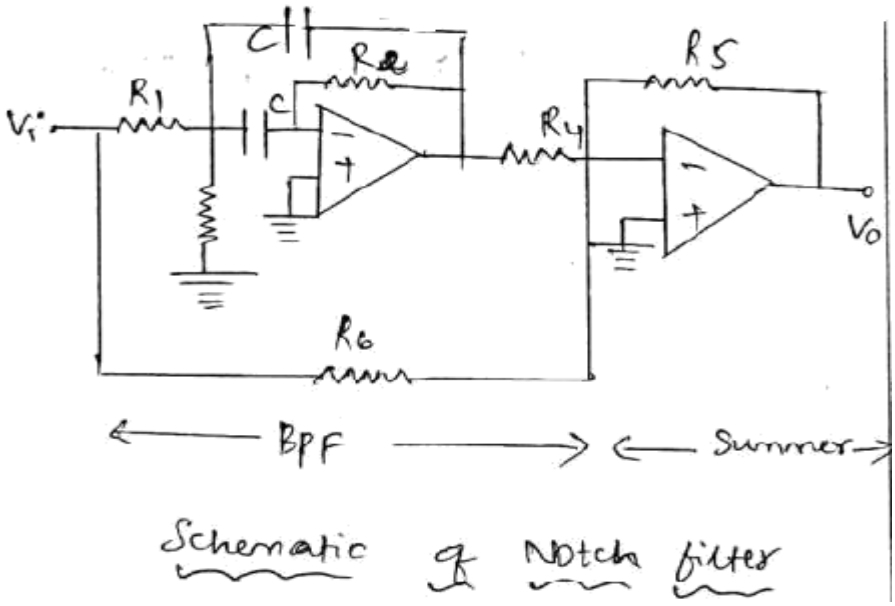


(b)

$$V_o(s) = A_o \times V_i(s) - \left[\frac{-A_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2}\right]$$

$$V_o(s) = A_o \times V_i(s) + \frac{A_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2}$$

$$\boxed{\frac{V_o(s)}{V_i(s)} = \frac{A_o (s^2 + \alpha \omega_o^2)}{s^2 + \alpha \omega_o s + \omega_o^2}}$$



Schematic of Notch filter

Wide band reject filter

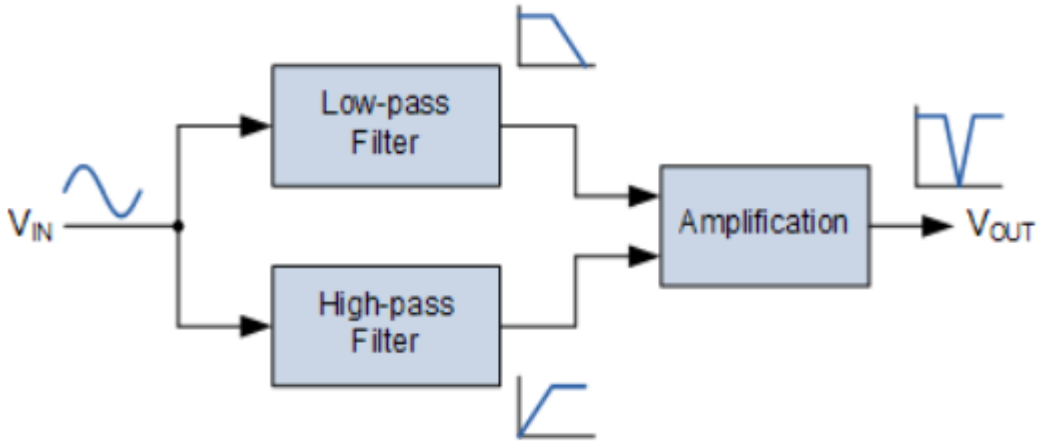


Figure (a) shows wide band reject filter using a low pass filter, a high pass filter and a summing amplifier. For a proper band reject response, the low cutoff frequency f_L of the high pass filter must be larger than the high cutoff frequency f_H of the low pass filter. Also, the pass band gain of both high pass and low pass sections must be equal.

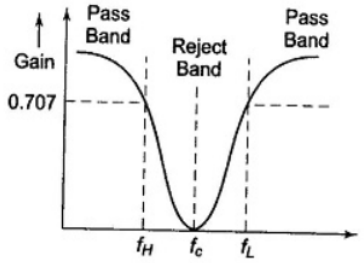
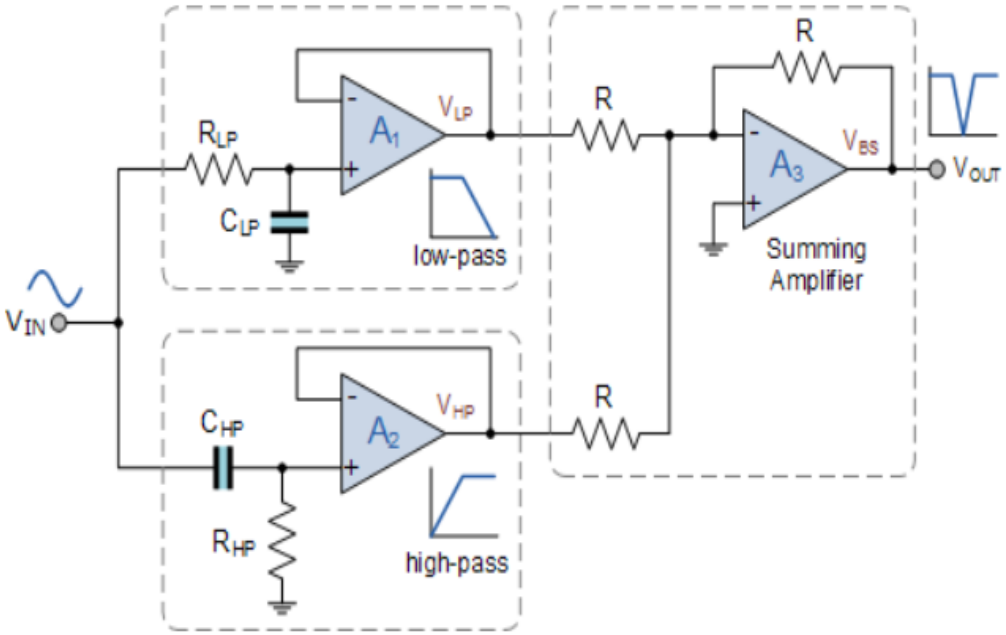
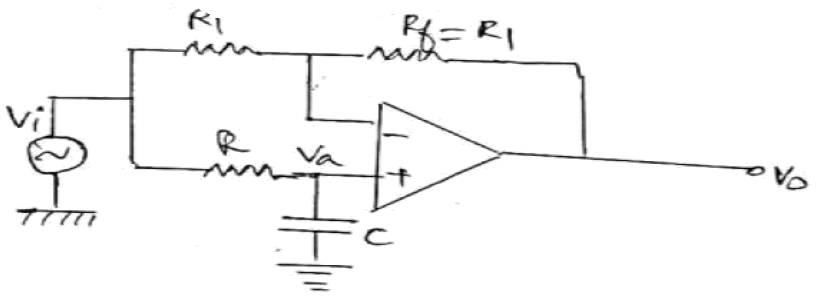


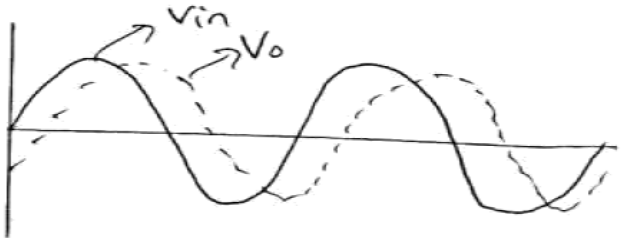
Fig. (b) Frequency Response of a Wide Band Reject Filter



3.7 All Pass Filter

An **all-pass filter** is that which **passes all frequency** components of the input signal without attenuation but provides predictable phase shifts for different frequencies of the input signals. The **all-pass filters** are also called delay equalizers or phase correctors.





$$V_o = -\frac{R_f}{R_1} V_i \quad [\text{gain of inverting terminal}]$$

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_a \quad [\text{gain of non-inverting terminal}]$$

$$V_o = -\frac{R_f}{R_1} V_i + \left[1 + \frac{R_f}{R_1}\right] V_a \quad \ldots\ldots (1)$$

$$V_a = \frac{V_i \cdot 1/sC}{R + 1/sC} \qquad \because R_f = R_1$$

Sub V_a in (1)

$$V_o = -R_1/R_1 \, V_i + (1+1) \frac{V_i \cdot 1/sC}{R + 1/sC}$$

$$= -V_i + \frac{2V_i\left(\frac{1}{sC}\right)}{R + \frac{1}{sC}}$$

$$= -V_i + \frac{\frac{2V_i}{sC}}{\frac{sCR+1}{sC}}$$

$$\Rightarrow \frac{-V_i sC + 2V_i}{sCR+1}$$

$$V_o = \frac{-V_i sC + 2V_i}{sCR+1}$$

$$\frac{V_o}{V_i} = \frac{1 - sCR}{1 + sCR}$$

$s = j\omega$

$$\left|\frac{V_o}{V_i}\right| = \frac{1 - j\omega CR}{1 + j\omega CR} \times \frac{1 - j\omega CR}{1 + j\omega CR}$$

$$\Rightarrow \frac{1^2 + j^2\omega^2 C^2 R^2 - 2j\omega RC}{1^2 - j^2\omega^2 C^2 R^2}$$

$$= \frac{1 - \omega^2 C^2 R^2}{1 + \omega^2 C^2 R^2} + \frac{(-2j\omega RC)}{1 + \omega^2 R^2 C^2}$$

$$= \frac{(1 - \omega^2 R^2 C^2)^2 + 4\omega^2 R^2 C^2}{(1 + \omega^2 R^2 C^2)^2}$$

$$= \frac{1 - 2\omega^2 R^2 C^2 + \omega^4 R^4 C^4}{(1 + \omega^2 R^2 C^2)^2}$$

$$= \frac{(1 + \omega^2 R^2 C^2)^2}{(1 + \omega^2 R^2 C^2)^2}$$

$$= 1$$

From equations given above it is obvious that the amplitude of v_{out} / v_{in} is unity, that is $|v_{out}| = |v_{in}|$ throughout the useful frequency range and the phase shift between the input and output voltages is a function of frequency.

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4. A/D AND D/A CONVETERS

4.1 Sample and Hold Circuit

- A sample and hold circuit is a circuit which samples an input signal and holds onto its last sampled value until the input is sampled again.
- Sample and hold circuits are commonly used in analogue to digital converts, communication circuits, PWM circuits etc.
- The circuit shown is based on uA 741 opamp, n-channel E MOSFET BS170 and few passive components.

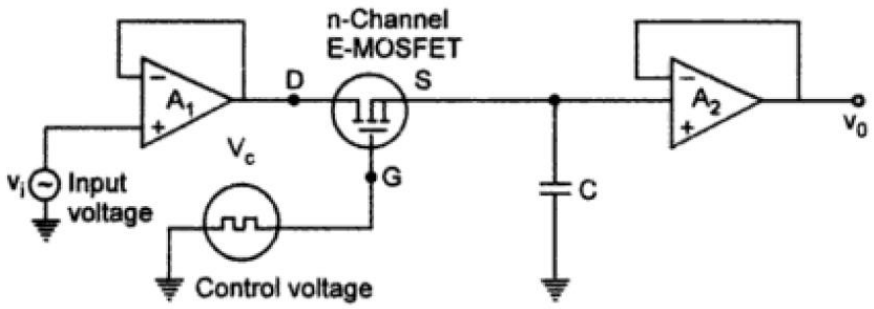
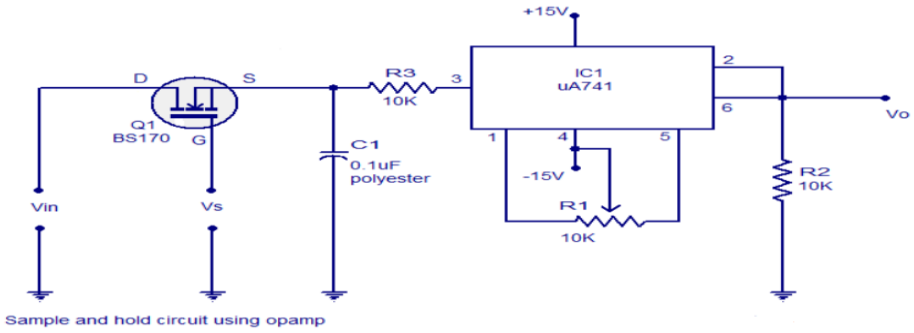


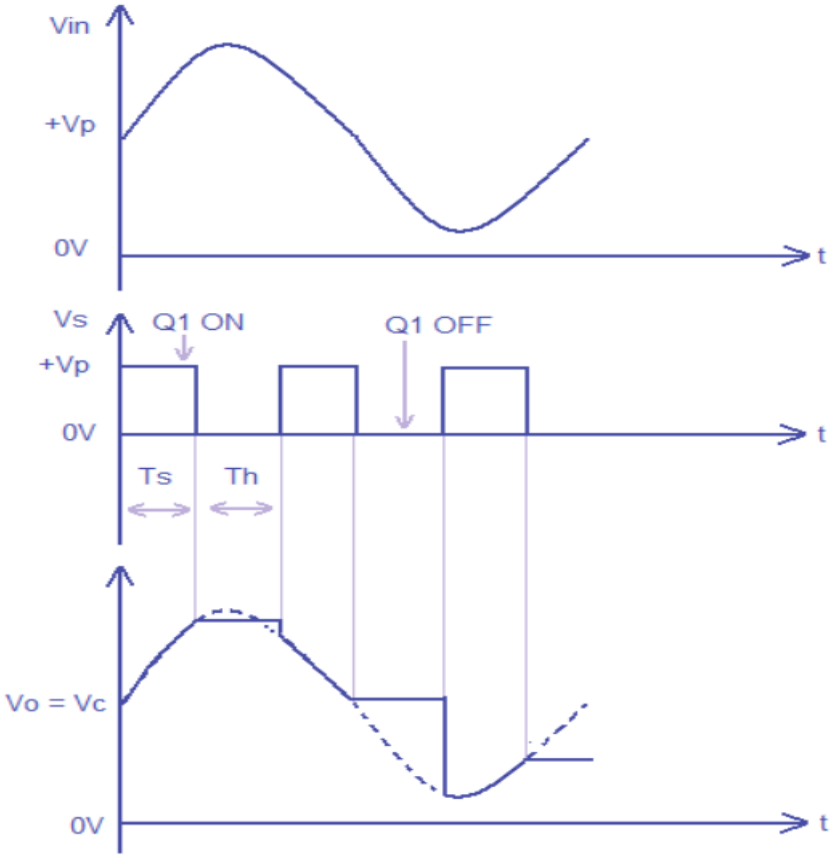
Fig. (a) Sample and hold circuit

- MOSFET BS170 (Q1) works as a switch while opamp uA741 is wired as a voltage follower.
- The signal to be sampled (Vin) is applied to the drain of MOSFET while the sample and hold control voltage (Vs) is applied to the source of the MOSFET.
- The source pin of the MOSFET is connected to the non inverting input of the opamp through the resistor R3.
- C1 which is a polyester capacitor serves as the charge storing device. Resistor R2 serves as the load resistor while preset R1 is used for adjusting the offset voltage.



Sample and hold circuit using opamp

- During the positive half cycle of the Vs, the MOSFET is ON which acts like a closed switch and the capacitor C1 is charged by the Vin and the same voltage (Vin) appears at the output of the opamp.
- When Vs is zero MOSFET is switched off and the only discharge path for C1 is through the inverting input of the opamp. Since the input impedance of the opamp is too high the voltage Vin is retained and it appears at the output of the opamp.
- The time periods of the Vs during which the voltage across the capacitor (Vc) is equal to Vin are called sample periods (Ts) and
- The time periods of Vs during which the voltage across the capacitor C1 (Vc) is held constant are called hold periods (Th).
- Taking a close look at the input and output wave forms of the circuit will make it easier to understand the working of the circuit.



The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.

4.2 AD and DA Converters

- The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion

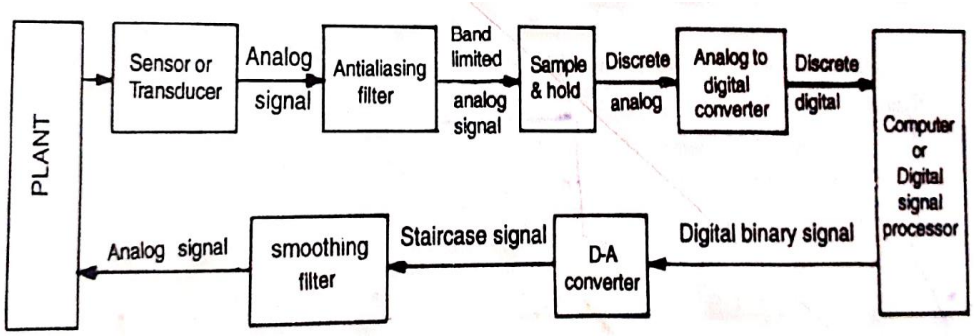


Fig: 4.2 AD and DA Converters

- The analog signal obtained from the transducer is band limited by antialiasing filter.
- The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal.
- The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit.
- The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm.
- The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC.
- The D/A converter is usually operated at the same frequency as the ADC.
- The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

Applications

- digital audio recording and playback,
- computer, music and video synthesis,
- pulse code modulation transmission,
- Data acquisition, digital multimeter,
- direct digital control, digital signal processing, microprocessor based instrumentation
- Both ADC and DAC are also known as data converters and are available in IC form.

4.3 Basic DAC Techniques

The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal.

The output of a DAC can be either a voltage or current.

For a voltage output DAC, the D/A converter is mathematically described as

$$V_0 = K\ V_{FS}\ (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

where,

V_0 = output voltage

V_{FS} = full scale output voltage

K = scaling factor usually adjusted to unity

$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left

d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$

d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

Resistive techniques

4.4 Weighted Resistor DAC

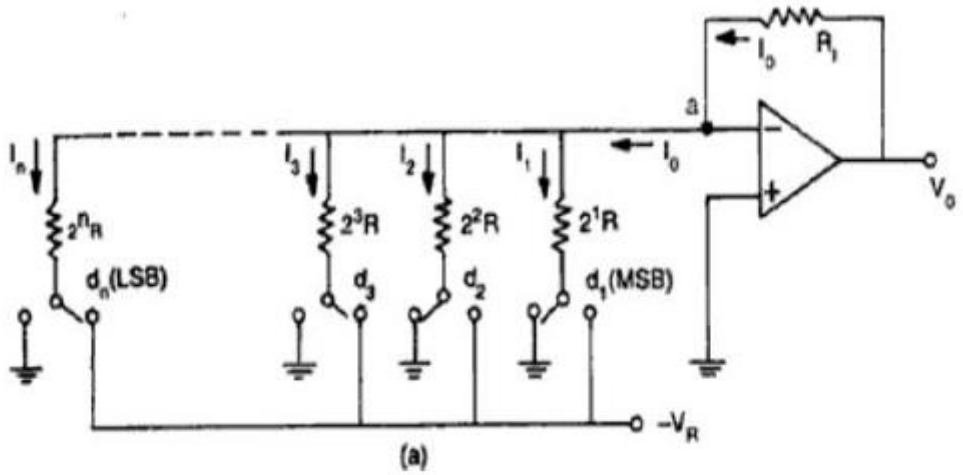


Fig: 4.2 AD and DA Converters

- One of the simplest circuits shown in Fig. (a) uses a summing amplifier with a binary weighted resistor network.
- It has n-electronic switches d_1, d_2.., d_n, controlled by binary input word. These switches are single pole double throw (SPDT) type.

- If the binary input to a particular switch is 1, it connects the resistance to the reference voltage (- V_R).
- And if the input bit is 0, the switch connects the resistor to the ground.

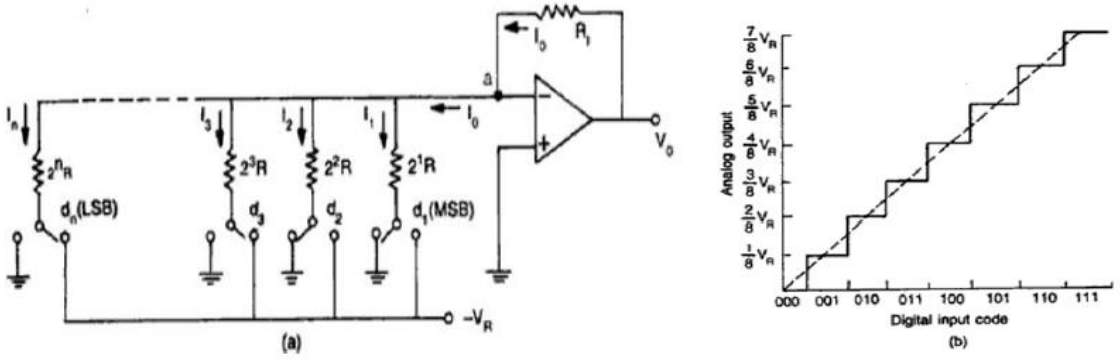


Fig. (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

Fig: 4.3 Weight Resistor DAC

From Fig. (a), the output current I_o, for an ideal op-amp can be written as

$$I_o = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_o = I_o R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

$$V_0 = K\, V_{FS} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad V_o = I_o R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

Comparing Eqns. it can be seen that if R_f =R then K = 1 and $V_{Fs} = V_R$

- The circuit shown in Fig.(a) uses a negative reference voltage.
- The analog output voltage is therefore positive staircase as shown in Fig.(b) for a 3-bit weighted resistor DAC.

It may be noted that

- Although the op-amp in Fig.(a) is connected in inverting mode, it can also be connected in non-inverting mode.

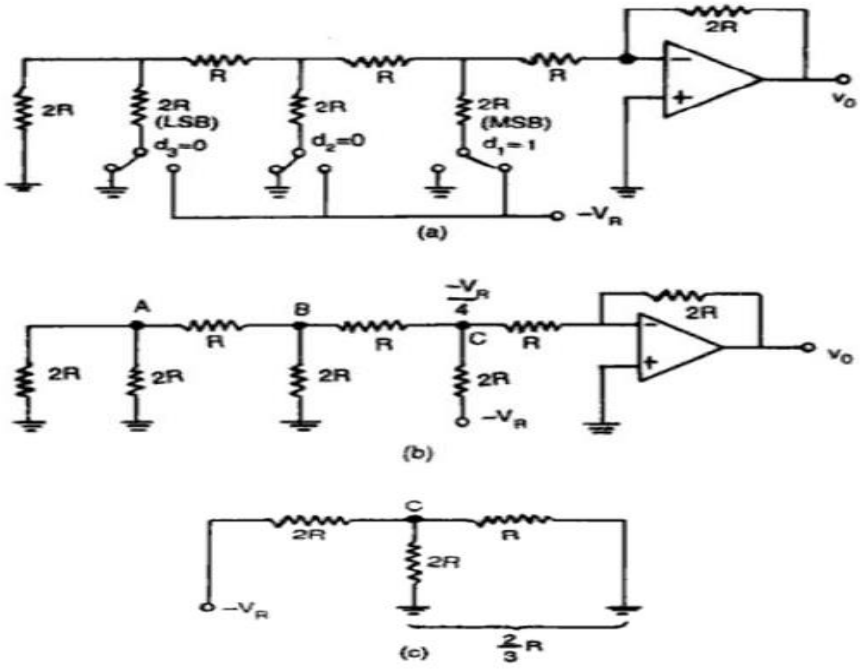
- The op-amp is simply working as a current to voltage converter.
- The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be + 5 V and the output will be negative
- The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature.

Disadvantages of binary weighted type DAC

- Wide range of resistor values required.
- For better resolution of output, the input **binary** word length has to be increased.
- As the number of bit increases, the range of resistance value increases.

4.4 R – 2R Ladder DAC

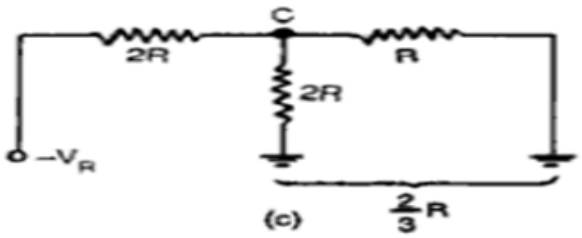
- Wide range of resistors is required in binary weighted resistor type DAC.
- This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.
- It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.
- For simplicity, consider a 3-bit DAC as shown in Fig. (a), where the switch position d_1, d_2, d_3 corresponds to the binary word 100.
- The circuit can be simplified to the equivalent form of Fig. (b) and finally to Fig. (c).



(a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

Fig: 4.4 R-2R ladder DAC

- The voltage at node C can be easily calculated by the set procedure of network analysis as



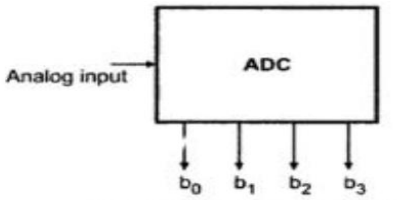
$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

The output voltage

$$V_0 = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

4.5 A/D Converters

A/D Converters



Symbol for 4-bit ADC

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function that of the D/A converter.

- Depending upon the type of application, ADCs are designed for microprocessor interfacing or to directly drive LCD or LED displays
- ADCS are classified broadly into two groups according to their Conversion technique.
  Direct type ADCs and Integrating type ADC
- Direct type ADCS compare a given analog signal with the internally generated equivalent signal.
- This group includes
  Flash (comparator) type converter
  counter type converter
  Tracking or servo converter
  Successive approximation type converter
- Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code.
- The two most widely used integrating type converters are
  Charge balancing ADC
  Dual slope ADC

- The most commonly used ADCs are successive approximation and the integrator type.
- The successive approximation ADCs are used in applications such as data loggers and instrumentation where conversion speed is important.
- The successive approximation and comparator type are faster but generally less accurate than integrating type converters.
- The flash (comparator) type is expensive for high degree of accuracy.
- The integrating type converter is used in applications such as digital meter panel meter and monitoring systems where the conversion accuracy is critical

4.6 The Parallel Comparator (Flash) A/D converter

This is the simplest possible A/D converter. the fastest and most expensive technique. Figure, (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder).

In Fig. (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R, and the ground.

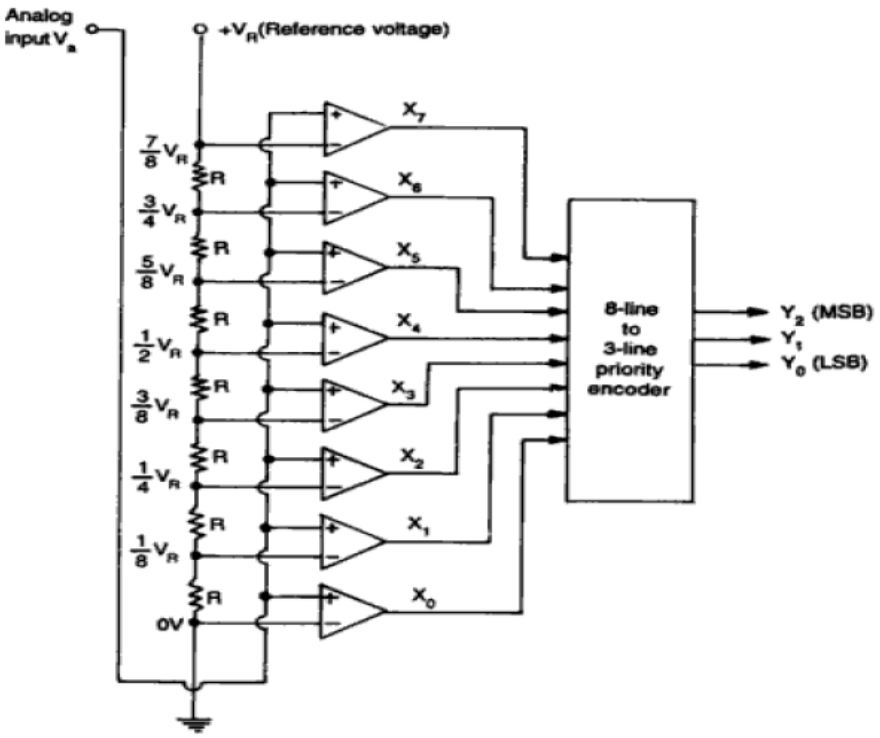


Fig. (a) Basic circuit of a flash type A/D converter

Fig: 4.5 Parallel Comparator (Flash) A/D converter

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

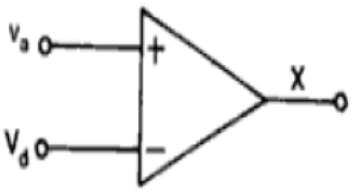


Fig. (b) Comparator and its truth table

Fig: 4.6 Comparator Truth table

- A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table.
- The purpose of the circuit is to compare the analog input voltage V_a, with each of the node voltages.
- The truth table for the flash type AD converter is shown in Fig. (c).
- The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially.
- Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder.
- By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. (c) Truth table for a flash type A/D converter

Fig: 4.7 Flash type A/D converter

Disadvantage of ADC

- The number of comparators required almost doubles for each added bit.
- A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators.
- In general, the number of comparators required is $2^n - 1$, where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.

4.7 Counter Type ADC

Principle of operation

- This ADC uses DAC for A to D conversion. The output of the DAC is continuously compared with the analog input to the ADC which is to be converted into digital output.
- When the output of the DAC becomes greater than this analog input, the corresponding digital input to the DAC is noted which represents the analog input to the ADC.

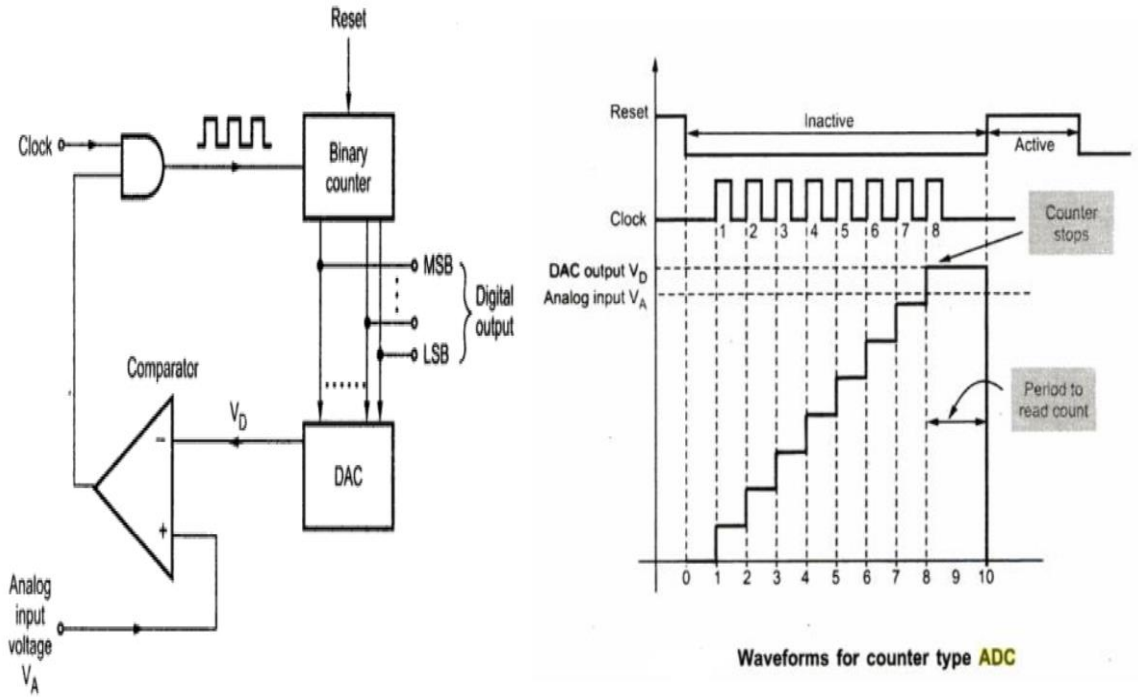


Fig: 4.8 Counter type ADC

As shown in the Fig. the counter type ADC consists of a binary counter, DAC, comparator and AND gate. The operation of the circuit is explained below.

i) Initially, the counter is reset, i.e. its output is set to zero by applying a reset pulse. The output of the counter is given as digital input to DAC. Since input to DAC is zero, its output V_D is zero.

ii) When the analog input voltage V_A is applied to ADC, it becomes greater than V_D. V_A acts as input voltage for non inverting terminal and V_D acts as input voltage for inverting terminal of the comparator. Since V_A is greater than V_D , the comparator output goes high.

iii) For an AND gate, one input is clock pulses and another input is the output of the comparator. Because of the high output of the comparator, the clock pulses are allowed to pass through the AND gate.

iv) The counter starts counting these close pulses. According to the number of clock pulses, the output of the counter goes on increasing. This increases the output of the DAC.

v) The above steps are continued till V_D is less than V_A.

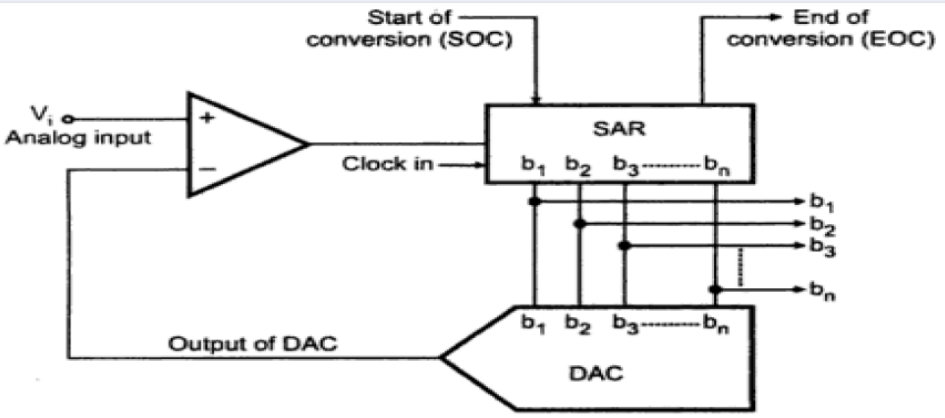
vi) As soon as DAC output V_D becomes greater than V_A, the comparator output goes low. This disables AND gate. So the clock pulses are not allowed to pass through the AND gate. The counting process of the binary counter is stopped.

vii) The output of the binary counter which is in digital form is noted which represents the digital equivalent of the analog input voltage V_A.

4.8 Successive Approximation ADC

- The basic idea is to adjust the DAC's input code such that its output is within $\pm$ 1/2 LSB of the analog input V_i to be A/D converted.
- The code that achieves this represents the desired ADC output. It uses very efficient code searching strategy called binary search. It completes searching process for n-bit conversion in just n clock periods.

Fig. shows the block diagram of successive approximation A/D converter.



Block diagram of successive approximation A/D converter

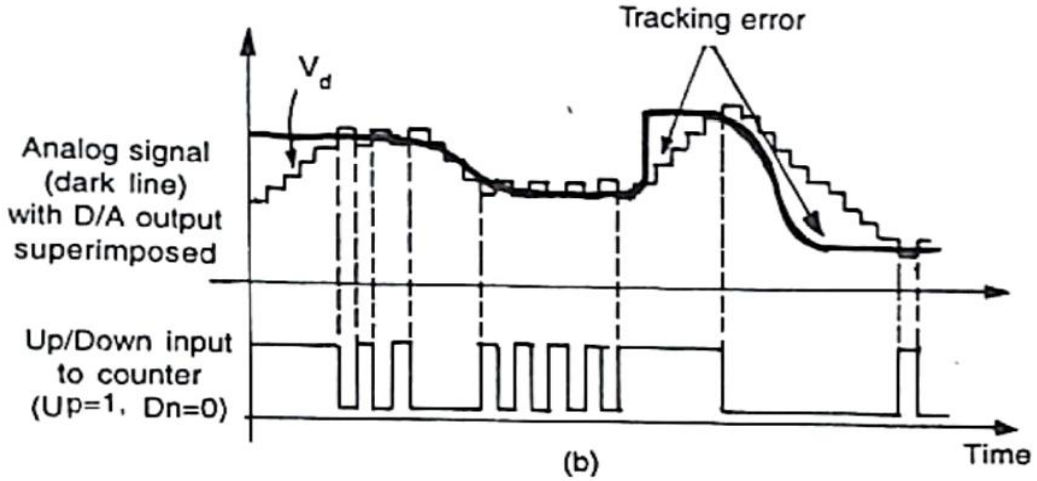
- It consists of a DAC, a comparator, and a successive approximation register (SAR).
- The external clock input sets the internal timing parameters.
- The control signal start of conversion (SOC) initiates an A/D conversion process and end of conversion signal is activated when the conversion is completed

The circuit operates as follows.

- With the arrival of the START command, the SAR sets the MSB d1= 1 with all other bits to zero so that the trial code is 10000000. The output V_d of the DAC is now compared with analog input Va.
- If Va is greater than the DAC output Vd then 10000000 is less than the correct digital representation.
- The MSB is left at'1' and the next lower significant bit is made '1' and further tested.
- However, if Va is less than the DAC output, then 10000000 is greater than the correct digital representation. So reset MSB to '0' and go on to the next lower significant bit.
- This procedure is repeated for all subsequent bits, one at a time until all bit positions have been tested.
- Whenever the DAC output crosses Va, the comparator changes state and this can be taken as the end of conversion (EOC) command.

correct digital representation	SAR output	comparator output
1101 0100	1000 0000	1 Va ≥ Vd
1101 0100	1100 0000	1 Va ≥ Vd
1101 0100	1110 0000	0 Va < Vd
1101 0100	1101 0000	1 Va ≥ Vd
1101 0100	1101 1000	0 Va < Vd
1101 0100	1101 0100	1 Va ≥ Vd
1101 0100	1101 0110	0 Va < Vd
1101 0100	1101 0101	0 Va < Vd
1101 0100	1101 0100	

- It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage.
- It requires eight pulses to establish the accurate output regardless of the value of the analog input. However, one additional clock pulse is used to load the output register and reinitialize the circuit.



(a) A tracking A/D converter (b) Waveforms associated with a tracking A/D converter

4.9 Voltage to current converter

Voltage to Current Converter with floating loads (V/I):

Voltage to current converter in which load resistor R_L is floating (not connected to ground). V_{in} is applied to the non- inverting input terminal, and the feedback voltage across R_1 devices

the inverting input terminal. This circuit is also called as a current – series negative feedback amplifier. Because the feedback voltage across R_1 (applied Non-inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id}.

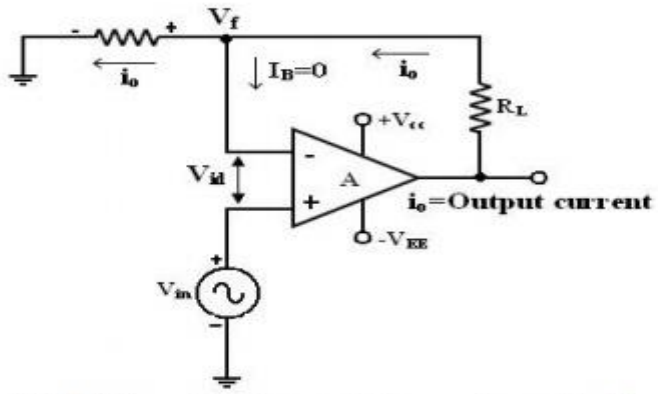


Fig. 2.7 Voltage to Current Converter with floating loads (V/I):

Writing KVL for the input loop,

$$\text{Voltage } V_{id} = V_f \text{ and}$$

$$I_B = 0 \text{ , } vi = R_L i_0$$

$$\text{where} = i_0 = v_i / R_L$$

From the fig input voltage Vin is converted into output current of V_{in}/R_L [V_{in} -> i_0]. In other words, input volt appears across R_1. If R_L is a precision resistor, the output current ($i_0 = V_{in}/R_1$) will be precisely fixed.

Applications:

1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED and Zener diode testers.

Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.

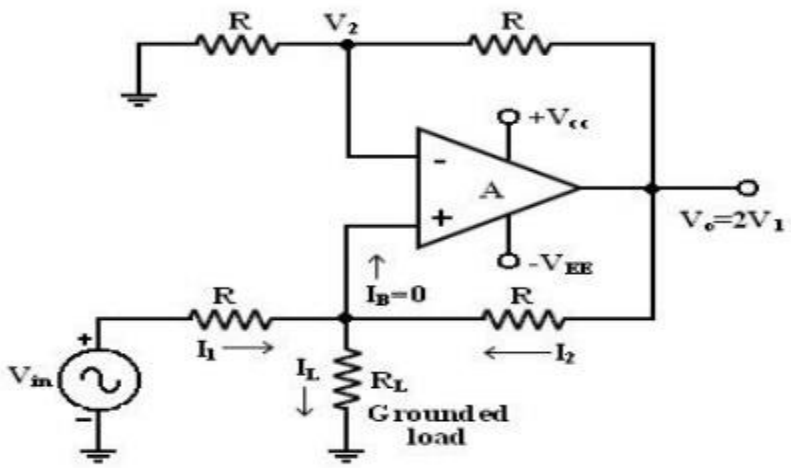


Fig 2.8 V – I converter with grounded load

Analysis of the circuit:

The analysis of the circuit can be done by following 2 steps.

1. To determine the voltage V_1 at the non-inverting (+) terminals and
2. To establish relationship between V_1 and the load current I_L. Applying KCL at node a,

$$R= R_f$$

$$I_1 +I_2=I_L$$

$$(V_i +V_a)/R + (V_0 –V_a)/R= I_L$$

$$V_o = (V_i +V_o - I_L R)/2 \text{ and gain } =1+ R/R= 2.$$

$$\therefore V_i =I_L R \; ; \; I_L=V_i/R$$

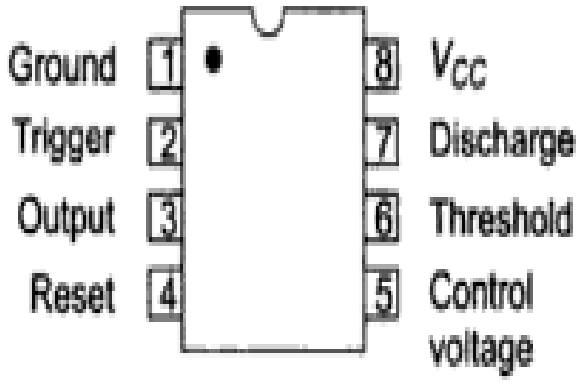
4.10 555 Timer

- The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions.
- IC NE/SE 555 is a highly stable device for generating accurate time delays. Commercially, this IC is available in 8-pin circular, TO-99 or 8-pin DIP or 14-pin DIP packages.

The salient features of 555 Timer IC's are:

- Compatible with both TTL and CMOS logic families.
- The maximum load current can go up to 200 mA.
- The typical power supply is from +5V to +18 V

Pin diagram of 555 timer



Features of 555 Timer Basic blocks

- 1. It has two basic operating modes: monostable and astable
- 2. It is available in three packages. 8 pin metal can, 8 pin dip, 14 pin dip.
- 3. It has very high temperature stability
-

Applications of 555 Timers

- 1. Astable multivibrator 6. Monostable multivibrator
- 2. Missing pulse detector 7. Linear ramp generator
- 3. Frequency divider 8. Pulse width modulation
- 4. FSK generator 9. Pulse position modulator
- 5. Schmitt trigger

General Description of the IC 555

- The positive dc power supply terminal is connected to pin 8 (Vcc) and negative terminal is connected to pin 1(Gnd). The ground pin acts as a common ground for all voltage references while using the IC.
- The output (pin 3) can assume a HIGH level (typically 0.5V less than Vcc) or a LOW level (approximately 0.1V).
- Two comparators, namely, upper comparator (UC) and lower comparator (LC) are used in the circuit.

- Three 5 kΩ internal resistors provide a potential divider arrangement. It provides a voltage of (2/3)Vcc to the (-) terminal of the upper comparator and (1/3)Vcc to the (+) input terminal of the lower comparator.
- A control voltage input terminal (pin 5) accepts a modulation control input voltage applied externally. It bypasses the noise or ripple from the supply.

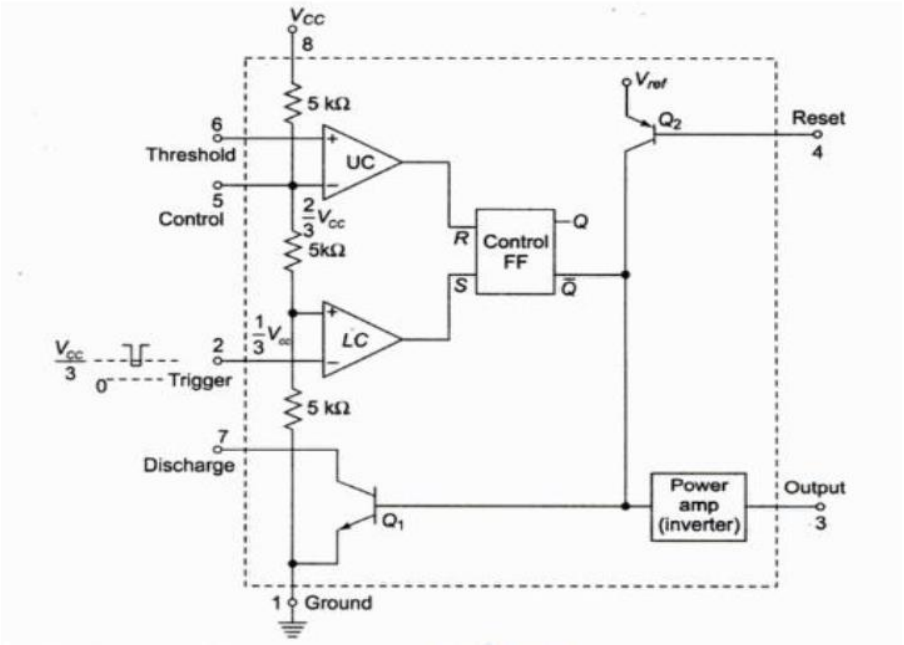


Fig: 4.9 Functional Block Diagram of IC 555 Timer

- The (+) input terminal of the UC is called the threshold terminal (pin 6) and the (-) input terminal of the LC is the trigger terminal (pin 2).
- The standby (stable) state makes the output Qbar of flip-flop (FF) HIGH. This makes the output of inverting power amplifier LOW.
- When a negative going trigger pulse is applied to pin 2, as the negative edge of the trigger passes through 1/3 (VCC), the output of the lower comparator becomes HIGH and it sets the control FF making Q=1and Qbar =0.
- When the threshold voltage Q = 1 at pin 6 exceeds 2/3 (Vcc), the output of upper comparator goes HIGH. This action resets the control FF with Q=0 and Qbar=1.
- The reset terminal (pin 4) allows the resetting of the timer by grounding the pin 4 or reducing its voltage level below 0.4V. This makes the output (pin 3) low overriding the operation of lower comparator.
- When not used, the reset terminal is connected to Vcc. Transistor Q_2, isolates the reset input from the FF and transistor Q_1.

- The reference voltage V_{ref} is made available internally from Vcc.
- Transistor Q_1 acts as a discharge transistor.
- When output (pin 3) is high, Q_1 is OFF making the discharge terminal (pin 7) open.
- When the output is low, Q_1 is forward-biased to ON condition. Then, the Discharge terminal appears as a short circuit to ground.

Table States of operation of IC 555

Sl. No.	Trigger (pin 2)	Threshold (pin 6)	Output state (pin 3)	Discharge state (pin 7)
1	Below $(1/3)V_{CC}$	Below $(2/3)V_{CC}$	High	Open
2	Below $(1/3)V_{CC}$	Above $(2/3)V_{CC}$	Last state remains	Last state remains
3	Above $(1/3)V_{CC}$	Below $(2/3)V_{CC}$	Last state remains	Laststate remains
4	Above $(1/3)V_{CC}$	Above $(2/3)V_{CC}$	Low	Ground

4.11 Monostable Multivibrator using 555 Timer

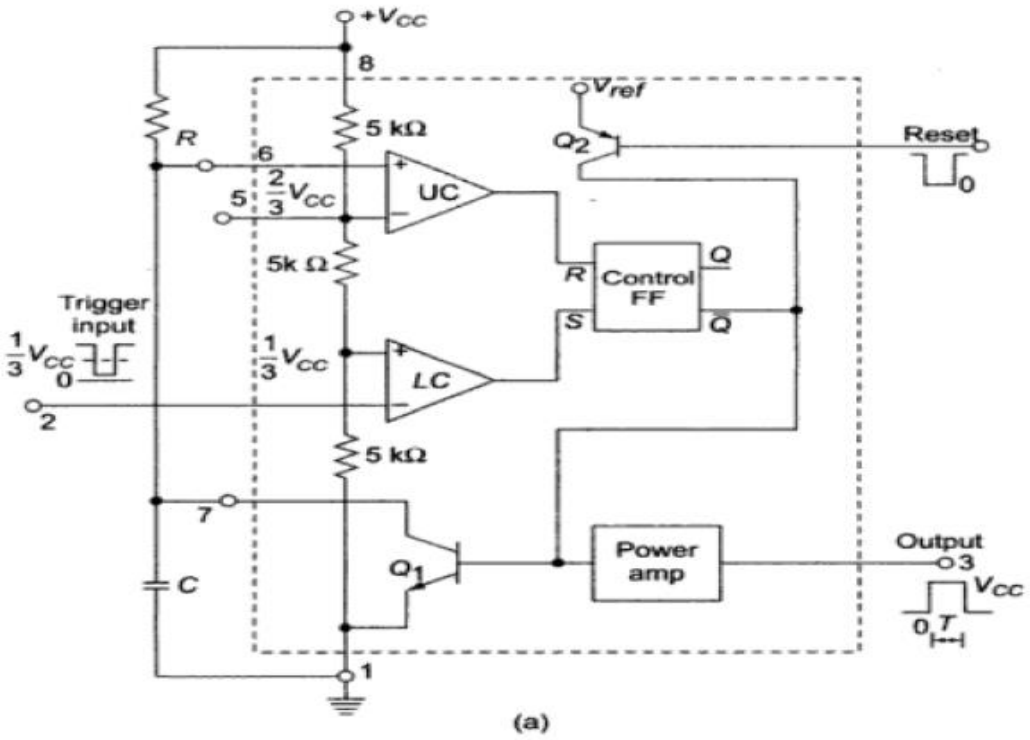


Fig: 4.9 Monostable Multivibrator using 555 Timer

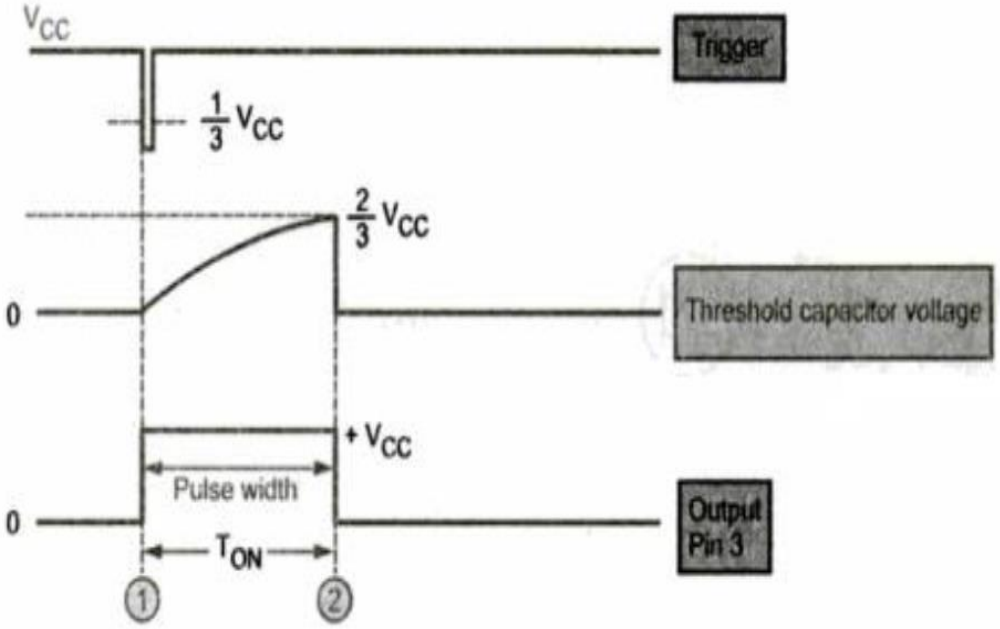


Fig. Waveforms of monostable operation

Derivation of Pulse Width

The voltage across capacitor increases exponentially and is given by

$$V_C = V\,(1 - e^{-t/CR})$$

If $V_C = 2/3\ V_{CC}$

then $\frac{2}{3} V_{CC} = V_{CC}\,(1 - e^{-t/CR})$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$$\therefore \quad -\frac{t}{CR} = -1.0986$$

$$\therefore \quad t = +1.0986\ CR$$

$$\therefore \quad t \approx 1.1\ CR$$

where C in farads, R in ohms, t in seconds.

Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e. 1.1 RC

Thus the pulse width denoted as W is given by,

$$W = 1.1\ RC$$

4.12 Astable Multivibrator using 555 Timer

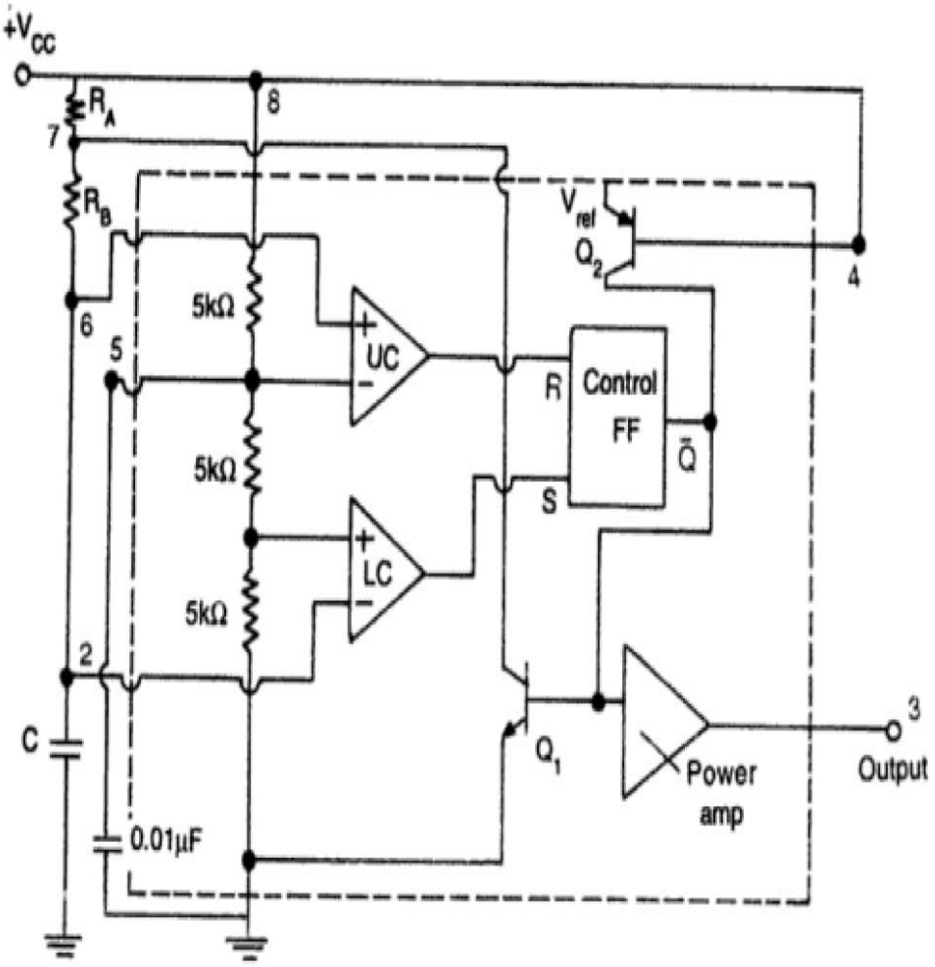


Fig. Functional diagram of astable multivibrator using 555 timer

Fig: 4.10 Astable Multivibrator using 555 Timer

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by

$$v_c = V_{cc}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{cc} is,

$$(2/3)\, V_{cc} = V_{cc}(1 - e^{-t_1/RC})$$

or, $$t_1 = 1.09\ RC$$

and the time t_2 to charge from 0 to (1/3) V_{cc} is,

$$(1/3)\, V_{cc} = V_{cc}(1 - e^{-t_2/RC})$$

or, $$t_2 = 0.405\ RC$$

So the time to charge from (1/3) V_{cc} to (2/3) V_{cc} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09\ RC - 0.405\ RC = 0.69\ RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C$$

The output is low while the capacitor discharges from (2/3) V_{cc} to (1/3) V_{cc} and the voltage across the capacitor is given by

$$(1/3)\, V_{cc} = (2/3)V_{cc}\, e^{-t/RC}$$

solving, we get $$t = 0.69\ RC$$

So, for the given circuit, $t_{LOW} = 0.69\ R_B C$

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\ (R_A + 2R_B)\ C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$$

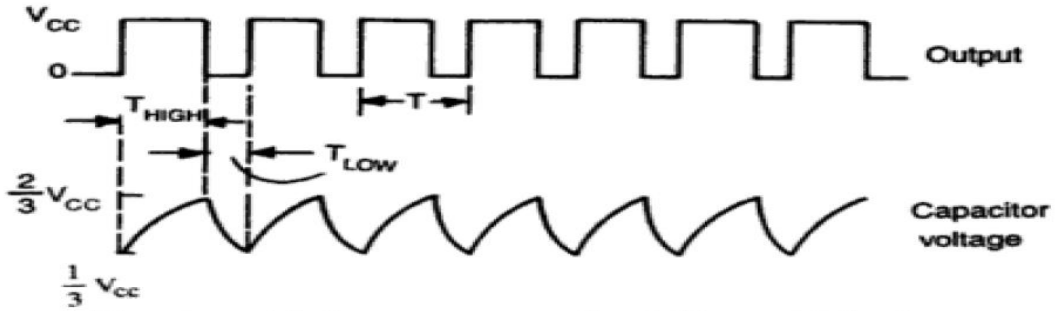


Fig. Timing sequence of astable multivibrator

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5. Amplifiers

5.1 Instrumentation Amplifier

Figure shows our modified differential amplifier called the instrumentation amplifier (IA). Op amps U1 and U2 act as voltage followers for the signals V_{in1} and V_{in2} which see the infinite input resistance of op amps U1 and U2. Assuming ideal op amps, the voltage at the inverting terminals of op amps U1 and U2 are equal to their corresponding input voltages. The resulting current flowing through resistor R1 is

$$I_1 = \frac{V_{in1} - V_{in2}}{R1}$$

Since no current flows into the terminals of the op amp, the current flowing through resistor R2 is also given by Equation.

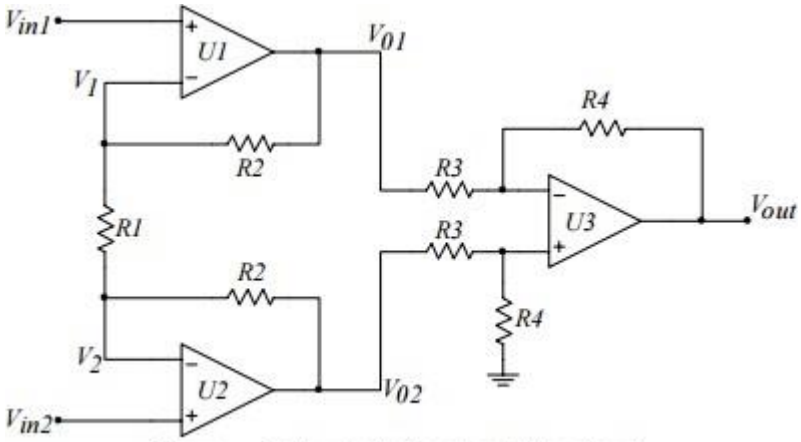


Figure Instrumentation Amplifier circuit

Fig: 5.1 Instrumentation Amplifier Circuit

Since our system is linear the voltage at the output of op-amp U1 and op-amp U2 is given by superposition as

$$V_{01} = \left(1 + \frac{R2}{R1}\right) V_{in1} - \frac{R2}{R1} V_{in2}$$

$$V_{02} = \left(1 + \frac{R2}{R1}\right) V_{in2} - \frac{R2}{R1} V_{in1}$$

Next we see that op amp U3 is arranged in the difference amplifier configuration .The output of the difference amplifier is

$$V_{out} = \frac{R4}{R3}\left(1+\frac{2R2}{R1}\right)(V_{in2} - V_{in1})$$

The differential gain, $\frac{R4}{R3}\left(1+\frac{2R2}{R1}\right)$, may be varied by changing only one resistor: $R1$.

5.2 Bridge amplifier

Definition

Op amp bridge amplifiers are electronic circuits used in measuring the unknown resistance of a transducer in one branch. Normally all the four branches will have equal resistances so that by Wheatstone bridge principle output voltage will be zero. However if one of the resistance in any one of the branch gets altered due to change in some physical parameter, the output voltage developed will be proportional to (ΔR/R)/(1+(ΔR/R)) if (ΔR/R) << 1 then V_o = A*(ΔR/R) from which ΔR can be known.

Circuit operation of Opamp bridge amplifier

The op amp bridge amplifier is shown below

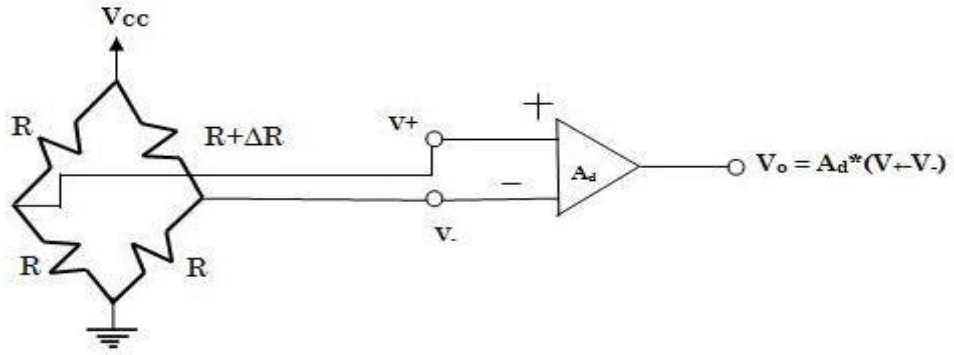


Fig: 5.2 Opamp bridge amplifier Circuit

In the figure shown above the resistance shown as R+ΔR can be any sensor such as platinum resistor, strain gauge, thermistor, sensistor etc. The resistors labelled as R are reference resistors with which the varying resistance can be measured. Since the opamp is in open loop configuration the output of opamp is given as

$$\mathbf{V_o = A_d*(V_+ - V_-)}$$

Where A_d is open loop differential gain of opamp. The current flowing through the input

terminals of an op amp will be zero (except for small bias currents) due to infinite input resistance of opamp. The Opamp bridge amplifier can be redrawn as follows

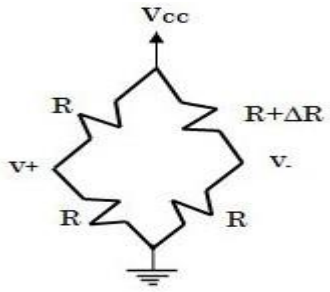


Fig: 5.3 Bridge Circuit

Using the voltage divide rule

The voltage at inverting terminal of amp $V_- = V*(R+\Delta R)/(R+R+\Delta R)$

$$V- = V*(R+\Delta R)/(2*R+\Delta R)$$

Dividing the numerator and denominator by R, we get

$$V- = V*((R+\Delta R)/R)/((2*R+\Delta R)/R)$$

$$V- = V*(1+(\Delta R/R))/(2+(\Delta R/R))$$

Let $\Delta R/R = \delta$, the voltage at inverting terminal of op amp V- = $V*(1+\delta)/(2+\delta)$ The voltage at inverting terminal of amp V- = V*R/(R+R)

$$V- = V/2$$

Hence the output of op amp is $V_o = A_d*(V_+-V_-) = A_d*(V/2-V*(1+\delta)/(2+\delta))$

$$V_o = A_d*V*(1/2-(1+\delta)/(2+\delta))$$

$V_o = A_d*V*(2+\delta-$
$2*(1+\delta))/(2*(2+\delta))$ $V_o =$
$A_d*V*(2+\delta-2-2*\delta))/(2*(2+\delta))$
$V_o = A_d*V*(-\delta)/(2*(2+\delta))$ for $(\Delta R/R) = \delta << 1$

The output voltage of op amp reduces to $V_o = A_d*V*(-\delta)/4$. When all the resistors are matched i.e. $\delta=0$, output voltage goes to zero.

Applications

Following are some of the applications of bridge amplifiers

- The very high value, closely matched input resistances characteristic of bridge amplifiers make them ideal for measuring low level voltages and currents—without loading down the signal source.
- Bridge amplifiers are used in signal conditioning circuits along with instrumentation amplifiers to improve Common Mode Rejection Ratio.

- Bridge amplifiers are used in Single supply common mode suppression circuits.
- Common bridge amplifier applications include strain and weight measurement using load cells and temperature measurement using resistive temperature detectors.

5.3 Biopotential Amplifiers

Definition: An amplifier used to process Biopotential are called bioelectric or Biopotential amplifiers.

Adjust gain

DC coupled: needed when signal is very slowly changing or is dc i.e. O_2 level may change pressure mmHg per min or hour

AC coupled: need to overcome electrode offset

Frequency Response: range that amplifier can work over i.e. ECG is 0.05 to 100 Hz

Low Frequency Response or High Frequency Response: frequencies where gain drops 3 dB below its mid frequency value.

Gain Types of Amplifiers:

- Low Gain Amplifier: gain between 1 and 10 where unity or 1 is most common (used for Isolation, buffering and possibly impedance transformation between signal source and readout device).often used for the measurement of action potentials and other relatively high amplitude bioelectric events.
- Medium Gain Amplifier: gain between 10 and 1000 used for ECG, EMG muscle potential etc.
- High Gain Amplifier: gain greater than 1000 used in very sensitive measurements such as EEG.

Two important parameters of Biopotential amplifier are noise and drift.

- Drift- Change in output signal voltage caused by changes in operating temperature.
- Noise-the thermal noise, generated in resistances and semiconductor devices.
- Good design and prudent component selection reduce these problems to negligible level.

Properties desired in Biopotential amplifier:

1. Single-ended output for differential input.
2. High CMRR
3. Extremely high input impedance
4. Variable gain adequate to the requirement
5. Frequency response variable through switch selection
6. Zero suppression: This is an optional feature that allow shift about the zero baseline by nulling offsets inherent in the signal.

It permits small varying signals superimposed on a larger dc signal to be processed in the amplifier.

5.4 Isolation Amplifiers

- To prevent accidental internal cardiac shock, the manufactures of modern bioelectric amplifiers use isolation amplifier.
- They provide upto 10^{12} ohm of insulation between patient connector and AC mains line cord.

Circuit Explanation:

- It is usually composed of an input amplifier, modulator and an output amplifier.
- Modulation includes amplitude, voltage to frequency duty cycle, pulse width, flyback loading and etc.
- Barriers can be optical, magnetic transformer, capacitive or even heat transfer
- Isolation amplifier is an energy converter, input common and output common are isolated.
- Electrical energy on the modulator side is converted to some non-electrical energy in

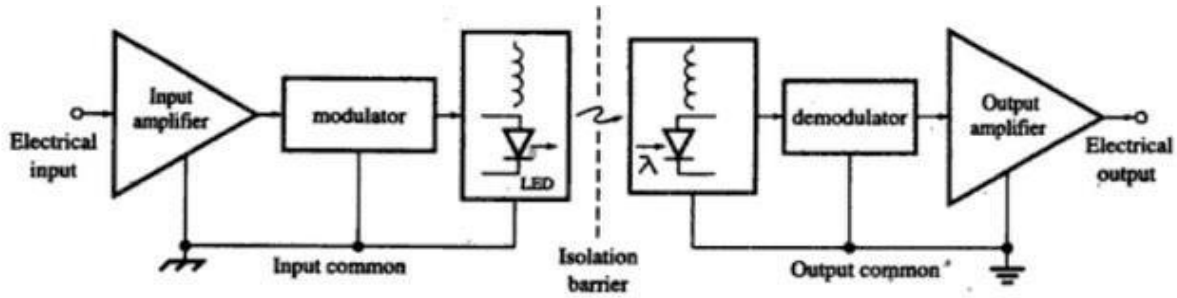


Fig: 5.4 Isolation Amplifier

- the barrier and then converted back to electrical energy on demodulator side.

Symbol of Isolation amplifier

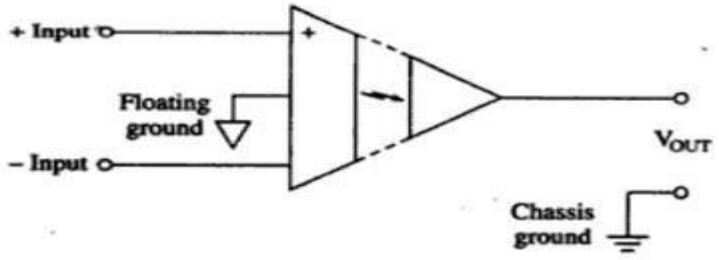


Fig: 5.5 Symbol of Isolation amplifier

- It actually operates on the principle of attenuation
- High barrier impedance acts in series between input and output.
- Therefore an interfering isolation mode voltage (1MV) referenced to the iso-amp's output must go through the large barrier resistance before it can mix with input signal.
- Hence most of the interfering voltage or noise is dropped across the barrier.

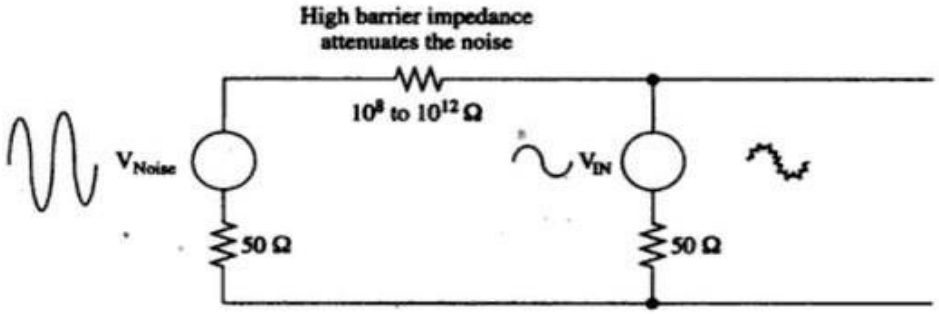


Fig: 5.6 High barrier impedance

- Normally the barrier is not infinite, so some error will appear in the output.
- The measure of how well isolation amplifier attenuates or rejects the interfering isolation mode voltage (IMV) is called Isolation mode rejection (IMR).
- The isolation mode rejection ratio in V/V is called IMRR

$$\text{IMRR in V/V} = \log^{-1} (\text{IMR}_{\text{dB}}/20).$$

$$\text{where } \underset{\text{(dB)}}{\text{IMR}} = 20 \log_{10} \underset{\text{(V/V Ratio)}}{\text{IMRR}}$$

- The error is gained up just like input signal and results in some dc or ac voltage that adds to normal signal.
- An isolation amplifier may have common mode noise on its input as well as isolation mode noise across its barrier.
- An isolation amplifier serves three purpose

  1. Break ground loops to permit incompatible circuits to be interfaced together while reducing noise.
  2. Amplify signals while passing only low leakage current to prevent shock to people.
  3. Withstand high voltage to protect people, circuits and equipment.

5.5. Design of Isolation Amplifiers

1. Battery Powered:

- It is simplest to use and implement but has problems in battery maintenance.
- For cardiac output computers, battery power is used universally.
- The biopotential amplifier is powered from a battery pack.
- If any external instrument (CRO, strip chart recorder) is used then some isolation techniques must be used.

2. Carrier:

- The circuitry inside the dashed line is isolated from ac power main and the rest of the circuitry is powered from ac mains.
- Isolation is provided by separation of the ground, power and signal paths in the two sections by transformers T_1 and T_2.
- It has a core material that is very inefficient at 60 Hz but works well in 20-250 KHz range.
- This feature allows the transformer to easily pass the carrier signal but impedes any

60 Hz energy if present.

- Carrier oscillator signal is coupled through transformer T_1 to the isolated stages.
- Part of the energy from the secondary of T_1 goes to the modular stage, remainder is rectified and filtered and then used as an isolated dc power supply.
- The dc output of this power supply is used to power the input amplifiers and modulator stages.
- An analog signal is applied to the input, is amplified by A_1 and then is applied to one input of modulator stage which modulates the amplitude of the signal onto the carrier.
- T2 couples the signal to the input of the demodulator stage on the non isolated side of the circuit. Envelop or synchronous demodulation is used.

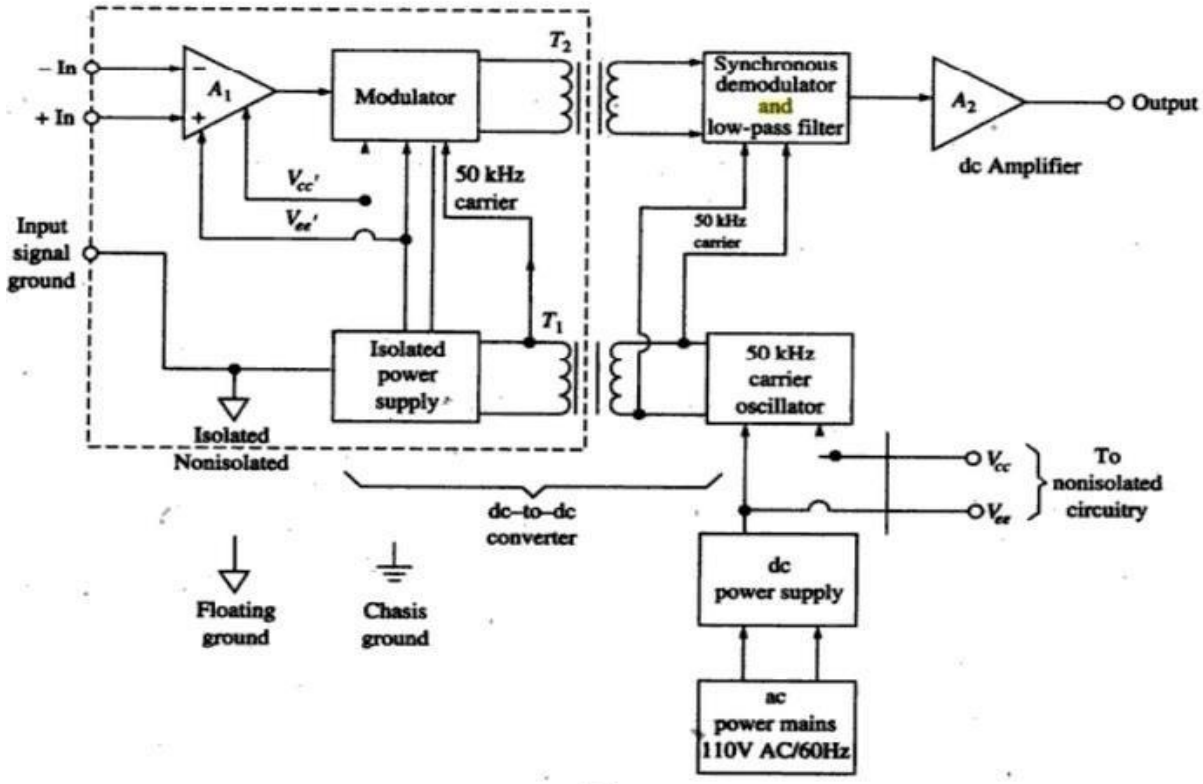


Fig: 5.7 Carrier isolation Amplifier

3. Optically Coupled:

- Electronic optocouplers (optoisolators) are sometimes used to provide the desired isolation.
- Two popular methods are used to provide optical coupling 1.carrier and 2.direct method.

- Carrier method is not used widely because of frequency response limitations.

A more common approach is shown in figure; this circuit uses the same dc-dc converter to power the isolated states.

- This will keep A_1 isolated from ac power mains but is not used in signal coupling process.
- LED in the optoisolators is driven by the output of isolated amplifier A_1.
- Q_1 serves as a series switch to vary the light output of the LED proportional to analog signal from A_1.
- It normally passes sufficient collector current to bias the LED into a linear portion of its operating curve.
- Output of the photo transistor N is ac-coupled to the remaining amplifiers on the non isolated side of the circuit.

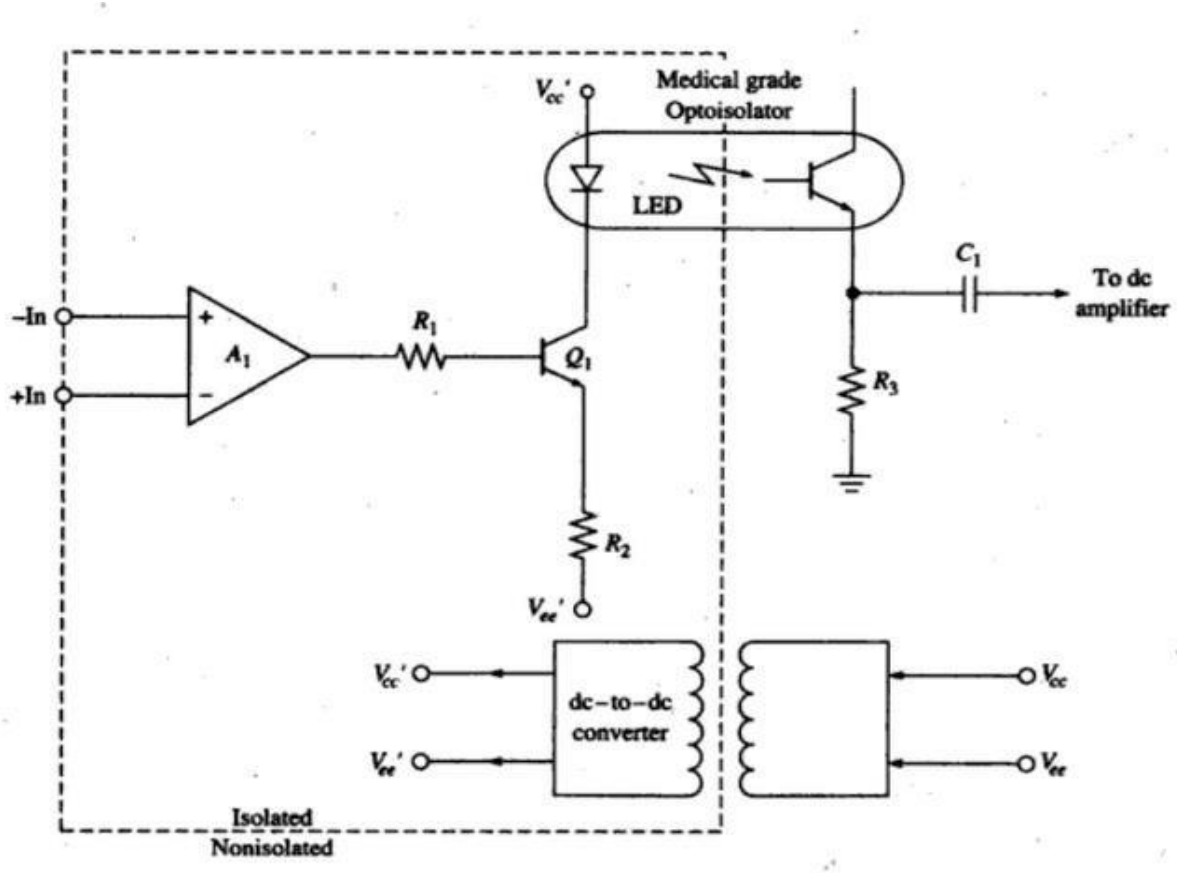


Fig: 5.8 optically coupled isolation Amplifier

4. Current Loading:

- A schematic of current loading isolation technique is shown in figure; it consists of dual JFET (Q1) and an operational amplifier.
- The output of A1 is connected to the isolated Vee through resistor R7.This power supply is dc-dc converter at 250 KHz.
- Transformer T1 provides isolation between floating power supplies on the isolated side and the normal mains – powered supplies.
- An input signal causes the output of A1 to vary the loading on the floating power supply through R7.
- It causes the variation of T1 primary current which is also proportional to analog signal.
- This current variation is converted to voltage by amplifier A2.
- An offset null control (R11) is provided to eliminate the offset at the output.

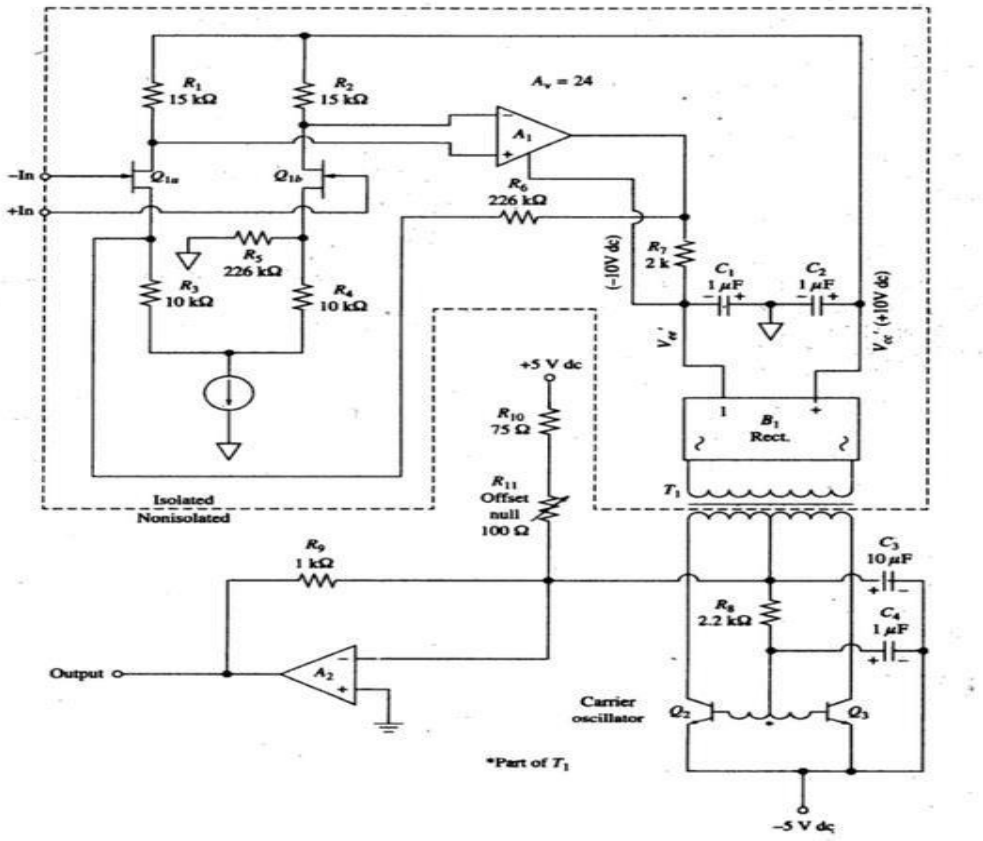
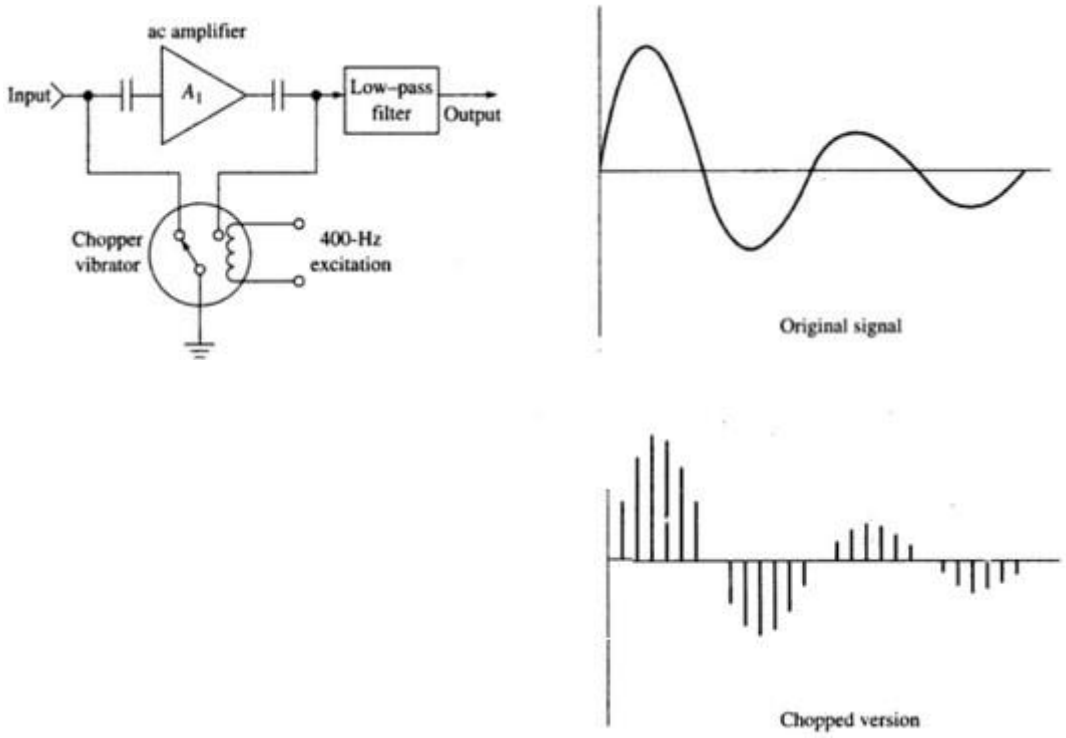


Fig: 5.9 Current loading isolation Amplifier

5. Chopper stabilized amplifiers:

- These are basically used to reduce two major problems when recording low biopotential (EEG).They are noise and dc drift.
- These circuits will sample or chop the analog signal at a frequency which will be passed through the ac coupled amplifier.
- The chopper is a vibrator driven single pole, double throw (SPDT) switch that grounds the amplifier input and output terminals on alternate swings of switch.
- Chopper coil is excited by 400Hz ac carrier signal. Chopper technique not only gains stability from ac coupled amplifier but also provides low noise operation.
- The sampling rate acts as a LPF for externally generated noise, through it adds noise of its own.
- To limit the noise further sometimes the ac coupled amplifier is allowed to act as band pass filter that passes only narrow range of frequencies.



- By limiting the bandwidth, we can limit the noise amplitude.

Fig: 5.10 Chopper Sabilized Amplifier

6. Input Guarding:

In most cases, the physiological signal of interest is accompanied by large common-mode (CM) signals. Frequently, several 100 mVs of signal will be coupled into the input cables of a biopotential amplifier. One such example is shown below.

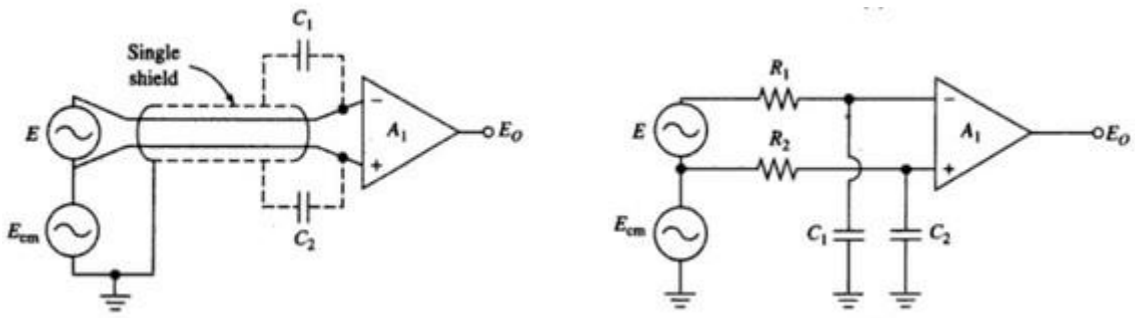


Fig: 5.11 Differential amplifier connected to a differential signal source

The circuit shows, a differential amplifier connected to a differential signal source through a shielded cable. E=differential signal, E_{cm} = common mode signal.

- If the usual practice of grounding is followed then the equivalent circuit is obtained. (Fig.b).
- Resistance R_1 and R_2 are the sum of cable resistance and the signal source output impedance.C_1 and C_2 represents the capacitance of shielded cable.
- In this circuit R_1=R_2 and C_1=C_2 should be maintained, otherwise the inputs become unbalanced to ground, then amplifier will be unable to distinguish the artifact from the real signal.
- The solution is to use input guarding. The main concept is to place the shield at the CM signal potential, which in effect places both sides of C_1 and C_2 at the same potential. The circuit is shown below.

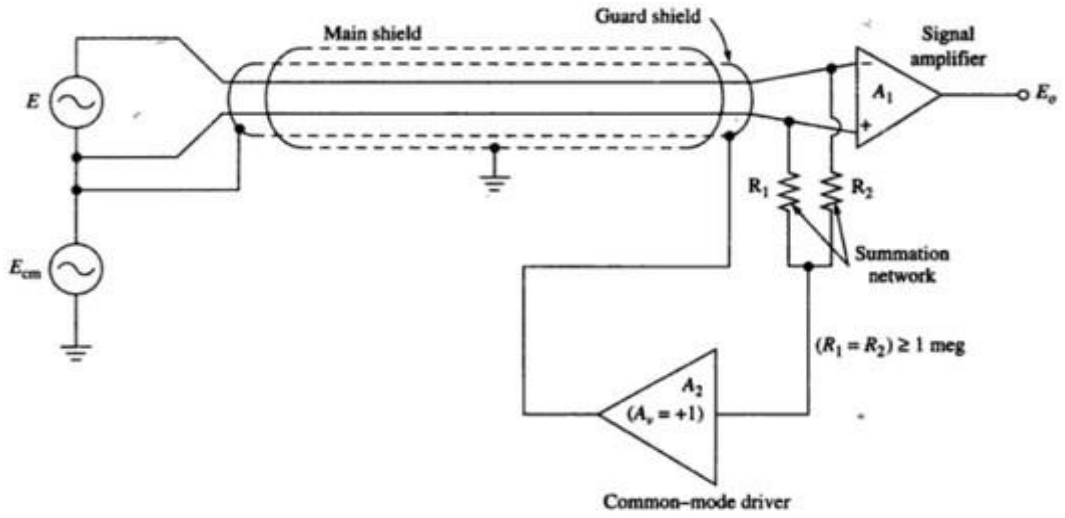


Fig: 5.12 Input Guarding

- Outer shield is useful when high intensity CM inference is expected.
- The drive source for the guard shield is derived by summing +IN and –IN signals in R1/R2 network.
- In ECG amplifier, the right leg of the patient is designated as common, so the guard shield may be connected to the right leg.

5.6 Voltage Regulators

The voltage regulator in its simplest form consists of Voltage reference, VR Error amplifier Feedback network Active series or shunt control element The voltage reference generates a voltage level which is applied to the comparator circuit, which is generally an error amplifier. The second input to the error amplifier is obtained through feedback network. Generally using the potential divider, the feedback signal is derived by sampling the output voltage. The error amplifier converts the difference between the output sample and the reference voltage into an error signal. This error signal in-turn controls the active element of the regulator circuit in order to compensate the change in the output voltage. Such an active element is generally a transistor.

Types of voltage regulators

Depending upon where the control element is connected in the regulator circuit, the regulators are basically classified as

Series voltage regulator

Shunt voltage regulator

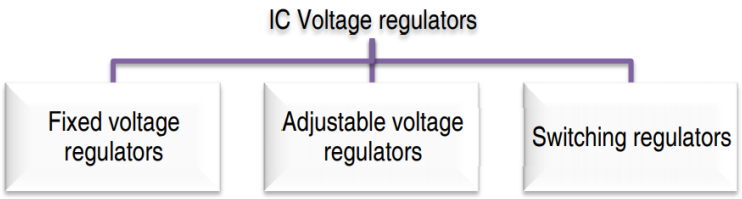
Each type provides a constant d.c output voltage which is regulated.

Advantages of IC voltage Regulators

1. Easy to use
2. It greatly simplifies power supply design
3. Due to mass production, low in cost
4. IC voltage regulators are versatile
5. Conveniently used for local regulation
6. These are provided with features lime built-in protection programmable output, current/voltage boosting, internal short circuit current limiting etc

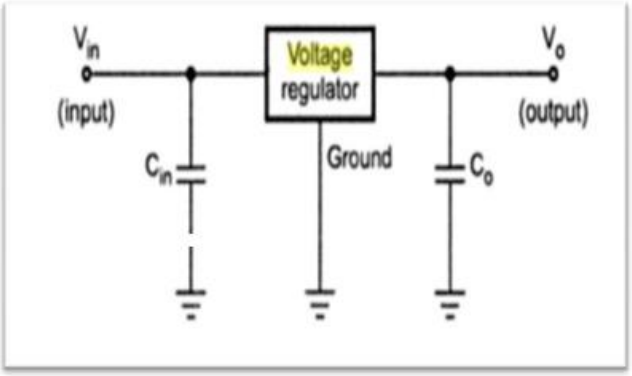
Classification of IC voltage regulators

The IC voltage regulators are classified as shown in the figure below.



5.6.1 Three terminal fixed voltage regulators

As the name suggest, three terminal voltage regulators have three terminals namely input which is unregulated (Vin), regulated output (Vo) and common or a ground terminal. These regulators do not require any feedback connections. The figure below shows the basic three terminal voltage regulators.



Basic regulator circuit (Three Terminals)

The capacitor C_{in} is required if regulator is located at appreciable distance more than 5 cm from a power supply filter. The output capacitor Co may not be needed but if used it improves the transient response of the regulator i.e., regulator response to the transient changes in the load. This capacitor also reduces the noise present at the output. The difference between Vin and Vo (Vin – Vo) is called as dropout voltage and it must be typically 2.0V even during the low point on the input ripple voltage, for the proper functioning of the regulator.

Three Terminal Fixed Voltage regulator ICs

There are basically two types of Three Terminal Fixed Voltage regulator ICs are available. One is positive output voltage and other has negative output voltage; but the output voltage is fixed.

There are two IC series.

1. 78XX series:

This is a positive regulator. The first two digits i.e.,78 indicates that the output voltage is positive. The second two digits 'XX' indicates output voltage of the regulator. The available ICs of this series are 7805(+5V), 7812 (+12V), 7815(+15V) etc. The output voltages are shown in brackets.

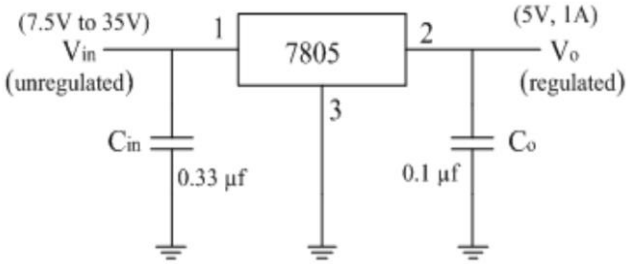
2. 79XX series:

This is a negative voltage regulator. The first two digits i.e.79 indicates that the output voltage is negative. The second two digits 'XX' indicates output voltage of the regulator. The available ICs of this series are 7905(-5V), 7912 (-12V), 7915(-15V) etc. The output voltages are shown in brackets.

These ICs are provided with adequate heat sinking and can deliver output currents more than 1A. These ICs require less external components. These are provided with internal thermal shut down, overload and short circuit protection.

These two series are available in two versions, like low power and high power. The low power versions are available in plastic and metal packages like transistors.

The high-power versions are packaged in TO-3 type metal can or in T-220 type modulated plastic packages like power transistors. The typical value of output resistance is 8mΩ.Typical connections of IC 7805 regulator are shown below.



Two basic categories of voltage regulation are:

• Line regulation

• Load regulation

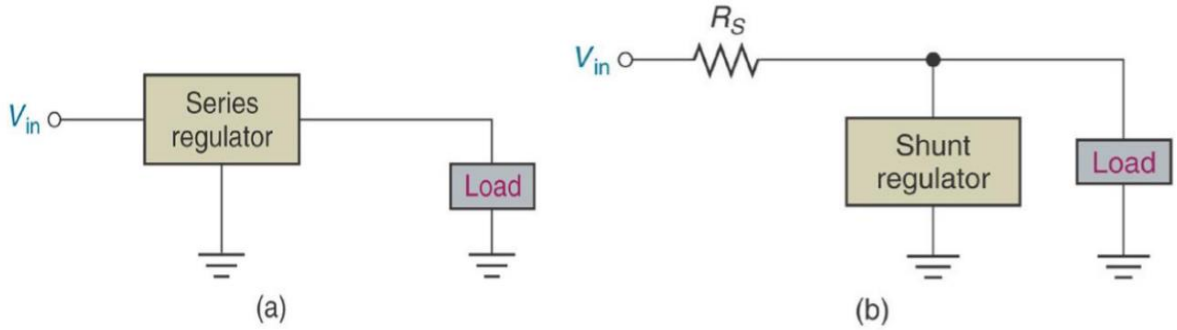
• The purpose of line regulation is to maintain a nearly constant output voltage when the input voltage varies.

• The purpose of load regulation is to maintain a nearly constant output voltage when the load varies.

Fundamental classes of voltage regulators are linear regulators and switching regulators

 Two basic types of linear regulator are the series regulator and the shunt regulator.

 The series regulator is connected in series with the load and the shunt regulator is connected in parallel with the load.

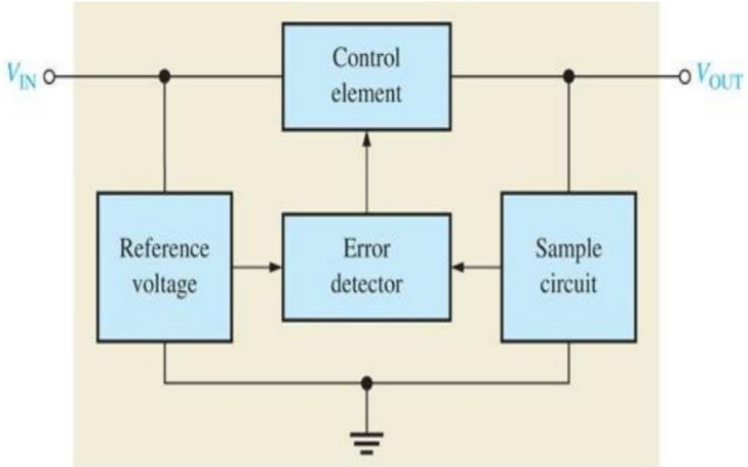


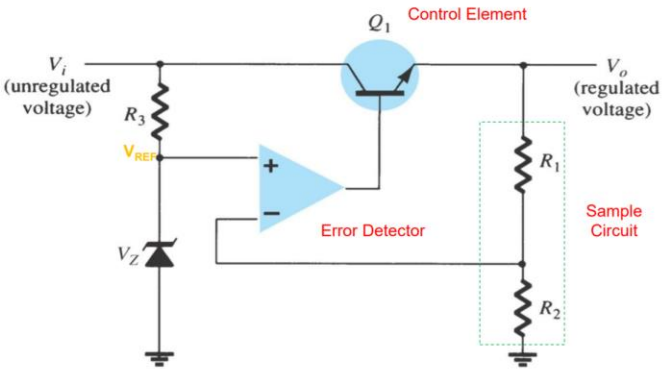
5.6.2 Series Regulator Circuit

Control element in series with load between input and output.

 Output sample circuit senses a change in output voltage.

 Error detector compares sample voltage with reference voltage → causes control element to compensate in order to maintain a constant output voltage.





 The resistor R1 and R2 sense a change in the output voltage and provide a feedback voltage.
 The error detector compares the feedback voltage with a Zener diode reference voltage.
 The resulting difference voltage causes the transistor Q1 controls the conduction to compensate the variation of the output voltage.
 The output voltage will be maintained at a constant value of:

$$V_o = \left(1 + \frac{R_1}{R_2}\right) V_Z$$

5.6.3 IC 723 – General Purpose Regulator

Disadvantages of fixed voltage regulator:

1. Do not have the shot circuit
2. Output voltage is not adjustable

These limitations can be overcoming in IC723.

Features of IC723:

1. Unregulated dc supply voltage at the input between 9.5V & 40V
2. Adjustable regulated output voltage between 2 to 3V.
3. Maximum load current of 150 mA (I_{Lmax} = 150mA).
4. With the additional transistor used, I_{Lmax} upto 10A is obtainable.
5. Positive or Negative supply operation
6. Internal Power dissipation of 800mW.
7. Built in short circuit protection.
8. Very low temperature drift.
9. High ripple rejection.

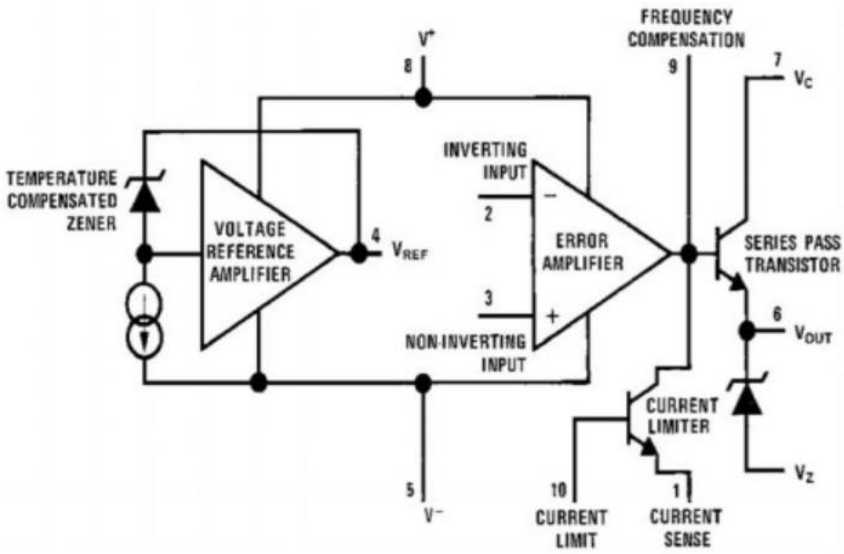


Fig. Functional block diagram of IC723

The simplified functional block diagram can be divided in to 4 blocks.

1. Reference Generating block:

The temperature compensated Zener diode, constant current source & voltage reference amplifier together from the reference generating block. The Zener diode is used to generate a fixed reference voltage internally. Constant current source will make the Zener diode to operate at affixed point & it is applied to the Non – inverting terminal of error amplifier. The Unregulated input voltage ±Vcc is applied to the voltage reference amplifier as well as error amplifier.

2. Error Amplifier:

Error amplifier is a high gain differential amplifier with 2 input (inverting & Non-inverting). The Non-inverting terminal is connected to the internally generated reference voltage. The Inverting terminal is connected to the full regulated output voltage.

3. Series Pass Transistor:

Q1 is the internal series pass transistor which is driven by the error amplifier. This transistor actually acts as a variable resistor & regulates the output voltage. The collector of transistor Q1 is connected to the Un-regulated power supply. The maximum collector voltage of Q1 is limited to 36Volts. The maximum current which can be supplied by Q1 is 150mA.

4. Circuitry to limit the current:

The internal transistor Q2 is used for current sensing & limiting. Q2 is normally OFF transistor. It turns ON when the IL exceeds a predetermined limit.

Low voltage, Low current is capable of supplying load voltage which is equal to or between 2 to 7Volts.

V_{load} = 2 to 7V and I_{load}= 50mA

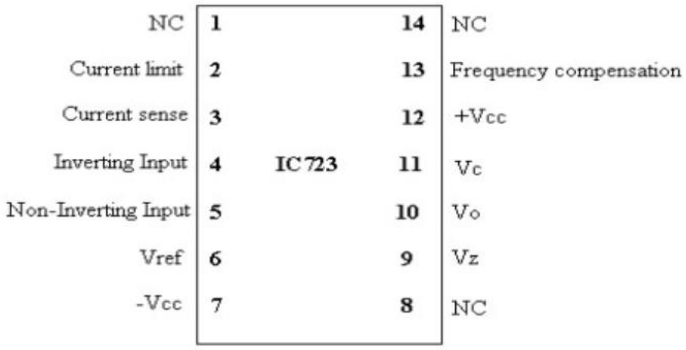


Fig. Pin diagram of IC723